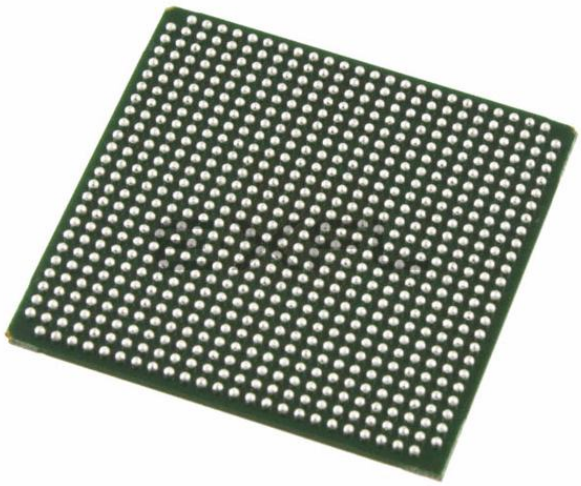
Lattice Semiconductor Corporation - LFE2-70E-6FN672C Datasheet



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Understanding Embedded - FPGAs (Field Programmable Gate Array)

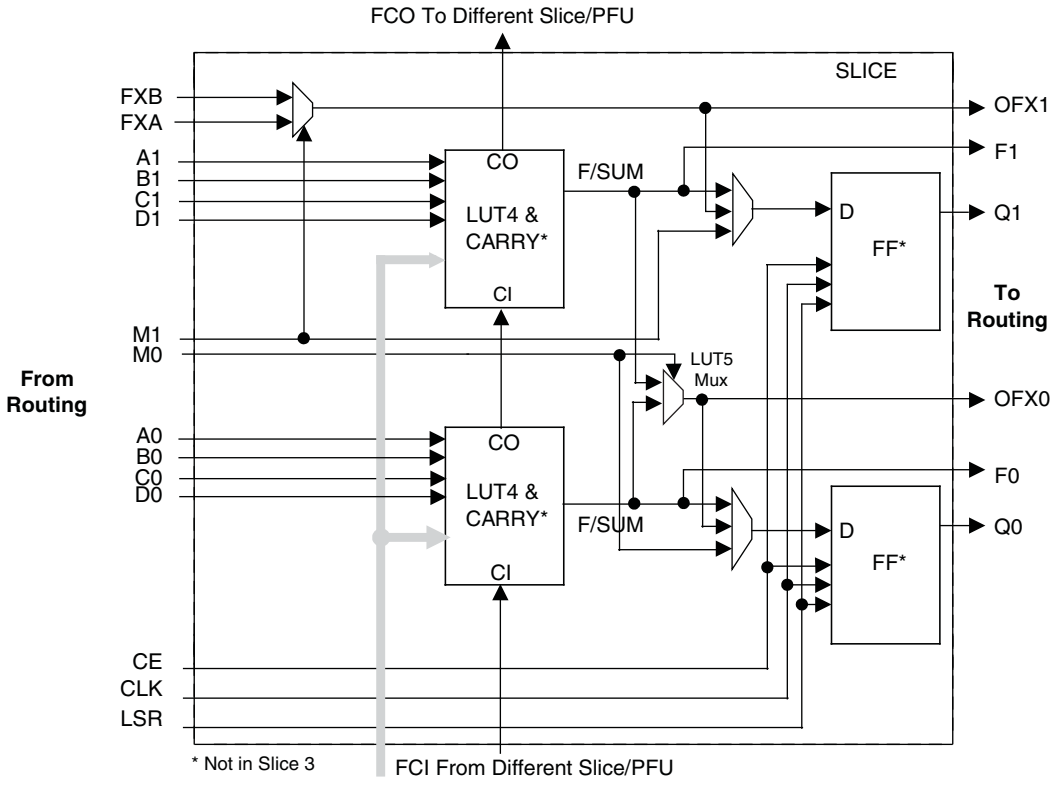
Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	8500
Number of Logic Elements/Cells	68000
Total RAM Bits	1056768
Number of I/O	500
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	672-BBGA
Supplier Device Package	672-FPBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfe2-70e-6fn672c

Figure 2-4. Slice Diagram



For Slices 0 and 2, memory control signals are generated from Slice 1 as follows:

WCK is CLK
WRE is from LSR
DI[3:2] for Slice 2 and DI[1:0] for Slice 0 data
WAD [A:D] is a 4bit address from slice 1 LUT input

Table 2-2. Slice Signal Descriptions

Function	Type	Signal Names	Description
Input	Data signal	A0, B0, C0, D0	Inputs to LUT4
Input	Data signal	A1, B1, C1, D1	Inputs to LUT4
Input	Multi-purpose	M0	Multipurpose Input
Input	Multi-purpose	M1	Multipurpose Input
Input	Control signal	CE	Clock Enable
Input	Control signal	LSR	Local Set/Reset
Input	Control signal	CLK	System Clock
Input	Inter-PFU signal	FC	Fast Carry-in[1]
Input	Inter-slice signal	FXA	Intermediate signal to generate LUT6 and LUT7
Input	Inter-slice signal	FXB	Intermediate signal to generate LUT6 and LUT7
Output	Data signals	F0, F1	LUT4 output register bypass signals
Output	Data signals	Q0, Q1	Register outputs
Output	Data signals	OFX0	Output of a LUT5 MUX
Output	Data signals	OFX1	Output of a LUT6, LUT7, LUT8[2] MUX depending on the slice
Output	Inter-PFU signal	FCO	Slice 2 of each PFU is the fast carry chain output[1]

1. See Figure 2-4 for connection details.
2. Requires two PFUs.

Modes of Operation

Each slice has up to four potential modes of operation: Logic, Ripple, RAM and ROM.

Logic Mode

In this mode, the LUTs in each slice are configured as 4-input combinatorial lookup tables. A LUT4 can have 16 possible input combinations. Any four input logic functions can be generated by programming this lookup table. Since there are two LUT4s per slice, a LUT5 can be constructed within one slice. Larger look-up tables such as LUT6, LUT7 and LUT8 can be constructed by concatenating other slices. Note LUT8 requires more than four slices.

Ripple Mode

Ripple mode supports the efficient implementation of small arithmetic functions. In ripple mode, the following functions can be implemented by each slice:

- Addition 2-bit
- Subtraction 2-bit
- Add/Subtract 2-bit using dynamic control
- Up counter 2-bit
- Down counter 2-bit
- Up/Down counter with Async clear
- Up/Down counter with preload (sync)
- Ripple mode multiplier building block
- Multiplier support
- Comparator functions of A and B inputs
  - A greater-than-or-equal-to B
  - A not-equal-to B
  - A less-than-or-equal-to B

Ripple Mode includes an optional configuration that performs arithmetic using fast carry chain methods. In this configuration (also referred to as CCU2 mode) two additional signals, Carry Generate and Carry Propagate, are generated on a per slice basis to allow fast arithmetic functions to be constructed by concatenating Slices.

RAM Mode

In this mode, a 16x4-bit distributed single port RAM (SPR) can be constructed using each LUT block in Slice 0 and Slice 2 as a 16x1-bit memory. Slice 1 is used to provide memory address and control signals. A 16x2-bit pseudo dual port RAM (PDPR) memory is created by using one Slice as the read-write port and the other companion slice as the read-only port.

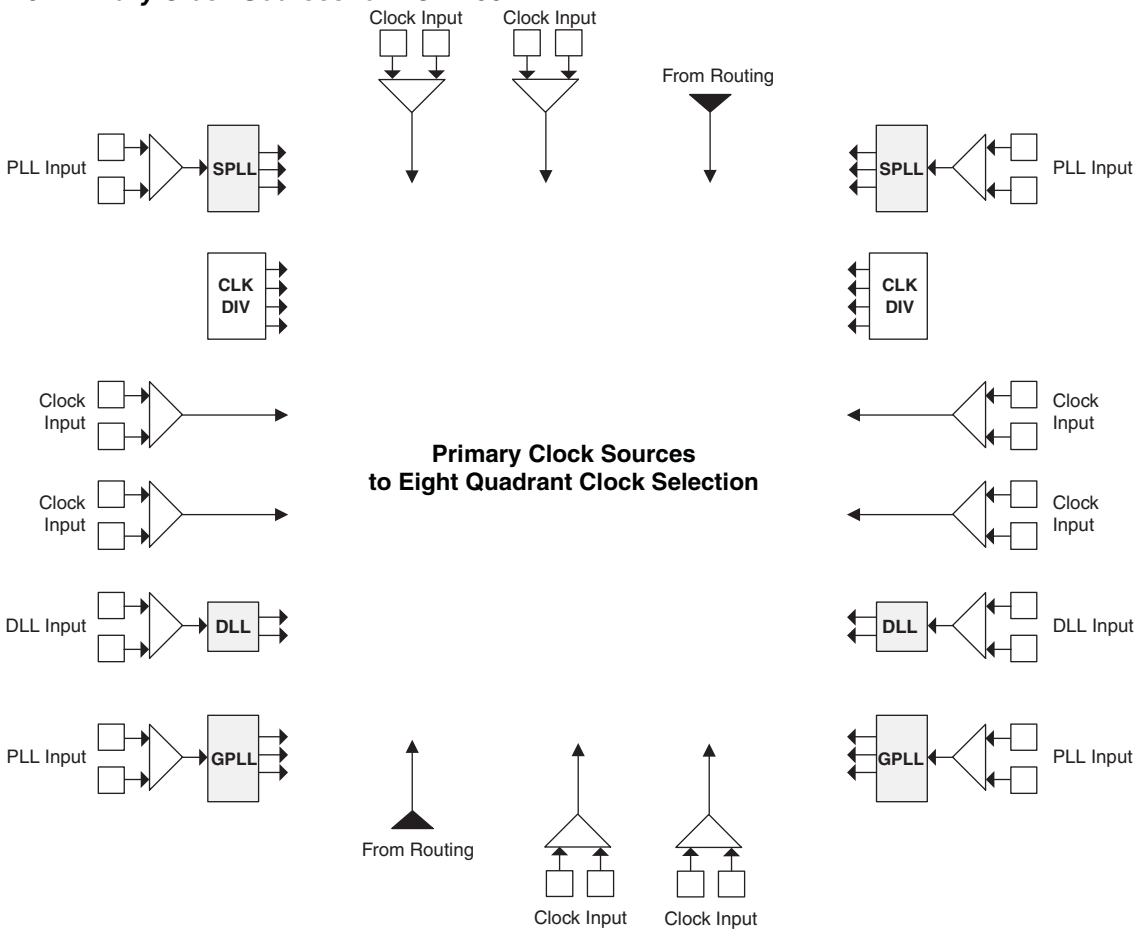
The Lattice design tools support the creation of a variety of different size memories. Where appropriate, the software will construct these using distributed memory primitives that represent the capabilities of the PFU. Table 2-3 shows the number of slices required to implement different distributed RAM primitives. For more information about using RAM in LatticeECP2/M devices, please see the list of additional technical documentation at the end of this data sheet.

Table 2-3. Number of Slices Required to Implement Distributed RAM

	SPR 16X4	PDPR 16X4
Number of slices	3	3

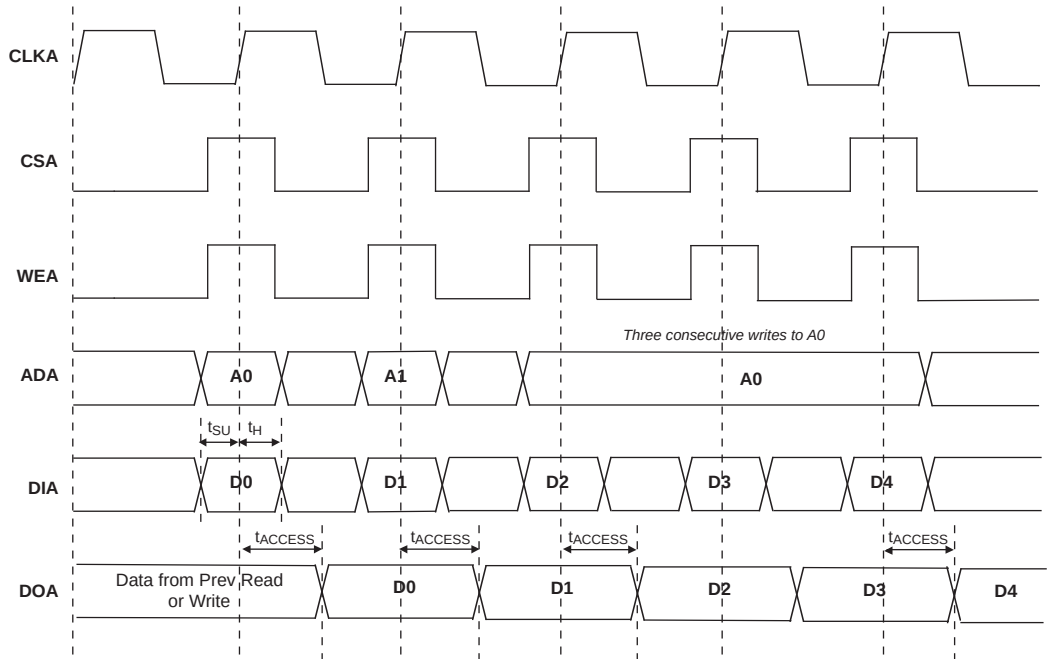
Note: SPR = Single Port RAM, PDPR = Pseudo Dual Port RAM

Figure 2-10. Primary Clock Sources for ECP2-50



Note: This diagram shows sources for the ECP2-50 device. Smaller LatticeECP2 devices have fewer SPLLs. All LatticeECP2M devices have six SPLLs.

Figure 3-11. Write Through (SP Read/Write on Port A, Input Registers Only)



Note: Input data and address are registered at the positive edge of the clock and output data appears after the positive edge of the clock.

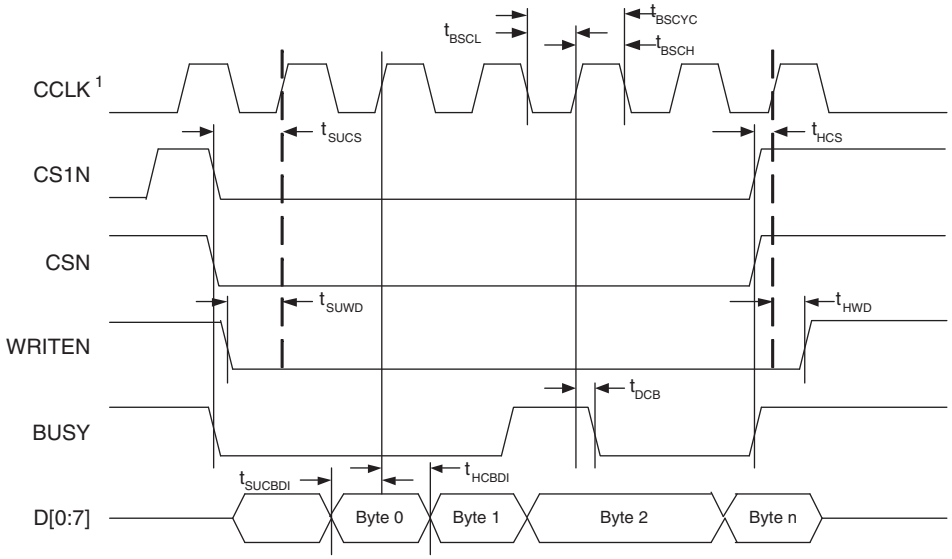
DLL Timing

Over Recommended Operating Conditions

Parameter	Description	Min.	Typ.	Max.	Units
f_{REF}	Input reference clock frequency (on-chip or off-chip)	100	—	500	MHz
f_{FB}	Feedback clock frequency (on-chip or off-chip)	100	—	500	MHz
f_{CLKOP}[1]	Output clock frequency, CLKOP	100	—	500	MHz
f_{CLKOS}[2]	Output clock frequency, CLKOS	25	—	500	MHz
t_{PJIT}	Output clock period jitter (clean input)		—	250	ps p-p
t_{CYJIT}	Output clock cycle to cycle jitter (clean input)			250	ps p-p
t_{DUTY}	Output clock duty cycle (at 50% levels, 50% duty cycle input clock, 50% duty cycle circuit turned off, time reference delay mode)	35		65	%
$t_{DUTYTRD}$	Output clock duty cycle (at 50% levels, arbitrary duty cycle input clock, 50% duty cycle circuit enabled, time reference delay mode)	40		60	%
$t_{DUTYCIR}$	Output clock duty cycle (at 50% levels, arbitrary duty cycle input clock, 50% duty cycle circuit enabled, clock injection removal mode)	40		60	%
t_{SKEW}[3]	Output clock to clock skew between two outputs with the same phase setting	—	—	100	ps
t_{PWH}	Input clock minimum pulse width high (at 80% level)	750	—	—	ps
t_{PWL}	Input clock minimum pulse width low (at 20% level)	750	—	—	ps
t_{INSTB}	Input clock period jitter	—	—	+/-250	ps
t_{LOCK}	DLL lock time	18,500	—	—	cycles
t_{RSWD}	Digital reset minimum pulse width (at 80% level)	3	—	—	ns
t_{PA}	Delay step size	16.5	42	59.4	ps
t_{RANGE1}	Max. delay setting for single delay block (144 taps)	2.376	6	8.553	ns
t_{RANGE4}	Max. delay setting for four chained delay blocks	9.504	24	34.214	ns

1. CLKOP runs at the same frequency as the input clock.
2. CLKOS minimum frequency is obtained with divide by 4.
3. This is intended to be a “path-matching” design guideline and is not a measurable specification.

Figure 3-15. sysCONFIG Parallel Port Write Cycle



1. In Master Parallel Mode the FPGA provides CCLK. In Slave Parallel Mode the external device provides CCLK.

Figure 3-16. sysCONFIG Slave Serial Port Timing

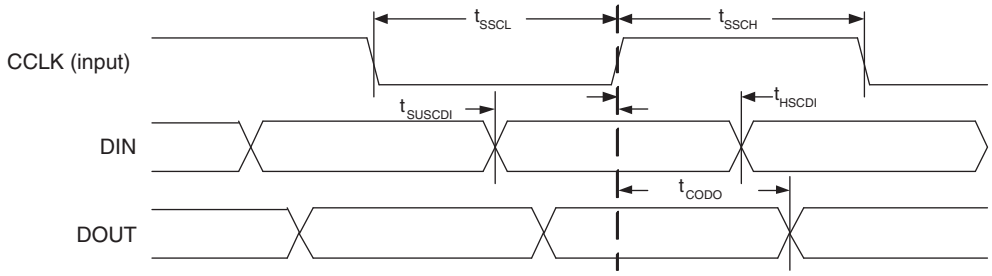
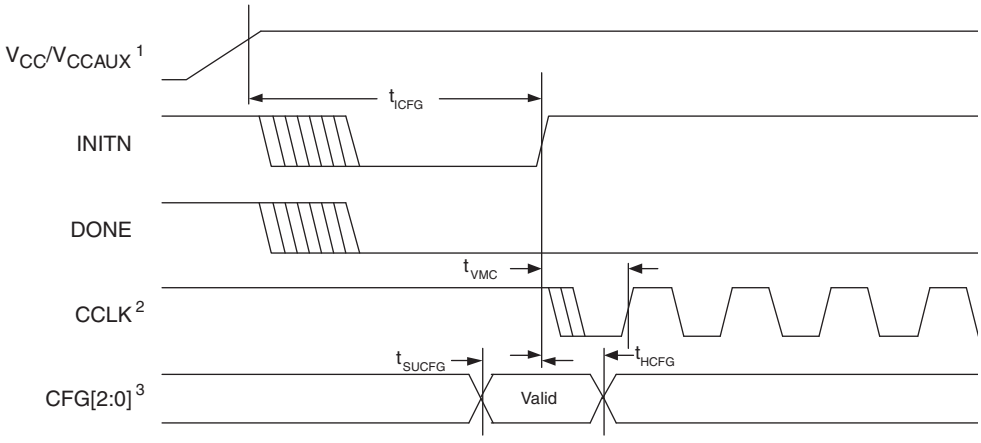


Figure 3-17. Power-On-Reset (POR) Timing



1. Time taken from V_{CC} or V_{CCAUX}, whichever is the last to reach its V_{MIN}.
2. Device is in a Master Mode.
3. The CFG pins are normally static (hard wired).

LFE2-20E/SE and LFE2-35E/SE Logic Signal Connections: 672 fpBGA (Cont.)

LFE2-20E/20SE					LFE2-35E/35SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
GND	GNDIO2	-			GNDIO2	-		
L21	PR18B	2	RDQ16	C (LVDS)*	PR24B	2	RDQ22	C (LVDS)*
K22	PR18A	2	RDQ16	T (LVDS)*	PR24A	2	RDQ22	T (LVDS)*
M24	PR17B	2	RDQ16	C	PR23B	2	RDQ22	C
N23	PR17A	2	RDQ16	T	PR23A	2	RDQ22	T
VCCIO	VCCIO2	2			VCCIO2	2		
K26	PR16B	2	RDQ16	C (LVDS)*	PR22B	2	RDQ22	C (LVDS)*
K25	PR16A	2	RDQS16	T (LVDS)*	PR22A	2	RDQS22	T (LVDS)*
M20	PR15B	2	RDQ16	C	PR21B	2	RDQ22	C
GND	GNDIO2	-			GNDIO2	-		
M19	PR15A	2	RDQ16	T	PR21A	2	RDQ22	T
L22	PR14B	2	RDQ16	C (LVDS)*	PR20B	2	RDQ22	C (LVDS)*
M22	PR14A	2	RDQ16	T (LVDS)*	PR20A	2	RDQ22	T (LVDS)*
K21	PR13B	2	RDQ16	C	PR19B	2	RDQ22	C
VCCIO	VCCIO2	2			VCCIO2	2		
M21	PR13A	2	RDQ16	T	PR19A	2	RDQ22	T
K24	PR12B	2	RDQ16	C (LVDS)*	PR18B	2	RDQ22	C (LVDS)*
J24	PR12A	2	RDQ16	T (LVDS)*	PR18A	2	RDQ22	T (LVDS)*
GND	GNDIO2	-			GNDIO2	-		
VCCIO	VCCIO2	2			VCCIO2	2		
L20	VCC	-			NC	-		
GND	GNDIO2	-			GNDIO2	-		
J26	NC	-			NC	-		
J25	NC	-			NC	-		
J23	NC	-			NC	-		
K23	NC	-			NC	-		
VCCIO	VCCIO2	2			VCCIO2	2		
H26	NC	-			NC	-		
H25	NC	-			NC	-		
H24	NC	-			NC	-		
GND	GNDIO2	-			GNDIO2	-		
H23	NC	-			NC	-		
VCCIO	VCCIO2	2			VCCIO2	2		
G26	PR11B	2	RDQ8	C	PR17B	2	RDQ14	C
GND	GNDIO2	-			GNDIO2	-		
G25	PR11A	2	RDQ8	T	PR17A	2	RDQ14	T
F26	PR10B	2	RDQ8	C (LVDS)*	PR16B	2	RDQ14	C (LVDS)*
F25	PR10A	2	RDQ8	T (LVDS)*	PR16A	2	RDQ14	T (LVDS)*
K20	PR9B	2	RDQ8	C	PR15B	2	RDQ14	C
VCCIO	VCCIO2	2			VCCIO2	2		
L19	PR9A	2	RDQ8	T	PR15A	2	RDQ14	T
E26	PR8B	2	RDQ8	C (LVDS)*	PR14B	2	RDQ14	C (LVDS)*
E25	PR8A	2	RDQS8	T (LVDS)*	PR14A	2	RDQS14	T (LVDS)*
GND	GNDIO2	-			GNDIO2	-		
J22	PR7B	2	RDQ8	C	PR13B	2	RDQ14	C
H22	PR7A	2	RDQ8	T	PR13A	2	RDQ14	T

LFE2-20E/SE and LFE2-35E/SE Logic Signal Connections: 672 fpBGA (Cont.)

LFE2-20E/20SE					LFE2-35E/35SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
N15	GND	-			GND	-		
N17	GND	-			GND	-		
P10	GND	-			GND	-		
P12	GND	-			GND	-		
P13	GND	-			GND	-		
P14	GND	-			GND	-		
P15	GND	-			GND	-		
P17	GND	-			GND	-		
R13	GND	-			GND	-		
R14	GND	-			GND	-		
T10	GND	-			GND	-		
T11	GND	-			GND	-		
T16	GND	-			GND	-		
T17	GND	-			GND	-		
T24	GND	-			GND	-		
T3	GND	-			GND	-		
U10	GND	-			GND	-		
U11	GND	-			GND	-		
U13	GND	-			GND	-		
U14	GND	-			GND	-		
U16	GND	-			GND	-		
U17	GND	-			GND	-		
V13	GND	-			GND	-		
V14	GND	-			GND	-		
V21	GND	-			GND	-		
V6	GND	-			GND	-		
M3	NC	-			NC	-		
N6	NC	-			NC	-		
P24	NC	-			NC	-		

* Supports true LVDS. Other differential signals must be emulated with external resistors.
** These dedicated input pins can be used for GPLLs or GDLLs within the respective quadrant.
***Due to packaging bond out option, this DQS does not have all the necessary DQ pins bonded out for a full 8-bit data width.

Note: VCCIO and GND pads are used to determine the average DC current drawn by I/Os between GND/VCCIO connections, or between the last GND/VCCIO in an I/O bank and the end of an I/O bank. The substrate pads listed in the Pin Table do not necessarily have a one to one connection with a package ball or pin.

LFE2-70E/SE Logic Signal Connections: 900 fpBGA (Cont.)

LFE2-70E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential
R14	GND	-		
R15	GND	-		
R16	GND	-		
R17	GND	-		
R18	GND	-		
R19	GND	-		
R20	GND	-		
T11	GND	-		
T12	GND	-		
T13	GND	-		
T14	GND	-		
T15	GND	-		
T16	GND	-		
T17	GND	-		
T18	GND	-		
T19	GND	-		
T20	GND	-		
U11	GND	-		
U12	GND	-		
U13	GND	-		
U14	GND	-		
U15	GND	-		
U16	GND	-		
U17	GND	-		
U18	GND	-		
U19	GND	-		
U20	GND	-		
V12	GND	-		
V13	GND	-		
V14	GND	-		
V15	GND	-		
V16	GND	-		
V17	GND	-		
V18	GND	-		
V19	GND	-		
V28	GND	-		
V3	GND	-		
W12	GND	-		
W13	GND	-		
W14	GND	-		
W15	GND	-		
W16	GND	-		
W17	GND	-		

LFE2M20E/SE and LFE2M35E/SE Logic Signal Connections: 484 fpBGA (Cont.)

LFE2M20E/SE					LFE2M35E/SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
V5	PL51A	6	LDQS51	T (LVDS)*	PL66A	6	LDQS66	T (LVDS)*
U4	PL51B	6	LDQ51	C (LVDS)*	PL66B	6	LDQ66	C (LVDS)*
V1	PL52A	6	LDQ51	T	PL67A	6	LDQ66	T
VCCIO	VCCIO6	6			VCCIO6	6		
V3	PL52B	6	LDQ51	C	PL67B	6	LDQ66	C
W1	PL53A	6	LDQ51	T (LVDS)*	PL68A	6	LDQ66	T (LVDS)*
Y1	PL53B	6	LDQ51	C (LVDS)*	PL68B	6	LDQ66	C (LVDS)*
AA1	PL54A	6	LDQ51	T	PL69A	6	LDQ66	T
GNDIO	GNDIO6	-			GNDIO6	-		
AA2	PL54B	6	LDQ51	C	PL69B	6	LDQ66	C
V4	TCK	-			TCK	-		
Y2	TDI	-			TDI	-		
Y3	TMS	-			TMS	-		
W3	TDO	-			TDO	-		
W4	VCCJ	-			VCCJ	-		
W5	PB2A	5	BDQ6	T	PB2A	5	BDQ6	T
Y4	PB2B	5	BDQ6	C	PB2B	5	BDQ6	C
W6	PB3A	5	BDQ6	T	PB3A	5	BDQ6	T
V6	PB3B	5	BDQ6	C	PB3B	5	BDQ6	C
AA3	PB4A	5	BDQ6	T	PB4A	5	BDQ6	T
VCCIO	VCCIO5	5			VCCIO5	5		
AB2	PB4B	5	BDQ6	C	PB4B	5	BDQ6	C
T8	PB5A	5	BDQ6	T	PB5A	5	BDQ6	T
U7	PB5B	5	BDQ6	C	PB5B	5	BDQ6	C
U8	PB6A	5	BDQS6	T	PB6A	5	BDQS6	T
GNDIO	GNDIO5	-			GNDIO5	-		
T9	PB6B	5	BDQ6	C	PB6B	5	BDQ6	C
V8	PB7A	5	BDQ6	T	PB7A	5	BDQ6	T
W8	PB7B	5	BDQ6	C	PB7B	5	BDQ6	C
Y6	PB8A	5	BDQ6	T	PB8A	5	BDQ6	T
VCCIO	VCCIO5	5			VCCIO5	5		
Y5	PB8B	5	BDQ6	C	PB8B	5	BDQ6	C
AB3	PB9A	5	BDQ6	T	PB9A	5	BDQ6	T
AB4	PB9B	5	BDQ6	C	PB9B	5	BDQ6	C
AB5	PB10A	5	BDQ6	T	PB10A	5	BDQ6	T
GNDIO	GNDIO5	-			GNDIO5	-		
AA6	PB10B	5	BDQ6	C	PB10B	5	BDQ6	C
V9	PB13A	5	BDQ15	T	PB31A	5	BDQ33	T
U9	PB13B	5	BDQ15	C	PB31B	5	BDQ33	C
VCCIO	VCCIO5	5			VCCIO5	5		
-	-	-			GNDIO5	-		
U10	PB14A	5	BDQ15	T	PB32A	5	BDQ33	T
T10	PB14B	5	BDQ15	C	PB32B	5	BDQ33	C
GNDIO	GNDIO5	-			GNDIO5	-		
W9	PB15A	5	BDQS15****	T	PB33A	5	BDQS33****	T
Y8	PB15B	5	BDQ15	C	PB33B	5	BDQ33	C
AA7	PB16A	5	VREF2_5/BDQ15	T	PB34A	5	VREF2_5/BDQ33	T
Y7	PB16B	5	VREF1_5/BDQ15	C	PB34B	5	VREF1_5/BDQ33	C

LFE2M50E/SE Logic Signal Connections: 484 fpBGA (Cont.)

LFE2M50E/SE				
Ball Number	**Ball/Pad Function**	**Bank**	**Dual Function**	**Differential**
D9	PT45A	0	VREF1_0	T
A2	PT44B	0		C
VCCIO	VCCIO0	0		
A3	PT44A	0		T
B3	PT43B	0		C
C4	PT43A	0		T
E10	PT42B	0		C
F10	PT42A	0		T
C7	PT41B	0		C
GNDIO	GNDIO0	-		
B6	PT41A	0		T
C6	PT40B	0		C
VCCIO	VCCIO0	0		
C5	PT40A	0		T
C8	PT39B	0		C
D8	PT39A	0		T
E8	PT38B	0		C
E9	PT38A	0		T
GNDIO	GNDIO0	-		
VCCIO	VCCIO0	0		
F8	PT10B	0		C
GNDIO	GNDIO0	-		
G8	PT10A	0		T
F7	PT9B	0		C
G7	PT9A	0		T
C3	PT8B	0		C
VCCIO	VCCIO0	0		
D4	PT8A	0		T
F6	PT7B	0		C
E6	PT7A	0		T
E5	PT6B	0		C
D6	PT6A	0		T
D3	PT5B	0		C
GNDIO	GNDIO0	-		
E3	PT5A	0		T
D5	PT4B	0		C
VCCIO	VCCIO0	0		
E4	PT4A	0		T
C2	PT3B	0		C
B2	PT3A	0		T
B1	PT2B	0		C
C1	PT2A	0		T
J10	VCC	-		

LFE2M50E/SE Logic Signal Connections: 484 fpBGA (Cont.)

LFE2M50E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential
J11	VCC	-		
J12	VCC	-		
J13	VCC	-		
K14	VCC	-		
K9	VCC	-		
L14	VCC	-		
L9	VCC	-		
M14	VCC	-		
M9	VCC	-		
N14	VCC	-		
N9	VCC	-		
P10	VCC	-		
P11	VCC	-		
P12	VCC	-		
P13	VCC	-		
B5	VCCIO0	0		
B9	VCCIO0	0		
E7	VCCIO0	0		
H9	VCCIO0	0		
D13	VCCIO1	1		
E16	VCCIO1	1		
H14	VCCIO1	1		
E21	VCCIO2	2		
G18	VCCIO2	2		
J15	VCCIO2	2		
K19	VCCIO2	2		
N19	VCCIO3	3		
P15	VCCIO3	3		
T18	VCCIO3	3		
V21	VCCIO3	3		
AA18	VCCIO4	4		
R14	VCCIO4	4		
V16	VCCIO4	4		
W13	VCCIO4	4		
AA5	VCCIO5	5		
R9	VCCIO5	5		
V7	VCCIO5	5		
W10	VCCIO5	5		
N4	VCCIO6	6		
P8	VCCIO6	6		
T5	VCCIO6	6		
V2	VCCIO6	6		
E2	VCCIO7	7		

LFE2M35E/SE and LFE2M50E/SE Logic Signal Connections: 672 fpBGA (Cont.)

LFE2M35E/SE					LFE2M50E/SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
K19	PR16A	2	RDQ15	T	PR19A	2		T
G24	PR15B	2	RDQ15	C (LVDS)*	PR18B	2		C*
G23	PR15A	2	RDQS15	T (LVDS)*	PR18A	2		T*
GNDIO	GNDIO2	-			GNDIO2	-		
J18	PR14B	2	RDQ15	C	PR14B	2		C
F22	PR14A	2	RDQ15	T	PR14A	2		T
-	-	-			VCCIO2	2		
F23	PR13B	2	RDQ15	C (LVDS)*	PR13B	2		C*
F24	PR13A	2	RDQ15	T (LVDS)*	PR13A	2		T*
VCCIO	VCCIO2	2			-	-		
H20	PR12B	2	RUM0_SPLLC_FB_A/RDQ15	C	PR12B	2	RUM0_SPLLC_FB_A	C
-	-	-			GNDIO2	-		
F21	PR12A	2	RUM0_SPLLT_FB_A/RDQ15	T	PR12A	2	RUM0_SPLLT_FB_A	T
G26	PR11B	2	RUM0_SPLLC_IN_A/RDQ15	C (LVDS)*	PR11B	2	RUM0_SPLLC_IN_A	C*
F26	PR11A	2	RUM0_SPLLT_IN_A/RDQ15	T (LVDS)*	PR11A	2	RUM0_SPLLT_IN_A	T*
-	-	-			VCCIO2	2		
E24	PR9B	2	VREF2_2	C	PR9B	2	VREF2_2	C
GNDIO	GNDIO2	-			GNDIO2	-		
E23	PR9A	2	VREF1_2	T	PR9A	2	VREF1_2	T
VCCIO	VCCIO4	4			VCCIO2	2		
H19	XRES	-			XRES	-		
C25	URC_SQ_VCCRX0	12			URC_SQ_VCCRX0	12		
A24	URC_SQ_HDINP0	12		T	URC_SQ_HDINP0	12		T
B25	URC_SQ_VCCIB0	12			URC_SQ_VCCIB0	12		
B24	URC_SQ_HDINN0	12		C	URC_SQ_HDINN0	12		C
C22	URC_SQ_VCCTX0	12			URC_SQ_VCCTX0	12		
A21	URC_SQ_HDOUTP0	12		T	URC_SQ_HDOUTP0	12		T
A22	URC_SQ_VCCOB0	12			URC_SQ_VCCOB0	12		
B21	URC_SQ_HDOUTN0	12		C	URC_SQ_HDOUTN0	12		C
C21	URC_SQ_VCCTX1	12			URC_SQ_VCCTX1	12		
B20	URC_SQ_HDOUTN1	12		C	URC_SQ_HDOUTN1	12		C
C20	URC_SQ_VCCOB1	12			URC_SQ_VCCOB1	12		
A20	URC_SQ_HDOUTP1	12		T	URC_SQ_HDOUTP1	12		T
C24	URC_SQ_VCCRX1	12			URC_SQ_VCCRX1	12		
B23	URC_SQ_HDINN1	12		C	URC_SQ_HDINN1	12		C
C23	URC_SQ_VCCIB1	12			URC_SQ_VCCIB1	12		
A23	URC_SQ_HDINP1	12		T	URC_SQ_HDINP1	12		T
B19	URC_SQ_VCCAUX33	12			URC_SQ_VCCAUX33	12		
E19	URC_SQ_REFCLKN	12		C	URC_SQ_REFCLKN	12		C
D19	URC_SQ_REFCLKP	12		T	URC_SQ_REFCLKP	12		T
C19	URC_SQ_VCCP	12			URC_SQ_VCCP	12		
A15	URC_SQ_HDINP2	12		T	URC_SQ_HDINP2	12		T

LFE2M50E/SE and LFE2M70E/SE Logic Signal Connections: 900 fpBGA (Cont.)

LFE2M50E/SE					LFE2M70E/SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
AH25	LRC_SQ_VCCOB1	13			LRC_SQ_VCCOB1	13		
AJ25	LRC_SQ_HDOUTN1	13		C	LRC_SQ_HDOUTN1	13		C
AH26	LRC_SQ_VCCTX1	13			LRC_SQ_VCCTX1	13		
AJ26	LRC_SQ_HDOUTN0	13		C	LRC_SQ_HDOUTN0	13		C
AK27	LRC_SQ_VCCOB0	13			LRC_SQ_VCCOB0	13		
AK26	LRC_SQ_HDOUTP0	13		T	LRC_SQ_HDOUTP0	13		T
AH27	LRC_SQ_VCCTX0	13			LRC_SQ_VCCTX0	13		
AJ29	LRC_SQ_HDINN0	13		C	LRC_SQ_HDINN0	13		C
AJ30	LRC_SQ_VCCIB0	13			LRC_SQ_VCCIB0	13		
AK29	LRC_SQ_HDINP0	13		T	LRC_SQ_HDINP0	13		T
AH30	LRC_SQ_VCCRX0	13			LRC_SQ_VCCRX0	13		
AG27	CFG2	8			CFG2	8		
AD25	CFG1	8			CFG1	8		
AG28	CFG0	8			CFG0	8		
AG30	PROGRAMN	8			PROGRAMN	8		
AG29	CCLK	8			CCLK	8		
AC24	INITN	8			INITN	8		
AF27	DONE	8			DONE	8		
GNDIO	GNDIO8	-			GNDIO8	-		
AF28	WRITEN***	8			WRITEN***	8		
AE26	CS1N***	8			CS1N***	8		
AB23	CSN***	8			CSN***	8		
AF29	D0/SPIFASTN***	8			D0/SPIFASTN***	8		
VCCIO	VCCIO8	8			VCCIO8	8		
AF30	D1***	8			D1***	8		
AD26	D2***	8			D2***	8		
AE29	D3***	8			D3***	8		
GNDIO	GNDIO8	-			GNDIO8	-		
AE30	D4***	8			D4***	8		
AD29	D5***	8			D5***	8		
AC25	D6***	8			D6***	8		
AD30	D7/SPID0***	8			D7/SPID0***	8		
VCCIO	VCCIO8	8			VCCIO8	8		
AA22	DI/CSSPI0N***	8			DI/CSSPI0N***	8		
AC26	DOUT/CSON/ CSSPI1N***	8			DOUT/CSON/ CSSPI1N***	8		
AA23	BUSY/SISPI***	8			BUSY/SISPI***	8		
AB22	RLM0_PLLCAP	3			RLM0_PLLCAP	3		
AC27	PR65B	3	RLM0_GDLLC_FB_A	C	PR85B	3	RLM0_GDLLC_FB_A/RDQ82	C
GNDIO	GNDIO3	-			GNDIO3	-		
AC28	PR65A	3	RLM0_GDLLT_FB_A	T	PR85A	3	RLM0_GDLLT_FB_A/RDQ82	T
AC29	PR64B	3	RLM0_GDLLC_IN_A**	C (LVDS)*	PR84B	3	RLM0_GDLLC_IN_A**/RDQ82	C (LVDS)*
AC30	PR64A	3	RLM0_GDLLT_IN_A**	T (LVDS)*	PR84A	3	RLM0_GDLLT_IN_A**/RDQ82	T (LVDS)*
AB30	PR63B	3	RLM0_GPLLC_IN_A**	C	PR83B	3	RLM0_GPLLC_IN_A**/RDQ82	C
VCCIO	VCCIO3	3			VCCIO3	3		
AA30	PR63A	3	RLM0_GPLLT_IN_A**	T	PR83A	3	RLM0_GPLLT_IN_A**/RDQ82	T
AB29	PR62B	3	RLM0_GPLLC_FB_A	C (LVDS)*	PR82B	3	RLM0_GPLLC_FB_A/RDQ82	C (LVDS)*
AB28	PR62A	3	RLM0_GPLLT_FB_A	T (LVDS)*	PR82A	3	RLM0_GPLLT_FB_A/RDQS82	T (LVDS)*
GNDIO	GNDIO3	-			GNDIO3	-		

LFE2M100E/SE Logic Signal Connections: 900 fpBGA (Cont.)

LFE2M100E/SE				
Ball Number	**Ball/Pad Function**	**Bank**	**Dual Function**	**Differential**
H14	PT61A	0		T
A14	PT60B	0		C
B14	PT60A	0		T
D13	PT59B	0		C
GNDIO	GNDIO0	-		
F13	PT59A	0		T
G13	PT58B	0		C
VCCIO	VCCIO0	0		
J11	PT58A	0		T
D4	PT57B	0		
D5	PT56A	0		
E5	PT55B	0		C
F6	PT55A	0		T
GNDIO	GNDIO0	-		
VCCIO	VCCIO0	0		
F7	PT52B	0		C
D8	PT52A	0		T
GNDIO	GNDIO0	-		
J13	PT50B	0		C
G11	PT50A	0		T
H13	PT49B	0		C
H12	PT49A	0		T
VCCIO	VCCIO0	0		
E8	PT48B	0		C
D9	PT48A	0		T
D12	PT46B	0		C
GNDIO	GNDIO0	-		
E13	PT46A	0		T
VCCIO	VCCIO0	0		
GNDIO	GNDIO0	-		
J12	PT31B	0		C
-	-	-		
VCCIO	VCCIO0	0		
H10	PT31A	0		T
E12	PT30B	0		C
D11	PT30A	0		T
H11	PT29B	0		C
F11	PT29A	0		T
C13	ULC_SQ_VCCRX0	11		
A12	ULC_SQ_HDINP0	11		T
B13	ULC_SQ_VCCIB0	11		
B12	ULC_SQ_HDINN0	11		C
C10	ULC_SQ_VCCTX0	11		

LFE2M70E/SE and LFE2M100E/SE Logic Signal Connections: 1152 fpBGA

LFE2M70E/SE				LFE2M100E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
VCCIO	VCCIO7	7			VCCIO7	7		
F4	PL9A	7	VREF2_7	T	PL9A	7	VREF2_7	T
F3	PL9B	7	VREF1_7	C	PL9B	7	VREF1_7	C
GNDIO	GNDIO7	-			GNDIO7	-		
E1	PL11A	7	LUM0_SPLLT_IN_A/LDQ15	T (LVDS)*	PL11A	7	LUM0_SPLLT_IN_A/LDQ15	T (LVDS)*
E2	PL11B	7	LUM0_SPLLC_IN_A/LDQ15	C (LVDS)*	PL11B	7	LUM0_SPLLC_IN_A/LDQ15	C (LVDS)*
K9	PL12A	7	LUM0_SPLLT_FB_A/LDQ15	T	PL12A	7	LUM0_SPLLT_FB_A/LDQ15	T
H7	PL12B	7	LUM0_SPLLC_FB_A/LDQ15	C	PL12B	7	LUM0_SPLLC_FB_A/LDQ15	C
VCCIO	VCCIO7	7			VCCIO7	7		
F1	PL13A	7	LDQ15	T (LVDS)*	PL13A	7	LDQ15	T (LVDS)*
F2	PL13B	7	LDQ15	C (LVDS)*	PL13B	7	LDQ15	C (LVDS)*
J8	PL14A	7	LDQ15	T	PL14A	7	LDQ15	T
H6	PL14B	7	LDQ15	C	PL14B	7	LDQ15	C
GNDIO	GNDIO7	-			GNDIO7	-		
G2	PL15A	7	LDQS15	T (LVDS)*	PL15A	7	LDQS15	T (LVDS)*
G1	PL15B	7	LDQ15	C (LVDS)*	PL15B	7	LDQ15	C (LVDS)*
J7	PL16A	7	LDQ15	T	PL16A	7	LDQ15	T
VCCIO	VCCIO7	7			VCCIO7	7		
L8	PL16B	7	LDQ15	C	PL16B	7	LDQ15	C
L9	PL17A	7	LDQ15	T (LVDS)*	PL17A	7	LDQ15	T (LVDS)*
L10	PL17B	7	LDQ15	C (LVDS)*	PL17B	7	LDQ15	C (LVDS)*
H5	PL18A	7	LDQ15	T	PL18A	7	LDQ15	T
GNDIO	GNDIO7	-			GNDIO7	-		
J6	PL18B	7	LDQ15	C	PL18B	7	LDQ15	C
H2	NC	-			PL19A	7	LDQ23	T (LVDS)*
H1	NC	-			PL19B	7	LDQ23	C (LVDS)*
G5	NC	-			PL20A	7	LDQ23	T
G6	NC	-			PL20B	7	LDQ23	C
M9	NC	-			PL21A	7	LDQ23	T (LVDS)*
-	-	-			VCCIO7	7		
M10	NC	-			PL21B	7	LDQ23	C (LVDS)*
H3	NC	-			PL22A	7	LDQ23	T
H4	NC	-			PL22B	7	LDQ23	C
J2	PL19A	7		T (LVDS)*	PL23A	7	LDQS23	T (LVDS)*
-	-	-			GNDIO7	-		
J1	PL19B	7		C (LVDS)*	PL23B	7	LDQ23	C (LVDS)*
K2	PL20A	7		T	PL24A	7	LDQ23	T
K1	PL20B	7		C	PL24B	7	LDQ23	C
VCCIO	VCCIO7	7			VCCIO7	7		
J4	PL21A	7		T (LVDS)*	PL25A	7	LDQ23	T (LVDS)*
J3	PL21B	7		C (LVDS)*	PL25B	7	LDQ23	C (LVDS)*
J5	PL22A	7		T	PL26A	7	LDQ23	T
K5	PL22B	7		C	PL26B	7	LDQ23	C
GNDIO	GNDIO7	-			GNDIO7	-		
L2	PL24A	7	LDQ28	T (LVDS)*	PL28A	7	LDQ32	T (LVDS)*
L1	PL24B	7	LDQ28	C (LVDS)*	PL28B	7	LDQ32	C (LVDS)*
L7	PL25A	7	LDQ28	T	PL29A	7	LDQ32	T
K6	PL25B	7	LDQ28	C	PL29B	7	LDQ32	C
VCCIO	VCCIO7	7			VCCIO7	7		

LFE2M70E/SE and LFE2M100E/SE Logic Signal Connections: 1152 fpBGA (Cont.)

LFE2M70E/SE				LFE2M100E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
E5	ULC_SQ_REFCLKN	11		C	ULC_SQ_REFCLKN	11		C
D5	ULC_SQ_REFCLKP	11		T	ULC_SQ_REFCLKP	11		T
D6	ULC_SQ_VCCP	11			ULC_SQ_VCCP	11		
C5	ULC_SQ_HDINP2	11		T	ULC_SQ_HDINP2	11		T
D4	ULC_SQ_VCCIB2	11			ULC_SQ_VCCIB2	11		
C4	ULC_SQ_HDINN2	11		C	ULC_SQ_HDINN2	11		C
B5	ULC_SQ_VCCRX2	11			ULC_SQ_VCCRX2	11		
A5	ULC_SQ_HDOUTP2	11		T	ULC_SQ_HDOUTP2	11		T
D3	ULC_SQ_VCCOB2	11			ULC_SQ_VCCOB2	11		
A4	ULC_SQ_HDOUTN2	11		C	ULC_SQ_HDOUTN2	11		C
B4	ULC_SQ_VCCTX2	11			ULC_SQ_VCCTX2	11		
A3	ULC_SQ_HDOUTN3	11		C	ULC_SQ_HDOUTN3	11		C
C1	ULC_SQ_VCCOB3	11			ULC_SQ_VCCOB3	11		
A2	ULC_SQ_HDOUTP3	11		T	ULC_SQ_HDOUTP3	11		T
B3	ULC_SQ_VCCTX3	11			ULC_SQ_VCCTX3	11		
C3	ULC_SQ_HDINN3	11		C	ULC_SQ_HDINN3	11		C
B1	ULC_SQ_VCCIB3	11			ULC_SQ_VCCIB3	11		
C2	ULC_SQ_HDINP3	11		T	ULC_SQ_HDINP3	11		T
B2	ULC_SQ_VCCRX3	11			ULC_SQ_VCCRX3	11		
AA13	VCC	-			VCC	-		
AA14	VCC	-			VCC	-		
AA15	VCC	-			VCC	-		
AA16	VCC	-			VCC	-		
AA17	VCC	-			VCC	-		
AA18	VCC	-			VCC	-		
AA19	VCC	-			VCC	-		
AA20	VCC	-			VCC	-		
AA21	VCC	-			VCC	-		
AA22	VCC	-			VCC	-		
AB14	VCC	-			VCC	-		
AB15	VCC	-			VCC	-		
AB20	VCC	-			VCC	-		
AB21	VCC	-			VCC	-		
N14	VCC	-			VCC	-		
N15	VCC	-			VCC	-		
N20	VCC	-			VCC	-		
N21	VCC	-			VCC	-		
P13	VCC	-			VCC	-		
P14	VCC	-			VCC	-		
P15	VCC	-			VCC	-		
P16	VCC	-			VCC	-		
P17	VCC	-			VCC	-		
P18	VCC	-			VCC	-		
P19	VCC	-			VCC	-		
P20	VCC	-			VCC	-		
P21	VCC	-			VCC	-		
P22	VCC	-			VCC	-		
R13	VCC	-			VCC	-		
R14	VCC	-			VCC	-		

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2M100E-5FN1152C	520	1.2V	-5	Lead-Free fpBGA	1152	COM	100
LFE2M100E-6FN1152C	520	1.2V	-6	Lead-Free fpBGA	1152	COM	100
LFE2M100E-7FN1152C	520	1.2V	-7	Lead-Free fpBGA	1152	COM	100
LFE2M100E-5FN900C	416	1.2V	-5	Lead-Free fpBGA	900	COM	100
LFE2M100E-6FN900C	416	1.2V	-6	Lead-Free fpBGA	900	COM	100
LFE2M100E-7FN900C	416	1.2V	-7	Lead-Free fpBGA	900	COM	100

Industrial

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2M20E-5FN484I	304	1.2V	-5	Lead-Free fpBGA	484	IND	20
LFE2M20E-6FN484I	304	1.2V	-6	Lead-Free fpBGA	484	IND	20
LFE2M20E-5FN256I	140	1.2V	-5	Lead-Free fpBGA	256	IND	20
LFE2M20E-6FN256I	140	1.2V	-6	Lead-Free fpBGA	256	IND	20

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2M35E-5FN672I	410	1.2V	-5	Lead-Free fpBGA	672	IND	35
LFE2M35E-6FN672I	410	1.2V	-6	Lead-Free fpBGA	672	IND	35
LFE2M35E-5FN484I	303	1.2V	-5	Lead-Free fpBGA	484	IND	35
LFE2M35E-6FN484I	303	1.2V	-6	Lead-Free fpBGA	484	IND	35
LFE2M35E-5FN256I	140	1.2V	-5	Lead-Free fpBGA	256	IND	35
LFE2M35E-6FN256I	140	1.2V	-6	Lead-Free fpBGA	256	IND	35

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2M50E-5FN900I	410	1.2V	-5	Lead-Free fpBGA	900	Ind	50
LFE2M50E-6FN900I	410	1.2V	-6	Lead-Free fpBGA	900	Ind	50
LFE2M50E-5FN672I	372	1.2V	-5	Lead-Free fpBGA	672	Ind	50
LFE2M50E-6FN672I	372	1.2V	-6	Lead-Free fpBGA	672	Ind	50
LFE2M50E-5FN484I	270	1.2V	-5	Lead-Free fpBGA	484	Ind	50
LFE2M50E-6FN484I	270	1.2V	-6	Lead-Free fpBGA	484	Ind	50

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2M70E-5FN1152I	436	1.2V	-5	Lead-Free fpBGA	1152	Ind	70
LFE2M70E-6FN1152I	436	1.2V	-6	Lead-Free fpBGA	1152	Ind	70
LFE2M70E-5FN900I	416	1.2V	-5	Lead-Free fpBGA	900	Ind	70
LFE2M70E-6FN900I	416	1.2V	-6	Lead-Free fpBGA	900	Ind	70

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2M70SE-5F1152C	436	1.2V	-5	fpBGA	1152	Com	70
LFE2M70SE-6F1152C	436	1.2V	-6	fpBGA	1152	Com	70
LFE2M70SE-7F1152C	436	1.2V	-7	fpBGA	1152	Com	70
LFE2M70SE-5F900C	416	1.2V	-5	fpBGA	900	Com	70
LFE2M70SE-6F900C	416	1.2V	-6	fpBGA	900	Com	70
LFE2M70SE-7F900C	416	1.2V	-7	fpBGA	900	Com	70

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2M100SE-5F1152C	520	1.2V	-5	fpBGA	1152	Com	100
LFE2M100SE-6F1152C	520	1.2V	-6	fpBGA	1152	Com	100
LFE2M100SE-7F1152C	520	1.2V	-7	fpBGA	1152	Com	100
LFE2M100SE-5F900C	416	1.2V	-5	fpBGA	900	Com	100
LFE2M100SE-6F900C	416	1.2V	-6	fpBGA	900	Com	100
LFE2M100SE-7F900C	416	1.2V	-7	fpBGA	900	Com	100

Date	Version	Section	Change Summary
November 2009 (cont.)	03.5 (cont.)	Pinout Information (cont.)	LatticeECP2M Pin Information Summary, LFE2M50, LFE2M70 and LFE2M100 table - corrected values for LFE2M50, 672 fpBGA in Available DDR-Interfaces per I/O Bank.
			Minor corrections in LFE2M20E/SE and LFE2M35E/SE Logic Signal Connections: 484 fpBGA table.
			Minor corrections in LFE2M50E/SE and LFE2M70E/SE Logic Signal Connections: 900 fpBGA table.
			Minor corrections in LFE2M100E/SE Logic Signal Connections: 900 fpBGA table.
			Updated LFE2-6E/SE and LFE2-12E/SE Logical Signal Connections (changed D1/SPIDS to D1).
		Ordering Information	Updated LatticeECP2M Part Number Description diagram.
March 2010	03.6	DC and Switching Characteristics	Footnote for SED operating frequency added to the sysCONFIG Port Timing Specifications table.
		Pinout Information	Changed Dual Function pin E7 to be D7/SPDI0 in Logic Signal Connections tables. Changed footnote (***) in Logic Signal Connections table.
July 2010	03.7	Architecture	Updated the Typical sysIO Behavior During Power-up text section.
		Pinout Information	Added reference to powerup information.
			Corrected reference to footnote for pins 131 and 132 for the LFE-20E/SE, 208 PQFP.
			Referenced footnote (***) for all D7/SPID0.
			Changed D7*** to D7/SPID0.
			Corrected *** footnote.
		All Sections	Included references to Lattice Diamond design software wherever ispLEVER and ispLeverCORE is specified.
April 2011	03.8	DC and Switching Characteristics	DC Electrical Characteristics table: - Added footnote 3 to I_{IH} - Added footnote 2 to I_{IL}, I_{IH} - Updated C1 and C2 typ. and max. data.
			DLL Timing table – Removed line for t_R and t_F.
			LatticeECP2/M sysCONFIG Port Timing Specifications table – added footnote to t_{DINIT}.
			Figure 3-18 – Corrected label to be PRGM (not PRGMRJ).
		Pinout Information	LFE2-12E/SE and LFE-20/SE Logical Signal Connections for 208 PQFP – Corrected Dual Function information for pins 112, 114, 117, 119.
January 2012	03.9	Multiple	Removed references to ispLEVER design software.
		Architecture	Corrected information regarding SED support.
		DC and Switching Characteristics	Added reference to ESD information.
June 2013	04.0	All	Updated document with new corporate logo.
		Architecture	Architecture Overview – Added information on the state of the register on power up and after configuration.