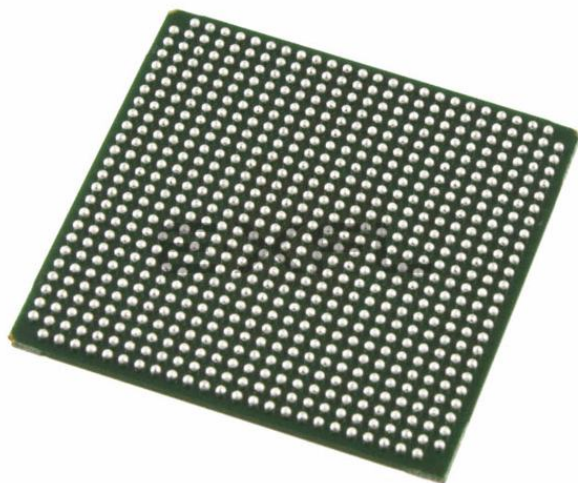




Welcome to [E-XFL.COM](#)

Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

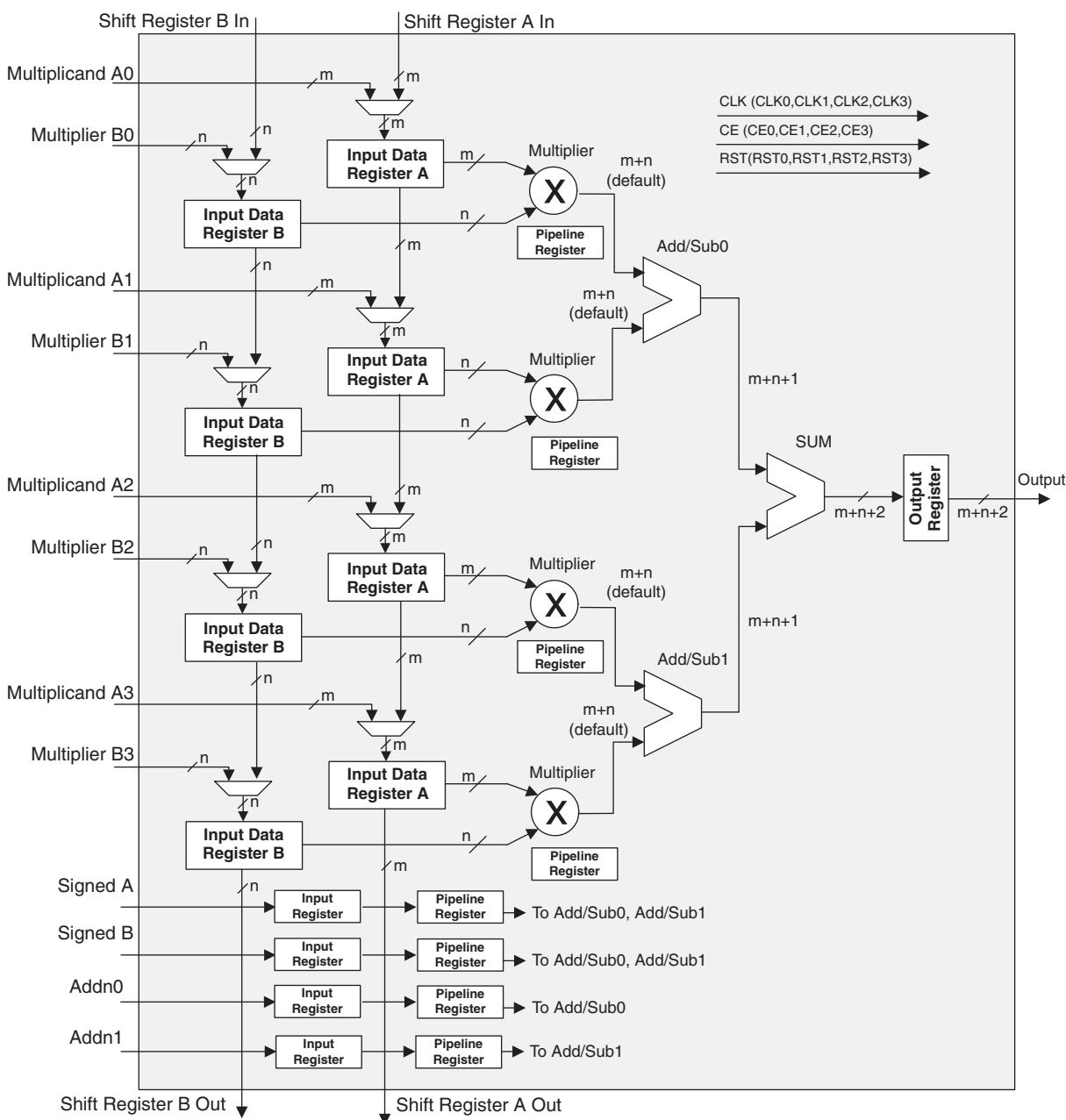
Details

Product Status	Obsolete
Number of LABs/CLBs	8500
Number of Logic Elements/Cells	68000
Total RAM Bits	1056768
Number of I/O	500
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	672-BBGA
Supplier Device Package	672-FPBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfe2-70e-7f672c

MULTADDSUBSUM sysDSP Element

In this case, the operands A0 and B0 are multiplied and the result is added/subtracted with the result of the multiplier operation of operands A1 and B1. Additionally the operands A2 and B2 are multiplied and the result is added/subtracted with the result of the multiplier operation of operands A3 and B3. The result of both addition/subtraction are added in a summation block. The user can enable the input, output and pipeline registers. Figure 2-26 shows the MULTADDSUBSUM sysDSP element.

Figure 2-26. MULTADDSUBSUM



Clock, Clock Enable and Reset Resources

Global Clock, Clock Enable and Reset signals from routing are available to every DSP block. Four Clock, Reset and Clock Enable signals are selected for the sysDSP block. From four clock sources (CLK0, CLK1, CLK2, CLK3)

DC Electrical Characteristics

Over Recommended Operating Conditions

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
$I_{IL}, I_{IH}^{1,2}$	Input or I/O Low Leakage	$0 \leq V_{IN} \leq (V_{CCIO} - 0.2V)$	—	—	10	μA
$I_{IH}^{1,3}$	Input or I/O High Leakage	$(V_{CCIO} - 0.2V) < V_{IN} \leq 3.6V$	—	—	150	μA
I_{PU}	I/O Active Pull-up Current	$0 \leq V_{IN} \leq 0.7 V_{CCIO}$	-30	—	-210	μA
I_{PD}	I/O Active Pull-down Current	$V_{IL} (MAX) \leq V_{IN} \leq V_{IH} (MAX)$	30	—	210	μA
I_{BHLS}	Bus Hold Low Sustaining Current	$V_{IN} = V_{IL} (MAX)$	30	—	—	μA
I_{BHHS}	Bus Hold High Sustaining Current	$V_{IN} = 0.7 V_{CCIO}$	-30	—	—	μA
I_{BHLO}	Bus Hold Low Overdrive Current	$0 \leq V_{IN} \leq V_{CCIO}$	—	—	210	μA
I_{BHHO}	Bus Hold High Overdrive Current	$0 \leq V_{IN} \leq V_{CCIO}$	—	—	-210	μA
V_{BHT}	Bus Hold Trip Points	$0 \leq V_{IN} \leq V_{IH} (MAX)$	$V_{IL} (MAX)$	—	$V_{IH} (MIN)$	V
$C1^4$	I/O Capacitance	$V_{CCIO} = 3.3V, 2.5V, 1.8V, 1.5V, 1.2V,$ $V_{CC} = 1.2V, V_{IO} = 0 \text{ to } V_{IH} (MAX)$	—	5	8	pf
$C2^4$	Dedicated Input Capacitance	$V_{CCIO} = 3.3V, 2.5V, 1.8V, 1.5V, 1.2V,$ $V_{CC} = 1.2V, V_{IO} = 0 \text{ to } V_{IH} (MAX)$	—	5	6	pf

1. Input or I/O leakage current is measured with the pin configured as an input or as an I/O with the output driver tri-stated. It is not measured with the output driver active. Bus maintenance circuits are disabled.
2. When used as V_{REF} maximum leakage = 25 μA
3. Applicable to general purpose I/Os in top and bottom banks.
4. T_A 25°C, $f = 1.0MHz$.

LVPECL

The LatticeECP2/M devices support the differential LVPECL standard. This standard is emulated using complementary LVCMOS outputs in conjunction with a parallel resistor across the driver outputs. The LVPECL input standard is supported by the LVDS differential input buffer. The scheme shown in Figure 3-3 is one possible solution for point-to-point signals.

Figure 3-3. Differential LVPECL

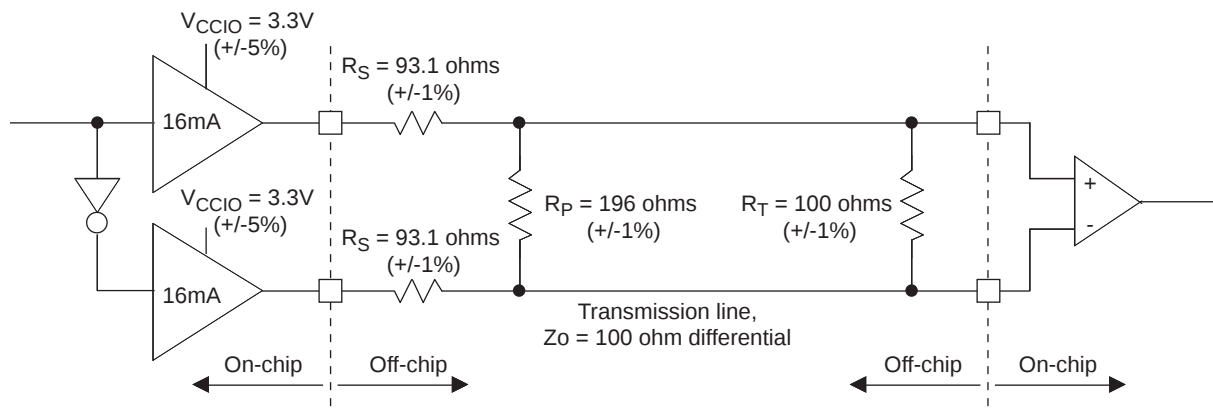


Table 3-4. LVPECL DC Conditions¹

Over Recommended Operating Conditions

Parameter	Description	Typical	Units
V_{CCIO}	Output Driver Supply ($\pm 5\%$)	3.30	V
Z_{OUT}	Driver Impedance	10	Ω
R_S	Driver Series Resistor ($\pm 1\%$)	93	Ω
R_P	Driver Parallel Resistor ($\pm 1\%$)	196	Ω
R_T	Receiver Termination ($\pm 1\%$)	100	Ω
V_{OH}	Output High Voltage	2.05	V
V_{OL}	Output Low Voltage	1.25	V
V_{OD}	Output Differential Voltage	0.80	V
V_{CM}	Output Common Mode Voltage	1.65	V
Z_{BACK}	Back Impedance	100.5	Ω
I_{DC}	DC Output Current	12.11	mA

1. For input buffer, see LVDS table.

LatticeECP2/M External Switching Characteristics⁹ (Continued)

Over Recommended Operating Conditions

Parameter	Description	Device	-7		-6		-5		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
t _{HPLL}	Clock to Data Hold - PIO Input Register	LFE2-6	1.00	—	1.20	—	1.40	—	ns
		LFE2-12	1.00	—	1.20	—	1.40	—	ns
		LFE2-20	1.00	—	1.20	—	1.40	—	ns
		LFE2-35	1.00	—	1.20	—	1.40	—	ns
		LFE2-50	1.00	—	1.20	—	1.40	—	ns
		LFE2-70	1.00	—	1.20	—	1.40	—	ns
		LFE2M20	1.00	—	1.20	—	1.40	—	ns
		LFE2M35	1.00	—	1.20	—	1.40	—	ns
		LFE2M50	1.00	—	1.20	—	1.40	—	ns
		LFE2M70	1.00	—	1.20	—	1.40	—	ns
		LFE2M100	1.00	—	1.20	—	1.40	—	ns
t _{SU_DELPLL}	Clock to Data Setup - PIO Input Register with Data Input Delay	LFE2-6	1.80	—	2.00	—	2.20	—	ns
		LFE2-12	1.80	—	2.00	—	2.20	—	ns
		LFE2-20	1.80	—	2.00	—	2.20	—	ns
		LFE2-35	1.80	—	2.00	—	2.20	—	ns
		LFE2-50	1.80	—	2.00	—	2.20	—	ns
		LFE2-70	1.80	—	2.00	—	2.20	—	ns
		LFE2M20	1.80	—	2.00	—	2.20	—	ns
		LFE2M35	1.80	—	2.00	—	2.20	—	ns
		LFE2M50	1.90	—	2.10	—	2.30	—	ns
		LFE2M70	1.90	—	2.10	—	2.30	—	ns
		LFE2M100	2.00	—	2.20	—	2.40	—	ns
t _{H_DELPLL}	Clock to Data Hold - PIO Input Register with Input Data Delay	LFE2-6	0.00	—	0.00	—	0.00	—	ns
		LFE2-12	0.00	—	0.00	—	0.00	—	ns
		LFE2-20	0.00	—	0.00	—	0.00	—	ns
		LFE2-35	0.00	—	0.00	—	0.00	—	ns
		LFE2-50	0.00	—	0.00	—	0.00	—	ns
		LFE2-70	0.00	—	0.00	—	0.00	—	ns
		LFE2M20	0.00	—	0.00	—	0.00	—	ns
		LFE2M35	0.00	—	0.00	—	0.00	—	ns
		LFE2M50	0.00	—	0.00	—	0.00	—	ns
		LFE2M70	0.00	—	0.00	—	0.00	—	ns
		LFE2M100	0.00	—	0.00	—	0.00	—	ns

DDR I/O Pin Parameters²

t _{DVADQ}	Data Valid After DQS (DDR Read)	ECP2/M	—	0.225	—	0.225	—	0.225	UI
t _{DVEDQ}	Data Hold After DQS (DDR Read)	ECP2/M	0.640	—	0.640	—	0.640	—	UI
t _{DQVBS}	Data Valid Before DQS (DDR Write)	ECP2/M	0.250	—	0.250	—	0.250	—	UI
t _{DQVAS}	Data Valid After DQS (DDR Write)	ECP2/M	0.250	—	0.250	—	0.250	—	UI
f _{MAX_DDR}	DDR Clock Frequency ⁶	ECP2/M	95	200	95	166	95	133	MHz

DDR2 I/O Pin Parameters³

t _{DVADQ}	Data Valid After DQS (DDR Read)	ECP2/M	—	0.225	—	0.225	—	0.225	UI
t _{DVEDQ}	Data Hold After DQS (DDR Read)	ECP2/M	0.640	—	0.640	—	0.640	—	UI

LatticeECP2/M External Switching Characteristics⁹ (Continued)

Over Recommended Operating Conditions

Parameter	Description	Device	-7		-6		-5		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
t _{DIBSPI}	Data Invalid Before Clock (Transmit)	ECP2-20	—	280	—	280	—	280	ps
		ECP2-35	—	280	—	280	—	280	ps
		ECP2-50	—	280	—	280	—	280	ps
		ECP2-70	—	280	—	280	—	280	ps
		ECP2M20	—	230	—	230	—	230	ps
		ECP2M35	—	230	—	230	—	230	ps
		ECP2M50	—	230	—	230	—	230	ps
		ECP2M70	—	230	—	230	—	230	ps
		ECP2M100	—	230	—	230	—	230	ps
XGMII I/O Pin Parameters (312 Mbps) ⁵									
t _{SUXGMII}	Data Setup Before Read Clock	ECP2/M	480	—	480	—	480	—	ps
t _{HXGMII}	Data Hold After Read Clock	ECP2/M	480	—	480	—	480	—	ps
t _{DVBCKXGMII}	Data Valid Before Clock	ECP2/M	960	—	960	—	960	—	ps
t _{DVACKXGMII}	Data Valid After Clock	ECP2/M	960	—	960	—	960	—	ps
Primary									
f _{MAX_PRI} ⁷	Frequency for Primary Clock Tree	ECP2/M	—	420	—	357	—	311	MHz
t _{W_PRI}	Clock Pulse Width for Primary Clock	ECP2/M	0.95	—	1.19	—	2.00	—	ns
t _{SKEW_PRI}	Primary Clock Skew Within a Bank	ECP2/M	—	300	—	360	—	420	ps
Edge Clock									
f _{MAX_EDGE} ⁷	Frequency for Edge Clock	ECP2/M	—	420	—	357	—	311	MHz
t _{W_EDGE}	Clock Pulse Width for Edge Clock	ECP2/M	0.95	—	1.19	—	2.00	—	ns
t _{SKEW_EDGE}	Edge Clock Skew Within an Edge of the Device	ECP2/M	—	300	—	360	—	420	ps

- General timing numbers based on LVCMOS 2.5, 12mA, 0pf load.
- DDR timing numbers based on SSTL25 for BGA packages only.
- DDR2 timing numbers based on SSTL18 for BGA packages only.
- SPI4.2 and SFI4 timing numbers based on LVDS25 for BGA packages only.
- XGMII timing numbers based on HSTL class I. A corresponding left/right dedicated clock buffer is used when using the SPI4.2 interface to the left or right edge of the device. For SPI4.2 mode, the software tool will help in selecting the appropriate clock buffer.
- IP will be used to support DDR and DDR2 memory data rates down to 95MHz. This approach uses a free-running clock and PFU register to sample the data instead of the hardwired DDR memory interface.
- Using the LVDS I/O standard.
- ECP2-6 and ECP2-12 do not support SPI4.2
- The AC numbers do not apply to PCLK6 and PCLK7.
- Applies to CLKOP only.
- Please refer to TN1159, [LatticeECP2/M Pin Assignment Recommendations](#) for best performance.

SERDES External Reference Clock (LatticeECP2M Family Only)

The external reference clock selection and its interface are a critical part of system applications for this product. Table 3-14 specifies reference clock requirements, over the full range of operating conditions.

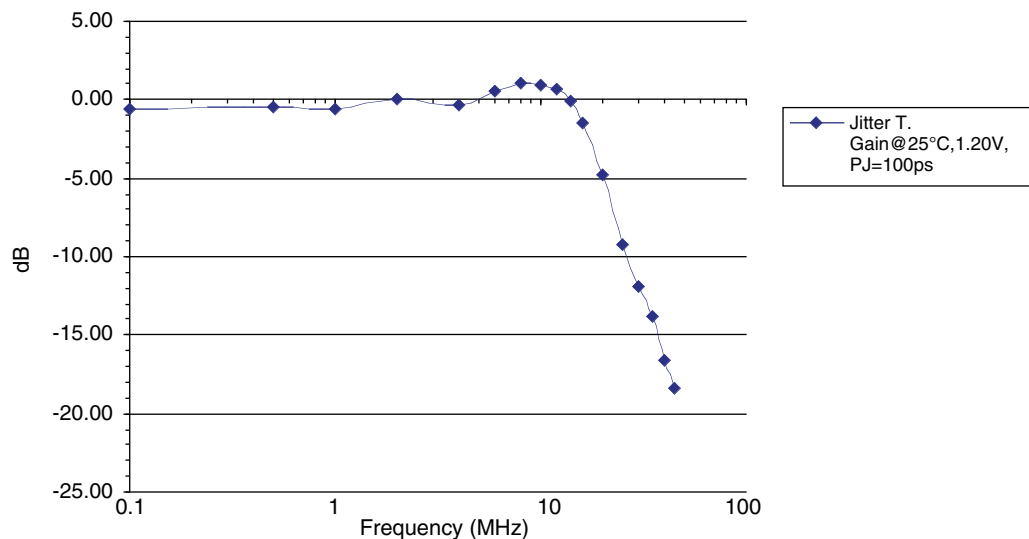
Table 3-14. External Reference Clock Specification (refclkp/refclkn)

Symbol	Description	Min.	Typ.	Max.	Units
F _{REF}	Frequency range	25	—	320	MHz
F _{REF-PPM}	Frequency tolerance	-300	—	300	ppm
V _{REF-IN-SE}	Input swing, single-ended clock ¹	100	—	1200	mV, p-p
V _{REF-IN}	Input levels	0	—	V _{CCP} + 0.8	V
V _{REF-CM-DC}	Input common mode range (DC coupled)	0.5	—	1.2	V
V _{REF-CM-AC}	Input common mode range (AC coupled) ²	0	—	1.5	V
D _{REF}	Duty cycle ³	40	—	60	%
T _{REF-R}	Rise time (20% to 80%)		500	1000	ps
T _{REF-F}	Fall time (80% to 20%)		500	1000	ps
Z _{REF-IN-TERM}	Input termination		50/2K		Ohms
C _{REF-IN-CAP}	Input capacitance ⁴	—	—	1.5	pF

1. The signal swing for a single-ended input clock must be as large as the p-p differential swing of a differential input clock to get the same gain at the input receiver. Lower swings for the clock may be possible, but will tend to increase jitter.
2. When AC coupled, the input common mode range is determined by:

$$(\text{Min input level}) + (\text{Peak-to-peak input swing})/2 \leq (\text{Input common mode voltage}) \leq (\text{Max input level}) - (\text{Peak-to-peak input swing})/2$$
3. Measured at 50% amplitude.
4. Input capacitance of 1.5pF is total capacitance, including both device and package.

Figure 3-13. Jitter Transfer



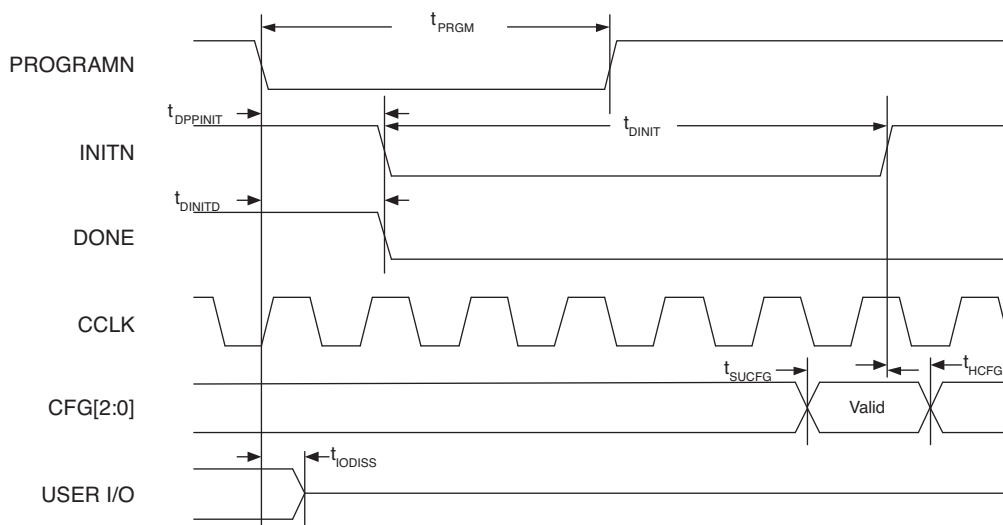
Note: This graph is for a nominal device.

SERDES Power-Down/Power-Up Specification

Table 3-15. Power-Down and Power-Up Specification

Symbol	Description	Max.	Units
t _{PWRDN}	Power-down time after all power down register bits set to '0'	10	μs
t _{PWRUP}	Power-up time after all power down register bits set to '1'	100	μs

Figure 3-18. Configuration from PROGRAMN Timing



1. The CFG pins are normally static (hard wired)

Figure 3-19. Wake-Up Timing

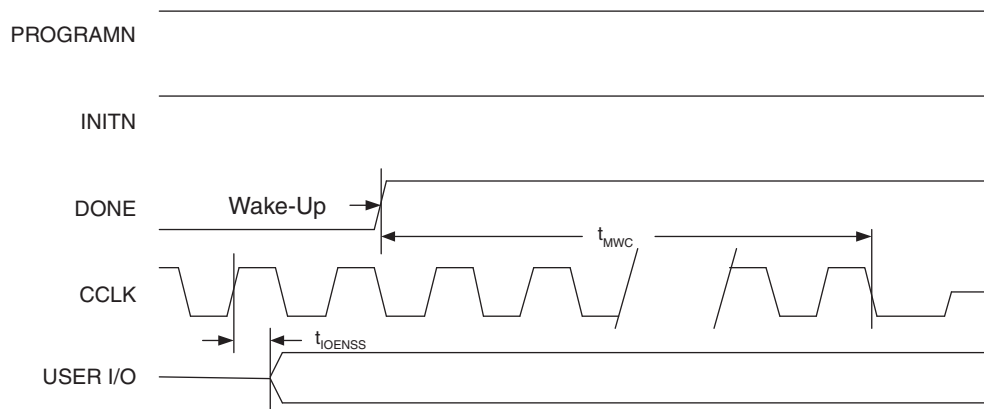
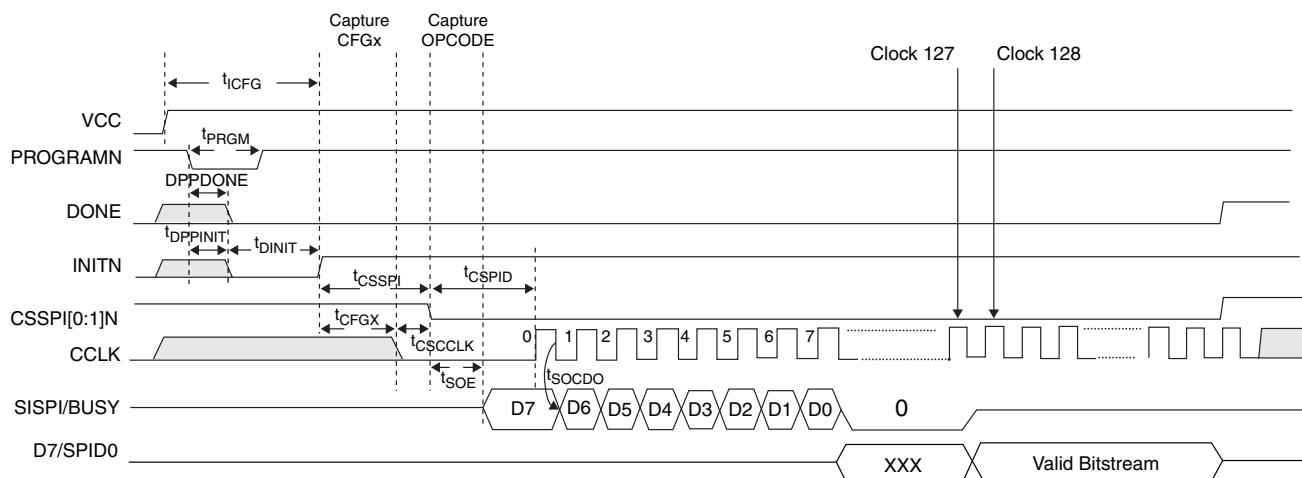


Figure 3-20. SPI/SPIm Configuration Waveforms



LFE2-6E/SE and LFE2-12E/SE Logic Signal Connections: 256 fpBGA (Cont.)

LFE2-6E/SE					LFE2-12E/SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
D5	PT2B	0	VREF2_0	C	PT2B	0	VREF2_0	C
E5	PT2A	0	VREF1_0	T	PT2A	0	VREF1_0	T
G7	VCC	-			VCC	-		
G9	VCC	-			VCC	-		
H7	VCC	-			VCC	-		
J10	VCC	-			VCC	-		
K10	VCC	-			VCC	-		
K8	VCC	-			VCC	-		
G8	VCCAUX	-			VCCAUX	-		
H10	VCCAUX	-			VCCAUX	-		
J7	VCCAUX	-			VCCAUX	-		
K9	VCCAUX	-			VCCAUX	-		
C5	VCCIO0	0			VCCIO0	0		
E7	VCCIO0	0			VCCIO0	0		
C12	VCCIO1	1			VCCIO1	1		
E10	VCCIO1	1			VCCIO1	1		
E14	VCCIO2	2			VCCIO2	2		
G12	VCCIO2	2			VCCIO2	2		
K12	VCCIO3	3			VCCIO3	3		
M14	VCCIO3	3			VCCIO3	3		
M10	VCCIO4	4			VCCIO4	4		
P12	VCCIO4	4			VCCIO4	4		
M7	VCCIO5	5			VCCIO5	5		
P5	VCCIO5	5			VCCIO5	5		
K5	VCCIO6	6			VCCIO6	6		
M3	VCCIO6	6			VCCIO6	6		
E3	VCCIO7	7			VCCIO7	7		
G5	VCCIO7	7			VCCIO7	7		
T15	VCCIO8	8			VCCIO8	8		
A1	GND	-			GND	-		
A16	GND	-			GND	-		
B12	GND	-			GND	-		
B5	GND	-			GND	-		
C8	GND	-			GND	-		
E15	GND	-			GND	-		
E2	GND	-			GND	-		
H14	GND	-			GND	-		
H8	GND	-			GND	-		
H9	GND	-			GND	-		
J3	GND	-			GND	-		
J8	GND	-			GND	-		
J9	GND	-			GND	-		
M15	GND	-			GND	-		
M2	GND	-			GND	-		
P9	GND	-			GND	-		

LFE2-20E/SE Logic Signal Connections: 256 fpBGA (Cont.)

LFE2-20E/SE					
Ball Number	Ball Number	Ball/Pad Function	Bank	Dual Function	Differential
A5	A5	PT36B	0		C
A3	A3	PT35B	0		C
A4	A4	PT36A	0		T
VCCIO	VCCIO	VCCIO0	0		
B3	B3	PT35A	0		T
A2	A2	PT34B	0		C
C7	C7	PT33B	0		C
B2	B2	PT34A	0		T
D7	D7	PT33A	0		T
D6	D6	PT32B	0		C
GND	GND	GNDIO0	-		
F7	F7	PT31B	0		C
C6	C6	PT32A	0		T
VCCIO	VCCIO	VCCIO0	0		
F6	F6	PT31A	0		T
C4	C4	PT30B	0		C
B4	B4	PT30A	0		T
-	GND	GNDIO0	0		
-	VCC	VCCIO	0		
D5	D5	PT2B	0	VREF2_0	C
E5	E5	PT2A	0	VREF1_0	T
G7	G7	VCC	-		
G9	G9	VCC	-		
H7	H7	VCC	-		
J10	J10	VCC	-		
K10	K10	VCC	-		
K8	K8	VCC	-		
G8	G8	VCCAUX	-		
H10	H10	VCCAUX	-		
J7	J7	VCCAUX	-		
K9	K9	VCCAUX	-		
C5	C5	VCCIO0	0		
E7	E7	VCCIO0	0		
C12	C12	VCCIO1	1		
E10	E10	VCCIO1	1		
E14	E14	VCCIO2	2		
G12	G12	VCCIO2	2		
K12	K12	VCCIO3	3		
M14	M14	VCCIO3	3		
M10	M10	VCCIO4	4		
P12	P12	VCCIO4	4		
M7	M7	VCCIO5	5		

LFE2-20E/SE and LFE2-35E/SE Logic Signal Connections: 672 fpBGA (Cont.)

LFE2-20E/20SE					LFE2-35E/35SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential	
GND	GNDIO5	-			GNDIO5	-			
W10	PB11A	5	BDQ15	T	PB11A	5	BDQ15	T	
Y10	PB11B	5	BDQ15	C	PB11B	5	BDQ15	C	
W11	PB12A	5	BDQ15	T	PB12A	5	BDQ15	T	
AA10	PB12B	5	BDQ15	C	PB12B	5	BDQ15	C	
AC8	PB13A	5	BDQ15	T	PB13A	5	BDQ15	T	
AD8	PB13B	5	BDQ15	C	PB13B	5	BDQ15	C	
VCCIO	VCCIO5	5			VCCIO5	5			
AB8	PB14A	5	BDQ15	T	PB14A	5	BDQ15	T	
AB10	PB14B	5	BDQ15	C	PB14B	5	BDQ15	C	
GND	GNDIO5	-			GNDIO5	-			
AE6	PB15A	5	BDQS15	T	PB15A	5	BDQS15	T	
AF6	PB15B	5	BDQ15	C	PB15B	5	BDQ15	C	
AA11	PB16A	5	BDQ15	T	PB16A	5	BDQ15	T	
AC9	PB16B	5	BDQ15	C	PB16B	5	BDQ15	C	
AB9	PB17A	5	BDQ15	T	PB17A	5	BDQ15	T	
AD9	PB17B	5	BDQ15	C	PB17B	5	BDQ15	C	
VCCIO	VCCIO5	5			VCCIO5	5			
Y11	PB18A	5	BDQ15	T	PB18A	5	BDQ15	T	
AB11	PB18B	5	BDQ15	C	PB18B	5	BDQ15	C	
AE7	PB19A	5	BDQ15	T	PB19A	5	BDQ15	T	
AF7	PB19B	5	BDQ15	C	PB19B	5	BDQ15	C	
GND	GNDIO5	-			GNDIO5	-			
AC10	PB20A	5	BDQ24	T	PB20A	5	BDQ24	T	
AD10	PB20B	5	BDQ24	C	PB20B	5	BDQ24	C	
AA12	PB21A	5	BDQ24	T	PB21A	5	BDQ24	T	
W12	PB21B	5	BDQ24	C	PB21B	5	BDQ24	C	
AB12	PB22A	5	BDQ24	T	PB22A	5	BDQ24	T	
VCCIO	VCCIO5	5			VCCIO5	5			
Y12	PB22B	5	BDQ24	C	PB22B	5	BDQ24	C	
AD12	PB23A	5	BDQ24	T	PB23A	5	BDQ24	T	
AC12	PB23B	5	BDQ24	C	PB23B	5	BDQ24	C	
AC13	PB24A	5	BDQS24	T	PB24A	5	BDQS24	T	
GND	GNDIO5	-			GNDIO5	-			
AA13	PB24B	5	BDQ24	C	PB24B	5	BDQ24	C	
AD13	PB25A	5	BDQ24	T	PB25A	5	BDQ24	T	
AC14	PB25B	5	BDQ24	C	PB25B	5	BDQ24	C	
AE8	PB26A	5	BDQ24	T	PB26A	5	BDQ24	T	
VCCIO	VCCIO5	5			VCCIO5	5			
AF8	PB26B	5	BDQ24	C	PB26B	5	BDQ24	C	
AB15	PB27A	5	BDQ24	T	PB27A	5	BDQ24	T	
Y13	PB27B	5	BDQ24	C	PB27B	5	BDQ24	C	
AE9	PB28A	5	BDQ24	T	PB28A	5	BDQ24	T	
GND	GNDIO5	-			GNDIO5	-			
AF9	PB28B	5	BDQ24	C	PB28B	5	BDQ24	C	
W13	PB29A	5	BDQ33	T	PB29A	5	BDQ33	T	

LFE2-70E/SE Logic Signal Connections: 900 fpBGA (Cont.)

LFE2-70E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential
AD2	PL90B	6	LDQ88	C (LVDS)*
AD7	PL91A	6	LDQ88	T
GND	GNDIO6	-		
AB9	PL91B	6	LDQ88	C
AD5	TCK	-		
AE7	TDI	-		
AD4	TMS	-		
AA9	TDO	-		
AD3	VCCJ	-		
AC8	PB2A	5	VREF2_5/BDQ6	T
AE8	PB2B	5	VREF1_5/BDQ6	C
AD8	PB3A	5	BDQ6	T
AF8	PB3B	5	BDQ6	C
AG7	PB4A	5	BDQ6	T
VCCIO	VCCIO5	5		
AH7	PB4B	5	BDQ6	C
AC9	PB5A	5	BDQ6	T
AE9	PB5B	5	BDQ6	C
AD9	PB6A	5	BDQS6	T
GND	GNDIO5	-		
AF9	PB6B	5	BDQ6	C
AB10	PB7A	5	BDQ6	T
AA10	PB7B	5	BDQ6	C
AJ7	PB8A	5	BDQ6	T
VCCIO	VCCIO5	5		
AK7	PB8B	5	BDQ6	C
AC10	PB9A	5	BDQ6	T
AE10	PB9B	5	BDQ6	C
AJ8	PB10A	5	BDQ6	T
GND	GNDIO5	-		
AK8	PB10B	5	BDQ6	C
AF6	PB11A	5	BDQ15	T
AF7	PB11B	5	BDQ15	C
AG5	PB12A	5	BDQ15	T
AH5	PB12B	5	BDQ15	C
AG6	PB13A	5	BDQ15	T
AH6	PB13B	5	BDQ15	C
VCCIO	VCCIO5	5		
AJ4	PB14A	5	BDQ15	T
AK4	PB14B	5	BDQ15	C
GND	GNDIO5	-		
AJ5	PB15A	5	BDQS15	T
AK5	PB15B	5	BDQ15	C

LFE2-70E/SE Logic Signal Connections: 900 fpBGA (Cont.)

LFE2-70E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential
G12	PT40B	0		C
E12	PT40A	0		T
VCCIO	VCCIO0	0		
B13	PT39B	0		C
A13	PT39A	0		T
H12	PT38B	0		C
F12	PT38A	0		T
C12	PT37B	0		C
GND	GNDIO0	-		
D12	PT37A	0		T
B12	PT36B	0		C
A12	PT36A	0		T
E11	PT35B	0		C
VCCIO	VCCIO0	0		
G11	PT35A	0		T
F11	PT34B	0		C
H11	PT34A	0		T
C11	PT33B	0		C
D11	PT33A	0		T
B11	PT32B	0		C
GND	GNDIO0	-		
A11	PT32A	0		T
E10	PT31B	0		C
VCCIO	VCCIO0	0		
G10	PT31A	0		T
F10	PT30B	0		C
H10	PT30A	0		T
D10	PT29B	0		C
C10	PT29A	0		T
GND	GNDIO0	-		
VCCIO	VCCIO0	0		
A7	PT16B	0		C
B7	PT16A	0		T
A6	PT15B	0		C
B6	PT15A	0		T
C7	PT14B	0		C
GND	GNDIO0	-		
D7	PT14A	0		T
D8	PT13B	0		C
VCCIO	VCCIO0	0		
E7	PT13A	0		T
C6	PT12B	0		C
D6	PT12A	0		T

LFE2-70E/SE Logic Signal Connections: 900 fpBGA (Cont.)

LFE2-70E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential
U10	VCCIO6	6		
U9	VCCIO6	6		
V10	VCCIO6	6		
W10	VCCIO6	6		
W9	VCCIO6	6		
Y9	VCCIO6	6		
L10	VCCIO7	7		
L9	VCCIO7	7		
M10	VCCIO7	7		
N10	VCCIO7	7		
P10	VCCIO7	7		
R10	VCCIO7	7		
AA21	VCCIO8	8		
Y21	VCCIO8	8		
AA15	VCCAUX	-		
AB11	VCCAUX	-		
AB19	VCCAUX	-		
AB20	VCCAUX	-		
J11	VCCAUX	-		
J12	VCCAUX	-		
J19	VCCAUX	-		
K19	VCCAUX	-		
L22	VCCAUX	-		
M9	VCCAUX	-		
N9	VCCAUX	-		
P21	VCCAUX	-		
P9	VCCAUX	-		
T10	VCCAUX	-		
T21	VCCAUX	-		
V9	VCCAUX	-		
W22	VCCAUX	-		
A1	GND	-		
A30	GND	-		
AC28	GND	-		
AC3	GND	-		
AH13	GND	-		
AH18	GND	-		
AH23	GND	-		
AH28	GND	-		
AH3	GND	-		
AH8	GND	-		
AK1	GND	-		
AK30	GND	-		

LFE2M50E/SE Logic Signal Connections: 484 fpBGA (Cont.)

LFE2M50E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential
D9	PT45A	0	VREF1_0	T
A2	PT44B	0		C
VCCIO	VCCIO0	0		
A3	PT44A	0		T
B3	PT43B	0		C
C4	PT43A	0		T
E10	PT42B	0		C
F10	PT42A	0		T
C7	PT41B	0		C
GNDIO	GNDIO0	-		
B6	PT41A	0		T
C6	PT40B	0		C
VCCIO	VCCIO0	0		
C5	PT40A	0		T
C8	PT39B	0		C
D8	PT39A	0		T
E8	PT38B	0		C
E9	PT38A	0		T
GNDIO	GNDIO0	-		
VCCIO	VCCIO0	0		
F8	PT10B	0		C
GNDIO	GNDIO0	-		
G8	PT10A	0		T
F7	PT9B	0		C
G7	PT9A	0		T
C3	PT8B	0		C
VCCIO	VCCIO0	0		
D4	PT8A	0		T
F6	PT7B	0		C
E6	PT7A	0		T
E5	PT6B	0		C
D6	PT6A	0		T
D3	PT5B	0		C
GNDIO	GNDIO0	-		
E3	PT5A	0		T
D5	PT4B	0		C
VCCIO	VCCIO0	0		
E4	PT4A	0		T
C2	PT3B	0		C
B2	PT3A	0		T
B1	PT2B	0		C
C1	PT2A	0		T
J10	VCC	-		

LFE2M50E/SE and LFE2M70E/SE Logic Signal Connections: 900 fpBGA (Cont.)

LFE2M50E/SE					LFE2M70E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential	
L5	PL23A	7	LDQ27	T (LVDS)*	PL33A	7	LDQ37	T (LVDS)*	
L4	PL23B	7	LDQ27	C (LVDS)*	PL33B	7	LDQ37	C (LVDS)*	
N9	PL24A	7	LDQ27	T	PL34A	7	LDQ37	T	
N7	PL24B	7	LDQ27	C	PL34B	7	LDQ37	C	
K2	PL25A	7	LDQ27	T (LVDS)*	PL35A	7	LDQ37	T (LVDS)*	
K1	PL25B	7	LDQ27	C (LVDS)*	PL35B	7	LDQ37	C (LVDS)*	
P9	PL26A	7	LDQ27	T	PL36A	7	LDQ37	T	
P7	PL26B	7	LDQ27	C	PL36B	7	LDQ37	C	
GNDIO	GNDIO7	-			GNDIO7	-			
M6	PL27A	7	LDQS27	T (LVDS)*	PL37A	7	LDQS37	T (LVDS)*	
M5	PL27B	7	LDQ27	C (LVDS)*	PL37B	7	LDQ37	C (LVDS)*	
N5	PL28A	7	LDQ27	T	PL38A	7	LDQ37	T	
N6	PL28B	7	LDQ27	C	PL38B	7	LDQ37	C	
M4	PL29A	7	LDQ27	T (LVDS)*	PL39A	7	LDQ37	T (LVDS)*	
M3	PL29B	7	LDQ27	C (LVDS)*	PL39B	7	LDQ37	C (LVDS)*	
P6	PL30A	7	LDQ27	T	PL40A	7	LDQ37	T	
GNDIO	GNDIO7	-			GNDIO7	-			
P8	PL30B	7	LDQ27	C	PL40B	7	LDQ37	C	
L3	PL32A	7	LUM3_SPLLT_IN_A/LDQ36	T (LVDS)*	PL42A	7	LUM3_SPLLT_IN_A/LDQ46	T (LVDS)*	
L2	PL32B	7	LUM3_SPLLC_IN_A/LDQ36	C (LVDS)*	PL42B	7	LUM3_SPLLC_IN_A/LDQ46	C (LVDS)*	
P5	PL33A	7	LUM3_SPLLT_FB_A/LDQ36	T	PL43A	7	LUM3_SPLLT_FB_A/LDQ46	T	
P4	PL33B	7	LUM3_SPLLC_FB_A/LDQ36	C	PL43B	7	LUM3_SPLLC_FB_A/LDQ46	C	
L1	PL34A	7	LDQ36	T (LVDS)*	PL44A	7	LDQ46	T (LVDS)*	
M2	PL34B	7	LDQ36	C (LVDS)*	PL44B	7	LDQ46	C (LVDS)*	
R5	PL35A	7	LDQ36	T	PL45A	7	LDQ46	T	
R4	PL35B	7	LDQ36	C	PL45B	7	LDQ46	C	
GNDIO	GNDIO7	-			GNDIO7	-			
M1	PL36A	7	LDQS36	T (LVDS)*	PL46A	7	LDQS46	T (LVDS)*	
N2	PL36B	7	LDQ36	C (LVDS)*	PL46B	7	LDQ46	C (LVDS)*	
R8	PL37A	7	LDQ36	T	PL47A	7	LDQ46	T	
T9	PL37B	7	LDQ36	C	PL47B	7	LDQ46	C	
P3	PL38A	7	LDQ36	T (LVDS)*	PL48A	7	LDQ46	T (LVDS)*	
P2	PL38B	7	LDQ36	C (LVDS)*	PL48B	7	LDQ46	C (LVDS)*	
N1	PL39A	7	PCLKT7_0/LDQ36	T	PL49A	7	PCLKT7_0/LDQ46	T	
GNDIO	GNDIO7	-			GNDIO7	-			
P1	PL39B	7	PCLKC7_0/LDQ36	C	PL49B	7	PCLKC7_0/LDQ46	C	
T5	PL41A	6	PCLKT6_0	T (LVDS)*	PL51A	6	PCLKT6_0/LDQ55	T (LVDS)*	
T4	PL41B	6	PCLKC6_0	C (LVDS)*	PL51B	6	PCLKC6_0/LDQ55	C (LVDS)*	
U7	PL42A	6	VREF2_6	T	PL52A	6	VREF2_6/LDQ55	T	
T8	PL42B	6	VREF1_6	C	PL52B	6	VREF1_6/LDQ55	C	
R3	PL43A	6		T (LVDS)*	PL53A	6	LDQ55	T (LVDS)*	
VCCIO	VCCIO6	6			VCCIO6	6			
R2	PL43B	6		C (LVDS)*	PL53B	6	LDQ55	C (LVDS)*	
R1	PL44A	6		T	PL54A	6	LDQ55	T	
T1	PL44B	6		C	PL54B	6	LDQ55	C	
GNDIO	GNDIO6	-			GNDIO6	-			
-	-	-			VCCIO6	6			
T3	PL45A	6	LLM3_SPLLT_IN_A	T (LVDS)*	PL57A	6	LLM3_SPLLT_IN_A/LDQ55	T (LVDS)*	

LFE2M50E/SE and LFE2M70E/SE Logic Signal Connections: 900 fpBGA (Cont.)

LFE2M50E/SE					LFE2M70E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential	
AH12	VCC	-			LLC_SQ_VCCR1X1	14			
AK8	PB16A	5	BDQ15	T	LLC_SQ_HDOUTP1	14		T	
AH8	NC	-			LLC_SQ_VCCOB1	14			
AJ8	PB16B	5	BDQ15	C	LLC_SQ_HDOUTN1	14		C	
AH9	VCC	-			LLC_SQ_VCCTX1	14			
AJ9	PB17B	5	BDQ15	C	LLC_SQ_HDOUTN0	14		C	
AK10	NC	-			LLC_SQ_VCCOB0	14			
AK9	PB17A	5	BDQ15	T	LLC_SQ_HDOUTP0	14		T	
AH10	VCC	-			LLC_SQ_VCCTX0	14			
AJ12	PB19B	5	BDQ15	C	LLC_SQ_HDINN0	14		C	
AJ13	NC	-			LLC_SQ_VCCIB0	14			
AK12	PB19A	5	BDQ15	T	LLC_SQ_HDINP0	14		T	
AH13	VCC	-			LLC_SQ_VCCR1X0	14			
AF10	PB3A	5	BDQ6	T	PB30A	5	BDQ33	T	
AE8	PB3B	5	BDQ6	C	PB30B	5	BDQ33	C	
AE11	PB4A	5	BDQ6	T	PB31A	5	BDQ33	T	
VCCIO	VCCIO5	5			VCCIO5	5			
AD9	PB4B	5	BDQ6	C	PB31B	5	BDQ33	C	
AE10	PB5A	5	BDQ6	T	PB32A	5	BDQ33	T	
AD10	PB5B	5	BDQ6	C	PB32B	5	BDQ33	C	
AE13	PB6A	5	BDQS6	T	PB33A	5	BDQS33	T	
GNDIO	GNDIO5	-			GNDIO5	-			
AC12	PB6B	5	BDQ6	C	PB33B	5	BDQ33	C	
AG2	PB7A	5	BDQ6	T	PB34A	5	BDQ33	T	
AG3	PB7B	5	BDQ6	C	PB34B	5	BDQ33	C	
AD13	PB8A	5	BDQ6	T	PB35A	5	BDQ33	T	
VCCIO	VCCIO5	5			VCCIO5	5			
AC13	PB8B	5	BDQ6	C	PB35B	5	BDQ33	C	
AE14	PB9A	5	BDQ6	T	PB36A	5	BDQ33	T	
AC14	PB9B	5	BDQ6	C	PB36B	5	BDQ33	C	
AF3	PB10A	5	BDQ6	T	PB37A	5	BDQ33	T	
GNDIO	GNDIO5	-			GNDIO5	-			
AF4	PB10B	5	BDQ6	C	PB37B	5	BDQ33	C	
VCCIO	VCCIO5	5			-	-			
AG4	PB20A	5	BDQ24	T	PB38A	5	BDQ42	T	
AG5	PB20B	5	BDQ24	C	PB38B	5	BDQ42	C	
GNDIO	GNDIO5	-			-	-			
VCCIO	VCCIO5	5			-	-			
AD11	PB24A	5	BDQS24****	T	PB39A	5	BDQ42	T	
AF13	PB24B	5	BDQ24	C	PB39B	5	BDQ42	C	
AF12	PB25A	5	BDQ24	T	PB40A	5	BDQ42	T	
-	-	-			VCCIO5	5			
AD14	PB25B	5	BDQ24	C	PB40B	5	BDQ42	C	
AG8	PB26A	5	BDQ24	T	PB41A	5	BDQ42	T	
AF8	PB26B	5	BDQ24	C	PB41B	5	BDQ42	C	
AE15	PB27A	5	BDQ24	T	PB42A	5	BDQS42****	T	
-	-	-			GNDIO5	-			
VCCIO	VCCIO5	5			-	-			

LFE2M50E/SE and LFE2M70E/SE Logic Signal Connections: 900 fpBGA (Cont.)

LFE2M50E/SE					LFE2M70E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential	
K3	VCCIO7	7			VCCIO7	7			
M10	VCCIO7	7			VCCIO7	7			
M7	VCCIO7	7			VCCIO7	7			
N10	VCCIO7	7			VCCIO7	7			
N3	VCCIO7	7			VCCIO7	7			
P10	VCCIO7	7			VCCIO7	7			
R6	VCCIO7	7			VCCIO7	7			
AA25	VCCIO8	8			VCCIO8	8			
AD28	VCCIO8	8			VCCIO8	8			
AA10	VCCAUX	-			VCCAUX	-			
AA11	VCCAUX	-			VCCAUX	-			
AA20	VCCAUX	-			VCCAUX	-			
AA21	VCCAUX	-			VCCAUX	-			
K10	VCCAUX	-			VCCAUX	-			
K11	VCCAUX	-			VCCAUX	-			
K20	VCCAUX	-			VCCAUX	-			
K21	VCCAUX	-			VCCAUX	-			
L10	VCCAUX	-			VCCAUX	-			
L11	VCCAUX	-			VCCAUX	-			
L20	VCCAUX	-			VCCAUX	-			
L21	VCCAUX	-			VCCAUX	-			
Y10	VCCAUX	-			VCCAUX	-			
Y11	VCCAUX	-			VCCAUX	-			
Y20	VCCAUX	-			VCCAUX	-			
Y21	VCCAUX	-			VCCAUX	-			
A1	GND	-			GND	-			
A13	GND	-			GND	-			
A18	GND	-			GND	-			
A24	GND	-			GND	-			
A30	GND	-			GND	-			
A7	GND	-			GND	-			
AA14	GND	-			GND	-			
AA15	GND	-			GND	-			
AA16	GND	-			GND	-			
AA17	GND	-			GND	-			
AA24	GND	-			GND	-			
AA27	GND	-			GND	-			
AA4	GND	-			GND	-			
AB24	GND	-			GND	-			
AB7	GND	-			GND	-			
AD12	GND	-			GND	-			
AD19	GND	-			GND	-			
AD27	GND	-			GND	-			
AE22	GND	-			GND	-			
AE27	GND	-			GND	-			
AE4	GND	-			GND	-			
AE9	GND	-			GND	-			
AF14	GND	-			GND	-			

LFE2M100E/SE Logic Signal Connections: 900 fpBGA (Cont.)

LFE2M100E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential
U15	GND	-		
U16	GND	-		
U17	GND	-		
U18	GND	-		
U20	GND	-		
V14	GND	-		
V15	GND	-		
V16	GND	-		
V17	GND	-		
V27	GND	-		
V4	GND	-		
W23	GND	-		
W8	GND	-		
Y14	GND	-		
Y15	GND	-		
Y16	GND	-		
Y17	GND	-		
AA26	NC	-		
AB10	NC	-		
AB11	NC	-		
AB12	NC	-		
AB13	NC	-		
AB14	NC	-		
AB15	NC	-		
AB16	NC	-		
AB17	NC	-		
AB19	NC	-		
AB20	NC	-		
AB21	NC	-		
AB9	NC	-		
AC10	NC	-		
AC11	NC	-		
AC21	NC	-		
AC22	NC	-		
AC8	NC	-		
AC9	NC	-		
AD21	NC	-		
AD22	NC	-		
AD4	NC	-		
AD5	NC	-		
AD6	NC	-		
AD7	NC	-		
AD8	NC	-		

LFE2M70E/SE and LFE2M100E/SE Logic Signal Connections: 1152 fpBGA (Cont.)

LFE2M70E/SE				LFE2M100E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
R21	VCC	-			VCC	-		
R22	VCC	-			VCC	-		
T14	VCC	-			VCC	-		
T21	VCC	-			VCC	-		
U14	VCC	-			VCC	-		
U21	VCC	-			VCC	-		
V14	VCC	-			VCC	-		
V21	VCC	-			VCC	-		
W14	VCC	-			VCC	-		
W21	VCC	-			VCC	-		
Y13	VCC	-			VCC	-		
Y14	VCC	-			VCC	-		
Y21	VCC	-			VCC	-		
Y22	VCC	-			VCC	-		
C12	VCCIO0	0			VCCIO0	0		
C16	VCCIO0	0			VCCIO0	0		
E14	VCCIO0	0			VCCIO0	0		
H12	VCCIO0	0			VCCIO0	0		
H16	VCCIO0	0			VCCIO0	0		
M14	VCCIO0	0			VCCIO0	0		
M15	VCCIO0	0			VCCIO0	0		
C19	VCCIO1	1			VCCIO1	1		
C23	VCCIO1	1			VCCIO1	1		
E21	VCCIO1	1			VCCIO1	1		
H19	VCCIO1	1			VCCIO1	1		
H23	VCCIO1	1			VCCIO1	1		
M20	VCCIO1	1			VCCIO1	1		
M21	VCCIO1	1			VCCIO1	1		
G32	VCCIO2	2			VCCIO2	2		
K28	VCCIO2	2			VCCIO2	2		
K32	VCCIO2	2			VCCIO2	2		
N27	VCCIO2	2			VCCIO2	2		
N32	VCCIO2	2			VCCIO2	2		
P23	VCCIO2	2			VCCIO2	2		
R23	VCCIO2	2			VCCIO2	2		
T27	VCCIO2	2			VCCIO2	2		
T32	VCCIO2	2			VCCIO2	2		
AA23	VCCIO3	3			VCCIO3	3		
AB27	VCCIO3	3			VCCIO3	3		
AB32	VCCIO3	3			VCCIO3	3		
AE28	VCCIO3	3			VCCIO3	3		
AE32	VCCIO3	3			VCCIO3	3		
AH32	VCCIO3	3			VCCIO3	3		
W27	VCCIO3	3			VCCIO3	3		
W32	VCCIO3	3			VCCIO3	3		
Y23	VCCIO3	3			VCCIO3	3		
AC20	VCCIO4	4			VCCIO4	4		
AC21	VCCIO4	4			VCCIO4	4		
AG19	VCCIO4	4			VCCIO4	4		

LFE2M70E/SE and LFE2M100E/SE Logic Signal Connections: 1152 fpBGA (Cont.)

LFE2M70E/SE				LFE2M100E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
AK12	NC	-			NC	-		
AK24	NC	-			NC	-		
AK25	NC	-			NC	-		
AK26	NC	-			NC	-		
AK4	NC	-			NC	-		
AK9	NC	-			NC	-		
AL11	NC	-			NC	-		
AL12	NC	-			NC	-		
AL34	NC	-			NC	-		
AM10	NC	-			NC	-		
AM11	NC	-			NC	-		
AM13	NC	-			NC	-		
AM25	NC	-			NC	-		
AN10	NC	-			NC	-		
AN11	NC	-			NC	-		
AN12	NC	-			NC	-		
AN13	NC	-			NC	-		
AN24	NC	-			NC	-		
AN25	NC	-			NC	-		
AP11	NC	-			NC	-		
AP12	NC	-			NC	-		
AP24	NC	-			NC	-		
B10	NC	-			NC	-		
B11	NC	-			NC	-		
B12	NC	-			NC	-		
B13	NC	-			NC	-		
B22	NC	-			NC	-		
B23	NC	-			NC	-		
B24	NC	-			NC	-		
B25	NC	-			NC	-		
C10	NC	-			NC	-		
C11	NC	-			NC	-		
C13	NC	-			NC	-		
C22	NC	-			NC	-		
C24	NC	-			NC	-		
C25	NC	-			NC	-		
D1	NC	-			NC	-		
D15	NC	-			NC	-		
D24	NC	-			NC	-		
D34	NC	-			NC	-		
E10	NC	-			NC	-		
E24	NC	-			NC	-		
E25	NC	-			NC	-		
E26	NC	-			NC	-		
E3	NC	-			NC	-		
E31	NC	-			NC	-		
E32	NC	-			NC	-		
E33	NC	-			NC	-		
E34	NC	-			NC	-		