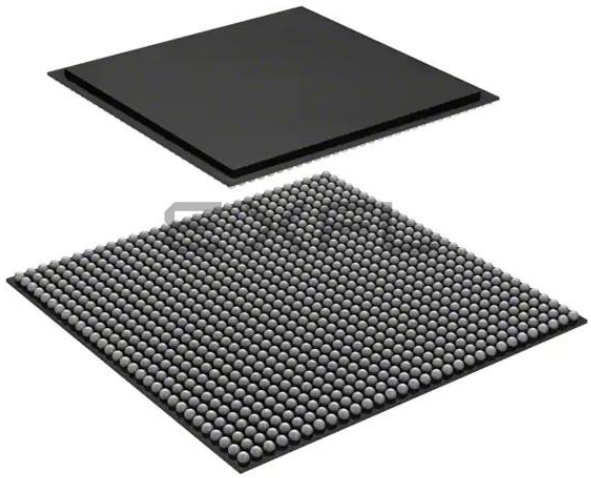
# Lattice Semiconductor Corporation - LFE2-70SE-5F900I Datasheet



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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

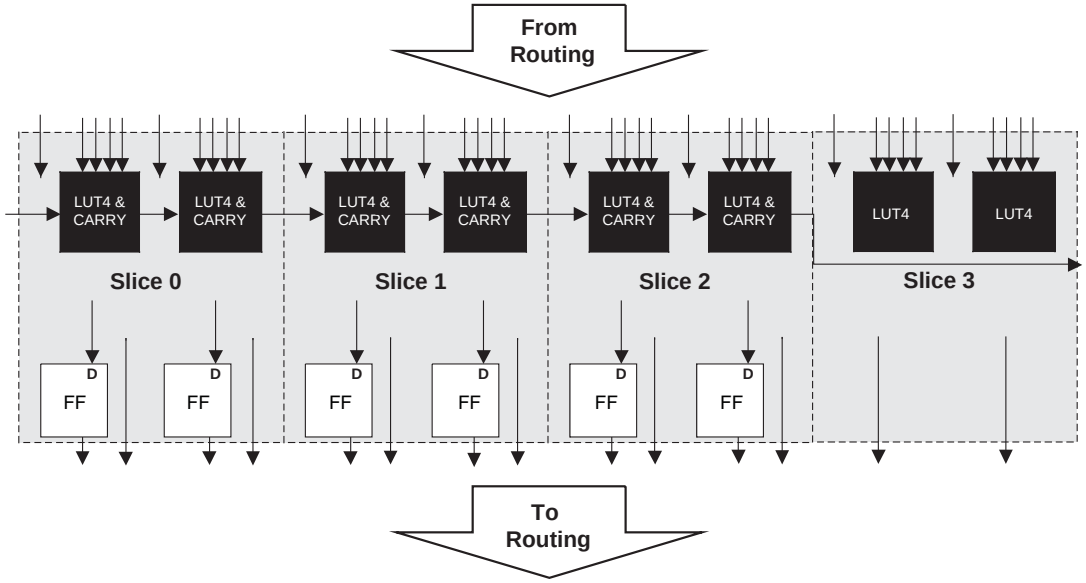
| Details | |
|---|---|
| Product Status | Obsolete |
| Number of LABs/CLBs | 8500 |
| Number of Logic Elements/Cells | 68000 |
| Total RAM Bits | 1056768 |
| Number of I/O | 583 |
| Number of Gates | - |
| Voltage - Supply | 1.14V ~ 1.26V |
| Mounting Type | Surface Mount |
| Operating Temperature | -40°C ~ 100°C (TJ) |
| Package / Case | 900-BBGA |
| Supplier Device Package | 900-FPBGA (31x31) |
| Purchase URL | https://www.e-xfl.com/product-detail/lattice-semiconductor/lfe2-70se-5f900i |

## PFU Blocks

The core of the LatticeECP2/M device consists of PFU blocks, which are provided in two forms, the PFU and PFF. The PFUs can be programmed to perform Logic, Arithmetic, Distributed RAM and Distributed ROM functions. PFF blocks can be programmed to perform Logic, Arithmetic and ROM functions. Except where necessary, the remainder of this data sheet will use the term PFU to refer to both PFU and PFF blocks.

Each PFU block consists of four interconnected slices, numbered 0-3 as shown in Figure 2-3. All the interconnections to and from PFU blocks are from routing. There are 50 inputs and 23 outputs associated with each PFU block.

***Figure 2-3. PFU Diagram***




## Slice

Slice 0 through Slice 2 contain two LUT4s feeding two registers, whereas Slice 3 contains two LUT4s only. For PFUs, Slice 0 and Slice 2 can also be configured as distributed memory, a capability not available in the PFF. Table 2-1 shows the capability of the slices in both PFF and PFU blocks along with the operation modes they enable. In addition, each PFU contains some logic that allows the LUTs to be combined to perform functions such as LUT5, LUT6, LUT7 and LUT8. There is control logic to perform set/reset functions (programmable as synchronous/asynchronous), clock select, chip-select and wider RAM/ROM functions. Figure 2-4 shows an overview of the internal logic of the slice. The registers in the slice can be configured for positive/negative and edge triggered or level sensitive clocks.

***Table 2-1. Resources and Modes Available per Slice***

| Slice | PFU BLock | | PFF Block | |
|---|---|---|---|---|
| | Resources | Modes | Resources | Modes |
| Slice 0 | 2 LUT4s and 2 Registers | Logic, Ripple, RAM, ROM | 2 LUT4s and 2 Registers | Logic, Ripple, ROM |
| Slice 1 | 2 LUT4s and 2 Registers | Logic, Ripple, ROM | 2 LUT4s and 2 Registers | Logic, Ripple, ROM |
| Slice 2 | 2 LUT4s and 2 Registers | Logic, Ripple, RAM, ROM | 2 LUT4s and 2 Registers | Logic, Ripple, ROM |
| Slice 3 | 2 LUT4s | Logic, ROM | 2 LUT4s | Logic, ROM |

Slices 0, 1 and 2 have 14 input signals: 13 signals from routing and one from the carry-chain (from the adjacent slice or PFU). There are seven outputs: six to routing and one to carry-chain (to the adjacent PFU). Slice 3 has 13 input signals from routing and four signals to routing. Table 2-2 lists the signals associated with Slice 0 to Slice 2.

## Modes of Operation

Each slice has up to four potential modes of operation: Logic, Ripple, RAM and ROM.

### Logic Mode

In this mode, the LUTs in each slice are configured as 4-input combinatorial lookup tables. A LUT4 can have 16 possible input combinations. Any four input logic functions can be generated by programming this lookup table. Since there are two LUT4s per slice, a LUT5 can be constructed within one slice. Larger look-up tables such as LUT6, LUT7 and LUT8 can be constructed by concatenating other slices. Note LUT8 requires more than four slices.

### Ripple Mode

Ripple mode supports the efficient implementation of small arithmetic functions. In ripple mode, the following functions can be implemented by each slice:

- Addition 2-bit
- Subtraction 2-bit
- Add/Subtract 2-bit using dynamic control
- Up counter 2-bit
- Down counter 2-bit
- Up/Down counter with Async clear
- Up/Down counter with preload (sync)
- Ripple mode multiplier building block
- Multiplier support
- Comparator functions of A and B inputs
  - A greater-than-or-equal-to B
  - A not-equal-to B
  - A less-than-or-equal-to B

Ripple Mode includes an optional configuration that performs arithmetic using fast carry chain methods. In this configuration (also referred to as CCU2 mode) two additional signals, Carry Generate and Carry Propagate, are generated on a per slice basis to allow fast arithmetic functions to be constructed by concatenating Slices.

### RAM Mode

In this mode, a 16x4-bit distributed single port RAM (SPR) can be constructed using each LUT block in Slice 0 and Slice 2 as a 16x1-bit memory. Slice 1 is used to provide memory address and control signals. A 16x2-bit pseudo dual port RAM (PDPR) memory is created by using one Slice as the read-write port and the other companion slice as the read-only port.

The Lattice design tools support the creation of a variety of different size memories. Where appropriate, the software will construct these using distributed memory primitives that represent the capabilities of the PFU. Table 2-3 shows the number of slices required to implement different distributed RAM primitives. For more information about using RAM in LatticeECP2/M devices, please see the list of additional technical documentation at the end of this data sheet.

***Table 2-3. Number of Slices Required to Implement Distributed RAM***

| | SPR 16X4 | PDPR 16X4 |
|---|---|---|
| Number of slices | 3 | 3 |

Note: SPR = Single Port RAM, PDPR = Pseudo Dual Port RAM

By combining input blocks of the complementary PIOs and sharing some registers from output blocks, a gearbox function can be implemented, which takes a double data rate signal applied to PIOA and converts it as four data streams, IPOS0A, IPOS1A, IPOS0B and IPOS1B. Figure 2-29 shows the diagram using this gearbox function. For more information about this topic, please see information regarding additional documentation at the end of this data sheet.

The signal DDRCLKPOL controls the polarity of the clock used in the synchronization registers. It ensures adequate timing when data is transferred from the DQS to the system clock domain. For further information about this topic, see the DDR Memory section of this data sheet.

***Figure 2-29. Input Register Block for Left, Right and Bottom Edges***

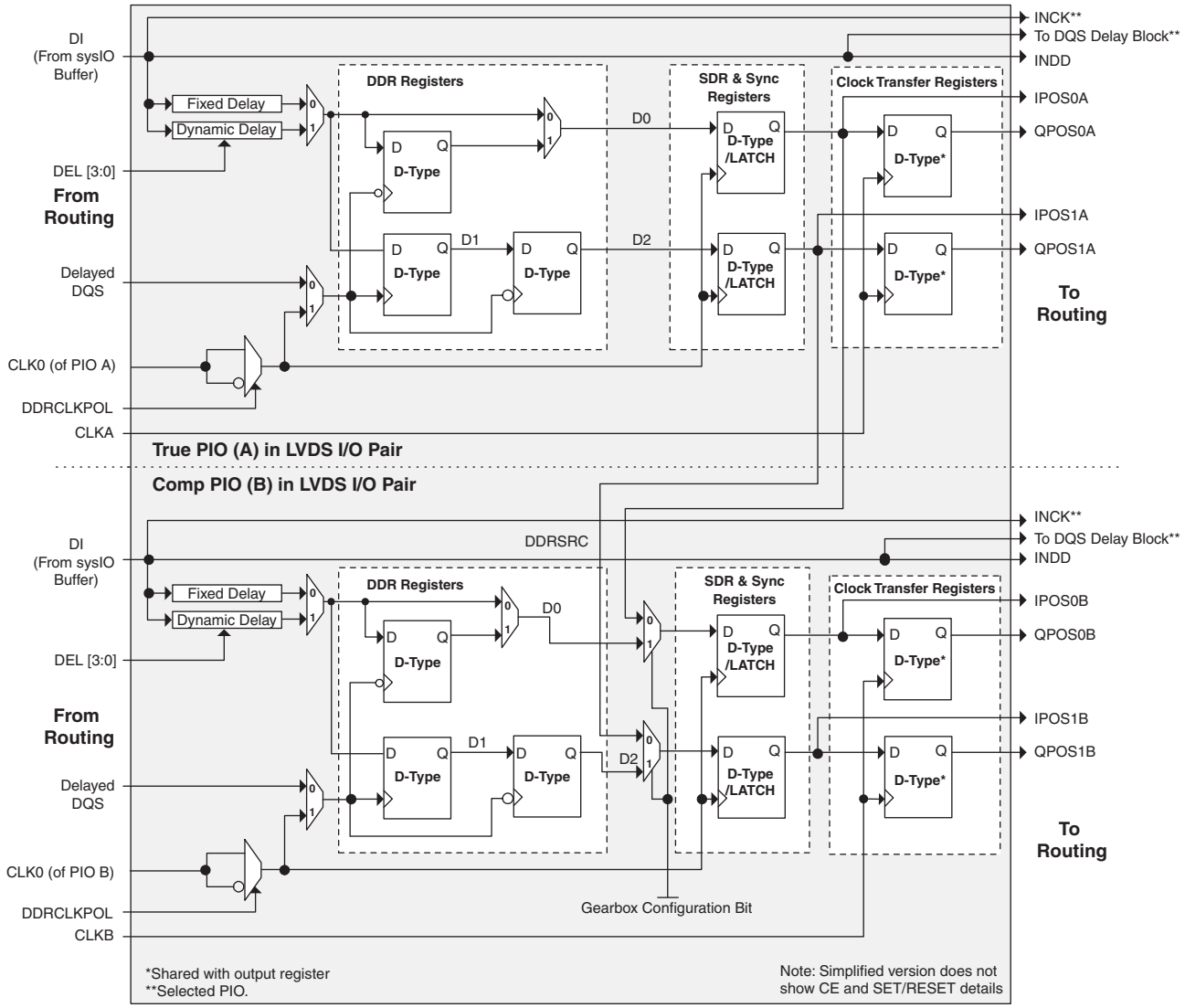
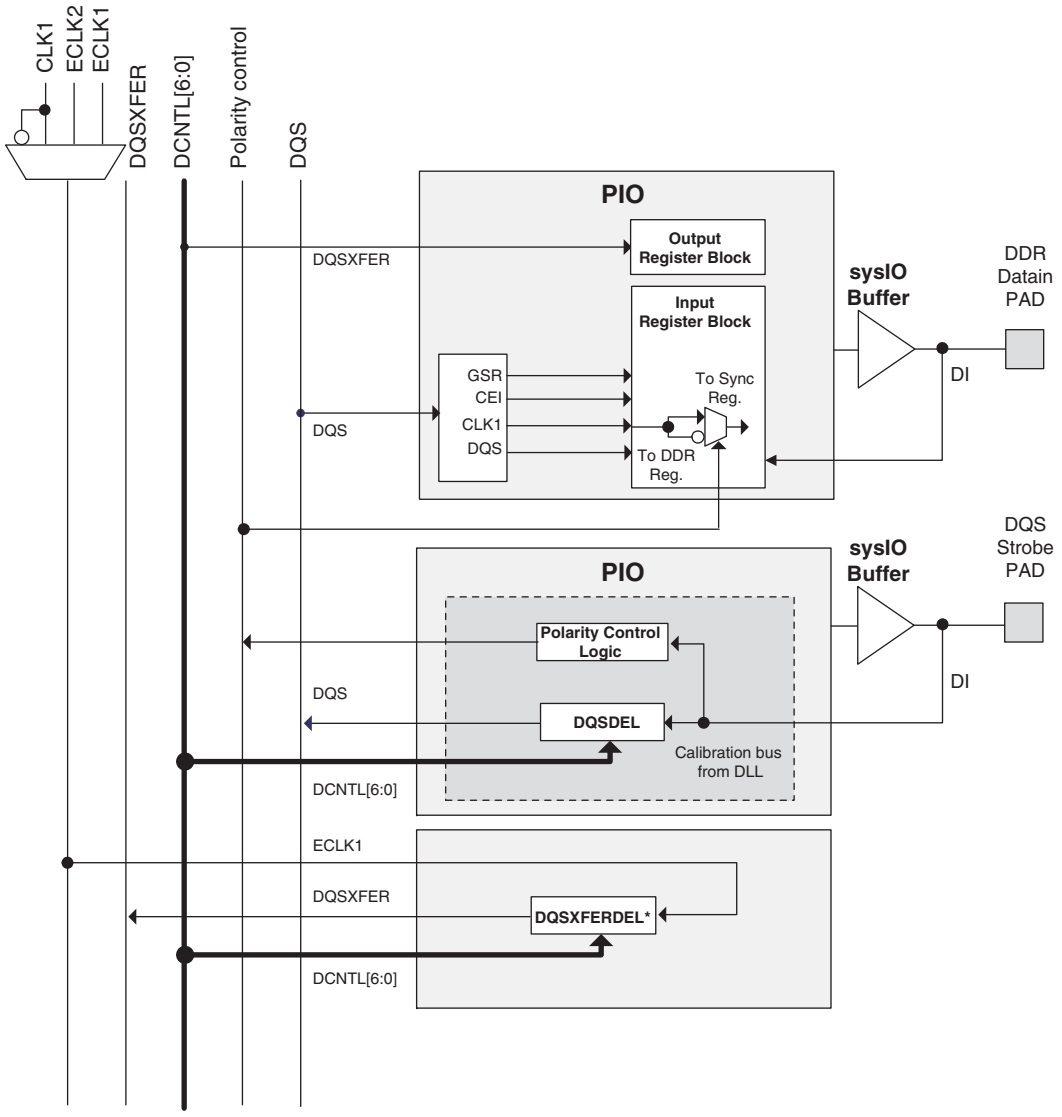


*Figure 2-36. DQS Local Bus*




*DQSXFERDEL shifts ECLK1 by 90% and is not associated with a particular PIO.

## Polarity Control Logic

In a typical DDR Memory interface design, the phase relationship between the incoming delayed DQS strobe and the internal system clock (during the READ cycle) is unknown.

The LatticeECP2/M family contains dedicated circuits to transfer data between these domains. To prevent set-up and hold violations, at the domain transfer between DQS (delayed) and the system clock, a clock polarity selector is used. This changes the edge on which the data is registered in the synchronizing registers in the input register block. This requires evaluation at the start of each READ cycle for the correct clock polarity.

Prior to the READ operation in DDR memories, DQS is in tristate (pulled by termination). The DDR memory device drives DQS low at the start of the preamble state. A dedicated circuit detects the first DQS rising edge after the preamble state. This signal is used to control the polarity of the clock to the synchronizing registers.

# DC Electrical Characteristics

**Over Recommended Operating Conditions**

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $I_{IL}$, $I_{IH}$[1, 2] | Input or I/O Low Leakage | $0 \le V_{IN} \le (V_{CCIO} - 0.2V)$ | — | — | 10 | µA |
| $I_{IH}$[1, 3] | Input or I/O High Leakage | $(V_{CCIO} - 0.2V) < V_{IN} \le 3.6V$ | — | — | 150 | µA |
| $I_{PU}$ | I/O Active Pull-up Current | $0 \le V_{IN} \le 0.7\ V_{CCIO}$ | -30 | — | -210 | µA |
| $I_{PD}$ | I/O Active Pull-down Current | $V_{IL}$ (MAX) $\le V_{IN} \le V_{IH}$ (MAX) | 30 | — | 210 | µA |
| $I_{BHLS}$ | Bus Hold Low Sustaining Current | $V_{IN} = V_{IL}$ (MAX) | 30 | — | — | µA |
| $I_{BHHS}$ | Bus Hold High Sustaining Current | $V_{IN} = 0.7\ V_{CCIO}$ | -30 | — | — | µA |
| $I_{BHLO}$ | Bus Hold Low Overdrive Current | $0 \le V_{IN} \le V_{CCIO}$ | — | — | 210 | µA |
| $I_{BHHO}$ | Bus Hold High Overdrive Current | $0 \le V_{IN} \le V_{CCIO}$ | — | — | -210 | µA |
| $V_{BHT}$ | Bus Hold Trip Points | $0 \le V_{IN} \le V_{IH}$ (MAX) | $V_{IL}$ (MAX) | — | $V_{IH}$ (MIN) | V |
| C1[4] | I/O Capacitance | $V_{CCIO}$ = 3.3V, 2.5V, 1.8V, 1.5V, 1.2V, $V_{CC}$ = 1.2V, $V_{IO}$ = 0 to $V_{IH}$ (MAX) | — | 5 | 8 | pf |
| C2[4] | Dedicated Input Capacitance | $V_{CCIO}$ = 3.3V, 2.5V, 1.8V, 1.5V, 1.2V, $V_{CC}$ = 1.2V, $V_{IO}$ = 0 to $V_{IH}$ (MAX) | — | 5 | 6 | pf |

1. Input or I/O leakage current is measured with the pin configured as an input or as an I/O with the output driver tri-stated. It is not measured with the output driver active. Bus maintenance circuits are disabled.
2. When used as $V_{REF}$, maximum leakage = 25uA
3. Applicable to general purpose I/Os in top and bottom banks.
4. $T_A$ 25°C, f = 1.0MHz.

## sysI/O Single-Ended DC Electrical Characteristics

| Input/Output Standard | $V_{IL}$ | | $V_{IH}$ | | $V_{OL}$ Max. (V) | $V_{OH}$ Min. (V) | $I_{OL}$[1] (mA) | $I_{OH}$[1] (mA) |
|---|---|---|---|---|---|---|---|---|
| | Min. (V) | Max. (V) | Min. (V) | Max. (V) | | | | |
| LVCMOS 3.3 | -0.3 | 0.8 | 2.0 | 3.6 | 0.4 | $V_{CCIO}$ - 0.4 | 20, 16, 12, 8, 4 | -20, -16, -12, -8, -4 |
| | | | | | 0.2 | $V_{CCIO}$ - 0.2 | 0.1 | -0.1 |
| LVTTL | -0.3 | 0.8 | 2.0 | 3.6 | 0.4 | $V_{CCIO}$ - 0.4 | 20, 16, 12, 8, 4 | -20, -16, -12, -8, -4 |
| | | | | | 0.2 | $V_{CCIO}$ - 0.2 | 0.1 | -0.1 |
| LVCMOS 2.5 | -0.3 | 0.7 | 1.7 | 3.6 | 0.4 | $V_{CCIO}$ - 0.4 | 20, 16, 12, 8, 4 | -20, -16, -12, -8, -4 |
| | | | | | 0.2 | $V_{CCIO}$ - 0.2 | 0.1 | -0.1 |
| LVCMOS 1.8 | -0.3 | 0.35 $V_{CCIO}$ | 0.65 $V_{CCIO}$ | 3.6 | 0.4 | $V_{CCIO}$ - 0.4 | 16, 12, 8, 4 | -16, -12, -8, -4 |
| | | | | | 0.2 | $V_{CCIO}$ - 0.2 | 0.1 | -0.1 |
| LVCMOS 1.5 | -0.3 | 0.35 $V_{CCIO}$ | 0.65 $V_{CCIO}$ | 3.6 | 0.4 | $V_{CCIO}$ - 0.4 | 8, 4 | -8, -4 |
| | | | | | 0.2 | $V_{CCIO}$ - 0.2 | 0.1 | -0.1 |
| LVCMOS 1.2 | -0.3 | 0.35 $V_{CC}$ | 0.65 $V_{CC}$ | 3.6 | 0.4 | $V_{CCIO}$ - 0.4 | 6, 2 | -6, -2 |
| | | | | | 0.2 | $V_{CCIO}$ - 0.2 | 0.1 | -0.1 |
| PCI | -0.3 | 0.3 $V_{CCIO}$ | 0.5 $V_{CCIO}$ | 3.6 | 0.1 $V_{CCIO}$ | 0.9 $V_{CCIO}$ | 1.5 | -0.5 |
| SSTL3 Class I | -0.3 | $V_{REF}$ - 0.2 | $V_{REF}$ + 0.2 | 3.6 | 0.7 | $V_{CCIO}$ - 1.1 | 8 | -8 |
| SSTL3 Class II | -0.3 | $V_{REF}$ - 0.2 | $V_{REF}$ + 0.2 | 3.6 | 0.5 | $V_{CCIO}$ - 0.9 | 16 | -16 |
| SSTL2 Class I | -0.3 | $V_{REF}$ - 0.18 | $V_{REF}$ + 0.18 | 3.6 | 0.54 | $V_{CCIO}$ - 0.62 | 7.6 | -7.6 |
| | | | | | | | 12 | -12 |
| SSTL2 Class II | -0.3 | $V_{REF}$ - 0.18 | $V_{REF}$ + 0.18 | 3.6 | 0.35 | $V_{CCIO}$ - 0.43 | 15.2 | -15.2 |
| | | | | | | | 20 | -20 |
| SSTL18 Class I | -0.3 | $V_{REF}$ - 0.125 | $V_{REF}$ + 0.125 | 3.6 | 0.4 | $V_{CCIO}$ - 0.4 | 6.7 | -6.7 |
| SSTL18 Class II | -0.3 | $V_{REF}$ - 0.125 | $V_{REF}$ + 0.125 | 3.6 | 0.28 | $V_{CCIO}$ - 0.28 | 8 | -8 |
| | | | | | | | 11 | -11 |
| HSTL Class I | -0.3 | $V_{REF}$ - 0.1 | $V_{REF}$ + 0.1 | 3.6 | 0.4 | $V_{CCIO}$ - 0.4 | 4 | -4 |
| | | | | | | | 8 | -8 |
| HSTL18 Class I | -0.3 | $V_{REF}$ - 0.1 | $V_{REF}$ + 0.1 | 3.6 | 0.4 | $V_{CCIO}$ - 0.4 | 8 | -8 |
| | | | | | | | 12 | -12 |
| HSTL18 Class II | -0.3 | $V_{REF}$ - 0.1 | $V_{REF}$ + 0.1 | 3.6 | 0.4 | $V_{CCIO}$ - 0.4 | 16 | -16 |

1. The average DC current drawn by I/Os between GND connections, or between the last GND in an I/O bank and the end of an I/O bank, as shown in the logic signal connections table shall not exceed n * 8mA, where n is the number of I/Os between bank GND connections or between the last GND in a bank and the end of a bank.

## LatticeECP2 Pin Information Summary, LFE2-20 and LFE2-35 (Cont.)

| Pin Type | | LFE2-20 | | | | LFE2-35 | |
|---|---|---|---|---|---|---|---|
| | | 208 PQFP | 256 fpBGA | 484 fpBGA | 672 fpBGA | 484 fpBGA | 672 fpBGA |
| Available DDR-Interfaces per I/O Bank[1] | Bank0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Bank1 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Bank2 | 0 | 1 | 2 | 2 | 2 | 3 |
| | Bank3 | 0 | 0 | 0 | 2 | 0 | 2 |
| | Bank4 | 0 | 2 | 3 | 3 | 3 | 3 |
| | Bank5 | 0 | 1 | 3 | 4 | 3 | 4 |
| | Bank6 | 0 | 1 | 2 | 3 | 1 | 3 |
| | Bank7 | 0 | 1 | 2 | 2 | 2 | 3 |
| | Bank8 | 0 | 0 | 0 | 0 | 0 | 0 |
| PCI Capable I/Os per Bank | Bank0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Bank1 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Bank2 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Bank3 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Bank4 | 19 | 32 | 46 | 50 | 46 | 54 |
| | Bank5 | 18 | 17 | 46 | 68 | 46 | 68 |
| | Bank6 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Bank7 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Bank8 | 0 | 0 | 0 | 0 | 0 | 0 |

1. Minimum requirement to implement a fully functional 8-bit wide DDR bus. Available DDR interface consists of at least 12 I/Os (1 DQS + 1 DQSB + 8 DQs + 1 DM + Bank VREF1).

## LatticeECP2 Pin Information Summary, LFE2-50 and LFE2-70

| Pin Type | | LFE2-50 | | LFE2-70 | |
|---|---|---|---|---|---|
| | | 484 fpBGA | 672 fpBGA | 672 fpBGA | 900 fpBGA |
| Single Ended User I/O | | 339 | 500 | 500 | 583 |
| Differential Pair User I/O | | 169 | 249 | 249 | 290 |
| Configuration | TAP Pins | 5 | 5 | 5 | 5 |
| | Muxed Pins | 14 | 14 | 14 | 14 |
| | Dedicated Pins (Non TAP) | 7 | 7 | 7 | 7 |
| Non Configuration | Muxed Pins | 68 | 79 | 79 | 89 |
| | Dedicated Pins | 3 | 3 | 3 | 3 |
| VCC | | 16 | 20 | 20 | 26 |
| VCCAUX | | 16 | 16 | 16 | 17 |
| VCCPLL | | 4 | 4 | 2 | 4 |
| VCCIO | Bank0 | 4 | 5 | 5 | 6 |
| | Bank1 | 4 | 5 | 5 | 6 |
| | Bank2 | 4 | 5 | 5 | 6 |
| | Bank3 | 4 | 5 | 5 | 6 |
| | Bank4 | 4 | 5 | 5 | 6 |
| | Bank5 | 4 | 5 | 5 | 6 |
| | Bank6 | 4 | 5 | 5 | 6 |
| | Bank7 | 4 | 5 | 5 | 6 |
| | Bank8 | 2 | 2 | 2 | 2 |
| GND, GND0 to GND7 | | 60 | 72 | 72 | 104 |
| NC | | 0 | 3 | 5 | 101 |
| Single Ended/ Differential I/O Pairs per Bank (including emulated with resistors) | Bank0 | 50/25 | 67/33 | 67/33 | 84/42 |
| | Bank1 | 46/23 | 66/33 | 66/33 | 76/38 |
| | Bank2 | 38/19 | 56/28 | 56/28 | 74/37 |
| | Bank3 | 22/11 | 48/24 | 48/24 | 48/24 |
| | Bank4 | 46/23 | 62/31 | 62/31 | 72/35 |
| | Bank5 | 46/23 | 68/34 | 68/34 | 80/40 |
| | Bank6 | 40/20 | 64/32 | 64/32 | 64/32 |
| | Bank7 | 37/18 | 55/27 | 55/27 | 71/35 |
| | Bank8 | 14/7 | 14/7 | 14/7 | 14/7 |
| True LVDS I/O Pairs per Bank | Bank0 (Top Edge) | 0 | 0 | 0 | 0 |
| | Bank1 (Top Edge) | 0 | 0 | 0 | 0 |
| | Bank2 (Right Edge) | 9 | 13 | 13 | 18 |
| | Bank3 (Right Edge) | 5 | 12 | 12 | 12 |
| | Bank4 (Bottom Edge) | 0 | 0 | 0 | 0 |
| | Bank5 (Bottom Edge) | 0 | 0 | 0 | 0 |
| | Bank6 (Left Edge) | 10 | 16 | 16 | 16 |
| | Bank7 (Left Edge) | 8 | 12 | 12 | 16 |
| | Bank8 (Right Edge) | 0 | 0 | 0 | 0 |

## LatticeECP2 Power Supply and NC (Cont.)

| Signals | 672 fpBGA[3] | 900 fpBGA[3] |
|---|---|---|
| VCC | **LFE2-20:** R8, P18, M8, L20, L12, L13, L14, L15, M11, M12, M15, M16, N11, N16, P11, P16, R11, R12, R15, R16, T12, T13, T14, T15<br>**LFE2-35/LFE2-50:** L12, L13, L14, L15, M11, M12, M15, M16, N11, N16, P11, P16, R11, R12, R15, R16, T12, T13, T14, T15<br>**LFE2-70:** L12, L13, L14, L15, M11, M12, M15, M16, N11, N16, P11, P16, R11, R12, R15, R16, T12, T13, T14, T15 | AA11, AA20, K11, K21, K22, L11, L12, L13, L18, L19, L20, M11, M20, N11, N20, V11, V20, W11, W20, Y10, Y11, Y12, Y13, Y18, Y19, Y20 |
| VCCIO0 | D11, D6, G9, J12, K12 | J13, J14, K12, K13, K14, K15 |
| VCCIO1 | D16, D21, G18, J15, K15 | J17, J18, J20, K17, K18, K20 |
| VCCIO2 | F23, J20, L23, M17, M18 | L21, M21, M22, N21, N22, R21 |
| VCCIO3 | AA23, R17, R18, T23, V20 | U21, U22, V21, V22, W21, Y22 |
| VCCIO4 | AC16, AC21, U15, V15, Y18 | AA16, AA17, AA18, AA19, AB17, AB18 |
| VCCIO5 | AC11, AC6, U12, V12, Y9 | AA12, AA13, AA14, AB12, AB13, AB14 |
| VCCIO6 | AA4, R10, R9, T4, V7 | U10, U9, V10, W10, W9, Y9 |
| VCCIO7 | F4, J7, L4, M10, M9 | L10, L9, M10, N10, P10, R10 |
| VCCIO8 | AE25, V18 | AA21, Y21 |
| VCCJ | AB5 | AD3 |
| VCCAUX | J10, J11, J16, J17, K18, L18, T18, U18, V16, V17, V10, V11, T9, U9, K9, L9 | AA15, AB11, AB19, AB20, J11, J12, J19, K19, L22, M9, N9, P21, P9, T10, T21, V9, W22 |
| VCCPLL | **LFE2-20:** None<br>**LFE2-35/LFE2-70:** R8, P18<br>**LFE2-50:** R8, P18, M8, L20 | P22, P8, T22, Y7 |
| GND[1] | A2, A25, AA18, AA24, AA3, AA9, AD11, AD16, AD21, AD6, AE1, AE26, AF2, AF25, B1, B26, C11, C16, C21, C6, F18, F24, F3, F9, J13, J14, J21, J6, K10, K11, K13, K14, K16, K17, L10, L11, L16, L17, L24, L3, M13, M14, N10, N12, N13, N14, N15, N17, P10, P12, P13, P14, P15, P17, R13, R14, T10, T11, T16, T17, T24, T3, U10, U11, U13, U14, U16, U17, V13, V14, V21, V6 | A1, A30, AC28, AC3, AH13, AH18, AH23, AH28, AH3, AH8, AK1, AK30, C13, C18, C23, C28, C3, C8, H28, H3, L14, L15, L16, L17, M12, M13, M14, M15, M16, M17, M18, M19, N12, N13, N14, N15, N16, N17, N18, N19, N28, N3, P11, P12, P13, P14, P15, P16, P17, P18, P19, P20, R11, R12, R13, R14, R15, R16, R17, R18, R19, R20, T11, T12, T13, T14, T15, T16, T17, T18, T19, T20, U11, U12, U13, U14, U15, U16, U17, U18, U19, U20, V12, V13, V14, V15, V16, V17, V18, V19, V28, V3, W12, W13, W14, W15, W16, W17, W18, W19, Y14, Y15, Y16, Y17 |
| NC[2] | **LFE2-20:** E4, E3, E2, E1, H6, H5, F2, F1, H8, J9, G4, G3, K3, K2, K1, L2, L1, M2, M1, N2, T1, T2, P8, P6, P5, P4, U1, V1, P3, R3, R4, U2, V2, W2, T6, R5, AA19, W17, Y19, Y17, AF20, AE20, AA20, W18, AD20, AE21, AF21, AF22, R22, T21, P26, P25, R24, R23, P20, R19, P21, P19, P23, P22, N22, R21, N26, N25, J26, J25, J23, K23, H26, H25, H24, H23, F22, E24, D25, C25, D24, B25, H21, G22, B24, C24, D23, C23, E19, C19, B21, B20, D19, B19, G17, E18, G19, F17, A20, A19, E17, D18, M3, N6, P24<br>**LFE2-35:** K3, K2, K1, L2, L1, M2, M1, N2, M8, P3, R3, R4, U2, V2, W2, AF20, AE20, AA20, W18, AD20, AE21, AF21, AF22, P26, P25, R24, R23, P20, R19, L20, J26, J25, J23, K23, H26, H25, H24, H23, E19, C19, B21, B20, D19, B19, G17, E18, G19, F17, A20, A19, E17, D18, M3, N6, P24<br>**LFE2-50:** N6, P24, M3<br>**LFE2-70:** M8, L20, M3, P24, N6 | A2, A3, A4, A5, AB28, AC4, AD23, AE1, AE2, AE29, AE3, AE30, AE4, AE5, AE6, AF1, AF2, AF23, AF26, AF27, AF28, AF29, AF3, AF30, AF4, AF5, AG1, AG13, AG16, AG18, AG2, AG26, AG27, AG28, AG29, AG3, AG30, AG4, AG8, AH1, AH16, AH2, AH26, AH27, AH29, AH30, AH4, AJ1, AJ2, AJ27, AJ28, AJ29, AJ3, AJ30, AK2, AK27, AK28, AK29, AK3, B1, B2, B3, B30, B4, B5, C1, C2, C29, C30, C4, D13, D18, D23, D28, D29, D3, D30, D4, E25, E26, E27, E28, E29, E3, E30, E4, E5, E6, F25, F5, F6, G6, G7, K10, K9, N27, N4, R1, R2, V27, V4 |

1. All grounds must be electrically connected at the board level. For fpBGA packages, the total number of GND balls is less than the actual number of GND logic connections from the die to the common package GND plane.
2. NC pins should not be connected to any active signals, VCC or GND.
3. Pin orientation A1 starts from the upper left corner of the top side view with alphabetical order ascending vertically and numerical order ascending horizontally.

# LFE2-12E/SE and LFE2-20E/SE Logic Signal Connections: 208 PQFP (Cont.)

| LFE2-12E/SE | | | | | LFE2-20E/SE | | | |
|---|---|---|---|---|---|---|---|---|
| Pin Number | Pin/Pad Function | Bank | Dual Function | Differential | Pin/Pad Function | Bank | Dual Function | Differential |
| 46 | PL28B | 6 | LDQ28 | C (LVDS)* | PL42B | 6 | LDQ42 | C (LVDS)* |
| 47 | PL30A | 6 | LDQ28 | | PL44A | 6 | LDQ42 | |
| 48 | TCK | - | | | TCK | - | | |
| 49 | TDI | - | | | TDI | - | | |
| 50 | TDO | - | | | TDO | - | | |
| 51 | VCCJ | - | | | VCCJ | - | | |
| 52 | TMS | - | | | TMS | - | | |
| 53 | PB2A | 5 | VREF2_5/BDQ6 | T | PB2A | 5 | VREF2_5/BDQ6 | T |
| 54 | PB2B | 5 | VREF1_5/BDQ6 | C | PB2B | 5 | VREF1_5/BDQ6 | C |
| 55 | VCCIO5 | 5 | | | VCCIO5 | 5 | | |
| 56 | PB6A | 5 | BDQS6 | T | PB6A | 5 | BDQS6 | T |
| 57 | PB6B | 5 | BDQ6 | C | PB6B | 5 | BDQ6 | C |
| 58 | PB8A | 5 | BDQ6 | T | PB8A | 5 | BDQ6 | T |
| 59 | PB8B | 5 | BDQ6 | C | PB8B | 5 | BDQ6 | C |
| 60 | GND | - | | | GND | - | | |
| 61 | PB12A | 5 | BDQ15 | T | PB12A | 5 | BDQ15 | T |
| 62 | PB12B | 5 | BDQ15 | C | PB12B | 5 | BDQ15 | C |
| 63 | VCCIO5 | 5 | | | VCCIO5 | 5 | | |
| 64 | PB16A | 5 | BDQ15 | T | PB16A | 5 | BDQ15 | T |
| 65 | PB16B | 5 | BDQ15 | C | PB16B | 5 | BDQ15 | C |
| 66 | PB18A | 5 | BDQ15 | T | PB18A | 5 | BDQ15 | T |
| 67 | PB18B | 5 | BDQ15 | C | PB18B | 5 | BDQ15 | C |
| 68 | GND | - | | | GND | - | | |
| 69 | PB20A | 5 | BDQ24 | T | PB30A | 5 | BDQ33 | T |
| 70 | VCCAUX | - | | | VCCAUX | - | | |
| 71 | PB20B | 5 | BDQ24 | C | PB30B | 5 | BDQ33 | C |
| 72 | PB22A | 5 | BDQ24 | T | PB32A | 5 | BDQ33 | T |
| 73 | PB22B | 5 | BDQ24 | C | PB32B | 5 | BDQ33 | C |
| 74 | VCC | - | | | VCC | - | | |
| 75 | PB26A | 5 | PCLKT5_0/BDQ24 | T | PB35A | 5 | PCLKT5_0/BDQ33 | T |
| 76 | PB26B | 5 | PCLKC5_0/BDQ24 | C | PB35B | 5 | PCLKC5_0/BDQ33 | C |
| 77 | GND | - | | | GND | - | | |
| 78 | PB31A | 4 | PCLKT4_0/BDQ33 | T | PB40A | 4 | PCLKT4_0/BDQ42 | T |
| 79 | PB31B | 4 | PCLKC4_0/BDQ33 | C | PB40B | 4 | PCLKC4_0/BDQ42 | C |
| 80 | VCC | - | | | VCC | - | | |
| 81 | GND | - | | | GND | - | | |
| 82 | PB34A | 4 | BDQ33 | T | PB42A | 4 | BDQS42 | T |
| 83 | PB34B | 4 | BDQ33 | C | PB42B | 4 | BDQ42 | C |
| 84 | PB36A | 4 | BDQ33 | T | PB44A | 4 | BDQ42 | T |
| 85 | PB36B | 4 | BDQ33 | C | PB44B | 4 | BDQ42 | C |
| 86 | VCCAUX | - | | | VCCAUX | - | | |
| 87 | PB40A | 4 | BDQ42 | T | PB50A | 4 | BDQ51 | T |
| 88 | PB40B | 4 | BDQ42 | C | PB50B | 4 | BDQ51 | C |
| 89 | GND | - | | | GND | - | | |
| 90 | PB42A | 4 | BDQS42 | T | PB52A | 4 | BDQ51 | T |
| 91 | PB42B | 4 | BDQ42 | C | PB52B | 4 | BDQ51 | C |

# LFE2-20E/SE and LFE2-35E/SE Logic Signal Connections: 672 fpBGA

| LFE2-20E/20SE | | | | | LFE2-35E/35SE | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| D2 | PL2A | 7 | VREF2_7 | T (LVDS)* | PL2A | 7 | VREF2_7/LDQ6 | T (LVDS)* |
| D1 | PL2B | 7 | VREF1_7 | C (LVDS)* | PL2B | 7 | VREF1_7/LDQ6 | C (LVDS)* |
| GND | GNDIO7 | - | | | GNDIO7 | - | | |
| F6 | PL3A | 7 | | T | PL3A | 7 | LDQ6 | T |
| F5 | PL3B | 7 | | C | PL3B | 7 | LDQ6 | C |
| VCCIO | VCCIO7 | 7 | | | VCCIO7 | 7 | | |
| E4 | NC | - | | | PL4A | 7 | LDQ6 | T (LVDS)* |
| E3 | NC | - | | | PL4B | 7 | LDQ6 | C (LVDS)* |
| E2 | NC | - | | | PL5A | 7 | LDQ6 | T |
| E1 | NC | - | | | PL5B | 7 | LDQ6 | C |
| GND | GNDIO7 | - | | | GNDIO7 | - | | |
| H6 | NC | - | | | PL6A | 7 | LDQS6 | T (LVDS)* |
| H5 | NC | - | | | PL6B | 7 | LDQ6 | C (LVDS)* |
| F2 | NC | - | | | PL7A | 7 | LDQ6 | T |
| VCCIO | VCCIO7 | 7 | | | VCCIO7 | 7 | | |
| F1 | NC | - | | | PL7B | 7 | LDQ6 | C |
| H8 | NC | - | | | PL8A | 7 | LDQ6 | T (LVDS)* |
| J9 | NC | - | | | PL8B | 7 | LDQ6 | C (LVDS)* |
| G4 | NC | - | | | PL9A | 7 | LDQ6 | T |
| GND | GNDIO7 | - | | | GNDIO7 | - | | |
| G3 | NC | - | | | PL9B | 7 | LDQ6 | C |
| H7 | PL4A | 7 | LDQ8 | T (LVDS)* | PL10A | 7 | LDQ14 | T (LVDS)* |
| J8 | PL4B | 7 | LDQ8 | C (LVDS)* | PL10B | 7 | LDQ14 | C (LVDS)* |
| G2 | PL5A | 7 | LDQ8 | T | PL11A | 7 | LDQ14 | T |
| G1 | PL5B | 7 | LDQ8 | C | PL11B | 7 | LDQ14 | C |
| H3 | PL6A | 7 | LDQ8 | T (LVDS)* | PL12A | 7 | LDQ14 | T (LVDS)* |
| VCCIO | VCCIO7 | 7 | | | VCCIO7 | 7 | | |
| H4 | PL6B | 7 | LDQ8 | C (LVDS)* | PL12B | 7 | LDQ14 | C (LVDS)* |
| J5 | PL7A | 7 | LDQ8 | T | PL13A | 7 | LDQ14 | T |
| J4 | PL7B | 7 | LDQ8 | C | PL13B | 7 | LDQ14 | C |
| J3 | PL8A | 7 | LDQS8 | T (LVDS)* | PL14A | 7 | LDQS14 | T (LVDS)* |
| GND | GNDIO7 | - | | | GNDIO7 | - | | |
| K4 | PL8B | 7 | LDQ8 | C (LVDS)* | PL14B | 7 | LDQ14 | C (LVDS)* |
| H1 | PL9A | 7 | LDQ8 | T | PL15A | 7 | LDQ14 | T |
| H2 | PL9B | 7 | LDQ8 | C | PL15B | 7 | LDQ14 | C |
| VCCIO | VCCIO7 | 7 | | | VCCIO7 | 7 | | |
| K6 | PL10A | 7 | LDQ8 | T (LVDS)* | PL16A | 7 | LDQ14 | T (LVDS)* |
| K7 | PL10B | 7 | LDQ8 | C (LVDS)* | PL16B | 7 | LDQ14 | C (LVDS)* |
| J1 | PL11A | 7 | LDQ8 | T | PL17A | 7 | LDQ14 | T |
| J2 | PL11B | 7 | LDQ8 | C | PL17B | 7 | LDQ14 | C |
| GND | GNDIO7 | - | | | GNDIO7 | - | | |
| VCCIO | VCCIO7 | 7 | | | VCCIO7 | 7 | | |
| K3 | NC | - | | | NC | - | | |
| K2 | NC | - | | | NC | - | | |
| GND | GNDIO7 | - | | | GNDIO7 | - | | |
| K1 | NC | - | | | NC | - | | |

# LFE2-20E/SE and LFE2-35E/SE Logic Signal Connections: 672 fpBGA (Cont.)

| LFE2-20E/20SE | | | | | LFE2-35E/35SE | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| U1 | NC | - | | | PL34A | 6 | LDQ31 | T |
| V1 | NC | - | | | PL34B | 6 | LDQ31 | C |
| GND | GNDIO6 | - | | | GNDIO6 | - | | |
| P3 | NC | - | | | NC | - | | |
| R3 | NC | - | | | NC | - | | |
| R4 | NC | - | | | NC | - | | |
| U2 | NC | - | | | NC | - | | |
| VCCIO | VCCIO6 | 6 | | | VCCIO6 | 6 | | |
| V2 | NC | - | | | NC | - | | |
| W2 | NC | - | | | NC | - | | |
| T6 | NC | - | | | PL38A | 6 | LDQ39 | T |
| R5 | NC | - | | | PL38B | 6 | LDQ39 | C |
| GND | GNDIO6 | - | | | GNDIO6 | - | | |
| R6 | PL25A | 6 | LDQS25*** | T (LVDS)* | PL39A | 6 | LDQS39*** | T (LVDS)* |
| R7 | PL25B | 6 | LDQ25 | C (LVDS)* | PL39B | 6 | LDQ39 | C (LVDS)* |
| W1 | PL26A | 6 | LDQ25 | T | PL40A | 6 | LDQ39 | T |
| VCCIO | VCCIO6 | 6 | | | VCCIO6 | 6 | | |
| Y2 | PL26B | 6 | LDQ25 | C | PL40B | 6 | LDQ39 | C |
| Y1 | PL27A | 6 | LLM0_GDLLT_IN_A**/LDQ25 | T (LVDS)* | PL41A | 6 | LLM0_GDLLT_IN_A**/LDQ39 | T (LVDS)* |
| AA2 | PL27B | 6 | LLM0_GDLLC_IN_A**/LDQ25 | C (LVDS)* | PL41B | 6 | LLM0_GDLLC_IN_A**/LDQ39 | C (LVDS)* |
| T5 | PL28A | 6 | LLM0_GDLLT_FB_A/LDQ25 | T | PL42A | 6 | LLM0_GDLLT_FB_A/LDQ39 | T |
| GND | GNDIO6 | - | | | GNDIO6 | - | | |
| T7 | PL28B | 6 | LLM0_GDLLC_FB_A/LDQ25 | C | PL42B | 6 | LLM0_GDLLC_FB_A/LDQ39 | C |
| R8 | VCC | 6 | | | VCCPLL | 6 | | |
| T8 | LLM0_PLLCAP | 6 | | | LLM0_PLLCAP | 6 | | |
| U3 | PL30A | 6 | LLM0_GPLLT_IN_A**/LDQ34 | T (LVDS)* | PL44A | 6 | LLM0_GPLLT_IN_A**/LDQ48 | T (LVDS)* |
| U4 | PL30B | 6 | LLM0_GPLLC_IN_A**/LDQ34 | C (LVDS)* | PL44B | 6 | LLM0_GPLLC_IN_A**/LDQ48 | C (LVDS)* |
| V3 | PL31A | 6 | LLM0_GPLLT_FB_A/LDQ34 | T | PL45A | 6 | LLM0_GPLLT_FB_A/LDQ48 | T |
| U5 | PL31B | 6 | LLM0_GPLLC_FB_A/LDQ34 | C | PL45B | 6 | LLM0_GPLLC_FB_A/LDQ48 | C |
| V4 | PL32A | 6 | LDQ34 | T (LVDS)* | PL46A | 6 | LDQ48 | T (LVDS)* |
| VCCIO | VCCIO6 | 6 | | | VCCIO6 | 6 | | |
| V5 | PL32B | 6 | LDQ34 | C (LVDS)* | PL46B | 6 | LDQ48 | C (LVDS)* |
| Y3 | PL33A | 6 | LDQ34 | T | PL47A | 6 | LDQ48 | T |
| Y4 | PL33B | 6 | LDQ34 | C | PL47B | 6 | LDQ48 | C |
| W3 | PL34A | 6 | LDQS34 | T (LVDS)* | PL48A | 6 | LDQS48 | T (LVDS)* |
| GND | GNDIO6 | - | | | GNDIO6 | - | | |
| W4 | PL34B | 6 | LDQ34 | C (LVDS)* | PL48B | 6 | LDQ48 | C (LVDS)* |
| AA1 | PL35A | 6 | LDQ34 | T | PL49A | 6 | LDQ48 | T |
| AB1 | PL35B | 6 | LDQ34 | C | PL49B | 6 | LDQ48 | C |
| VCCIO | VCCIO6 | 6 | | | VCCIO6 | 6 | | |
| U8 | PL36A | 6 | LDQ34 | T (LVDS)* | PL50A | 6 | LDQ48 | T (LVDS)* |
| U7 | PL36B | 6 | LDQ34 | C (LVDS)* | PL50B | 6 | LDQ48 | C (LVDS)* |
| V8 | PL37A | 6 | LDQ34 | T | PL51A | 6 | LDQ48 | T |
| U6 | PL37B | 6 | LDQ34 | C | PL51B | 6 | LDQ48 | C |
| GND | GNDIO6 | - | | | GNDIO6 | - | | |
| W6 | PL38A | 6 | LDQ42 | T (LVDS)* | PL52A | 6 | LDQ56 | T (LVDS)* |

# LFE2-20E/SE and LFE2-35E/SE Logic Signal Connections: 672 fpBGA (Cont.)

| LFE2-20E/20SE | | | | | LFE2-35E/35SE | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| G24 | PR6B | 2 | RDQ8 | C (LVDS)* | PR12B | 2 | RDQ14 | C (LVDS)* |
| G23 | PR6A | 2 | RDQ8 | T (LVDS)* | PR12A | 2 | RDQ14 | T (LVDS)* |
| VCCIO | VCCIO2 | 2 | | | VCCIO2 | 2 | | |
| K19 | PR5B | 2 | RDQ8 | C | PR11B | 2 | RDQ14 | C |
| J19 | PR5A | 2 | RDQ8 | T | PR11A | 2 | RDQ14 | T |
| D26 | PR4B | 2 | RDQ8 | C (LVDS)* | PR10B | 2 | RDQ14 | C (LVDS)* |
| C26 | PR4A | 2 | RDQ8 | T (LVDS)* | PR10A | 2 | RDQ14 | T (LVDS)* |
| F22 | NC | - | | | PR9B | 2 | RDQ6 | C |
| E24 | NC | - | | | PR9A | 2 | RDQ6 | T |
| GND | GNDIO2 | - | | | GNDIO2 | - | | |
| D25 | NC | - | | | PR8B | 2 | RDQ6 | C (LVDS)* |
| C25 | NC | - | | | PR8A | 2 | RDQ6 | T (LVDS)* |
| D24 | NC | - | | | PR7B | 2 | RDQ6 | C |
| B25 | NC | - | | | PR7A | 2 | RDQ6 | T |
| VCCIO | VCCIO2 | 2 | | | VCCIO2 | 2 | | |
| H21 | NC | - | | | PR6B | 2 | RDQ6 | C (LVDS)* |
| G22 | NC | - | | | PR6A | 2 | RDQS6 | T (LVDS)* |
| B24 | NC | - | | | PR5B | 2 | RDQ6 | C |
| GND | GNDIO2 | - | | | GNDIO2 | - | | |
| C24 | NC | - | | | PR5A | 2 | RDQ6 | T |
| D23 | NC | - | | | PR4B | 2 | RDQ6 | C (LVDS)* |
| C23 | NC | - | | | PR4A | 2 | RDQ6 | T (LVDS)* |
| G21 | PR3B | 2 | | C | PR3B | 2 | RDQ6 | C |
| VCCIO | VCCIO2 | 2 | | | VCCIO2 | 2 | | |
| H20 | PR3A | 2 | | T | PR3A | 2 | RDQ6 | T |
| GND | GNDIO2 | - | | | GNDIO2 | - | | |
| E22 | PR2B | 2 | VREF2_2 | C (LVDS)* | PR2B | 2 | VREF2_2/RDQ6 | C (LVDS)* |
| F21 | PR2A | 2 | VREF1_2 | T (LVDS)* | PR2A | 2 | VREF1_2/RDQ6 | T (LVDS)* |
| E23 | PT64B | 1 | VREF2_1 | C | PT73B | 1 | VREF2_1 | C |
| GND | GNDIO1 | - | | | GNDIO1 | - | | |
| D22 | PT64A | 1 | VREF1_1 | T | PT73A | 1 | VREF1_1 | T |
| G20 | PT63B | 1 | | C | PT72B | 1 | | C |
| J18 | PT63A | 1 | | T | PT72A | 1 | | T |
| F20 | PT62B | 1 | | C | PT71B | 1 | | C |
| VCCIO | VCCIO1 | 1 | | | VCCIO1 | 1 | | |
| H19 | PT62A | 1 | | T | PT71A | 1 | | T |
| A24 | PT61B | 1 | | C | PT70B | 1 | | C |
| A23 | PT61A | 1 | | T | PT70A | 1 | | T |
| E21 | PT60B | 1 | | C | PT69B | 1 | | C |
| F19 | PT60A | 1 | | T | PT69A | 1 | | T |
| C22 | PT59B | 1 | | C | PT68B | 1 | | C |
| GND | GNDIO1 | - | | | GNDIO1 | - | | |
| E20 | PT59A | 1 | | T | PT68A | 1 | | T |
| B22 | PT58B | 1 | | C | PT67B | 1 | | C |
| VCCIO | VCCIO1 | 1 | | | VCCIO1 | 1 | | |
| B23 | PT58A | 1 | | T | PT67A | 1 | | T |

# LFE2-50E/SE and LFE2-70E/SE Logic Signal Connections: 672 fpBGA (Cont.)

| LFE2-50E/SE | | | | | LFE2-70E/SE | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| D4 | PT7B | 0 | | C | PT7B | 0 | | C |
| D3 | PT7A | 0 | | T | PT7A | 0 | | T |
| C2 | PT6B | 0 | | C | PT6B | 0 | | C |
| C1 | PT6A | 0 | | T | PT6A | 0 | | T |
| G8 | PT5B | 0 | | C | PT5B | 0 | | C |
| GND | GNDIO0 | - | | | GNDIO0 | - | | |
| G7 | PT5A | 0 | | T | PT5A | 0 | | T |
| E7 | PT4B | 0 | | C | PT4B | 0 | | C |
| VCCIO | VCCIO0 | 0 | | | VCCIO0 | 0 | | |
| F7 | PT4A | 0 | | T | PT4A | 0 | | T |
| E6 | PT3B | 0 | | C | PT3B | 0 | | C |
| E5 | PT3A | 0 | | T | PT3A | 0 | | T |
| G6 | PT2B | 0 | VREF2_0 | C | PT2B | 0 | VREF2_0 | C |
| G5 | PT2A | 0 | VREF1_0 | T | PT2A | 0 | VREF1_0 | T |
| L12 | VCC | - | | | VCC | - | | |
| L13 | VCC | - | | | VCC | - | | |
| L14 | VCC | - | | | VCC | - | | |
| L15 | VCC | - | | | VCC | - | | |
| M11 | VCC | - | | | VCC | - | | |
| M12 | VCC | - | | | VCC | - | | |
| M15 | VCC | - | | | VCC | - | | |
| M16 | VCC | - | | | VCC | - | | |
| N11 | VCC | - | | | VCC | - | | |
| N16 | VCC | - | | | VCC | - | | |
| P11 | VCC | - | | | VCC | - | | |
| P16 | VCC | - | | | VCC | - | | |
| R11 | VCC | - | | | VCC | - | | |
| R12 | VCC | - | | | VCC | - | | |
| R15 | VCC | - | | | VCC | - | | |
| R16 | VCC | - | | | VCC | - | | |
| T12 | VCC | - | | | VCC | - | | |
| T13 | VCC | - | | | VCC | - | | |
| T14 | VCC | - | | | VCC | - | | |
| T15 | VCC | - | | | VCC | - | | |
| D11 | VCCIO0 | 0 | | | VCCIO0 | 0 | | |
| D6 | VCCIO0 | 0 | | | VCCIO0 | 0 | | |
| G9 | VCCIO0 | 0 | | | VCCIO0 | 0 | | |
| K12 | VCCIO0 | 0 | | | VCCIO0 | 0 | | |
| J12 | VCCIO0 | 0 | | | VCCIO0 | 0 | | |
| D16 | VCCIO1 | 1 | | | VCCIO1 | 1 | | |
| D21 | VCCIO1 | 1 | | | VCCIO1 | 1 | | |
| G18 | VCCIO1 | 1 | | | VCCIO1 | 1 | | |
| J15 | VCCIO1 | 1 | | | VCCIO1 | 1 | | |
| K15 | VCCIO1 | 1 | | | VCCIO1 | 1 | | |
| F23 | VCCIO2 | 2 | | | VCCIO2 | 2 | | |
| J20 | VCCIO2 | 2 | | | VCCIO2 | 2 | | |

## LFE2-70E/SE Logic Signal Connections: 900 fpBGA (Cont.)

| LFE2-70E/SE | | | | |
|---|---|---|---|---|
| **Ball Number** | **Ball/Pad Function** | **Bank** | **Dual Function** | **Differential** |
| K1 | PL27B | 7 | LDQ29 | C (LVDS)* |
| K5 | PL28A | 7 | LDQ29 | T |
| K7 | PL28B | 7 | LDQ29 | C |
| GND | GNDIO7 | - | | |
| K4 | PL29A | 7 | LDQS29 | T (LVDS)* |
| K3 | PL29B | 7 | LDQ29 | C (LVDS)* |
| L8 | PL30A | 7 | LDQ29 | T |
| VCCIO | VCCIO7 | 7 | | |
| L6 | PL30B | 7 | LDQ29 | C |
| L2 | PL31A | 7 | LDQ29 | T (LVDS)* |
| L1 | PL31B | 7 | LDQ29 | C (LVDS)* |
| L7 | PL32A | 7 | LDQ29 | T |
| GND | GNDIO7 | - | | |
| L5 | PL32B | 7 | LDQ29 | C |
| L4 | PL33A | 7 | LDQ37 | T (LVDS)* |
| L3 | PL33B | 7 | LDQ37 | C (LVDS)* |
| M8 | PL34A | 7 | LDQ37 | T |
| M6 | PL34B | 7 | LDQ37 | C |
| VCCIO | VCCIO7 | 7 | | |
| M2 | PL35A | 7 | LDQ37 | T (LVDS)* |
| M1 | PL35B | 7 | LDQ37 | C (LVDS)* |
| M7 | PL36A | 7 | LDQ37 | T |
| M5 | PL36B | 7 | LDQ37 | C |
| GND | GNDIO7 | - | | |
| M4 | PL37A | 7 | LDQS37 | T (LVDS)* |
| M3 | PL37B | 7 | LDQ37 | C (LVDS)* |
| N6 | PL38A | 7 | LUM0_SPLLT_IN_A/LDQ37 | T |
| VCCIO | VCCIO7 | 7 | | |
| N8 | PL38B | 7 | LUM0_SPLLC_IN_A/LDQ37 | C |
| N5 | PL39A | 7 | LUM0_SPLLT_FB_A/LDQ37 | T |
| N7 | PL39B | 7 | LUM0_SPLLC_FB_A/LDQ37 | C |
| GND | GNDIO7 | - | | |
| VCCIO | VCCIO7 | 7 | | |
| T9 | PL50A | 7 | LDQ54 | |
| R9 | PL51A | 7 | LDQ54 | T |
| P7 | PL51B | 7 | LDQ54 | C |
| VCCIO | VCCIO7 | 7 | | |
| N2 | PL52A | 7 | LDQ54 | T (LVDS)* |
| N1 | PL52B | 7 | LDQ54 | C (LVDS)* |
| P6 | PL53A | 7 | LDQ54 | T |
| P5 | PL53B | 7 | LDQ54 | C |
| GND | GNDIO7 | - | | |
| P4 | PL54A | 7 | LDQS54 | T (LVDS)* |

## LFE2-70E/SE Logic Signal Connections: 900 fpBGA (Cont.)

| LFE2-70E/SE | | | | |
|---|---|---|---|---|
| **Ball Number** | **Ball/Pad Function** | **Bank** | **Dual Function** | **Differential** |
| AD18 | PB66A | 4 | BDQ69 | T |
| AF18 | PB66B | 4 | BDQ69 | C |
| AC18 | PB67A | 4 | BDQ69 | T |
| AE18 | PB67B | 4 | BDQ69 | C |
| VCCIO | VCCIO4 | 4 | | |
| AG19 | PB68A | 4 | BDQ69 | T |
| AH19 | PB68B | 4 | BDQ69 | C |
| GND | GNDIO4 | - | | |
| AE19 | PB69A | 4 | BDQS69 | T |
| AF19 | PB69B | 4 | BDQ69 | C |
| AC19 | PB70A | 4 | BDQ69 | T |
| AD19 | PB70B | 4 | BDQ69 | C |
| AJ19 | PB71A | 4 | BDQ69 | T |
| AK19 | PB71B | 4 | BDQ69 | C |
| VCCIO | VCCIO4 | 4 | | |
| AF20 | PB72A | 4 | BDQ69 | T |
| AH20 | PB72B | 4 | BDQ69 | C |
| AE20 | PB73A | 4 | BDQ69 | T |
| AG20 | PB73B | 4 | BDQ69 | C |
| GND | GNDIO4 | - | | |
| AD20 | PB74A | 4 | BDQ78 | T |
| AC20 | PB74B | 4 | BDQ78 | C |
| AH21 | PB75A | 4 | BDQ78 | T |
| AF21 | PB75B | 4 | BDQ78 | C |
| AJ20 | PB76A | 4 | BDQ78 | T |
| VCCIO | VCCIO4 | 4 | | |
| AK20 | PB76B | 4 | BDQ78 | C |
| AG21 | PB77A | 4 | BDQ78 | T |
| AE21 | PB77B | 4 | BDQ78 | C |
| AD21 | PB78A | 4 | BDQS78 | T |
| GND | GNDIO4 | - | | |
| AC21 | PB78B | 4 | BDQ78 | C |
| AD22 | PB79A | 4 | BDQ78 | T |
| AB21 | PB79B | 4 | BDQ78 | C |
| AJ21 | PB80A | 4 | BDQ78 | T |
| VCCIO | VCCIO4 | 4 | | |
| AK21 | PB80B | 4 | BDQ78 | C |
| GND | GNDIO4 | - | | |
| VCCIO | VCCIO4 | 4 | | |
| AJ25 | PB87A | 4 | BDQS87*** | T |
| AK24 | PB87B | 4 | BDQ87 | C |
| AJ24 | PB88A | 4 | BDQ87 | T |
| AK25 | PB88B | 4 | BDQ87 | C |

# LFE2M20E/SE and LFE2M35E/SE Logic Signal Connections: 484 fpBGA (Cont.)

| LFE2M20E/SE | | | | | LFE2M35E/SE | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| V5 | PL51A | 6 | LDQS51 | T (LVDS)* | PL66A | 6 | LDQS66 | T (LVDS)* |
| U4 | PL51B | 6 | LDQ51 | C (LVDS)* | PL66B | 6 | LDQ66 | C (LVDS)* |
| V1 | PL52A | 6 | LDQ51 | T | PL67A | 6 | LDQ66 | T |
| VCCIO | VCCIO6 | 6 | | | VCCIO6 | 6 | | |
| V3 | PL52B | 6 | LDQ51 | C | PL67B | 6 | LDQ66 | C |
| W1 | PL53A | 6 | LDQ51 | T (LVDS)* | PL68A | 6 | LDQ66 | T (LVDS)* |
| Y1 | PL53B | 6 | LDQ51 | C (LVDS)* | PL68B | 6 | LDQ66 | C (LVDS)* |
| AA1 | PL54A | 6 | LDQ51 | T | PL69A | 6 | LDQ66 | T |
| GNDIO | GNDIO6 | - | | | GNDIO6 | - | | |
| AA2 | PL54B | 6 | LDQ51 | C | PL69B | 6 | LDQ66 | C |
| V4 | TCK | - | | | TCK | - | | |
| Y2 | TDI | - | | | TDI | - | | |
| Y3 | TMS | - | | | TMS | - | | |
| W3 | TDO | - | | | TDO | - | | |
| W4 | VCCJ | - | | | VCCJ | - | | |
| W5 | PB2A | 5 | BDQ6 | T | PB2A | 5 | BDQ6 | T |
| Y4 | PB2B | 5 | BDQ6 | C | PB2B | 5 | BDQ6 | C |
| W6 | PB3A | 5 | BDQ6 | T | PB3A | 5 | BDQ6 | T |
| V6 | PB3B | 5 | BDQ6 | C | PB3B | 5 | BDQ6 | C |
| AA3 | PB4A | 5 | BDQ6 | T | PB4A | 5 | BDQ6 | T |
| VCCIO | VCCIO5 | 5 | | | VCCIO5 | 5 | | |
| AB2 | PB4B | 5 | BDQ6 | C | PB4B | 5 | BDQ6 | C |
| T8 | PB5A | 5 | BDQ6 | T | PB5A | 5 | BDQ6 | T |
| U7 | PB5B | 5 | BDQ6 | C | PB5B | 5 | BDQ6 | C |
| U8 | PB6A | 5 | BDQS6 | T | PB6A | 5 | BDQS6 | T |
| GNDIO | GNDIO5 | - | | | GNDIO5 | - | | |
| T9 | PB6B | 5 | BDQ6 | C | PB6B | 5 | BDQ6 | C |
| V8 | PB7A | 5 | BDQ6 | T | PB7A | 5 | BDQ6 | T |
| W8 | PB7B | 5 | BDQ6 | C | PB7B | 5 | BDQ6 | C |
| Y6 | PB8A | 5 | BDQ6 | T | PB8A | 5 | BDQ6 | T |
| VCCIO | VCCIO5 | 5 | | | VCCIO5 | 5 | | |
| Y5 | PB8B | 5 | BDQ6 | C | PB8B | 5 | BDQ6 | C |
| AB3 | PB9A | 5 | BDQ6 | T | PB9A | 5 | BDQ6 | T |
| AB4 | PB9B | 5 | BDQ6 | C | PB9B | 5 | BDQ6 | C |
| AB5 | PB10A | 5 | BDQ6 | T | PB10A | 5 | BDQ6 | T |
| GNDIO | GNDIO5 | - | | | GNDIO5 | - | | |
| AA6 | PB10B | 5 | BDQ6 | C | PB10B | 5 | BDQ6 | C |
| V9 | PB13A | 5 | BDQ15 | T | PB31A | 5 | BDQ33 | T |
| U9 | PB13B | 5 | BDQ15 | C | PB31B | 5 | BDQ33 | C |
| VCCIO | VCCIO5 | 5 | | | VCCIO5 | 5 | | |
| - | - | - | | | GNDIO5 | - | | |
| U10 | PB14A | 5 | BDQ15 | T | PB32A | 5 | BDQ33 | T |
| T10 | PB14B | 5 | BDQ15 | C | PB32B | 5 | BDQ33 | C |
| GNDIO | GNDIO5 | - | | | GNDIO5 | - | | |
| W9 | PB15A | 5 | BDQS15**** | T | PB33A | 5 | BDQS33**** | T |
| Y8 | PB15B | 5 | BDQ15 | C | PB33B | 5 | BDQ33 | C |
| AA7 | PB16A | 5 | VREF2_5/BDQ15 | T | PB34A | 5 | VREF2_5/BDQ33 | T |
| Y7 | PB16B | 5 | VREF1_5/BDQ15 | C | PB34B | 5 | VREF1_5/BDQ33 | C |

## LFE2M100E/SE Logic Signal Connections: 900 fpBGA (Cont.)

| LFE2M100E/SE | | | | |
|---|---|---|---|---|
| **Ball Number** | **Ball/Pad Function** | **Bank** | **Dual Function** | **Differential** |
| AB27 | PR97A | 3 | RDQ99 | T (LVDS)* |
| VCCIO | VCCIO3 | 3 | | |
| Y24 | PR96B | 3 | RDQ99 | C |
| Y25 | PR96A | 3 | RDQ99 | T |
| AA29 | PR95B | 3 | RDQ99 | C (LVDS)* |
| Y28 | PR95A | 3 | RDQ99 | T (LVDS)* |
| Y30 | PR93B | 3 | RDQ90 | C |
| Y29 | PR93A | 3 | RDQ90 | T |
| GNDIO | GNDIO3 | - | | |
| VCCIO | VCCIO3 | 3 | | |
| W22 | PR83B | 3 | RDQ81 | C (LVDS)* |
| V22 | PR83A | 3 | RDQ81 | T (LVDS)* |
| Y27 | PR82B | 3 | RDQ81 | C |
| VCCIO | VCCIO3 | 3 | | |
| Y26 | PR82A | 3 | RDQ81 | T |
| W30 | PR81B | 3 | RDQ81 | C (LVDS)* |
| W29 | PR81A | 3 | RDQS81 | T (LVDS)* |
| GNDIO | GNDIO3 | - | | |
| W25 | PR80B | 3 | RDQ81 | C |
| W26 | PR80A | 3 | RDQ81 | T |
| U29 | PR79B | 3 | RDQ81 | C (LVDS)* |
| V29 | PR79A | 3 | RDQ81 | T (LVDS)* |
| VCCIO | VCCIO3 | 3 | | |
| V30 | PR78B | 3 | RDQ81 | C |
| U30 | PR78A | 3 | RDQ81 | T |
| W27 | PR77B | 3 | RDQ81 | C (LVDS)* |
| W28 | PR77A | 3 | RDQ81 | T (LVDS)* |
| V24 | PR75B | 3 | RDQ72 | C |
| V25 | PR75A | 3 | RDQ72 | T |
| GNDIO | GNDIO3 | - | | |
| U28 | PR74B | 3 | RDQ72 | C (LVDS)* |
| U27 | PR74A | 3 | RDQ72 | T (LVDS)* |
| U23 | PR73B | 3 | RDQ72 | C |
| V23 | PR73A | 3 | RDQ72 | T |
| VCCIO | VCCIO3 | 3 | | |
| V26 | PR72B | 3 | RDQ72 | C (LVDS)* |
| U26 | PR72A | 3 | RDQS72 | T (LVDS)* |
| U25 | PR71B | 3 | RDQ72 | C |
| GNDIO | GNDIO3 | - | | |
| U24 | PR71A | 3 | RDQ72 | T |
| T30 | PR70B | 3 | RDQ72 | C (LVDS)* |
| R30 | PR70A | 3 | RDQ72 | T (LVDS)* |
| T23 | PR69B | 3 | RDQ72 | C |

## LFE2M100E/SE Logic Signal Connections: 900 fpBGA (Cont.)

| LFE2M100E/SE | | | | |
|---|---|---|---|---|
| **Ball Number** | **Ball/Pad Function** | **Bank** | **Dual Function** | **Differential** |
| H14 | PT61A | 0 | | T |
| A14 | PT60B | 0 | | C |
| B14 | PT60A | 0 | | T |
| D13 | PT59B | 0 | | C |
| GNDIO | GNDIO0 | - | | |
| F13 | PT59A | 0 | | T |
| G13 | PT58B | 0 | | C |
| VCCIO | VCCIO0 | 0 | | |
| J11 | PT58A | 0 | | T |
| D4 | PT57B | 0 | | |
| D5 | PT56A | 0 | | |
| E5 | PT55B | 0 | | C |
| F6 | PT55A | 0 | | T |
| GNDIO | GNDIO0 | - | | |
| VCCIO | VCCIO0 | 0 | | |
| F7 | PT52B | 0 | | C |
| D8 | PT52A | 0 | | T |
| GNDIO | GNDIO0 | - | | |
| J13 | PT50B | 0 | | C |
| G11 | PT50A | 0 | | T |
| H13 | PT49B | 0 | | C |
| H12 | PT49A | 0 | | T |
| VCCIO | VCCIO0 | 0 | | |
| E8 | PT48B | 0 | | C |
| D9 | PT48A | 0 | | T |
| D12 | PT46B | 0 | | C |
| GNDIO | GNDIO0 | - | | |
| E13 | PT46A | 0 | | T |
| VCCIO | VCCIO0 | 0 | | |
| GNDIO | GNDIO0 | - | | |
| J12 | PT31B | 0 | | C |
| - | - | - | | |
| VCCIO | VCCIO0 | 0 | | |
| H10 | PT31A | 0 | | T |
| E12 | PT30B | 0 | | C |
| D11 | PT30A | 0 | | T |
| H11 | PT29B | 0 | | C |
| F11 | PT29A | 0 | | T |
| C13 | ULC_SQ_VCCRX0 | 11 | | |
| A12 | ULC_SQ_HDINP0 | 11 | | T |
| B13 | ULC_SQ_VCCIB0 | 11 | | |
| B12 | ULC_SQ_HDINN0 | 11 | | C |
| C10 | ULC_SQ_VCCTX0 | 11 | | |

# LatticeECP2/M Family Data Sheet Supplemental Information

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## For Further Information

A variety of technical notes for the LatticeECP2/M family are available on the Lattice web site at www.latticesemi.com.

- TN1102, LatticeECP2/M sysIO Usage Guide
- TN1103, LatticeECP2/M sysCLOCK PLL Design and Usage Guide
- TN1104, LatticeECP2/M Memory Usage Guide
- TN1105, LatticeECP2/M High-Speed I/O Interface
- TN1106, Power Estimation and Management for LatticeECP2/M Devices
- TN1107, LatticeECP2/M sysDSP Usage Guide
- TN1108, LatticeECP2/M sysCONFIG Usage Guide
- TN1109, LatticeECP2/M Configuration Encryption Usage Guide
- TN1113, LatticeECP2/M Soft Error Detection (SED) Usage Guide
- TN1124, LatticeECP2M SERDES/PCS Usage Guide
- TN1162, LatticeECP2/M Hardware Checklist

For further information about interface standards refer to the following web sites:

- JEDEC Standards (LVTTL, LVCMOS, SSTL, HSTL): www.jedec.org
- PCI: www.pcisig.com