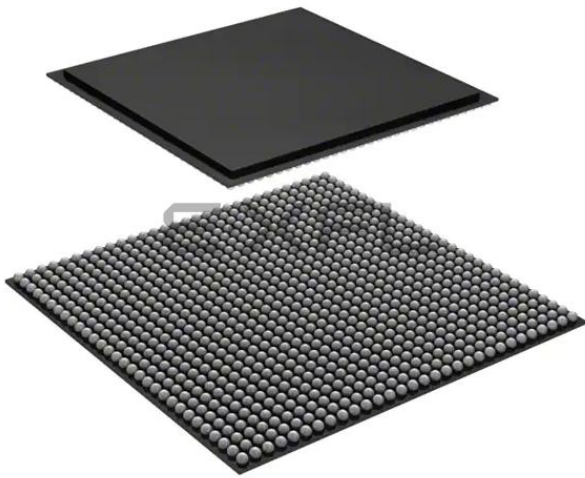




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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	8500
Number of Logic Elements/Cells	68000
Total RAM Bits	1056768
Number of I/O	583
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	900-BBGA
Supplier Device Package	900-FPBGA (31x31)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfe2-70se-6f900i

Edge Clock Sources

Edge clock resources can be driven from a variety of sources at the same edge. Edge clock resources can be driven from adjacent edge clock PIOs, primary clock PIOs, PLLs/DLLs and clock dividers as shown in Figure 2-12.

Figure 2-12. Edge Clock Sources

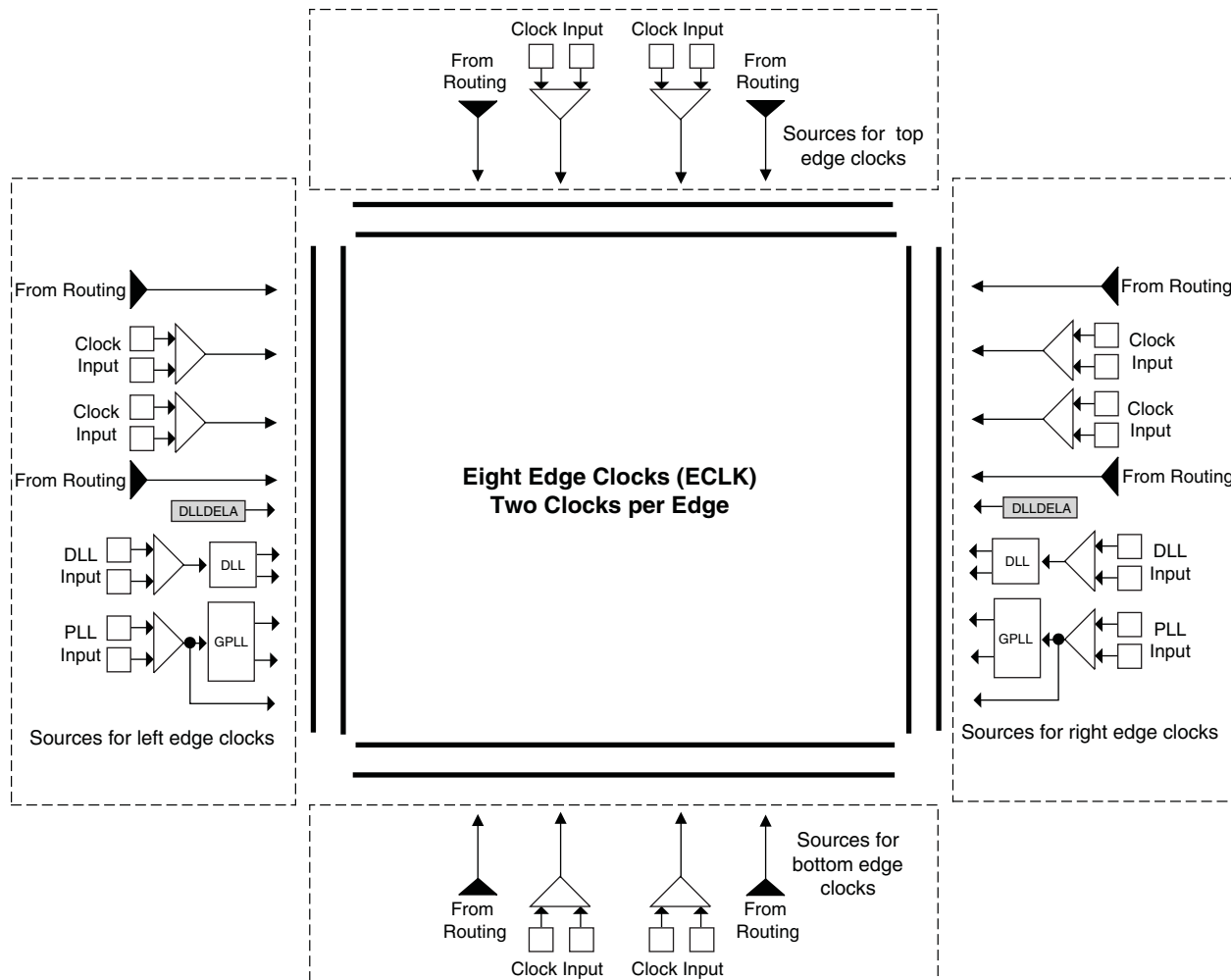
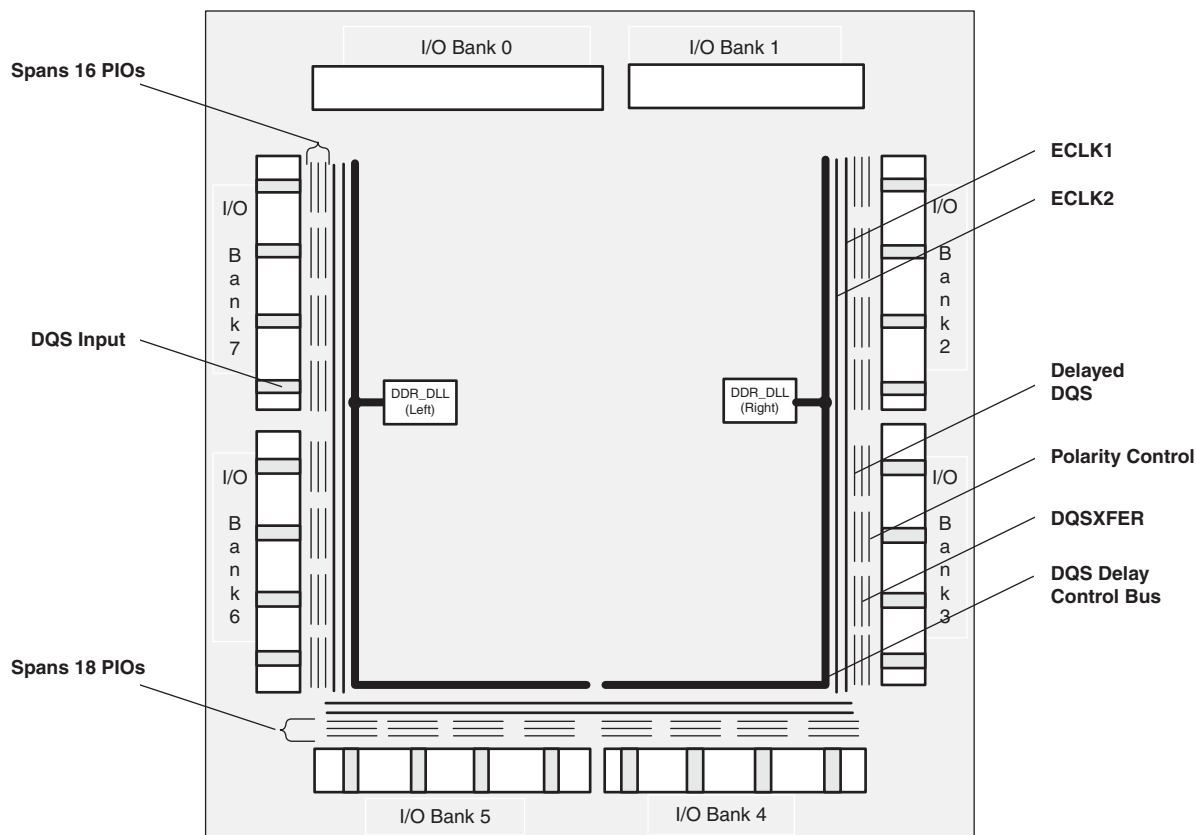


Figure 2-35. Edge Clock, DLL Calibration and DQS Local Bus Distribution



Note: Bank 8 is not shown.

DQSXFER

LatticeECP2/M devices provide a DQSXFER signal to the output buffer to assist it in data transfer to DDR memories that require DQS strobe be shifted 90°. This shifted DQS strobe is generated by the DQSDEL block. The DQSXFER signal runs the span of the data bus.

sysI/O Buffer

Each I/O is associated with a flexible buffer referred to as a sysI/O buffer. These buffers are arranged around the periphery of the device in groups referred to as banks. The sysI/O buffers allow users to implement the wide variety of standards that are found in today's systems including LVCMOS, SSTL, HSTL, LVDS and LVPECL.

sysI/O Buffer Banks

LatticeECP2/M devices have nine sysI/O buffer banks: eight banks for user I/Os arranged two per side. The ninth sysI/O buffer bank (Bank 8) is located adjacent to Bank 3 and has dedicated/shared I/Os for configuration. When a shared pin is not used for configuration it is available as a user I/O. Each bank is capable of supporting multiple I/O standards. Each sysI/O bank has its own I/O supply voltage (V_{CCIO}). In addition, each bank, except Bank 8, has voltage references, V_{REF1} and V_{REF2} , which allow it to be completely independent from the others. Bank 8 shares two voltage references, V_{REF1} and V_{REF2} , with Bank 3. Figure 2-37 shows the nine banks and their associated supplies.

In LatticeECP2/M devices, single-ended output buffers and ratioed input buffers (LVTTL, LVCMOS and PCI) are powered using V_{CCIO} . LVTTL, LVCMOS33, LVCMOS25 and LVCMOS12 can also be set as fixed threshold inputs independent of V_{CCIO} .

Each bank can support up to two separate V_{REF} voltages, V_{REF1} and V_{REF2} , that set the threshold for the referenced input buffers. Some dedicated I/O pins in a bank can be configured to be a reference voltage supply pin. Each I/O is individually configurable based on the bank's supply and reference voltages.

for checking soft errors (SED) in SRAM. SED can be run on a programmed device when the user logic is not active. If a soft error occurs, during user mode (normal operation) the device can be programmed to either reload from a known good boot image or generate an error signal.

For further information about Soft Error Detect (SED) support, please see the list of additional technical documentation at the end of this data sheet.

External Resistor

LatticeECP2/M devices require a single external, 10K ohm $\pm 1\%$ value between the XRES pin and ground. Device configuration will not be completed if this resistor is missing. There is no boundary scan register on the external resistor pad.

On-Chip Oscillator

Every LatticeECP2/M device has an internal CMOS oscillator which is used to derive a Master Clock for configuration. The oscillator and the Master Clock run continuously and are available to user logic after configuration is completed. The software default value of the Master Clock is 2.5MHz. Table 2-16 lists all the available Master Configuration Clock frequencies for normal non-encrypted mode and encrypted mode. When a different Master Clock is selected during the design process, the following sequence takes place:

1. Device powers up with a Master Clock frequency of 3.1MHz.
2. During configuration, users select a different master clock frequency.
3. The Master Clock frequency changes to the selected frequency once the clock configuration bits are received.
4. If the user does not select a master clock frequency, then the configuration bitstream defaults to the Master Clock frequency of 2.5MHz.

This internal CMOS oscillator is available to the user by routing it as an input clock to the clock tree. For further information about the use of this oscillator for configuration or user mode, please see the list of additional technical documentation at the end of this data sheet.

Table 2-16. Selectable Master Clock (CCLK) Frequencies During Configuration

Non-Encrypted Mode CCLK (MHz)			Encrypted Mode CCLK (MHz)
2.5 ¹	13.0	45.0	2.5 ¹
4.3	15.0	55.0	5.4
5.4	20.0	60.0	10.0
6.9	26.0	—	—
8.1	30.0	—	—
9.2	34.0	—	—
10.0	41.0	130.0	—

1. Software default frequency.

Density Shifting

The LatticeECP2/M family is designed to ensure that different density devices in the same family and in the same package have the same pinout. Furthermore, the architecture ensures a high success rate when performing design migration from lower density devices to higher density devices. In many cases, it is also possible to shift a lower utilization design targeted for a high-density device to a lower density device. However, the exact details of the final resource utilization will impact the likelihood of success in each case. Design migration between LatticeECP2 and LatticeECP2M families is not possible. For specific requirements relating to sysCONFIG pins of the ECP2M50, M70 and M100, see the Logic Signal Connections tables.

LatticeECP2 Supply Current (Standby)^{1, 2, 3, 4}
Over Recommended Operating Conditions

Symbol	Parameter	Device	Typ. ⁵	Units
I_{CC}	Core Power Supply Current	ECP2-6	10	mA
		ECP2-12	20	mA
		ECP2-20	30	mA
		ECP2-35	50	mA
		ECP2-50	70	mA
		ECP2-70	100	mA
I_{CCAUX}	Auxiliary Power Supply Current	ECP2-6	24	mA
		ECP2-12	24	mA
		ECP2-20	24	mA
		ECP2-35	24	mA
		ECP2-50	24	mA
		ECP2-70	24	mA
I_{CCGPLL}	GPLL Power Supply Current (per GPLL)	ECP2-35, -50, -70 Only	0.5	mA
I_{CCSPLL}	GPLL Power Supply Current (per SPLL)	ECP2-35, -50, -70 Only	0.5	mA
I_{CCIO}	Bank Power Supply Current (Per Bank)	ECP2-6	2	mA
		ECP2-12	2	mA
		ECP2-20	2	mA
		ECP2-35	2	mA
		ECP2-50	2	mA
		ECP2-70	2	mA
I_{CCJ}	VCCJ Power Supply Current	All Devices	3	mA

1. For further information about supply current, please see the list of additional technical documentation at the end of this data sheet.
2. Assumes all outputs are tristated, all inputs are configured as LVCMOS and held at the V_{CCIO} or GND.
3. Frequency 0MHz.
4. Pattern represents a "blank" configuration data file.
5. $T_J = 25^{\circ}\text{C}$, power supplies at normal voltage.

LatticeECP2/M External Switching Characteristics⁹

Over Recommended Operating Conditions

Parameter	Description	Device	-7		-6		-5		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
General I/O Pin Parameters (using Primary Clock without PLL) ¹									
t _{CO}	Clock to Output - PIO Output Register	LFE2-6	—	3.50	—	3.90	—	4.20	ns
		LFE2-12	—	3.50	—	3.90	—	4.20	ns
		LFE2-20	—	3.50	—	3.90	—	4.20	ns
		LFE2-35	—	3.50	—	3.90	—	4.20	ns
		LFE2-50	—	3.50	—	3.90	—	4.20	ns
		LFE2-70	—	3.70	—	4.10	—	4.40	ns
		LFE2M20	—	3.90	—	4.30	—	4.70	ns
		LFE2M35	—	3.90	—	4.30	—	4.70	ns
		LFE2M50	—	4.50	—	5.00	—	5.40	ns
		LFE2M70	—	4.50	—	5.00	—	5.40	ns
		LFE2M100	—	4.50	—	5.00	—	5.40	ns
t _{SU}	Clock to Data Setup - PIO Input Register	LFE2-6	0.00	—	0.00	—	0.00	—	ns
		LFE2-12	0.00	—	0.00	—	0.00	—	ns
		LFE2-20	0.00	—	0.00	—	0.00	—	ns
		LFE2-35	0.00	—	0.00	—	0.00	—	ns
		LFE2-50	0.00	—	0.00	—	0.00	—	ns
		LFE2-70	0.00	—	0.00	—	0.00	—	ns
		LFE2M20	0.00	—	0.00	—	0.00	—	ns
		LFE2M35	0.00	—	0.00	—	0.00	—	ns
		LFE2M50	0.00	—	0.00	—	0.00	—	ns
		LFE2M70	0.00	—	0.00	—	0.00	—	ns
		LFE2M100	0.00	—	0.00	—	0.00	—	ns
t _H	Clock to Data Hold - PIO Input Register	LFE2-6	1.40	—	1.70	—	1.90	—	ns
		LFE2-12	1.40	—	1.70	—	1.90	—	ns
		LFE2-20	1.40	—	1.70	—	1.90	—	ns
		LFE2-35	1.40	—	1.70	—	1.90	—	ns
		LFE2-50	1.40	—	1.70	—	1.90	—	ns
		LFE2-70	1.40	—	1.70	—	1.90	—	ns
		LFE2M20	1.40	—	1.70	—	1.90	—	ns
		LFE2M35	1.40	—	1.70	—	1.90	—	ns
		LFE2M50	1.80	—	2.10	—	2.30	—	ns
		LFE2M70	1.80	—	2.10	—	2.30	—	ns
		LFE2M100	1.80	—	2.10	—	2.30	—	ns

LatticeECP2M Power Supply and NC (Cont.)

Signal	672 fpBGA	900 fpBGA
V _{CC}	LFE2M35: AD13, AD14, AD16, AD17, AD19, AD21, AD22, AD24, AD25, L12, L13, L14, L15, M11, M12, M15, M16, N11, N16, P11, P16, R11, R12, R15, R16, T12, T13, T14, T15 LFE2M50: L12, L13, L14, L15, M11, M12, M15, M16, N11, N16, P11, P16, R11, R12, R15, R16, T12, T13, T14, T15	LFE2M50: AH1, AH4, AH5, AH2, AH7, AH12, AH9, AH10, AH13, C13, C10, C9, C12, C7, C2, C5, C4, C1, L12, L13, L18, L19, M11, M12, M13, M14, M15, M16, M17, M18, M19, M20, N11, N12, N19, N20, P12, P19, R12, R19, T12, T19, U12, U19, V11, V12, V19, V20, W11, W12, W13, W14, W15, W16, W17, W18, W19, W20, Y12, Y13, Y18, Y19 LFE2M70/LFE2M100: L12, L13, L18, L19, M11, M12, M13, M14, M15, M16, M17, M18, M19, M20, N11, N12, N19, N20, P12, P19, R12, R19, T12, T19, U12, U19, V11, V12, V19, V20, W11, W12, W13, W14, W15, W16, W17, W18, W19, W20, Y12, Y13, Y18, Y19
V _{CCIO0}	B12, B7, F11, J13, K12	D14, E6, E9, F12, K12, K13
V _{CCIO1}	D18, F16, J14, K15	D17, E22, E25, F19, K18, K19
V _{CCIO2}	G25, L21, M17, M25, N18	F28, J25, K28, M21, M24, N21, N28, P21, R25
V _{CCIO3}	P18, R17, R25, T21, Y25	AA28, AB25, AE28, T25, U21, V21, V28, W21, W24
V _{CCIO4}	AA16, AC18, U15, V14	AA18, AA19, AE19, AF22, AG17, AG25
V _{CCIO5}	AA11, AE12, AE7, U12, V13	AA12, AA13, AE12, AF9, AG14, AG6
V _{CCIO6}	P9, R10, R2, T6, Y2	AA3, AB6, AE3, T6, U10, V10, V3, W10, W7
V _{CCIO7}	G2, L6, M10, M2, N9	F3, J6, K3, M10, M7, N10, N3, P10, R6
V _{CCIO8}	AC24, U17	AA25, AD28
V _{CCJ}	AA7	AG1
V _{CCAUX}	LFE2M35: AE19, J11, J12, J15, J16, L18, L9, M18, M9, R18, R9, T18, T9, V11, V12, V15, V16 LFE2M50: J11, J12, J15, J16, L18, L9, M18, M9, R18, R9, T18, T9, V11, V12, V15, V16	LFE2M50: AJ7, B7, AA10, AA11, AA20, AA21, K10, K11, K20, K21, L10, L11, L20, L21, Y10, Y11, Y20, Y21 LFE2M70/LFE2M100: AA10, AA11, AA20, AA21, K10, K11, K20, K21, L10, L11, L20, L21, Y10, Y11, Y20, Y21
V _{CCPLL}	H7, K6, P7, R8, V18, P20, J17, G19	N13, N18, V13, V18
SERDES Power ³	LFE2M35: C25, B25, C22, A22, C21, C20, C24, C23, B19, C19, C15, C14, C18, C17, A16, C16, B13, C13 LFE2M50: AD13, AE13, AD16, AF16, AD17, AD18, AD14, AD15, AD19, AE19, AD23, AD24, AD20, AD21, AF22, AD22, AE25, AD25, C25, B25, C22, A22, C21, C20, C24, C23, B19, C19, C15, C14, C18, C17, A16, C16, B13, C13	LFE2M50: AH18, AJ18, AH21, AK21, AH22, AH23, AH19, AH20, AH24, AJ24, AH28, AH29, AH25, AH26, AK27, AH27, AJ30, AH30, C30, B30, C27, A27, C26, C25, C29, C28, B24, C24, C20, C19, C23, C22, A21, C21, B18, C18 LFE2M70/LFE2M100: C13, B13, C10, A10, C9, C8, C12, C11, B7, C7, C3, C2, C6, C5, A4, C4, B1, C1, C30, B30, C27, A27, C26, C25, C29, C28, B24, C24, C20, C19, C23, C22, A21, C21, B18, C18, AH18, AJ18, AH21, AK21, AH22, AH23, AH19, AH20, AH24, AJ24, AH28, AH29, AH25, AH26, AK27, AH27, AJ30, AH30, AH1, AJ1, AH4, AK4, AH5, AH6, AH2, AH3, AH7, AJ7, AH11, AH12, AH8, AH9, AK10, AH10, AJ13, AH13

LFE2-6E/SE and LFE2-12E/SE Logic Signal Connections: 256 fpBGA (Cont.)

LFE2-6E/SE					LFE2-12E/SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
F15	PR11B	2	RDQ10	C	PR11B	2	RDQ10	C
G11	PR12B	2	RDQ10	C (LVDS)*	PR12B	2	RDQ10	C (LVDS)*
F14	PR11A	2	RDQ10	T	PR11A	2	RDQ10	T
VCCIO	VCCIO2	2			VCCIO2	2		
F12	PR12A	2	RDQ10	T (LVDS)*	PR12A	2	RDQ10	T (LVDS)*
G14	PR10B	2	RDQ10	C (LVDS)*	PR10B	2	RDQ10	C (LVDS)*
G13	PR10A	2	RDQS10	T (LVDS)*	PR10A	2	RDQS10	T (LVDS)*
GND	GNDIO2	-			GNDIO2	-		
F16	PR8B	2	RDQ10	C (LVDS)*	PR8B	2	RDQ10	C (LVDS)*
F9	PR9B	2	RDQ10	C	PR9B	2	RDQ10	C
E16	PR8A	2	RDQ10	T (LVDS)*	PR8A	2	RDQ10	T (LVDS)*
F10	PR9A	2	RDQ10	T	PR9A	2	RDQ10	T
VCCIO	VCCIO2	2			VCCIO2	2		
D16	PR7B	2	RDQ10	C	PR7B	2	RDQ10	C
D15	PR7A	2	RDQ10	T	PR7A	2	RDQ10	T
C15	PR4B	2		C (LVDS)*	PR4B	2		C (LVDS)*
C16	PR5B	2		C	PR5B	2		C
GND	GNDIO2	-			GNDIO2	-		
D14	PR4A	2		T (LVDS)*	PR4A	2		T (LVDS)*
B16	PR5A	2		T	PR5A	2		T
F13	PR2B	2	VREF2_2	C (LVDS)*	PR2B	2	VREF2_2	C (LVDS)*
VCCIO	VCCIO2	2			VCCIO2	2		
E13	PR2A	2	VREF1_2	T (LVDS)*	PR2A	2	VREF1_2	T (LVDS)*
F11	PT28B	1	VREF2_1	C	PT55B	1	VREF2_1	C
E11	PT28A	1	VREF1_1	T	PT55A	1	VREF1_1	T
GND	GNDIO1	-			GNDIO1	-		
A15	PT27B	1		C	PT54B	1		C
E12	PT26B	1		C	PT53B	1		C
B15	PT27A	1		T	PT54A	1		T
VCCIO	VCCIO1	1			VCCIO1	1		
D12	PT26A	1		T	PT53A	1		T
B14	PT25B	1		C	PT52B	1		C
C14	PT24B	1		C	PT51B	1		C
A14	PT25A	1		T	PT52A	1		T
D13	PT24A	1		T	PT51A	1		T
C13	PT23B	1		C	PT50B	1		C
GND	GNDIO1	-			GNDIO1	-		
A13	PT22B	1		C	PT49B	1		C
B13	PT23A	1		T	PT50A	1		T
VCCIO	VCCIO1	1			VCCIO1	1		
A12	PT22A	1		T	PT49A	1		T
B11	PT21B	1		C	PT48B	1		C
D11	PT20B	1		C	PT47B	1		C
A11	PT21A	1		T	PT48A	1		T
C11	PT20A	1		T	PT47A	1		T

LFE2-20E/SE Logic Signal Connections: 256 fpBGA (Cont.)

LFE2-20E/SE					
Ball Number	Ball Number	Ball/Pad Function	Bank	Dual Function	Differential
GND	GND	GNDIO5	-		
R4	R4	PB33A	5	BDQS33	T
L6	L6	PB34A	5	BDQ33	T
T4	T4	PB33B	5	BDQ33	C
L7	L7	PB34B	5	BDQ33	C
N7	N7	PB35A	5	PCLKT5_0/BDQ33	T
VCCIO	VCCIO	VCCIO5	5		
M8	M8	PB35B	5	PCLKC5_0/BDQ33	C
GND	GND	GNDIO5	-		
P7	P7	PB40A	4	PCLKT4_0/BDQ42	T
R8	R8	PB40B	4	PCLKC4_0/BDQ42	C
VCCIO	VCCIO	VCCIO4	4		
T5	T5	PB41A	4	BDQ42	T
T6	T6	PB41B	4	BDQ42	C
T8	T8	PB42A	4	BDQS42	T
GND	GND	GNDIO4	-		
R7	R7	PB43A	4	BDQ42	T
T9	T9	PB42B	4	BDQ42	C
T7	T7	PB43B	4	BDQ42	C
L8	L8	PB44A	4	BDQ42	T
VCCIO	VCCIO	VCCIO4	4		
P8	P8	PB45A	4	BDQ42	T
L9	L9	PB44B	4	BDQ42	C
N8	N8	PB45B	4	BDQ42	C
R9	R9	PB46A	4	BDQ42	T
GND	GND	GNDIO4	-		
R10	R10	PB46B	4	BDQ42	C
-	VCC	VCCIO	4		
-	GND	GNDIO4	4		
N9	N9	PB56A	4	BDQ60	T
T10	T10	PB57A	4	BDQ60	T
M9	M9	PB56B	4	BDQ60	C
R11	R11	PB57B	4	BDQ60	C
P10	P10	PB58A	4	BDQ60	T
N11	N11	PB59A	4	BDQ60	T
VCCIO	VCCIO	VCCIO4	4		
N10	N10	PB58B	4	BDQ60	C
P11	P11	PB59B	4	BDQ60	C
T11	T11	PB60A	4	BDQS60	T
GND	GND	GNDIO4	-		
M11	M11	PB61A	4	BDQ60	T
T12	T12	PB60B	4	BDQ60	C

LFE2-12E/SE and LFE2-20E/SE Logic Signal Connections: 484 fpBGA
(Cont.)

LFE2-12E/12SE					LFE2-20E/20SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
M6	PL15B	6	PCLKC6_0	C (LVDS)*	PL21B	6	PCLKC6_0/LDQ25	C (LVDS)*
M3	PL16A	6	VREF2_6	T	PL22A	6	VREF2_6/LDQ25	T
GNDIO	GNDIO6	-			-	-		
M4	PL16B	6	VREF1_6	C	PL22B	6	VREF1_6/LDQ25	C
-	-	-			VCCIO6	6		
N1	NC	-			PL24A	6	LDQ25	T
M2	NC	-			PL23A	6	LDQ25	T (LVDS)*
N2	NC	-			PL24B	6	LDQ25	C
M1	NC	-			PL23B	6	LDQ25	C (LVDS)*
-	-	-			GNDIO	-		
N3	NC	-			PL25A	6	LDQS25	T (LVDS)*
N5	NC	-			PL26A	6	LDQ25	T
N4	NC	-			PL25B	6	LDQ25	C (LVDS)*
-	-	-			VCCIO6	6		
P5	NC	-			PL26B	6	LDQ25	C
P1	PL17A	6	LLM0_GDLLT_IN_A**	T (LVDS)*	PL27A	6	LLM0_GDLLT_IN_A**/LDQ25	T (LVDS)*
P2	PL17B	6	LLM0_GDLLC_IN_A**	C (LVDS)*	PL27B	6	LLM0_GDLLC_IN_A**/LDQ25	C (LVDS)*
P4	PL18A	6	LLM0_GDLLT_FB_A	T	PL28A	6	LLM0_GDLLT_FB_A/LDQ25	T
-	-	-			GNDIO	-		
R4	PL18B	6	LLM0_GDLLC_FB_A	C	PL28B	6	LLM0_GDLLC_FB_A/LDQ25	C
P6	LLM0_PLLCAP	6			LLM0_PLLCAP	6		
R1	PL20A	6	LLM0_GPLLT_IN_A**	T (LVDS)*	PL30A	6	LLM0_GPLLT_IN_A**/LDQ34	T (LVDS)*
GNDIO	GNDIO6	-			-	-		
R3	PL21A	6	LLM0_GPLLT_FB_A	T	PL31A	6	LLM0_GPLLT_FB_A/LDQ34	T
R2	PL20B	6	LLM0_GPLLC_IN_A**	C (LVDS)*	PL30B	6	LLM0_GPLLC_IN_A/LDQ34	C (LVDS)*
T4	PL21B	6	LLM0_GPLLC_FB_A	C	PL31B	6	LLM0_GPLLC_FB_A/LDQ34	C
T5	PL23A	6		T	PL33A	6	LDQ34	T
VCCIO	VCCIO6	6			VCCIO6	6		
T1	PL22A	6		T (LVDS)*	PL32A	6	LDQ34	T (LVDS)*
T3	PL23B	6		C	PL33B	6	LDQ34	C
T2	PL22B	6		C (LVDS)*	PL32B	6	LDQ34	C (LVDS)*
GNDIO	GNDIO6	-			GNDIO6	-		
-	-	-			VCCIO6	6		
V1	PL25A	6	LDQ28	T	PL39A	6	LDQ42	T
-	-	-			GNDIO	-		
V2	PL25B	6	LDQ28	C	PL39B	6	LDQ42	C
U1	PL24A	6	LDQ28	T (LVDS)*	PL38A	6	LDQ42	T (LVDS)*
U3	PL27A	6	LDQ28	T	PL41A	6	LDQ42	T
VCCIO	VCCIO6	6			VCCIO6	6		
U2	PL24B	6	LDQ28	C (LVDS)*	PL38B	6	LDQ42	C (LVDS)*
U4	PL27B	6	LDQ28	C	PL41B	6	LDQ42	C
R6	PL26A	6	LDQ28	T (LVDS)*	PL40A	6	LDQ42	T (LVDS)*
R7	PL29A	6	LDQ28	T	PL43A	6	LDQ42	T
GNDIO	GNDIO6	-			GNDIO	-		

LFE2-12E/SE and LFE2-20E/SE Logic Signal Connections: 484 fpBGA (Cont.)

LFE2-12E/12SE					LFE2-20E/20SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential	
T7	PL29B	6	LDQ28	C	PL43B	6	LDQ42	C	
T6	PL26B	6	LDQ28	C (LVDS)*	PL40B	6	LDQ42	C (LVDS)*	
AA2	PL31A	6	LDQ28	T	PL45A	6	LDQ42	T	
VCCIO	VCCIO6	6			VCCIO6	6			
Y1	PL28A	6	LDQS28	T (LVDS)*	PL42A	6	LDQS42	T (LVDS)*	
AA1	PL31B	6	LDQ28	C	PL45B	6	LDQ42	C	
W1	PL28B	6	LDQ28	C (LVDS)*	PL42B	6	LDQ42	C (LVDS)*	
V3	PL30B	6	LDQ28	C (LVDS)*	PL44B	6	LDQ42	C (LVDS)*	
GNDIO	GNDIO6	-			GNDIO	-			
V4	PL30A	6	LDQ28	T (LVDS)*	PL44A	6	LDQ42	T (LVDS)*	
U5	TDI	-			TDI	-			
U7	TCK	-			TCK	-			
V6	TDO	-			TDO	-			
V5	TMS	-			TMS	-			
T8	VCCJ	-			VCCJ	-			
W4	PB3A	5	BDQ6	T	PB3A	5	BDQ6	T	
Y3	PB2A	5	VREF2_5/BDQ6	T	PB2A	5	VREF2_5/BDQ6	T	
W3	PB3B	5	BDQ6	C	PB3B	5	BDQ6	C	
Y2	PB2B	5	VREF1_5/BDQ6	C	PB2B	5	VREF1_5/BDQ6	C	
AB3	PB5A	5	BDQ6	T	PB5A	5	BDQ6	T	
VCCIO	VCCIO5	5			VCCIO5	5			
W5	PB4A	5	BDQ6	T	PB4A	5	BDQ6	T	
AB2	PB5B	5	BDQ6	C	PB5B	5	BDQ6	C	
W6	PB4B	5	BDQ6	C	PB4B	5	BDQ6	C	
AB5	PB7A	5	BDQ6	T	PB7A	5	BDQ6	T	
GNDIO	GNDIO5	-			GNDIO	-			
Y4	PB6A	5	BDQS6	T	PB6A	5	BDQS6	T	
AB4	PB7B	5	BDQ6	C	PB7B	5	BDQ6	C	
AA3	PB6B	5	BDQ6	C	PB6B	5	BDQ6	C	
AB6	PB9A	5	BDQ6	T	PB9A	5	BDQ6	T	
VCCIO	VCCIO5	5			VCCIO5	5			
AA5	PB8A	5	BDQ6	T	PB8A	5	BDQ6	T	
AA6	PB9B	5	BDQ6	C	PB9B	5	BDQ6	C	
Y5	PB8B	5	BDQ6	C	PB8B	5	BDQ6	C	
GNDIO	GNDIO5	-			GNDIO	-			
-	-	-			VCCIO5	5			
Y6	PB12A	5	BDQ15	T	PB21A	5	BDQ24	T	
W7	PB11A	5	BDQ15	T	PB20A	5	BDQ24	T	
Y7	PB12B	5	BDQ15	C	PB21B	5	BDQ24	C	
W8	PB11B	5	BDQ15	C	PB20B	5	BDQ24	C	
U8	PB14A	5	BDQ15	T	PB23A	5	BDQ24	T	
VCCIO	VCCIO5	5			VCCIO5	5			
AA7	PB13A	5	BDQ15	T	PB22A	5	BDQ24	T	
U9	PB14B	5	BDQ15	C	PB23B	5	BDQ24	C	

LFE2-12E/SE and LFE2-20E/SE Logic Signal Connections: 484 fpBGA (Cont.)

LFE2-12E/12SE					LFE2-20E/20SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential	
R8	VCCIO6	6			VCCIO6	6			
J8	VCCIO7	7			VCCIO7	7			
K7	VCCIO7	7			VCCIO7	7			
L7	VCCIO7	7			VCCIO7	7			
M7	VCCIO7	7			VCCIO7	7			
P15	VCCIO8	8			VCCIO8	8			
R15	VCCIO8	8			VCCIO8	8			
C5	VCCAUX	-			VCCAUX	-			
D11	VCCAUX	-			VCCAUX	-			
E17	VCCAUX	-			VCCAUX	-			
E6	VCCAUX	-			VCCAUX	-			
F13	VCCAUX	-			VCCAUX	-			
G18	VCCAUX	-			VCCAUX	-			
G5	VCCAUX	-			VCCAUX	-			
K5	VCCAUX	-			VCCAUX	-			
M17	VCCAUX	-			VCCAUX	-			
P17	VCCAUX	-			VCCAUX	-			
R5	VCCAUX	-			VCCAUX	-			
V11	VCCAUX	-			VCCAUX	-			
V13	VCCAUX	-			VCCAUX	-			
V15	VCCAUX	-			VCCAUX	-			
V7	VCCAUX	-			VCCAUX	-			
V8	VCCAUX	-			VCCAUX	-			
A1	GND	-			GND	-			
A22	GND	-			GND	-			
AA19	GND	-			GND	-			
AA4	GND	-			GND	-			
AB1	GND	-			GND	-			
AB22	GND	-			GND	-			
B19	GND	-			GND	-			
B4	GND	-			GND	-			
C14	GND	-			GND	-			
C9	GND	-			GND	-			
D2	GND	-			GND	-			
D21	GND	-			GND	-			
F17	GND	-			GND	-			
F6	GND	-			GND	-			
H10	GND	-			GND	-			
H11	GND	-			GND	-			
H12	GND	-			GND	-			
H13	GND	-			GND	-			
J14	GND	-			GND	-			
J20	GND	-			GND	-			
J3	GND	-			GND	-			

LFE2-35E/SE and LFE2-50E/SE Logic Signal Connections: 484 fpBGA (Cont.)

LFE2-35E/SE					LFE2-50E/SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
U8	PB23A	5	BDQ24	T	PB32A	5	BDQ33	T
U9	PB23B	5	BDQ24	C	PB32B	5	BDQ33	C
W9	PB24A	5	BDQS24	T	PB33A	5	BDQS33	T
GNDIO	GNDIO5	-			GNDIO5	-		
V9	PB24B	5	BDQ24	C	PB33B	5	BDQ33	C
Y8	PB25A	5	BDQ24	T	PB34A	5	BDQ33	T
AA8	PB25B	5	BDQ24	C	PB34B	5	BDQ33	C
W10	PB26A	5	BDQ24	T	PB35A	5	BDQ33	T
VCCIO	VCCIO5	5			VCCIO	5		
V10	PB26B	5	BDQ24	C	PB35B	5	BDQ33	C
AB8	PB27A	5	BDQ24	T	PB36A	5	BDQ33	T
AA9	PB27B	5	BDQ24	C	PB36B	5	BDQ33	C
GNDIO	GNDIO5	-			GNDIO5	-		
AB9	PB29A	5	BDQ33	T	PB38A	5	BDQ42	T
AB10	PB29B	5	BDQ33	C	PB38B	5	BDQ42	C
Y10	PB30A	5	BDQ33	T	PB39A	5	BDQ42	T
AA10	PB30B	5	BDQ33	C	PB39B	5	BDQ42	C
U10	PB31A	5	BDQ33	T	PB40A	5	BDQ42	T
U11	PB31B	5	BDQ33	C	PB40B	5	BDQ42	C
VCCIO	VCCIO5	5			VCCIO	5		
AB11	PB32A	5	BDQ33	T	PB41A	5	BDQ42	T
AA11	PB32B	5	BDQ33	C	PB41B	5	BDQ42	C
GNDIO	GNDIO5	-			GNDIO5	-		
Y11	PB33A	5	BDQS33	T	PB42A	5	BDQS42	T
W11	PB33B	5	BDQ33	C	PB42B	5	BDQ42	C
AB12	PB34A	5	BDQ33	T	PB43A	5	BDQ42	T
AA12	PB34B	5	BDQ33	C	PB43B	5	BDQ42	C
AB13	PB35A	5	PCLKT5_0/BDQ33	T	PB44A	5	PCLKT5_0/BDQ42	T
AB14	PB35B	5	PCLKC5_0/BDQ33	C	PB44B	5	PCLKC5_0/BDQ42	C
VCCIO	VCCIO5	5			VCCIO	5		
GNDIO	GNDIO5	-			GNDIO5	-		
U12	PB40A	4	PCLKT4_0/BDQ42	T	PB49A	4	PCLKT4_0/BDQ51	T
VCCIO	VCCIO4	4			VCCIO	4		
V12	PB40B	4	PCLKC4_0/BDQ42	C	PB49B	4	PCLKC4_0/BDQ51	C
Y12	PB41A	4	BDQ42	T	PB50A	4	BDQ51	T
W12	PB41B	4	BDQ42	C	PB50B	4	BDQ51	C
AA13	PB42A	4	BDQS42	T	PB51A	4	BDQS51	T
GNDIO	GNDIO4	-			GNDIO4	-		
Y13	PB42B	4	BDQ42	C	PB51B	4	BDQ51	C
U13	PB43A	4	BDQ42	T	PB52A	4	BDQ51	T
U14	PB43B	4	BDQ42	C	PB52B	4	BDQ51	C
AB15	PB44A	4	BDQ42	T	PB53A	4	BDQ51	T
VCCIO	VCCIO4	4			VCCIO	4		
AA14	PB44B	4	BDQ42	C	PB53B	4	BDQ51	C
AB16	PB45A	4	BDQ42	T	PB54A	4	BDQ51	T
AB17	PB45B	4	BDQ42	C	PB54B	4	BDQ51	C

LFE2-20E/SE and LFE2-35E/SE Logic Signal Connections: 672 fpBGA (Cont.)

LFE2-20E/20SE					LFE2-35E/35SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential	
C20	PT57B	1		C	PT66B	1		C	
D20	PT57A	1		T	PT66A	1		T	
A22	PT56B	1		C	PT65B	1		C	
A21	PT56A	1		T	PT65A	1		T	
GND	GNDIO1	-			GNDIO1	-			
E19	NC	-			NC	-			
C19	NC	-			NC	-			
VCCIO	VCCIO1	1			VCCIO1	1			
B21	NC	-			NC	-			
B20	NC	-			NC	-			
D19	NC	-			NC	-			
B19	NC	-			NC	-			
GND	GNDIO1	-			GNDIO1	-			
G17	NC	-			NC	-			
E18	NC	-			NC	-			
G19	NC	-			NC	-			
F17	NC	-			NC	-			
VCCIO	VCCIO1	1			VCCIO1	1			
A20	NC	-			NC	-			
A19	NC	-			NC	-			
E17	NC	-			NC	-			
D18	NC	-			NC	-			
B18	PT55B	1		C	PT55B	1		C	
GND	GNDIO1	-			GNDIO1	-			
A18	PT55A	1		T	PT55A	1		T	
E16	PT54B	1		C	PT54B	1		C	
G16	PT54A	1		T	PT54A	1		T	
F16	PT53B	1		C	PT53B	1		C	
VCCIO	VCCIO1	1			VCCIO1	1			
H18	PT53A	1		T	PT53A	1		T	
A17	PT52B	1		C	PT52B	1		C	
B17	PT52A	1		T	PT52A	1		T	
C18	PT51B	1		C	PT51B	1		C	
B16	PT51A	1		T	PT51A	1		T	
C17	PT50B	1		C	PT50B	1		C	
GND	GNDIO1	-			GNDIO1	-			
D17	PT50A	1		T	PT50A	1		T	
E15	PT49B	1		C	PT49B	1		C	
VCCIO	VCCIO1	1			VCCIO1	1			
G15	PT49A	1		T	PT49A	1		T	
A16	PT48B	1		C	PT48B	1		C	
B15	PT48A	1		T	PT48A	1		T	
D15	PT47B	1		C	PT47B	1		C	
F15	PT47A	1		T	PT47A	1		T	
A14	PT46B	1		C	PT46B	1		C	
B14	PT46A	1		T	PT46A	1		T	

LFE2-50E/SE and LFE2-70E/SE Logic Signal Connections: 672 fpBGA (Cont.)

LFE2-50E/SE					LFE2-70E/SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
A2	GND	-			GND	-		
A25	GND	-			GND	-		
AA18	GND	-			GND	-		
AA24	GND	-			GND	-		
AA3	GND	-			GND	-		
AA9	GND	-			GND	-		
AD11	GND	-			GND	-		
AD16	GND	-			GND	-		
AD21	GND	-			GND	-		
AD6	GND	-			GND	-		
AE1	GND	-			GND	-		
AE26	GND	-			GND	-		
AF2	GND	-			GND	-		
AF25	GND	-			GND	-		
B1	GND	-			GND	-		
B26	GND	-			GND	-		
C11	GND	-			GND	-		
C16	GND	-			GND	-		
C21	GND	-			GND	-		
C6	GND	-			GND	-		
F18	GND	-			GND	-		
F24	GND	-			GND	-		
F3	GND	-			GND	-		
F9	GND	-			GND	-		
J13	GND	-			GND	-		
J14	GND	-			GND	-		
J21	GND	-			GND	-		
J6	GND	-			GND	-		
K10	GND	-			GND	-		
K11	GND	-			GND	-		
K13	GND	-			GND	-		
K14	GND	-			GND	-		
K16	GND	-			GND	-		
K17	GND	-			GND	-		
L10	GND	-			GND	-		
L11	GND	-			GND	-		
L16	GND	-			GND	-		
L17	GND	-			GND	-		
L24	GND	-			GND	-		
L3	GND	-			GND	-		
M13	GND	-			GND	-		
M14	GND	-			GND	-		
N10	GND	-			GND	-		
N12	GND	-			GND	-		
N13	GND	-			GND	-		
N14	GND	-			GND	-		

LFE2-70E/SE Logic Signal Connections: 900 fpBGA (Cont.)

LFE2-70E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential
P3	PL54B	7	LDQ54	C (LVDS)*
R6	PL55A	7	LDQ54	T
VCCIO	VCCIO7	7		
R8	PL55B	7	LDQ54	C
P2	PL56A	7	LDQ54	T (LVDS)*
P1	PL56B	7	LDQ54	C (LVDS)*
R5	PL57A	7	PCLKT7_0/LDQ54	T
GND	GNDIO7	-		
R7	PL57B	7	PCLKC7_0/LDQ54	C
R4	PL59A	6	PCLKT6_0/LDQ63	T (LVDS)*
R3	PL59B	6	PCLKC6_0/LDQ63	C (LVDS)*
T5	PL60A	6	VREF2_6/LDQ63	T
T7	PL60B	6	VREF1_6/LDQ63	C
T3	PL61A	6	LDQ63	T (LVDS)*
VCCIO	VCCIO6	6		
T4	PL61B	6	LDQ63	C (LVDS)*
T6	PL62A	6	LDQ63	T
T8	PL62B	6	LDQ63	C
T2	PL63A	6	LDQS63	T (LVDS)*
GND	GNDIO6	-		
T1	PL63B	6	LDQ63	C (LVDS)*
U7	PL64A	6	LDQ63	T
U5	PL64B	6	LDQ63	C
VCCIO	VCCIO6	6		
U4	PL65A	6	LDQ63	T (LVDS)*
U3	PL65B	6	LDQ63	C (LVDS)*
U8	PL66A	6	LDQ63	T
U6	PL66B	6	LDQ63	C
GND	GNDIO6	-		
U2	PL67A	6	LDQ71	T (LVDS)*
U1	PL67B	6	LDQ71	C (LVDS)*
V7	PL68A	6	LDQ71	T
V5	PL68B	6	LDQ71	C
VCCIO	VCCIO6	6		
V2	PL69A	6	LDQ71	T (LVDS)*
V1	PL69B	6	LDQ71	C (LVDS)*
V8	PL70A	6	LDQ71	T
V6	PL70B	6	LDQ71	C
GND	GNDIO6	-		
W1	PL71A	6	LDQS71	T (LVDS)*
W2	PL71B	6	LDQ71	C (LVDS)*
W5	PL72A	6	LDQ71	T
VCCIO	VCCIO6	6		

LFE2-70E/SE Logic Signal Connections: 900 fpBGA (Cont.)

LFE2-70E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential
U10	VCCIO6	6		
U9	VCCIO6	6		
V10	VCCIO6	6		
W10	VCCIO6	6		
W9	VCCIO6	6		
Y9	VCCIO6	6		
L10	VCCIO7	7		
L9	VCCIO7	7		
M10	VCCIO7	7		
N10	VCCIO7	7		
P10	VCCIO7	7		
R10	VCCIO7	7		
AA21	VCCIO8	8		
Y21	VCCIO8	8		
AA15	VCCAUX	-		
AB11	VCCAUX	-		
AB19	VCCAUX	-		
AB20	VCCAUX	-		
J11	VCCAUX	-		
J12	VCCAUX	-		
J19	VCCAUX	-		
K19	VCCAUX	-		
L22	VCCAUX	-		
M9	VCCAUX	-		
N9	VCCAUX	-		
P21	VCCAUX	-		
P9	VCCAUX	-		
T10	VCCAUX	-		
T21	VCCAUX	-		
V9	VCCAUX	-		
W22	VCCAUX	-		
A1	GND	-		
A30	GND	-		
AC28	GND	-		
AC3	GND	-		
AH13	GND	-		
AH18	GND	-		
AH23	GND	-		
AH28	GND	-		
AH3	GND	-		
AH8	GND	-		
AK1	GND	-		
AK30	GND	-		

LFE2M20E/SE and LFE2M35E/SE Logic Signal Connections: 484 fpBGA (Cont.)

LFE2M20E/SE					LFE2M35E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential	
L4	PL24B	7	LDQ22	C (LVDS)*	PL34B	7	LDQ32	C (LVDS)*	
M1	PL25A	7	PCLKT7_0/LDQ22	T	PL35A	7	PCLKT7_0/LDQ32	T	
GNDIO	GNDIO7	-			GNDIO7	-			
M2	PL25B	7	PCLKC7_0/LDQ22	C	PL35B	7	PCLKC7_0/LDQ32	C	
M6	PL27A	6	PCLKT6_0	T (LVDS)*	PL37A	6	PCLKT6_0	T (LVDS)*	
M5	PL27B	6	PCLKC6_0	C (LVDS)*	PL37B	6	PCLKC6_0	C (LVDS)*	
M3	PL28A	6	VREF2_6	T	PL38A	6	VREF2_6	T	
M4	PL28B	6	VREF1_6	C	PL38B	6	VREF1_6	C	
VCCIO	VCCIO6	6			VCCIO6	6			
N7	PL31A	6	LLM1_SPLLT_IN_A	T (LVDS)*	PL41A	6	LLM2_SPLLT_IN_A	T (LVDS)*	
GNDIO	GNDIO6	-			GNDIO6	-			
N6	PL31B	6	LLM1_SPLLC_IN_A	C (LVDS)*	PL41B	6	LLM2_SPLLC_IN_A	C (LVDS)*	
N1	PL32A	6	LLM1_SPLLT_FB_A	T	PL42A	6	LLM2_SPLLT_FB_A	T	
N2	PL32B	6	LLM1_SPLLC_FB_A	C	PL42B	6	LLM2_SPLLC_FB_A	C	
VCCIO	VCCIO6	6			VCCIO6	6			
GNDIO	GNDIO6	-			GNDIO6	-			
P6	PL38A	6	LDQS38****	T (LVDS)*	PL48A	6	LDQS48****	T (LVDS)*	
N5	PL38B	6	LDQ38	C (LVDS)*	PL48B	6	LDQ48	C (LVDS)*	
P1	PL39A	6	LDQ38	T	PL49A	6	LDQ48	T	
VCCIO	VCCIO6	6			VCCIO6	6			
P2	PL39B	6	LDQ38	C	PL49B	6	LDQ48	C	
P3	PL40A	6	LDQ38	T (LVDS)*	PL50A	6	LDQ48	T (LVDS)*	
P4	PL40B	6	LDQ38	C (LVDS)*	PL50B	6	LDQ48	C (LVDS)*	
P5	PL41A	6	LDQ38	T	PL51A	6	LDQ48	T	
GNDIO	GNDIO6	-			GNDIO6	-			
P7	PL41B	6	LDQ38	C	PL51B	6	LDQ48	C	
R1	PL42A	6	LLM0_GPLLT_IN_A**	T (LVDS)*	PL57A	6	LLM0_GPLLT_IN_A**/LDQS57****	T (LVDS)*	
GNDIO	GNDIO6	-			GNDIO6	-			
R2	PL42B	6	LLM0_GPLLC_IN_A**	C (LVDS)*	PL57B	6	LLM0_GPLLC_IN_A**/LDQ57	C (LVDS)*	
R3	PL43A	6	LLM0_GPLLT_FB_A	T	PL58A	6	LLM0_GPLLT_FB_A/LDQ57	T	
R4	PL43B	6	LLM0_GPLLC_FB_A	C	PL58B	6	LLM0_GPLLC_FB_A/LDQ57	C	
VCCIO	VCCIO6	6			VCCIO6	6			
R6	PL44A	6	LLM0_GDLT_IN_A**	T (LVDS)*	PL59A	6	LLM0_GDLT_IN_A**/LDQ57	T (LVDS)*	
R5	PL44B	6	LLM0_GDLLC_IN_A**	C (LVDS)*	PL59B	6	LLM0_GDLLC_IN_A**/LDQ57	C (LVDS)*	
T1	PL45A	6	LLM0_GDLT_FB_A	T	PL60A	6	LLM0_GDLT_FB_A/LDQ57	T	
T2	PL45B	6	LLM0_GDLLC_FB_A	C	PL60B	6	LLM0_GDLLC_FB_A/LDQ57	C	
GNDIO	GNDIO6	-			GNDIO6	-			
R7	LLM0_PLLCAP	6			LLM0_PLLCAP	6			
T6	PL47A	6	LDQ51	T (LVDS)*	PL62A	6	LDQ66	T (LVDS)*	
T7	PL47B	6	LDQ51	C (LVDS)*	PL62B	6	LDQ66	C (LVDS)*	
U1	PL48A	6	LDQ51	T	PL63A	6	LDQ66	T	
U2	PL48B	6	LDQ51	C	PL63B	6	LDQ66	C	
VCCIO	VCCIO6	6			VCCIO6	6			
T3	PL49A	6	LDQ51	T (LVDS)*	PL64A	6	LDQ66	T (LVDS)*	
U3	PL49B	6	LDQ51	C (LVDS)*	PL64B	6	LDQ66	C (LVDS)*	
U6	PL50A	6	LDQ51	T	NC	-			
U5	PL50B	6	LDQ51	C	PL65B	6	LDQ66	C	
GNDIO	GNDIO6	-			GNDIO6	-			

LFE2M50E/SE and LFE2M70E/SE Logic Signal Connections: 900 fpBGA (Cont.)

LFE2M50E/SE					LFE2M70E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential	
AA6	NC	-			PL79B	6	LDQ82	C	
AB4	NC	-			PL80A	6	LDQ82	T (LVDS)*	
-	-	-			VCCIO6	6			
AB5	NC	-			PL80B	6	LDQ82	C (LVDS)*	
AA8	NC	-			PL81A	6	LDQ82	T	
AA9	NC	-			PL81B	6	LDQ82	C	
AC1	PL62A	6	LLM0_GPLLT_IN_A**	T (LVDS)*	PL82A	6	LLM0_GPLLT_IN_A**/LDQS82	T (LVDS)*	
GNDIO	GNDIO6	-			GNDIO6	-			
AC2	PL62B	6	LLM0_GPLLC_IN_A**	C (LVDS)*	PL82B	6	LLM0_GPLLC_IN_A**/LDQ82	C (LVDS)*	
AC4	PL63A	6	LLM0_GPLLT_FB_A	T	PL83A	6	LLM0_GPLLT_FB_A/LDQ82	T	
AC3	PL63B	6	LLM0_GPLLC_FB_A	C	PL83B	6	LLM0_GPLLC_FB_A/LDQ82	C	
VCCIO	VCCIO6	6			VCCIO6	6			
AC7	PL64A	6	LLM0_GDLLT_IN_A**	T (LVDS)*	PL84A	6	LLM0_GDLLT_IN_A**/LDQ82	T (LVDS)*	
AC6	PL64B	6	LLM0_GDLLC_IN_A**	C (LVDS)*	PL84B	6	LLM0_GDLLC_IN_A**/LDQ82	C (LVDS)*	
AC5	PL65A	6	LLM0_GDLLT_FB_A	T	PL85A	6	LLM0_GDLLT_FB_A/LDQ82	T	
AD3	PL65B	6	LLM0_GDLLC_FB_A	C	PL85B	6	LLM0_GDLLC_FB_A/LDQ82	C	
GNDIO	GNDIO6	-			GNDIO6	-			
AB8	LLM0_PLLCAP	6			LLM0_PLLCAP	6			
AD2	PL67A	6	LDQ71	T (LVDS)*	PL87A	6		T	
AD1	PL67B	6	LDQ71	C (LVDS)*	PL87B	6		C	
AE2	TCK	-			TCK	-			
AE1	TDI	-			TDI	-			
AF2	TMS	-			TMS	-			
AF1	TDO	-			TDO	-			
AG1	VCCJ	-			VCCJ	-			
AH1	VCC	-			LLC_SQ_VCCR3	14			
AK2	PB11A	5	BDQ15	T	LLC_SQ_HDINP3	14		T	
AJ1	NC	-			LLC_SQ_VCCIB3	14			
AJ2	PB11B	5	BDQ15	C	LLC_SQ_HDINN3	14		C	
AH4	VCC	-			LLC_SQ_VCCTX3	14			
AK5	PB13A	5	BDQ15	T	LLC_SQ_HDOUTP3	14		T	
AK4	NC	-			LLC_SQ_VCCOB3	14			
AJ5	PB13B	5	BDQ15	C	LLC_SQ_HDOUTN3	14		C	
AH5	VCC	-			LLC_SQ_VCCTX2	14			
AJ6	PB14B	5	BDQ15	C	LLC_SQ_HDOUTN2	14		C	
AH6	NC	-			LLC_SQ_VCCOB2	14			
AK6	PB14A	5	BDQ15	T	LLC_SQ_HDOUTP2	14		T	
AH2	VCC	-			LLC_SQ_VCCR2	14			
AJ3	PB12B	5	BDQ15	C	LLC_SQ_HDINN2	14		C	
AH3	NC	-			LLC_SQ_VCCIB2	14			
AK3	PB12A	5	BDQ15	T	LLC_SQ_HDINP2	14		T	
AH7	VCC	-			LLC_SQ_VCCP	14			
AG7	PB15A	5	BDQS15	T	LLC_SQ_REFCLKP	14		T	
AF7	PB15B	5	BDQ15	C	LLC_SQ_REFCLKN	14		C	
AJ7	VCCAUX	-			LLC_SQ_VCCAUX33	14			
AK11	PB18A	5	BDQ15	T	LLC_SQ_HDINP1	14		T	
AH11	NC	-			LLC_SQ_VCCIB1	14			
AJ11	PB18B	5	BDQ15	C	LLC_SQ_HDINN1	14		C	

LFE2M100E/SE Logic Signal Connections: 900 fpBGA (Cont.)

LFE2M100E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential
M23	GND	-		
M8	GND	-		
N14	GND	-		
N15	GND	-		
N16	GND	-		
N17	GND	-		
N27	GND	-		
N4	GND	-		
P11	GND	-		
P13	GND	-		
P14	GND	-		
P15	GND	-		
P16	GND	-		
P17	GND	-		
P18	GND	-		
P20	GND	-		
R10	GND	-		
R11	GND	-		
R13	GND	-		
R14	GND	-		
R15	GND	-		
R16	GND	-		
R17	GND	-		
R18	GND	-		
R20	GND	-		
R21	GND	-		
R24	GND	-		
R7	GND	-		
T10	GND	-		
T11	GND	-		
T13	GND	-		
T14	GND	-		
T15	GND	-		
T16	GND	-		
T17	GND	-		
T18	GND	-		
T20	GND	-		
T21	GND	-		
T24	GND	-		
T7	GND	-		
U11	GND	-		
U13	GND	-		
U14	GND	-		