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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	11875
Number of Logic Elements/Cells	95000
Total RAM Bits	5435392
Number of I/O	416
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	900-BBGA
Supplier Device Package	900-FPBGA (31x31)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfe2m100e-5fn900i

Figure 2-1. Simplified Block Diagram, ECP2-6 Device (Top Level)

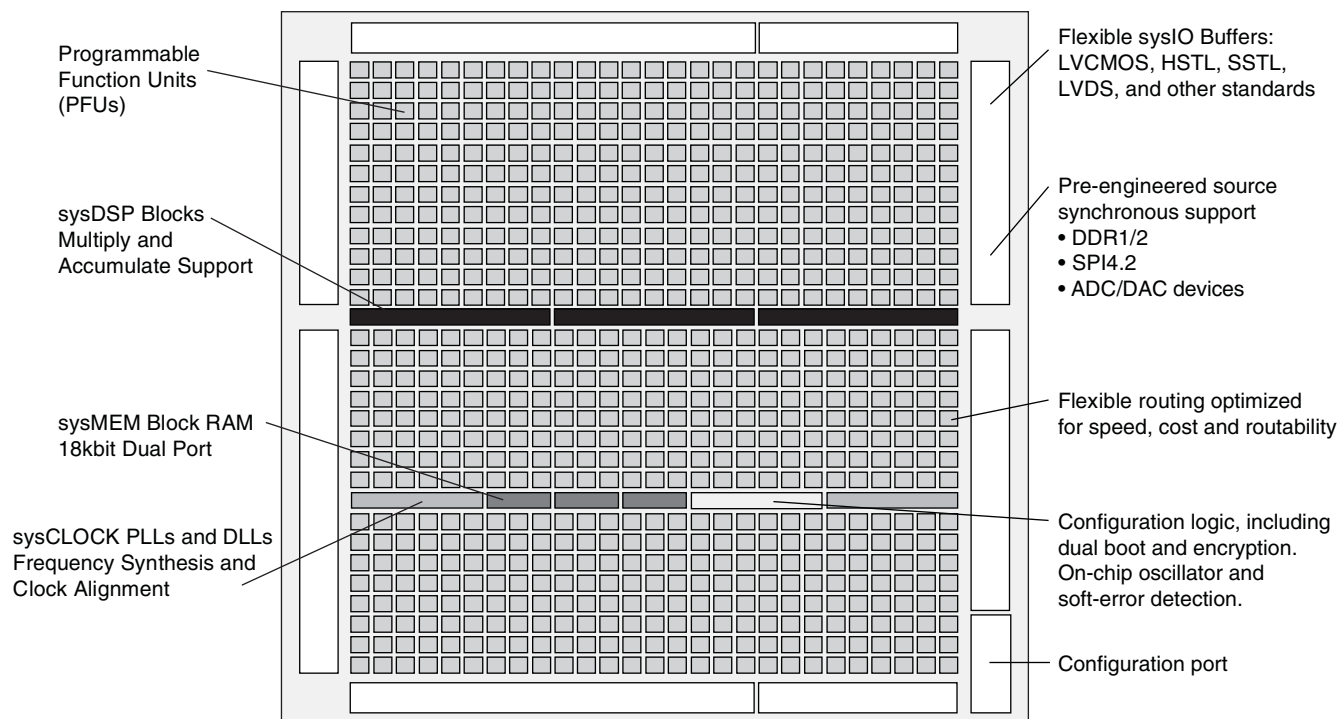
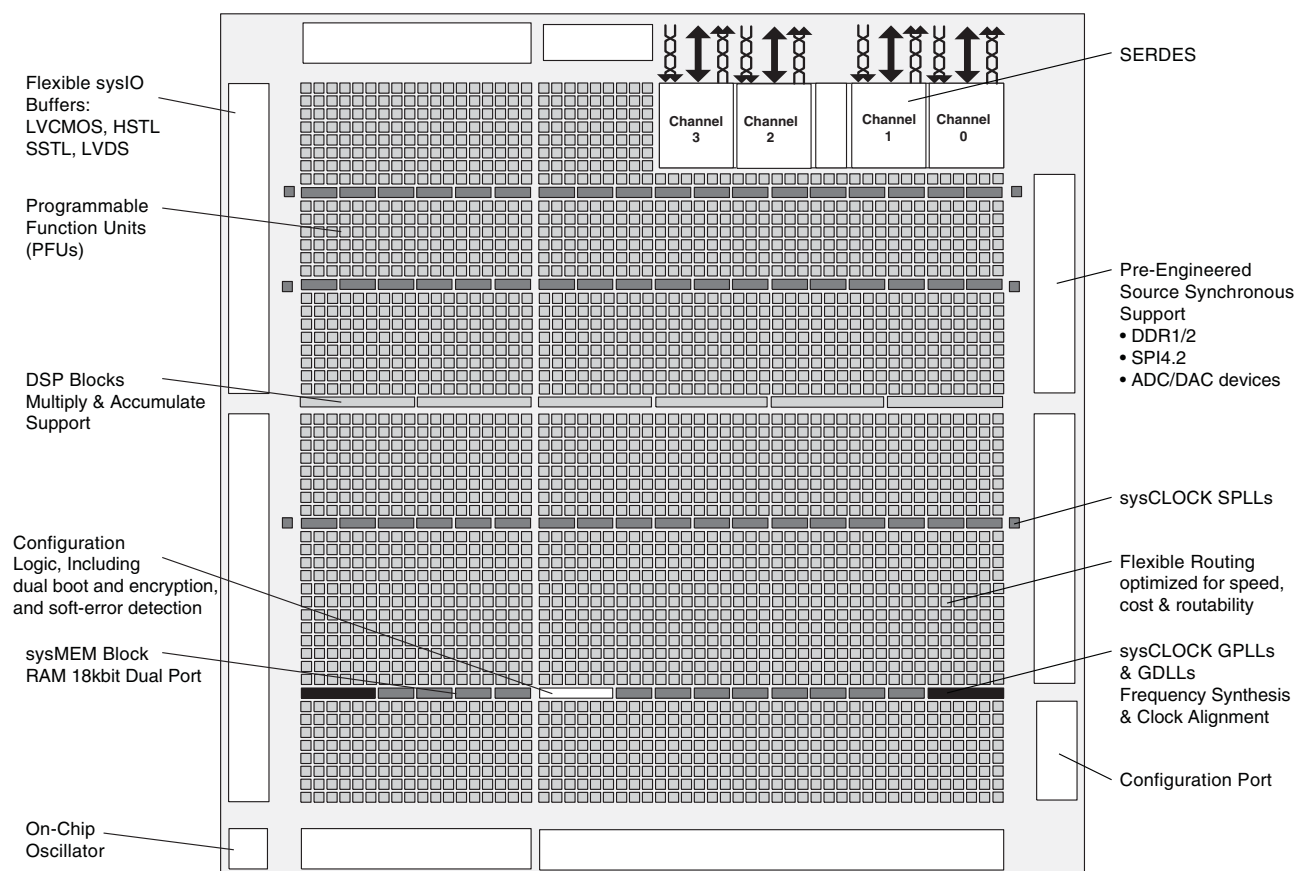


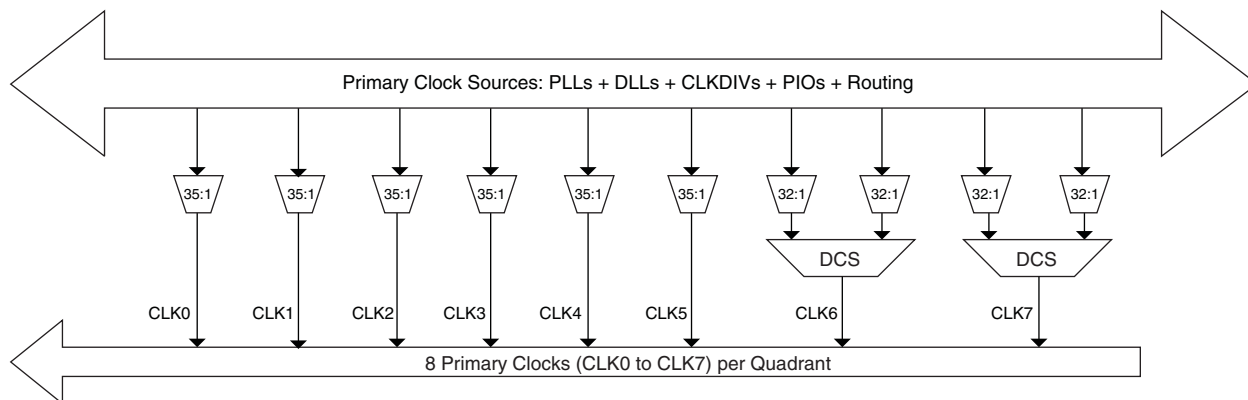
Figure 2-2. Simplified Block Diagram, ECP2M20 Device (Top Level)



Primary Clock Routing

The clock routing structure in LatticeECP2/M devices consists of a network of eight primary clock lines (CLK0 through CLK7) per quadrant. The primary clocks of each quadrant are generated from muxes located in the center of the device. All the clock sources are connected to these muxes. Figure 2-13 shows the clock routing for one quadrant. Each quadrant mux is identical. If desired, any clock can be routed globally

Figure 2-13. Per Quadrant Primary Clock Selection

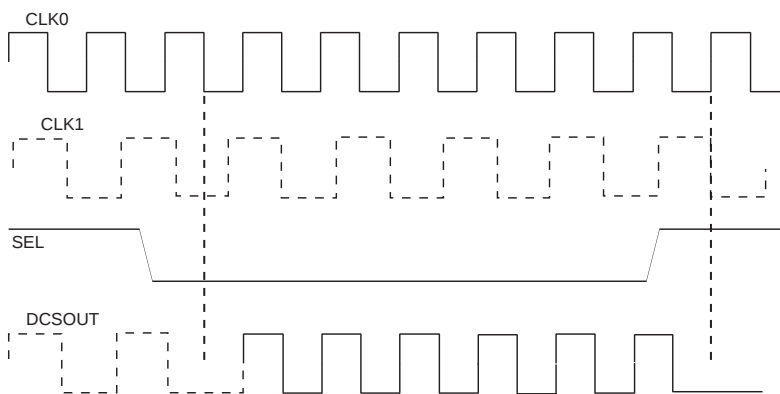


Dynamic Clock Select (DCS)

The DCS is a smart multiplexer function available in the primary clock routing. It switches between two independent input clock sources without any glitches or runt pulses. This is achieved regardless of when the select signal is toggled. There are two DCS blocks per quadrant; in total, there are eight DCS blocks per device. The inputs to the DCS block come from the center muxes. The output of the DCS is connected to primary clocks CLK6 and CLK7 (see Figure 2-13).

Figure 2-14 shows the timing waveforms of the default DCS operating mode. The DCS block can be programmed to other modes. For more information about the DCS, please see the list of additional technical documentation at the end of this data sheet.

Figure 2-14. DCS Waveforms



Secondary Clock/Control Routing

Secondary clocks in the LatticeECP2 devices are region-based resources. The benefit of region-based resources is the relatively low injection delay and skew within the region, as compared to primary clocks. EBR/DSP rows and a special vertical routing channel bound the secondary clock regions. This special vertical routing channel aligns with either the left edge of the center DSP block in the DSP row or the center of the DSP row. Figure 2-15 shows

If an EBR is pre-loaded during configuration, the GSR input must be disabled or the release of the GSR during device Wake Up must occur before the release of the device I/Os becomes active.

These instructions apply to all EBR RAM and ROM implementations.

Note that there are no reset restrictions if the EBR synchronous reset is used and the EBR GSR input is disabled.

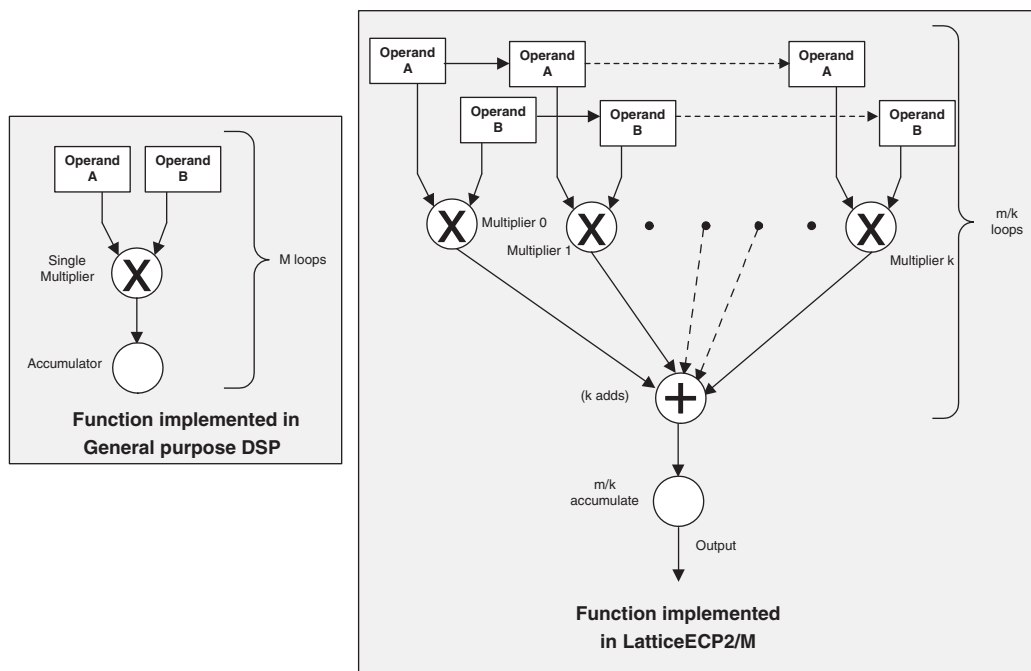
sysDSP™ Block

The LatticeECP2/M family provides a sysDSP block, making it ideally suited for low cost, high performance Digital Signal Processing (DSP) applications. Typical functions used in these applications are Finite Impulse Response (FIR) filters, Fast Fourier Transforms (FFT) functions, Correlators, Reed-Solomon/Turbo/Convolution encoders and decoders. These complex signal processing functions use similar building blocks such as multiply-adders and multiply-accumulators.

sysDSP Block Approach Compared to General DSP

Conventional general-purpose DSP chips typically contain one to four (Multiply and Accumulate) MAC units with fixed data-width multipliers; this leads to limited parallelism and limited throughput. Their throughput is increased by higher clock speeds. The LatticeECP2/M, on the other hand, has many DSP blocks that support different data-widths. This allows the designer to use highly parallel implementations of DSP functions. The designer can optimize the DSP performance vs. area by choosing an appropriate level of parallelism. Figure 2-22 compares the fully serial and the mixed parallel and serial implementations.

Figure 2-22. Comparison of General DSP and LatticeECP2/M Approaches



sysDSP Block Capabilities

The sysDSP block in the LatticeECP2/M family supports four functional elements in three 9, 18 and 36 data path widths. The user selects a function element for a DSP block and then selects the width and type (signed/unsigned) of its operands. The operands in the LatticeECP2/M family sysDSP Blocks can be either signed or unsigned but not mixed within a function element. Similarly, the operand widths cannot be mixed within a block. In the LatticeECP2/M family the DSP elements can be concatenated.

The resources in each sysDSP block can be configured to support the following elements:

Top Edge

The PICs on the top edge are different from PIOs on the left, right and bottom edges. PIOs on this edge do not have DDR registers or DQS signals.

The exact DQS pins are shown in a dual function in the Logic Signal Connections table in this data sheet. Additional detail is provided in the Signal Descriptions table. The DQS signal from the bus is used to strobe the DDR data from the memory into input register blocks. Interfaces on the left and right edges are designed for DDR memories that support 16 bits of data, whereas interfaces on the bottom are designed for memories that support 18 bits of data.

Figure 2-33. DQS Input Routing for the Left and Right Edges of the Device

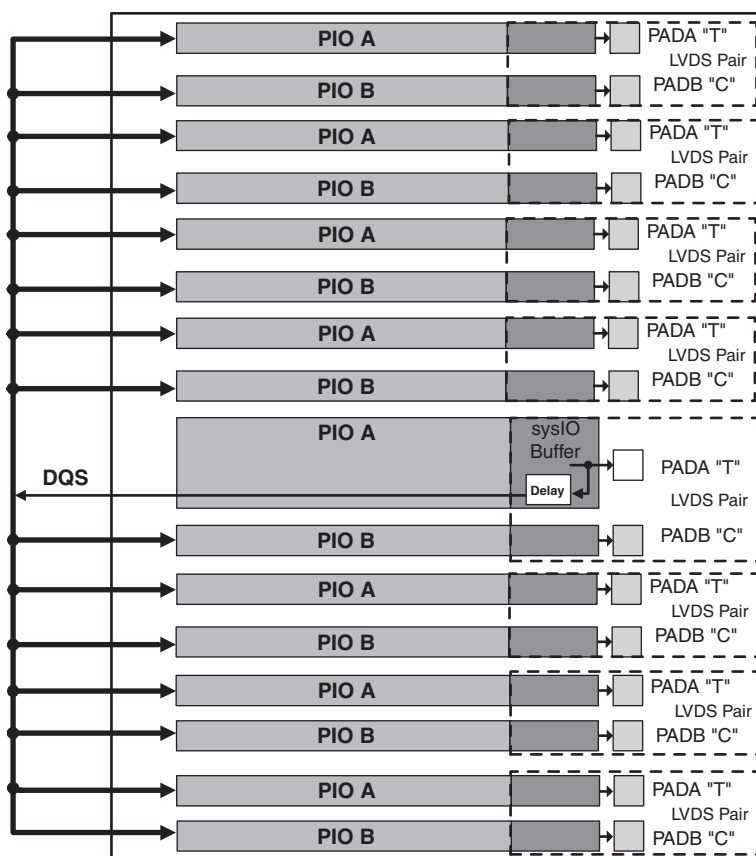
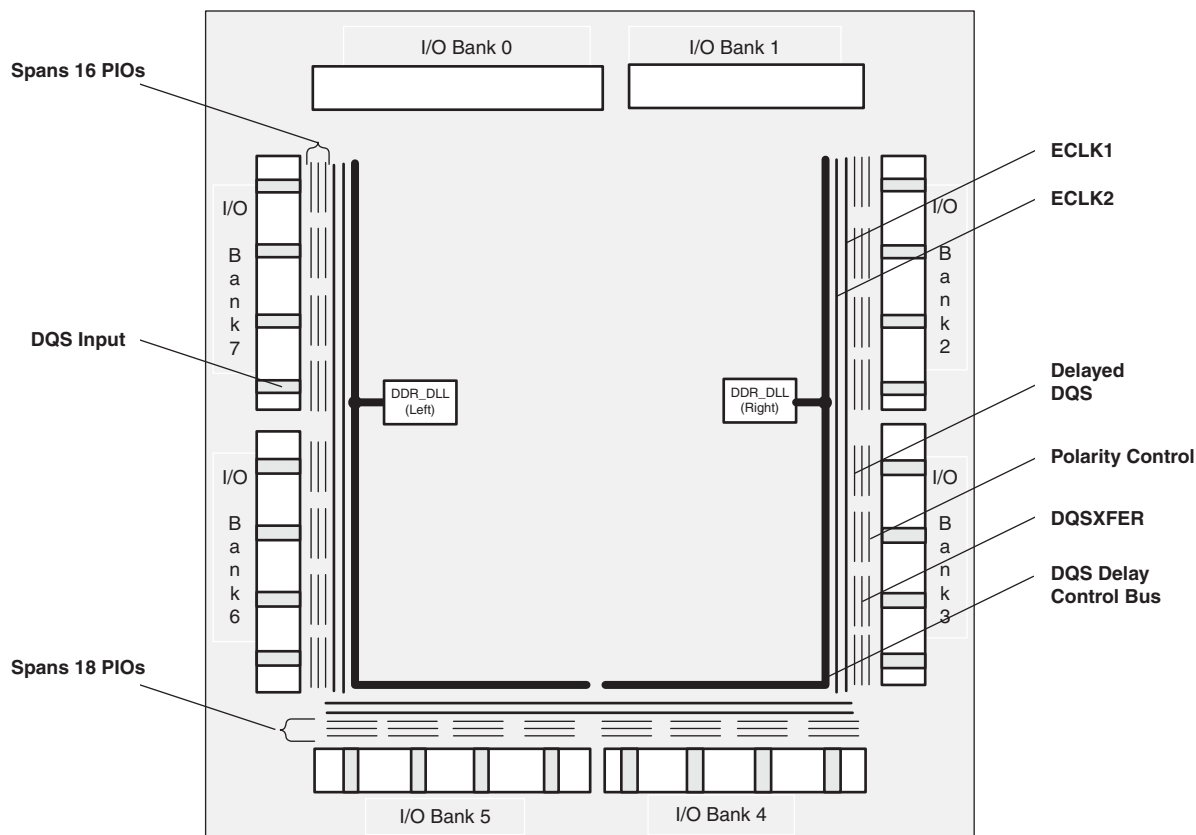


Figure 2-35. Edge Clock, DLL Calibration and DQS Local Bus Distribution



Note: Bank 8 is not shown.

Typical Building Block Function Performance¹

Pin-to-Pin Performance (LVCMOS25 12mA Drive)

Function	-7 Timing	Units
Basic Functions		
16-bit Decoder	3.8	ns
32-bit Decoder	4.5	ns
64-bit Decoder	5.0	ns
4:1 MUX	3.2	ns
8:1 MUX	3.4	ns
16:1 MUX	3.5	ns
32:1 MUX	4.0	ns

1. These timing numbers were generated using the ispLEVER 8.0 design tool. Exact performance may vary with device and tool version. The tool uses internal parameters that have been characterized but are not tested on every device.

Register-to-Register Performance

Function	-7 Timing	Units
Basic Functions		
16-bit Decoder	599	MHz
32-bit Decoder	542	MHz
64-bit Decoder	417	MHz
4:1 MUX	847	MHz
8:1 MUX	803	MHz
16:1 MUX	660	MHz
32:1 MUX	577	MHz
8-bit Adder	591	MHz
16-bit Adder	500	MHz
64-bit Adder	306	MHz
16-bit Counter	488	MHz
32-bit Counter	378	MHz
64-bit Counter	260	MHz
64-bit Accumulator	253	MHz
Embedded Memory Functions		
512x36 Single Port RAM, EBR Output Registers	370	MHz
1024x18 True-Dual Port RAM (Write Through or Normal, EBR Output Registers)	370	MHz
1024x18 True-Dual Port RAM (Write Through or Normal, PLC Output Registers)	280	MHz
Distributed Memory Functions		
16x4 Pseudo-Dual Port RAM (One PFU)	819	MHz
32x4 Pseudo-Dual Port RAM	521	MHz
64x8 Pseudo-Dual Port RAM	435	MHz
DSP Functions		
18x18 Multiplier (All Registers)	420	MHz
9x9 Multiplier (All Registers)	420	MHz

LatticeECP2/M External Switching Characteristics⁹ (Continued)

Over Recommended Operating Conditions

Parameter	Description	Device	-7		-6		-5		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
t _{DIBSPI}	Data Invalid Before Clock (Transmit)	ECP2-20	—	280	—	280	—	280	ps
		ECP2-35	—	280	—	280	—	280	ps
		ECP2-50	—	280	—	280	—	280	ps
		ECP2-70	—	280	—	280	—	280	ps
		ECP2M20	—	230	—	230	—	230	ps
		ECP2M35	—	230	—	230	—	230	ps
		ECP2M50	—	230	—	230	—	230	ps
		ECP2M70	—	230	—	230	—	230	ps
		ECP2M100	—	230	—	230	—	230	ps
XGMII I/O Pin Parameters (312 Mbps) ⁵									
t _{SUXGMII}	Data Setup Before Read Clock	ECP2/M	480	—	480	—	480	—	ps
t _{HXGMII}	Data Hold After Read Clock	ECP2/M	480	—	480	—	480	—	ps
t _{DVBCKXGMII}	Data Valid Before Clock	ECP2/M	960	—	960	—	960	—	ps
t _{DVACKXGMII}	Data Valid After Clock	ECP2/M	960	—	960	—	960	—	ps
Primary									
f _{MAX_PRI} ⁷	Frequency for Primary Clock Tree	ECP2/M	—	420	—	357	—	311	MHz
t _{W_PRI}	Clock Pulse Width for Primary Clock	ECP2/M	0.95	—	1.19	—	2.00	—	ns
t _{SKEW_PRI}	Primary Clock Skew Within a Bank	ECP2/M	—	300	—	360	—	420	ps
Edge Clock									
f _{MAX_EDGE} ⁷	Frequency for Edge Clock	ECP2/M	—	420	—	357	—	311	MHz
t _{W_EDGE}	Clock Pulse Width for Edge Clock	ECP2/M	0.95	—	1.19	—	2.00	—	ns
t _{SKEW_EDGE}	Edge Clock Skew Within an Edge of the Device	ECP2/M	—	300	—	360	—	420	ps

- General timing numbers based on LVCMOS 2.5, 12mA, 0pf load.
- DDR timing numbers based on SSTL25 for BGA packages only.
- DDR2 timing numbers based on SSTL18 for BGA packages only.
- SPI4.2 and SFI4 timing numbers based on LVDS25 for BGA packages only.
- XGMII timing numbers based on HSTL class I. A corresponding left/right dedicated clock buffer is used when using the SPI4.2 interface to the left or right edge of the device. For SPI4.2 mode, the software tool will help in selecting the appropriate clock buffer.
- IP will be used to support DDR and DDR2 memory data rates down to 95MHz. This approach uses a free-running clock and PFU register to sample the data instead of the hardwired DDR memory interface.
- Using the LVDS I/O standard.
- ECP2-6 and ECP2-12 do not support SPI4.2
- The AC numbers do not apply to PCLK6 and PCLK7.
- Applies to CLKOP only.
- Please refer to TN1159, [LatticeECP2/M Pin Assignment Recommendations](#) for best performance.

SERDES High-Speed Data Transmitter (LatticeECP2M Family Only)^{1, 2}

Table 3-7. Serial Output Timing and Levels

Symbol	Description	Frequency	Min.	Typ.	Max.	Units
V _{TX-DIFF-P-P-1}	Differential swing (1V setting) ^{1, 2}	0.25 to 3.125 Gbps	0.79	0.99	1.19	V, p-p
V _{TX-DIFF-P-P-1.25}	Differential swing (1.25V setting) ^{1, 2}	0.25 to 3.125 Gbps	1.00	1.25	1.50	V, p-p
V _{TX-DIFF-P-P-1.3}	Differential swing (1.3V setting) ^{1, 2}	0.25 to 3.125 Gbps	1.04	1.30	1.56	V, p-p
V _{TX-DIFF-P-P-1.35}	Differential swing (1.35V setting) ^{1, 2}	0.25 to 3.125 Gbps	1.08	1.35	1.62	V, p-p
V _{OCM}	Output common mode voltage	—	V _{CCOB} - 0.75	V _{CCOB} - 0.60	V _{CCOB} - 0.45	V
T _{TX-R}	Rise time (20% to 80%)	—	—	70	—	ps
T _{TX-F}	Fall time (80% to 20%)	—	—	70	—	ps
Z _{TX-OI-SE}	Output impedance 50/75/HiZ K Ohms (single-ended)	—	—	50/70 HiZ	—	Ohms
R _{TX-RL}	Return loss (with package)	—	—	9	—	dB

1. All measurements are with 50 ohm impedance.

2. See TN1124, [LatticeECP2M SERDES/PCS Usage Guide](#) for actual binary settings.

Table 3-8. Channel Output Jitter - x10 Mode

Description	Frequency	Min.	Typ.	Max.	Units
Deterministic	3.125 Gbps	—	0.08	0.12	UI, p-p
Random	3.125 Gbps	—	0.22	0.38	UI, p-p
Total	3.125 Gbps	—	0.33	0.43	UI, p-p
Deterministic	2.5 Gbps	—	0.08	0.17	UI, p-p
Random	2.5 Gbps	—	0.20	0.25	UI, p-p
Total	2.5 Gbps	—	0.25	0.35	UI, p-p
Deterministic	1.25 Gbps	—	0.03	0.10	UI, p-p
Random	1.25 Gbps	—	0.14	0.19	UI, p-p
Total	1.25 Gbps	—	0.17	0.24	UI, p-p
Deterministic	250 Mbps	—	0.04	0.17	UI, p-p
Random	250 Mbps	—	0.12	0.13	UI, p-p
Total	250 Mbps	—	0.15	0.29	UI, p-p

Note: Values are measured with PRBS 2⁷-1, all channels operating, FPGA Logic active, I/Os around SERDES pins quiet, reference clock at x10 mode.

LFE2-6E/SE and LFE2-12E/SE Logic Signal Connections: 256 fpBGA

LFE2-6E/SE					LFE2-12E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential	
C3	PL2A	7	VREF2_7	T (LVDS)*	PL2A	7	VREF2_7	T (LVDS)*	
C2	PL2B	7	VREF1_7	C (LVDS)*	PL2B	7	VREF1_7	C (LVDS)*	
VCCIO	VCCIO7	7			VCCIO7	7			
-	-	-			-	-			
D3	PL5A	7		T	PL5A	7		T	
D4	PL4A	7		T (LVDS)*	PL4A	7		T (LVDS)*	
D2	PL5B	7		C	PL5B	7		C	
GND	GNDIO7	-			GNDIO7	-			
E4	PL4B	7		C (LVDS)*	PL4B	7		C (LVDS)*	
B1	PL7A	7	LDQ10	T	PL7A	7	LDQ10	T	
C1	PL7B	7	LDQ10	C	PL7B	7	LDQ10	C	
F5	PL9A	7	LDQ10	T	PL9A	7	LDQ10	T	
VCCIO	VCCIO7	7			VCCIO7	7			
F4	PL8A	7	LDQ10	T (LVDS)*	PL8A	7	LDQ10	T (LVDS)*	
G6	PL9B	7	LDQ10	C	PL9B	7	LDQ10	C	
G4	PL8B	7	LDQ10	C (LVDS)*	PL8B	7	LDQ10	C (LVDS)*	
D1	PL10A	7	LDQS10	T (LVDS)*	PL10A	7	LDQS10	T (LVDS)*	
GND	GNDIO7	-			GNDIO7	-			
E1	PL10B	7	LDQ10	C (LVDS)*	PL10B	7	LDQ10	C (LVDS)*	
F3	PL11A	7	LDQ10	T	PL11A	7	LDQ10	T	
G3	PL11B	7	LDQ10	C	PL11B	7	LDQ10	C	
VCCIO	VCCIO7	7			VCCIO7	7			
F2	PL12A	7	LDQ10	T (LVDS)*	PL12A	7	LDQ10	T (LVDS)*	
F1	PL12B	7	LDQ10	C (LVDS)*	PL12B	7	LDQ10	C (LVDS)*	
GND	GNDIO7	-			GNDIO7	-			
G2	PL13A	7	PCLKT7_0/LDQ10	T	PL13A	7	PCLKT7_0/LDQ10	T	
G1	PL13B	7	PCLKC7_0/LDQ10	C	PL13B	7	PCLKC7_0/LDQ10	C	
H6	PL15A	6	PCLKT6_0	T (LVDS)*	PL15A	6	PCLKT6_0	T (LVDS)*	
VCCIO	VCCIO6	6			VCCIO6	6			
H5	PL15B	6	PCLKC6_0	C (LVDS)*	PL15B	6	PCLKC6_0	C (LVDS)*	
H4	PL16A	6	VREF2_6	T	PL16A	6	VREF2_6	T	
GND	GNDIO6	-			GNDIO6	-			
H3	PL16B	6	VREF1_6	C	PL16B	6	VREF1_6	C	
H2	PL17A	6	LLM0_GDLLT_IN_A**	T (LVDS)*	PL17A	6	LLM0_GDLLT_IN_A**	T (LVDS)*	
H1	PL17B	6	LLM0_GDLLC_IN_A**	C (LVDS)*	PL17B	6	LLM0_GDLLC_IN_A**	C (LVDS)*	
G10	VCC	-			VCC	-			
J4	PL18A	6	LLM0_GDLLT_FB_A	T	PL18A	6	LLM0_GDLLT_FB_A	T	
J5	PL18B	6	LLM0_GDLLC_FB_A	C	PL18B	6	LLM0_GDLLC_FB_A	C	
J6	LLM0_PLLCAP	6			LLM0_PLLCAP	6			
K4	PL20A	6	LLM0_GPLLT_IN_A**	T (LVDS)*	PL20A	6	LLM0_GPLLT_IN_A**	T (LVDS)*	
GND	GNDIO6	-			GNDIO6	-			
J1	PL21A	6	LLM0_GPLLT_FB_A	T	PL21A	6	LLM0_GPLLT_FB_A	T	
K3	PL20B	6	LLM0_GPLLC_IN_A**	C (LVDS)*	PL20B	6	LLM0_GPLLC_IN_A**	C (LVDS)*	
VCCIO	VCCIO6	6			VCCIO6	6			
J2	PL21B	6	LLM0_GPLLC_FB_A	C	PL21B	6	LLM0_GPLLC_FB_A	C	

LFE2-35E/SE and LFE2-50E/SE Logic Signal Connections: 484 fpBGA

LFE2-35E/SE					LFE2-50E/SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
E4	PL2A	7	VREF2_7/LDQ6	T (LVDS)*	PL2A	7	VREF2_7	T (LVDS)*
E5	PL2B	7	VREF1_7/LDQ6	C (LVDS)*	PL2B	7	VREF1_7	C (LVDS)*
VCCIO	VCCIO7	-			GNDIO7	-		
GNDIO	GNDIO7	-			VCCIO	7		
E3	PL10A	7	LDQ14	T (LVDS)*	PL12A	7	LDQ16	T (LVDS)*
F3	PL10B	7	LDQ14	C (LVDS)*	PL12B	7	LDQ16	C (LVDS)*
F4	PL11A	7	LDQ14	T	PL13A	7	LDQ16	T
F5	PL11B	7	LDQ14	C	PL13B	7	LDQ16	C
E2	PL12A	7	LDQ14	T (LVDS)*	PL14A	7	LDQ16	T (LVDS)*
VCCIO	VCCIO7	7			VCCIO	7		
E1	PL12B	7	LDQ14	C (LVDS)*	PL14B	7	LDQ16	C (LVDS)*
G6	PL13A	7	LDQ14	T	PL15A	7	LDQ16	T
G7	PL13B	7	LDQ14	C	PL15B	7	LDQ16	C
H4	PL14A	7	LDQS14	T (LVDS)*	PL16A	7	LDQS16	T (LVDS)*
GNDIO	GNDIO7	-			GNDIO7	-		
H5	PL14B	7	LDQ14	C (LVDS)*	PL16B	7	LDQ16	C (LVDS)*
F1	PL15A	7	LDQ14	T	PL17A	7	LDQ16	T
F2	PL15B	7	LDQ14	C	PL17B	7	LDQ16	C
VCCIO	VCCIO7	7			VCCIO	7		
G3	PL16A	7	LDQ14	T (LVDS)*	PL18A	7	LDQ16	T (LVDS)*
G4	PL16B	7	LDQ14	C (LVDS)*	PL18B	7	LDQ16	C (LVDS)*
G1	PL17A	7	LDQ14	T	PL19A	7	LDQ16	T
G2	PL17B	7	LDQ14	C	PL19B	7	LDQ16	C
GNDIO	GNDIO7	-			GNDIO7	-		
-	-	-			VCCIO	7		
H6	NC	-			PL25A	7	LUM0_SPLLT_IN_A/LDQ24	T
-	-	-			VCCIO	7		
J6	NC	-			PL25B	7	LUM0_SPLLC_IN_A/LDQ24	C
H3	NC	-			PL26A	7	LUM0_SPLLT_FB_A/LDQ24	T
H2	NC	-			PL26B	7	LUM0_SPLLC_FB_A/LDQ24	C
-	-	-			GNDIO7	-		
-	-	-			VCCIO	7		
H1	PL18A	7	LDQ22		PL37A	7	LDQ41	
J4	PL19A	7	LDQ22	T	PL38A	7	LDQ41	T
J5	PL19B	7	LDQ22	C	PL38B	7	LDQ41	C
VCCIO	VCCIO7	7			VCCIO	7		
J2	PL20A	7	LDQ22	T (LVDS)*	PL39A	7	LDQ41	T (LVDS)*
J1	PL20B	7	LDQ22	C (LVDS)*	PL39B	7	LDQ41	C (LVDS)*
L6	PL21A	7	LDQ22	T	PL40A	7	LDQ41	T
L5	PL21B	7	LDQ22	C	PL40B	7	LDQ41	C
GNDIO	GNDIO7	-			GNDIO7	-		
K3	PL22A	7	LDQS22	T (LVDS)*	PL41A	7	LDQS41	T (LVDS)*
K4	PL22B	7	LDQ22	C (LVDS)*	PL41B	7	LDQ41	C (LVDS)*
K2	PL23A	7	LDQ22	T	PL42A	7	LDQ41	T
VCCIO	VCCIO7	7			VCCIO	7		

LFE2-35E/SE and LFE2-50E/SE Logic Signal Connections: 484 fpBGA (Cont.)

LFE2-35E/SE					LFE2-50E/SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
J22	PR29B	3	RDQ31	C (LVDS)*	PR48B	3	RDQ50	C (LVDS)*
H22	PR29A	3	RDQ31	T (LVDS)*	PR48A	3	RDQ50	T (LVDS)*
VCCIO	VCCIO3	3			VCCIO	3		
M20	PR28B	3	VREF2_3/RDQ31	C	PR47B	3	VREF2_3/RDQ50	C
L21	PR28A	3	VREF1_3/RDQ31	T	PR47A	3	VREF1_3/RDQ50	T
K21	PR27B	3	PCLKC3_0/RDQ31	C (LVDS)*	PR46B	3	PCLKC3_0/RDQ50	C (LVDS)*
J21	PR27A	3	PCLKT3_0/RDQ31	T (LVDS)*	PR46A	3	PCLKT3_0/RDQ50	T (LVDS)*
M18	PR25B	2	PCLKC2_0/RDQ22	C	PR44B	2	PCLKC2_0/RDQ41	C
L17	PR25A	2	PCLKT2_0/RDQ22	T	PR44A	2	PCLKT2_0/RDQ41	T
GNDIO	GNDIO2	-			GNDIO2	-		
L19	PR24B	2	RDQ22	C (LVDS)*	PR43B	2	RDQ41	C (LVDS)*
L20	PR24A	2	RDQ22	T (LVDS)*	PR43A	2	RDQ41	T (LVDS)*
L18	PR23B	2	RDQ22	C	PR42B	2	RDQ41	C
K17	PR23A	2	RDQ22	T	PR42A	2	RDQ41	T
VCCIO	VCCIO2	2			VCCIO	2		
K18	PR22B	2	RDQ22	C (LVDS)*	PR41B	2	RDQ41	C (LVDS)*
K19	PR22A	2	RDQS22	T (LVDS)*	PR41A	2	RDQS41	T (LVDS)*
G22	PR21B	2	RDQ22	C	PR40B	2	RDQ41	C
GNDIO	GNDIO2	-			GNDIO2	-		
F22	PR21A	2	RDQ22	T	PR40A	2	RDQ41	T
J17	PR20B	2	RDQ22	C (LVDS)*	PR39B	2	RDQ41	C (LVDS)*
J18	PR20A	2	RDQ22	T (LVDS)*	PR39A	2	RDQ41	T (LVDS)*
K20	PR19B	2	RDQ22	C	PR38B	2	RDQ41	C
VCCIO	VCCIO2	2			VCCIO	2		
J19	PR19A	2	RDQ22	T	PR38A	2	RDQ41	T
H21	PR18B	2	RDQ22	C (LVDS)*	PR37B	2	RDQ41	C (LVDS)*
G21	PR18A	2	RDQ22	T (LVDS)*	PR37A	2	RDQ41	T (LVDS)*
-	-	-			GNDIO2	-		
-	-	-			VCCIO	2		
H17	NC	-			PR26B	2	RUM0_SPLLC_FB_A/RDQ24	C
H16	NC	-			PR26A	2	RUM0_SPLLT_FB_A/RDQ24	T
H20	NC	-			PR25B	2	RUM0_SPLLC_IN_A/RDQ24	C
H18	NC	-			PR25A	2	RUM0_SPLLT_IN_A/RDQ24	T
-	-	-			GNDIO2	-		
-	-	-			VCCIO	2		
F21	PR17B	2	RDQ14	C	PR19B	2	RDQ16	C
GNDIO	GNDIO2	-			GNDIO2	-		
E22	PR17A	2	RDQ14	T	PR19A	2	RDQ16	T
D22	PR16B	2	RDQ14	C (LVDS)*	PR18B	2	RDQ16	C (LVDS)*
E21	PR16A	2	RDQ14	T (LVDS)*	PR18A	2	RDQ16	T (LVDS)*
G20	PR15B	2	RDQ14	C	PR17B	2	RDQ16	C
VCCIO	VCCIO2	2			VCCIO	2		
F20	PR15A	2	RDQ14	T	PR17A	2	RDQ16	T
H19	PR14B	2	RDQ14	C (LVDS)*	PR16B	2	RDQ16	C (LVDS)*
G19	PR14A	2	RDQS14	T (LVDS)*	PR16A	2	RDQS16	T (LVDS)*
GNDIO	GNDIO2	-			GNDIO2	-		

LFE2M-20E/SE and LFE2M-35E/SE Logic Signal Connections: 256 fpBGA (Cont.)

LFE2M20E/SE					LFE2M35E/SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
N11	CCLK	8			CCLK	8		
M11	INITN	8			INITN	8		
N13	DONE	8			DONE	8		
GNDIO	GNDIO8	-			GNDIO8	-		
M12	PR53B	8	WRITEN	C	PR68B	8	WRITEN	C
M13	PR53A	8	CS1N	T	PR68A	8	CS1N	T
N14	PR52B	8	CSN	C	PR67B	8	CSN	C
N15	PR52A	8	D0/SPIFASTN	T	PR67A	8	D0/SPIFASTN	T
VCCIO	VCCIO8	8			VCCIO8	8		
N16	PR51B	8	D1	C	PR66B	8	D1	C
M16	PR51A	8	D2	T	PR66A	8	D2	T
L12	PR50B	8	D3	C	PR65B	8	D3	C
GNDIO	GNDIO8	-			GNDIO8	-		
L13	PR50A	8	D4	T	PR65A	8	D4	T
L16	PR49B	8	D5	C	PR64B	8	D5	C
K16	PR49A	8	D6	T	PR64A	8	D6	T
L14	PR48B	8	D7/SPID0***	C	PR63B	8	D7/SPID0***	C
VCCIO	VCCIO8	8			VCCIO8	8		
L15	PR48A	8	DI/CSSPI0N	T	PR63A	8	DI/CSSPI0N	T
K13	PR47B	8	DOUT/CSON/CSSPI1N	C	PR62B	8	DOUT/CSON/CSSPI1N	C
K14	PR47A	8	BUSY/SISPI	T	PR62A	8	BUSY/SISPI	T
K11	RLM0_PLLCAP	3			RLM0_PLLCAP	3		
K15	PR45B	3	RLM0_GDLLC_FB_A	C	PR60B	3	RLM0_GDLLC_FB_A/RDQ57	C
GNDIO	GNDIO3	-			GNDIO3	-		
J16	PR45A	3	RLM0_GDLLT_FB_A	T	PR60A	3	RLM0_GDLLT_FB_A/RDQ57	T
H16	PR44B	3	RLM0_GDLLC_IN_A	C (LVDS)*	PR59B	3	RLM0_GDLLC_IN_A**/RDQ57	C (LVDS)*
J15	PR44A	3	RLM0_GDLLT_IN_A	T (LVDS)*	PR59A	3	RLM0_GDLLT_IN_A**/RDQ57	T (LVDS)*
J14	PR43B	3	RLM0_GPLLC_IN_A	C	PR58B	3	RLM0_GPLLC_IN_A**/RDQ57	C
VCCIO	VCCIO3	3			VCCIO3	3		
J13	PR43A	3	RLM0_GPLLT_IN_A	T	PR58A	3	RLM0_GPLLT_IN_A**/RDQ57	T
H13	PR42B	3	RLM0_GPLLC_FB_A	C (LVDS)*	PR57B	3	RLM0_GPLLC_FB_A/RDQ57	C (LVDS)*
H12	PR42A	3	RLM0_GPLLT_FB_A	T (LVDS)*	PR57A	3	RLM0_GPLLT_FB_A/RDQS57***	T (LVDS)*
GNDIO	GNDIO3	-			GNDIO3	-		
VCCIO	VCCIO3	3			VCCIO3	3		
G16	PR32B	3	RLM1_SPLLC_FB_A	C	PR42B	3	RLM2_SPLLC_FB_A	C
VCCIO	VCCIO3	3			VCCIO3	3		
H15	PR32A	3	RLM1_SPLLT_FB_A	T	PR42A	3	RLM2_SPLLT_FB_A	T
E16	PR31B	3	RLM1_SPLLC_IN_A	C (LVDS)*	PR41B	3	RLM2_SPLLC_IN_A	C (LVDS)*
F15	PR31A	3	RLM1_SPLLT_IN_A	T (LVDS)*	PR41A	3	RLM2_SPLLT_IN_A	T (LVDS)*
GNDIO	GNDIO3	-			GNDIO3	-		
VCCIO	VCCIO3	3			VCCIO3	3		
F16	PR28B	3	VREF2_3	C	PR38B	3	VREF2_3	C
G15	PR28A	3	VREF1_3	T	PR38A	3	VREF1_3	T
J11	PR27B	3	PCLKC3_0	C (LVDS)*	PR37B	3	PCLKC3_0	C (LVDS)*
J12	PR27A	3	PCLKT3_0	T (LVDS)*	PR37A	3	PCLKT3_0	T (LVDS)*
G14	PR25B	2	PCLKC2_0/RDQ22	C	PR35B	2	PCLKC2_0/RDQ32	C
G13	PR25A	2	PCLKT2_0/RDQ22	T	PR35A	2	PCLKT2_0/RDQ32	T
GNDIO	GNDIO2	-			GNDIO2	-		

LFE2M-20E/SE and LFE2M-35E/SE Logic Signal Connections: 256 fpBGA (Cont.)

LFE2M20E/SE					LFE2M35E/SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
A3	GND	-			GND	-		
A9	GND	-			GND	-		
B12	GND	-			GND	-		
B6	GND	-			GND	-		
E15	GND	-			GND	-		
E2	GND	-			GND	-		
H14	GND	-			GND	-		
H8	GND	-			GND	-		
H9	GND	-			GND	-		
J3	GND	-			GND	-		
J8	GND	-			GND	-		
J9	GND	-			GND	-		
M15	GND	-			GND	-		
M2	GND	-			GND	-		
P9	GND	-			GND	-		
R12	GND	-			GND	-		
R5	GND	-			GND	-		
T1	GND	-			GND	-		
T16	GND	-			GND	-		
D10	NC	-			NC	-		
D11	NC	-			NC	-		
D12	NC	-			NC	-		
D13	NC	-			NC	-		
D14	NC	-			NC	-		
D4	NC	-			NC	-		
D5	NC	-			NC	-		
D6	NC	-			NC	-		
D7	NC	-			NC	-		
E11	NC	-			NC	-		
E6	NC	-			NC	-		
E8	NC	-			NC	-		
E9	NC	-			NC	-		
F10	NC	-			NC	-		
F7	NC	-			NC	-		
F8	NC	-			NC	-		
F9	NC	-			NC	-		

* Supports true LVDS. Other differential signals must be emulated with external resistors.

** These dedicated input pins can be used for GPLLs or GDLLs within the respective quadrant.

***Due to packaging bond out option, this DQS does not have all the necessary DQ pins bonded out for a full 8-bit data width.

Note: VCCIO and GND pads are used to determine the average DC current drawn by I/Os between GND/VCCIO connections, or between the last GND/VCCIO in an I/O bank and the end of an I/O bank. The substrate pads listed in the Pin Table do not necessarily have a one to one connection with a package ball or pin.

LFE2M20E/SE and LFE2M35E/SE Logic Signal Connections: 484 fpBGA (Cont.)

LFE2M20E/SE					LFE2M35E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential	
AB6	PB17A	5	PCLKT5_0/BDQ15	T	PB35A	5	PCLKT5_0/BDQ33	T	
AB7	PB17B	5	PCLKC5_0/BDQ15	C	PB35B	5	PCLKC5_0/BDQ33	C	
VCCIO	VCCIO5	5			VCCIO5	5			
GNDIO	GNDIO5	-			GNDIO5	-			
AA8	PB22A	4	PCLKT4_0/BDQ24	T	PB40A	4	PCLKT4_0/BDQ42	T	
VCCIO	VCCIO4	4			VCCIO4	4			
AB8	PB22B	4	PCLKC4_0/BDQ24	C	PB40B	4	PCLKC4_0/BDQ42	C	
AA9	PB23A	4	VREF2_4/BDQ24	T	PB41A	4	VREF2_4/BDQ42	T	
Y9	PB23B	4	VREF1_4/BDQ24	C	PB41B	4	VREF1_4/BDQ42	C	
AB9	PB24A	4	BDQS24****	T	PB42A	4	BDQS42****	T	
GNDIO	GNDIO4	-			GNDIO4	-			
AB10	PB24B	4	BDQ24	C	PB42B	4	BDQ42	C	
AA10	PB25A	4	BDQ24	T	PB43A	4	BDQ42	T	
Y11	PB25B	4	BDQ24	C	PB43B	4	BDQ42	C	
VCCIO	VCCIO4	4			VCCIO4	4			
GNDIO	GNDIO4	-			GNDIO4	-			
V10	PB29A	4	BDQ33	T	PB47A	4	BDQ51	T	
U11	PB29B	4	BDQ33	C	PB47B	4	BDQ51	C	
V11	PB30A	4	BDQ33	T	PB48A	4	BDQ51	T	
W11	PB30B	4	BDQ33	C	PB48B	4	BDQ51	C	
AA11	PB31A	4	BDQ33	T	PB49A	4	BDQ51	T	
AB11	PB31B	4	BDQ33	C	PB49B	4	BDQ51	C	
VCCIO	VCCIO4	4			VCCIO4	4			
T11	PB32A	4	BDQ33	T	PB50A	4	BDQ51	T	
U12	PB32B	4	BDQ33	C	PB50B	4	BDQ51	C	
GNDIO	GNDIO4	-			GNDIO4	-			
AA12	PB33A	4	BDQS33	T	PB51A	4	BDQS51	T	
Y12	PB33B	4	BDQ33	C	PB51B	4	BDQ51	C	
V12	PB34A	4	BDQ33	T	PB52A	4	BDQ51	T	
W12	PB34B	4	BDQ33	C	PB52B	4	BDQ51	C	
AB12	PB35A	4	BDQ33	T	PB53A	4	BDQ51	T	
AA13	PB35B	4	BDQ33	C	PB53B	4	BDQ51	C	
VCCIO	VCCIO4	4			VCCIO4	4			
T12	PB36A	4	BDQ33	T	PB54A	4	BDQ51	T	
U13	PB36B	4	BDQ33	C	PB54B	4	BDQ51	C	
V13	PB37A	4	BDQ33	T	PB55A	4	BDQ51	T	
T13	PB37B	4	BDQ33	C	PB55B	4	BDQ51	C	
GNDIO	GNDIO4	-			GNDIO4	-			
AB13	PB38A	4	BDQ42	T	PB56A	4	BDQ60	T	
AB14	PB38B	4	BDQ42	C	PB56B	4	BDQ60	C	
U14	PB39A	4	BDQ42	T	PB57A	4	BDQ60	T	
T14	PB39B	4	BDQ42	C	PB57B	4	BDQ60	C	
AA14	PB40A	4	BDQ42	T	PB58A	4	BDQ60	T	
VCCIO	VCCIO4	4			VCCIO4	4			
Y14	PB40B	4	BDQ42	C	PB58B	4	BDQ60	C	
W14	PB41A	4	BDQ42	T	PB59A	4	BDQ60	T	
V14	PB41B	4	BDQ42	C	PB59B	4	BDQ60	C	
AB15	PB42A	4	BDQS42	T	PB60A	4	BDQS60	T	

LFE2M20E/SE and LFE2M35E/SE Logic Signal Connections: 484 fpBGA (Cont.)

LFE2M20E/SE					LFE2M35E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential	
L18	PR31A	3	RLM1_SPLLT_IN_A	T (LVDS)*	PR41A	3	RLM2_SPLLT_IN_A	T (LVDS)*	
GNDIO	GNDIO3	-			GNDIO3	-			
L20	PR30B	3		C	PR40B	3		C	
L19	PR30A	3		T	PR40A	3		T	
K16	PR29B	3		C (LVDS)*	PR39B	3		C (LVDS)*	
K17	PR29A	3		T (LVDS)*	PR39A	3		T (LVDS)*	
VCCIO	VCCIO3	3			VCCIO3	3			
J16	PR28B	3	VREF2_3	C	PR38B	3	VREF2_3	C	
K18	PR28A	3	VREF1_3	T	PR38A	3	VREF1_3	T	
J22	PR27B	3	PCLKC3_0	C (LVDS)*	PR37B	3	PCLKC3_0	C (LVDS)*	
J21	PR27A	3	PCLKT3_0	T (LVDS)*	PR37A	3	PCLKT3_0	T (LVDS)*	
H22	PR25B	2	PCLKC2_0/RDQ22	C	PR35B	2	PCLKC2_0/RDQ32	C	
H21	PR25A	2	PCLKT2_0/RDQ22	T	PR35A	2	PCLKT2_0/RDQ32	T	
GNDIO	GNDIO2	-			GNDIO2	-			
J17	PR24B	2	RDQ22	C (LVDS)*	PR34B	2	RDQ32	C (LVDS)*	
J18	PR24A	2	RDQ22	T (LVDS)*	PR34A	2	RDQ32	T (LVDS)*	
J20	PR23B	2	RDQ22	C	PR33B	2	RDQ32	C	
J19	PR23A	2	RDQ22	T	PR33A	2	RDQ32	T	
VCCIO	VCCIO2	2			VCCIO2	2			
H16	PR22B	2	RDQ22	C (LVDS)*	PR32B	2	RDQ32	C (LVDS)*	
H17	PR22A	2	RDQS22	T (LVDS)*	PR32A	2	RDQS32	T (LVDS)*	
G22	PR21B	2	RDQ22	C	PR31B	2	RDQ32	C	
GNDIO	GNDIO2	-			GNDIO2	-			
G21	PR21A	2	RDQ22	T	PR31A	2	RDQ32	T	
H20	PR20B	2	RDQ22	C (LVDS)*	PR30B	2	RDQ32	C (LVDS)*	
H19	PR20A	2	RDQ22	T (LVDS)*	PR30A	2	RDQ32	T (LVDS)*	
G16	PR19B	2	RUM1_SPLLC_FB_A/RDQ22	C	PR29B	2	RUM1_SPLLC_FB_A/RDQ32	C	
VCCIO	VCCIO2	2			VCCIO2	2			
H18	PR19A	2	RUM1_SPLLT_FB_A/RDQ22	T	PR29A	2	RUM1_SPLLT_FB_A/RDQ32	T	
F22	PR18B	2	RUM1_SPLLC_IN_A/RDQ22	C (LVDS)*	PR28B	2	RUM1_SPLLC_IN_A/RDQ32	C (LVDS)*	
F21	PR18A	2	RUM1_SPLLT_IN_A/RDQ22	T (LVDS)*	PR28A	2	RUM1_SPLLT_IN_A/RDQ32	T (LVDS)*	
GNDIO	GNDIO2	-			-	-			
G20	PR16B	2		C	PR26B	2	RDQ23	C	
VCCIO	VCCIO2	2			-	-			
F20	PR16A	2		T	PR26A	2	RDQ23	T	
-	-	-			GNDIO2	-			
G17	PR15B	2		C (LVDS)*	PR25B	2	RDQ23	C (LVDS)*	
F17	PR15A	2		T (LVDS)*	PR25A	2	RDQ23	T (LVDS)*	
-	-	-			VCCIO2	2			
GNDIO	GNDIO2	-			GNDIO2	-			
E22	PR14B	2		C	PR14B	2	RDQ15	C	
D22	PR14A	2		T	PR14A	2	RDQ15	T	
E20	PR13B	2		C (LVDS)*	PR13B	2	RDQ15	C (LVDS)*	
D20	PR13A	2		T (LVDS)*	PR13A	2	RDQ15	T (LVDS)*	
VCCIO	VCCIO2	2			VCCIO2	2			
D19	PR12B	2	RUM0_SPLLC_FB_A	C	PR12B	2	RUM0_SPLLC_FB_A/RDQ15	C	
E19	PR12A	2	RUM0_SPLLT_FB_A	T	PR12A	2	RUM0_SPLLT_FB_A/RDQ15	T	
F18	PR11B	2	RUM0_SPLLC_IN_A	C (LVDS)*	PR11B	2	RUM0_SPLLC_IN_A/RDQ15	C (LVDS)*	

LFE2M50E/SE and LFE2M70E/SE Logic Signal Connections: 900 fpBGA (Cont.)

LFE2M50E/SE					LFE2M70E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential	
AJ17	PB62B	4	BDQ60	C	PB71B	4	BDQ69	C	
VCCIO	VCCIO4	4			VCCIO4	4			
AF26	PB64A	4	BDQ60	T	PB73A	4	BDQ69	T	
AE25	PB64B	4	BDQ60	C	PB73B	4	BDQ69	C	
GNDIO	GNDIO4	-			GNDIO4	-			
AD24	PB65A	4	BDQ69	T	PB74A	4	BDQ78	T	
AE24	PB65B	4	BDQ69	C	PB74B	4	BDQ78	C	
AD18	PB66A	4	BDQ69	T	PB75A	4	BDQ78	T	
AC18	PB66B	4	BDQ69	C	PB75B	4	BDQ78	C	
AE18	PB67A	4	BDQ69	T	PB76A	4	BDQ78	T	
AG19	PB67B	4	BDQ69	C	PB76B	4	BDQ78	C	
VCCIO	VCCIO4	4			VCCIO4	4			
GNDIO	GNDIO4	-			GNDIO4	-			
AC19	PB69A	4	BDQS69	T	PB78A	4	BDQS78	T	
AD20	PB69B	4	BDQ69	C	PB78B	4	BDQ78	C	
AB18	PB70A	4	BDQ69	T	PB79A	4	BDQ78	T	
AC20	PB70B	4	BDQ69	C	PB79B	4	BDQ78	C	
AE20	PB71A	4	BDQ69	T	PB80A	4	BDQ78	T	
AE21	PB71B	4	BDQ69	C	PB80B	4	BDQ78	C	
VCCIO	VCCIO4	4			VCCIO4	4			
AC23	PB72A	4	BDQ69	T	PB81A	4	BDQ78	T	
AD23	PB72B	4	BDQ69	C	PB81B	4	BDQ78	C	
GNDIO	GNDIO4	-			GNDIO4	-			
AH18	LRC_SQ_VCCR3	13			LRC_SQ_VCCR3	13			
AK19	LRC_SQ_HDINP3	13		T	LRC_SQ_HDINP3	13		T	
AJ18	LRC_SQ_VCCIB3	13			LRC_SQ_VCCIB3	13			
AJ19	LRC_SQ_HDINN3	13		C	LRC_SQ_HDINN3	13		C	
AH21	LRC_SQ_VCCTX3	13			LRC_SQ_VCCTX3	13			
AK22	LRC_SQ_HDOUTP3	13		T	LRC_SQ_HDOUTP3	13		T	
AK21	LRC_SQ_VCCOB3	13			LRC_SQ_VCCOB3	13			
AJ22	LRC_SQ_HDOUTN3	13		C	LRC_SQ_HDOUTN3	13		C	
AH22	LRC_SQ_VCCTX2	13			LRC_SQ_VCCTX2	13			
AJ23	LRC_SQ_HDOUTN2	13		C	LRC_SQ_HDOUTN2	13		C	
AH23	LRC_SQ_VCCOB2	13			LRC_SQ_VCCOB2	13			
AK23	LRC_SQ_HDOUTP2	13		T	LRC_SQ_HDOUTP2	13		T	
AH19	LRC_SQ_VCCR2	13			LRC_SQ_VCCR2	13			
AJ20	LRC_SQ_HDINN2	13		C	LRC_SQ_HDINN2	13		C	
AH20	LRC_SQ_VCCIB2	13			LRC_SQ_VCCIB2	13			
AK20	LRC_SQ_HDINP2	13		T	LRC_SQ_HDINP2	13		T	
AH24	LRC_SQ_VCCP	13			LRC_SQ_VCCP	13			
AG24	LRC_SQ_REFCLKP	13		T	LRC_SQ_REFCLKP	13		T	
AF24	LRC_SQ_REFCLKN	13		C	LRC_SQ_REFCLKN	13		C	
AJ24	LRC_SQ_VCCAUX33	13			LRC_SQ_VCCAUX33	13			
AK28	LRC_SQ_HDINP1	13		T	LRC_SQ_HDINP1	13		T	
AH28	LRC_SQ_VCCIB1	13			LRC_SQ_VCCIB1	13			
AJ28	LRC_SQ_HDINN1	13		C	LRC_SQ_HDINN1	13		C	
AH29	LRC_SQ_VCCR1	13			LRC_SQ_VCCR1	13			
AK25	LRC_SQ_HDOUTP1	13		T	LRC_SQ_HDOUTP1	13		T	

LFE2M70E/SE and LFE2M100E/SE Logic Signal Connections: 1152 fpBGA (Cont.)

LFE2M70E/SE				LFE2M100E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
M2	PL26A	7	LDQ28	T (LVDS)*	PL30A	7	LDQ32	T (LVDS)*
M1	PL26B	7	LDQ28	C (LVDS)*	PL30B	7	LDQ32	C (LVDS)*
L6	PL27A	7	LDQ28	T	PL31A	7	LDQ32	T
L5	PL27B	7	LDQ28	C	PL31B	7	LDQ32	C
GNDIO	GNDIO7	-			GNDIO7	-		
L3	PL28A	7	LDQS28	T (LVDS)*	PL32A	7	LDQS32	T (LVDS)*
L4	PL28B	7	LDQ28	C (LVDS)*	PL32B	7	LDQ32	C (LVDS)*
M3	PL29A	7	LDQ28	T	PL33A	7	LDQ32	T
VCCIO	VCCIO7	7			VCCIO7	7		
M4	PL29B	7	LDQ28	C	PL33B	7	LDQ32	C
N1	PL30A	7	LDQ28	T (LVDS)*	PL34A	7	LDQ32	T (LVDS)*
N2	PL30B	7	LDQ28	C (LVDS)*	PL34B	7	LDQ32	C (LVDS)*
M5	PL31A	7	LDQ28	T	PL35A	7	LDQ32	T
GNDIO	GNDIO7	-			GNDIO7	-		
N6	PL31B	7	LDQ28	C	PL35B	7	LDQ32	C
P3	NC	-			PL37A	7		T (LVDS)*
-	-	-			GNDIO7	-		
P4	NC	-			PL37B	7		C (LVDS)*
P9	NC	-			PL38A	7		T
M7	NC	-			PL38B	7		C
-	-	-			VCCIO7	7		
P1	NC	-			PL39A	7		T (LVDS)*
P2	NC	-			PL39B	7		C (LVDS)*
N7	NC	-			PL40A	7		T
P7	NC	-			PL40B	7		C
-	-	-			GNDIO7	-		
P5	PL33A	7	LDQ37	T (LVDS)*	PL41A	7	LDQ45	T (LVDS)*
N5	PL33B	7	LDQ37	C (LVDS)*	PL41B	7	LDQ45	C (LVDS)*
P8	PL34A	7	LDQ37	T	PL42A	7	LDQ45	T
P6	PL34B	7	LDQ37	C	PL42B	7	LDQ45	C
VCCIO	VCCIO7	7			VCCIO7	7		
R3	PL35A	7	LDQ37	T (LVDS)*	PL43A	7	LDQ45	T (LVDS)*
R4	PL35B	7	LDQ37	C (LVDS)*	PL43B	7	LDQ45	C (LVDS)*
R10	PL36A	7	LDQ37	T	PL44A	7	LDQ45	T
P11	PL36B	7	LDQ37	C	PL44B	7	LDQ45	C
GNDIO	GNDIO7	-			GNDIO7	-		
R7	PL37A	7	LDQS37	T (LVDS)*	PL45A	7	LDQS45	T (LVDS)*
R8	PL37B	7	LDQ37	C (LVDS)*	PL45B	7	LDQ45	C (LVDS)*
R5	PL38A	7	LDQ37	T	PL46A	7	LDQ45	T
VCCIO	VCCIO7	7			VCCIO7	7		
T5	PL38B	7	LDQ37	C	PL46B	7	LDQ45	C
R1	PL39A	7	LDQ37	T (LVDS)*	PL47A	7	LDQ45	T (LVDS)*
R2	PL39B	7	LDQ37	C (LVDS)*	PL47B	7	LDQ45	C (LVDS)*
R11	PL40A	7	LDQ37	T	PL48A	7	LDQ45	T
GNDIO	GNDIO7	-			GNDIO7	-		
T10	PL40B	7	LDQ37	C	PL48B	7	LDQ45	C
T1	PL42A	7	LUM3_SPLLT_IN_A/LDQ46	T (LVDS)*	PL50A	7	LUM3_SPLLT_IN_A/LDQ54	T (LVDS)*
T2	PL42B	7	LUM3_SPLLC_IN_A/LDQ46	C (LVDS)*	PL50B	7	LUM3_SPLLC_IN_A/LDQ54	C (LVDS)*
U10	PL43A	7	LUM3_SPLLT_FB_A/LDQ46	T	PL51A	7	LUM3_SPLLT_FB_A/LDQ54	T

LFE2M70E/SE and LFE2M100E/SE Logic Signal Connections: 1152 fpBGA (Cont.)

LFE2M70E/SE				LFE2M100E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
E5	ULC_SQ_REFCLKN	11		C	ULC_SQ_REFCLKN	11		C
D5	ULC_SQ_REFCLKP	11		T	ULC_SQ_REFCLKP	11		T
D6	ULC_SQ_VCCP	11			ULC_SQ_VCCP	11		
C5	ULC_SQ_HDINP2	11		T	ULC_SQ_HDINP2	11		T
D4	ULC_SQ_VCCIB2	11			ULC_SQ_VCCIB2	11		
C4	ULC_SQ_HDINN2	11		C	ULC_SQ_HDINN2	11		C
B5	ULC_SQ_VCCRX2	11			ULC_SQ_VCCRX2	11		
A5	ULC_SQ_HDOUTP2	11		T	ULC_SQ_HDOUTP2	11		T
D3	ULC_SQ_VCCOB2	11			ULC_SQ_VCCOB2	11		
A4	ULC_SQ_HDOUTN2	11		C	ULC_SQ_HDOUTN2	11		C
B4	ULC_SQ_VCCTX2	11			ULC_SQ_VCCTX2	11		
A3	ULC_SQ_HDOUTN3	11		C	ULC_SQ_HDOUTN3	11		C
C1	ULC_SQ_VCCOB3	11			ULC_SQ_VCCOB3	11		
A2	ULC_SQ_HDOUTP3	11		T	ULC_SQ_HDOUTP3	11		T
B3	ULC_SQ_VCCTX3	11			ULC_SQ_VCCTX3	11		
C3	ULC_SQ_HDINN3	11		C	ULC_SQ_HDINN3	11		C
B1	ULC_SQ_VCCIB3	11			ULC_SQ_VCCIB3	11		
C2	ULC_SQ_HDINP3	11		T	ULC_SQ_HDINP3	11		T
B2	ULC_SQ_VCCRX3	11			ULC_SQ_VCCRX3	11		
AA13	VCC	-			VCC	-		
AA14	VCC	-			VCC	-		
AA15	VCC	-			VCC	-		
AA16	VCC	-			VCC	-		
AA17	VCC	-			VCC	-		
AA18	VCC	-			VCC	-		
AA19	VCC	-			VCC	-		
AA20	VCC	-			VCC	-		
AA21	VCC	-			VCC	-		
AA22	VCC	-			VCC	-		
AB14	VCC	-			VCC	-		
AB15	VCC	-			VCC	-		
AB20	VCC	-			VCC	-		
AB21	VCC	-			VCC	-		
N14	VCC	-			VCC	-		
N15	VCC	-			VCC	-		
N20	VCC	-			VCC	-		
N21	VCC	-			VCC	-		
P13	VCC	-			VCC	-		
P14	VCC	-			VCC	-		
P15	VCC	-			VCC	-		
P16	VCC	-			VCC	-		
P17	VCC	-			VCC	-		
P18	VCC	-			VCC	-		
P19	VCC	-			VCC	-		
P20	VCC	-			VCC	-		
P21	VCC	-			VCC	-		
P22	VCC	-			VCC	-		
R13	VCC	-			VCC	-		
R14	VCC	-			VCC	-		

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2M100E-5F1152C	520	1.2V	-5	fpBGA	1152	COM	100
LFE2M100E-6F1152C	520	1.2V	-6	fpBGA	1152	COM	100
LFE2M100E-7F1152C	520	1.2V	-7	fpBGA	1152	COM	100
LFE2M100E-5F900C	416	1.2V	-5	fpBGA	900	COM	100
LFE2M100E-6F900C	416	1.2V	-6	fpBGA	900	COM	100
LFE2M100E-7F900C	416	1.2V	-7	fpBGA	900	COM	100

Date	Version	Section	Change Summary
November 2009 (cont.)	03.5 (cont.)	Pinout Information (cont.)	LatticeECP2M Pin Information Summary, LFE2M50, LFE2M70 and LFE2M100 table - corrected values for LFE2M50, 672 fpBGA in Available DDR-Interfaces per I/O Bank.
			Minor corrections in LFE2M20E/SE and LFE2M35E/SE Logic Signal Connections: 484 fpBGA table.
			Minor corrections in LFE2M50E/SE and LFE2M70E/SE Logic Signal Connections: 900 fpBGA table.
			Minor corrections in LFE2M100E/SE Logic Signal Connections: 900 fpBGA table.
			Updated LFE2-6E/SE and LFE2-12E/SE Logical Signal Connections (changed D1/SPIDS to D1).
		Ordering Information	Updated LatticeECP2M Part Number Description diagram.
March 2010	03.6	DC and Switching Characteristics	Footnote for SED operating frequency added to the sysCONFIG Port Timing Specifications table.
		Pinout Information	Changed Dual Function pin E7 to be D7/SPDI0 in Logic Signal Connections tables. Changed footnote (***) in Logic Signal Connections table.
July 2010	03.7	Architecture	Updated the Typical sysIO Behavior During Power-up text section.
		Pinout Information	Added reference to powerup information.
			Corrected reference to footnote for pins 131 and 132 for the LFE-20E/SE, 208 PQFP.
			Referenced footnote (***) for all D7/SPID0.
			Changed D7*** to D7/SPID0.
			Corrected *** footnote.
		All Sections	Included references to Lattice Diamond design software wherever ispLEVER and ispLeverCORE is specified.
April 2011	03.8	DC and Switching Characteristics	DC Electrical Characteristics table: - Added footnote 3 to I_{IH} - Added footnote 2 to I_{IL} , I_{IH} - Updated C1 and C2 typ. and max. data.
			DLL Timing table – Removed line for t_R and t_F
			LatticeECP2/M sysCONFIG Port Timing Specifications table – added footnote to t_{DINIT} .
			Figure 3-18 – Corrected label to be PRGM (not PRGMRJ).
		Pinout Information	LFE2-12E/SE and LFE-20/SE Logical Signal Connections for 208 PQFP – Corrected Dual Function information for pins 112, 114, 117, 119.
January 2012	03.9	Multiple	Removed references to ispLEVER design software.
		Architecture	Corrected information regarding SED support.
		DC and Switching Characteristics	Added reference to ESD information.
June 2013	04.0	All	Updated document with new corporate logo.
		Architecture	Architecture Overview – Added information on the state of the register on power up and after configuration.