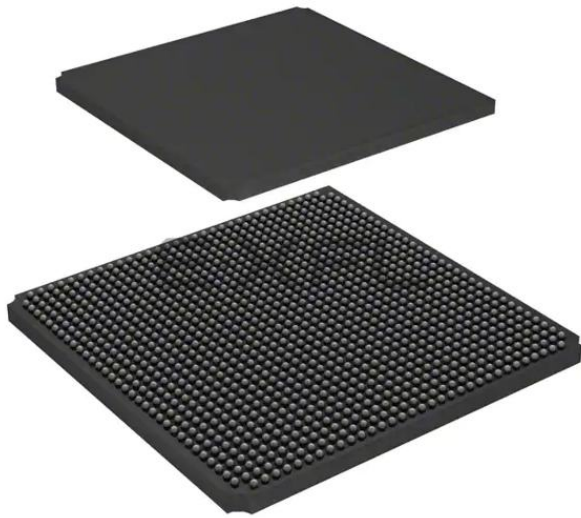




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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	11875
Number of Logic Elements/Cells	95000
Total RAM Bits	5435392
Number of I/O	520
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1152-BBGA
Supplier Device Package	1152-FPBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfe2m100e-6f1152c

ROM Mode

ROM mode uses the LUT logic; hence, Slices 0 through 3 can be used in ROM mode. Preloading is accomplished through the programming interface during PFU configuration.

Routing

There are many resources provided in the LatticeECP2/M devices to route signals individually or as buses with related control signals. The routing resources consist of switching circuitry, buffers and metal interconnect (routing) segments.

The inter-PFU connections are made with x1 (spans two PFU), x2 (spans three PFU) and x6 (spans seven PFU). The x1 and x2 connections provide fast and efficient connections in horizontal and vertical directions. The x2 and x6 resources are buffered, allowing the routing of both short and long connections between PFUs.

The LatticeECP2/M family has an enhanced routing architecture that produces a compact design. The Diamond design software takes the output of the synthesis tool and places and routes the design. Generally, the place and route tool is completely automatic, although an interactive routing editor is available to optimize the design.

sysCLOCK Phase Locked Loops (GPLL/SPLL)

The sysCLOCK PLLs provide the ability to synthesize clock frequencies. All the devices in the LatticeECP2/M family support two General Purpose PLLs (GPLLs) which are full-featured PLLs. In addition, some of the larger devices have two to six Standard PLLs (SPLLs) that have a subset of GPLL functionality.

General Purpose PLL (GPLL)

The architecture of the GPLL is shown in Figure 2-5. A description of the GPLL functionality follows.

CLKI is the reference frequency (generated either from the pin or from routing) for the PLL. CLKI feeds into the Input Clock Divider block. The CLKFB is the feedback signal (generated from CLKOP or from a user clock PIN/logic). This signal feeds into the Feedback Divider. The Feedback Divider is used to multiply the reference frequency.

The Delay Adjust Block adjusts either the delays of the reference or feedback signals. The Delay Adjust Block can either be programmed during configuration or can be adjusted dynamically. The setup, hold or clock-to-out times of the device can be improved by programming a delay in the feedback or input path of the PLL, which will advance or delay the output clock with reference to the input clock.

Following the Delay Adjust Block, both the input path and feedback signals enter the Voltage Controlled Oscillator (VCO) block. In this block the difference between the input path and feedback signals is used to control the frequency and phase of the oscillator. A LOCK signal is generated by the VCO to indicate that the VCO has locked onto the input clock signal. In dynamic mode, the PLL may lose lock after a dynamic delay adjustment and not relock until the t_{LOCK} parameter has been satisfied. LatticeECP2/M devices have two dedicated pins on the left and right edges of the device for connecting optional external capacitors to the VCO. This allows the PLLs to operate at a lower frequency. This is a shared resource that can only be used by one PLL (GPLL or SPLL) per side.

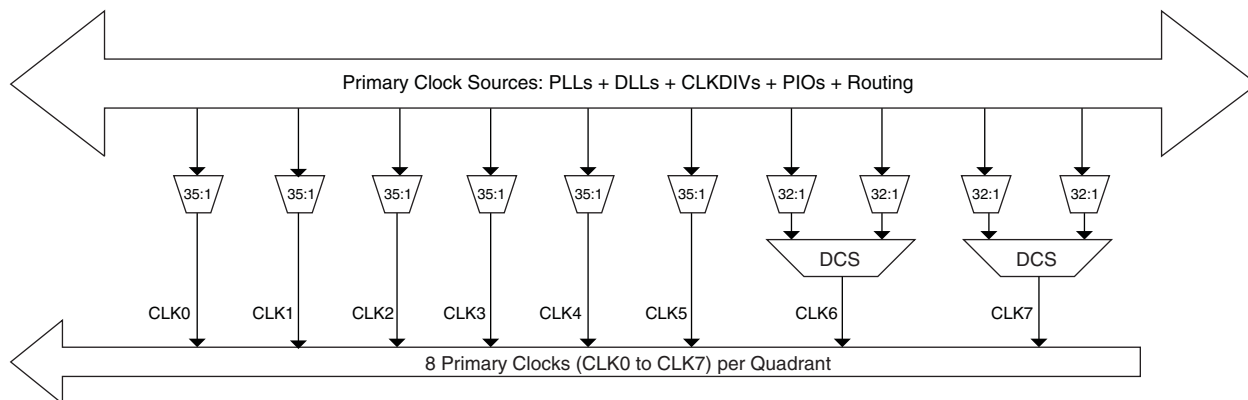
The output of the VCO then enters the post-scalar divider. The post-scalar divider allows the VCO to operate at higher frequencies than the clock output (CLKOP), thereby increasing the frequency range. A secondary divider takes the CLKOP signal and uses it to derive lower frequency outputs (CLKOK). The Phase/Duty Select block adjusts the phase and duty cycle of the CLKOP signal and generates the CLKOS signal. The phase/duty cycle setting can be pre-programmed or dynamically adjusted.

The primary output from the post scalar divider CLKOP along with the outputs from the secondary divider (CLKOK) and Phase/Duty select (CLKOS) are fed to the clock distribution network.

Primary Clock Routing

The clock routing structure in LatticeECP2/M devices consists of a network of eight primary clock lines (CLK0 through CLK7) per quadrant. The primary clocks of each quadrant are generated from muxes located in the center of the device. All the clock sources are connected to these muxes. Figure 2-13 shows the clock routing for one quadrant. Each quadrant mux is identical. If desired, any clock can be routed globally

Figure 2-13. Per Quadrant Primary Clock Selection

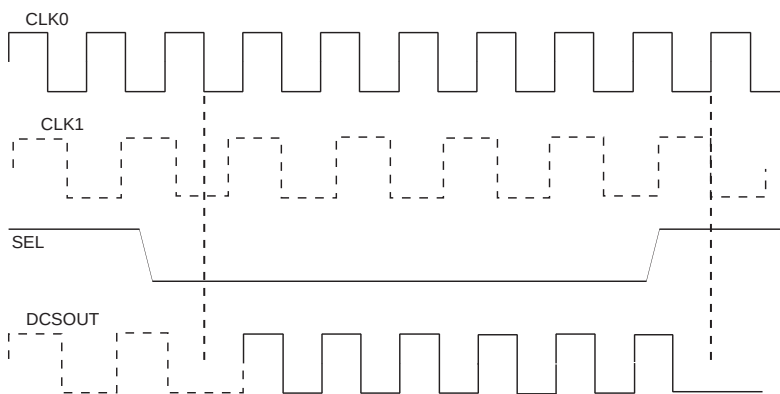


Dynamic Clock Select (DCS)

The DCS is a smart multiplexer function available in the primary clock routing. It switches between two independent input clock sources without any glitches or runt pulses. This is achieved regardless of when the select signal is toggled. There are two DCS blocks per quadrant; in total, there are eight DCS blocks per device. The inputs to the DCS block come from the center muxes. The output of the DCS is connected to primary clocks CLK6 and CLK7 (see Figure 2-13).

Figure 2-14 shows the timing waveforms of the default DCS operating mode. The DCS block can be programmed to other modes. For more information about the DCS, please see the list of additional technical documentation at the end of this data sheet.

Figure 2-14. DCS Waveforms



Secondary Clock/Control Routing

Secondary clocks in the LatticeECP2 devices are region-based resources. The benefit of region-based resources is the relatively low injection delay and skew within the region, as compared to primary clocks. EBR/DSP rows and a special vertical routing channel bound the secondary clock regions. This special vertical routing channel aligns with either the left edge of the center DSP block in the DSP row or the center of the DSP row. Figure 2-15 shows

If an EBR is pre-loaded during configuration, the GSR input must be disabled or the release of the GSR during device Wake Up must occur before the release of the device I/Os becomes active.

These instructions apply to all EBR RAM and ROM implementations.

Note that there are no reset restrictions if the EBR synchronous reset is used and the EBR GSR input is disabled.

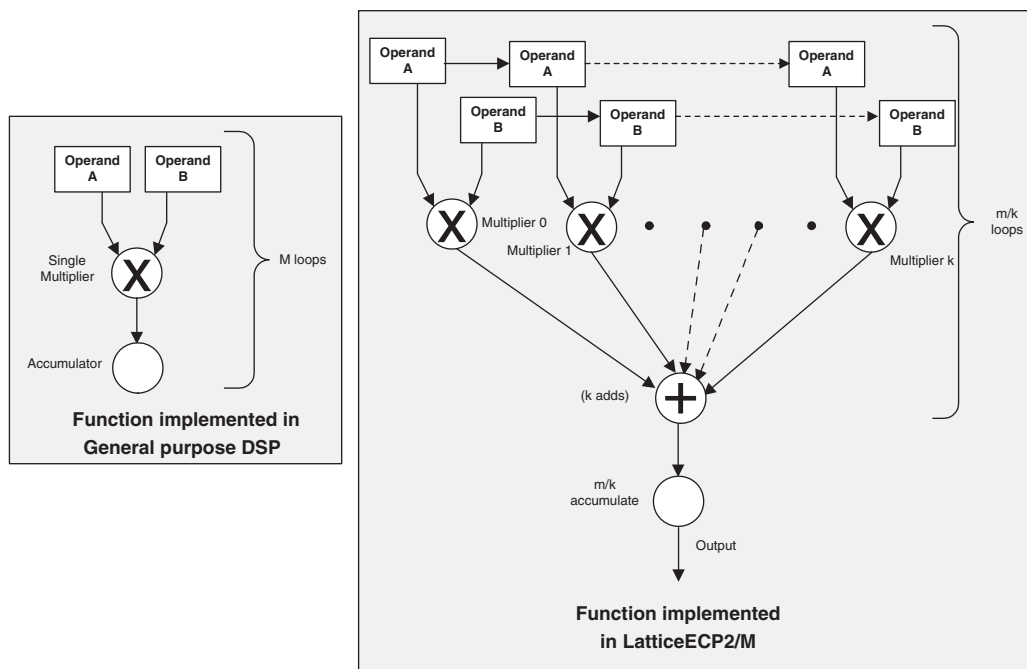
sysDSP™ Block

The LatticeECP2/M family provides a sysDSP block, making it ideally suited for low cost, high performance Digital Signal Processing (DSP) applications. Typical functions used in these applications are Finite Impulse Response (FIR) filters, Fast Fourier Transforms (FFT) functions, Correlators, Reed-Solomon/Turbo/Convolution encoders and decoders. These complex signal processing functions use similar building blocks such as multiply-adders and multiply-accumulators.

sysDSP Block Approach Compared to General DSP

Conventional general-purpose DSP chips typically contain one to four (Multiply and Accumulate) MAC units with fixed data-width multipliers; this leads to limited parallelism and limited throughput. Their throughput is increased by higher clock speeds. The LatticeECP2/M, on the other hand, has many DSP blocks that support different data-widths. This allows the designer to use highly parallel implementations of DSP functions. The designer can optimize the DSP performance vs. area by choosing an appropriate level of parallelism. Figure 2-22 compares the fully serial and the mixed parallel and serial implementations.

Figure 2-22. Comparison of General DSP and LatticeECP2/M Approaches



sysDSP Block Capabilities

The sysDSP block in the LatticeECP2/M family supports four functional elements in three 9, 18 and 36 data path widths. The user selects a function element for a DSP block and then selects the width and type (signed/unsigned) of its operands. The operands in the LatticeECP2/M family sysDSP Blocks can be either signed or unsigned but not mixed within a function element. Similarly, the operand widths cannot be mixed within a block. In the LatticeECP2/M family the DSP elements can be concatenated.

The resources in each sysDSP block can be configured to support the following elements:

sysI/O Differential Electrical Characteristics

LVDS

Over Recommended Operating Conditions

Parameter	Description	Test Conditions	Min.	Typ.	Max.	Units
$V_{INP} V_{INM}$	Input Voltage		0	—	2.4	V
V_{CM}	Input Common Mode Voltage	Half the Sum of the Two Inputs	0.05	—	2.35	V
V_{THD}	Differential Input Threshold	Difference Between the Two Inputs	+/-100	—	—	mV
I_{IN}	Input Current	Power On or Power Off	—	—	+/-10	μ A
V_{OH}	Output High Voltage for V_{OP} or V_{OM}	$R_T = 100$ Ohm	—	1.38	1.60	V
V_{OL}	Output Low Voltage for V_{OP} or V_{OM}	$R_T = 100$ Ohm	0.9V	1.03	—	V
V_{OD}	Output Voltage Differential	$(V_{OP} - V_{OM})$, $R_T = 100$ Ohm	250	350	450	mV
ΔV_{OD}	Change in V_{OD} Between High and Low		—	—	50	mV
V_{OS}	Output Voltage Offset	$(V_{OP} + V_{OM})/2$, $R_T = 100$ Ohm	1.125	1.20	1.375	V
ΔV_{OS}	Change in V_{OS} Between H and L		—	—	50	mV
I_{SA}	Output Short Circuit Current	$V_{OD} = 0V$ Driver Outputs Shorted to Ground	—	—	24	mA
I_{SAB}	Output Short Circuit Current	$V_{OD} = 0V$ Driver Outputs Shorted to Each Other	—	—	12	mA

Differential HSTL and SSTL

Differential HSTL and SSTL outputs are implemented as a pair of complementary single-ended outputs. All allowable single-ended output classes (class I and class II) are supported in this mode.

For further information about LVPECL, RSDS, MLVDS, BLVDS and other differential interfaces please see the list of additional technical information at the end of this data sheet.

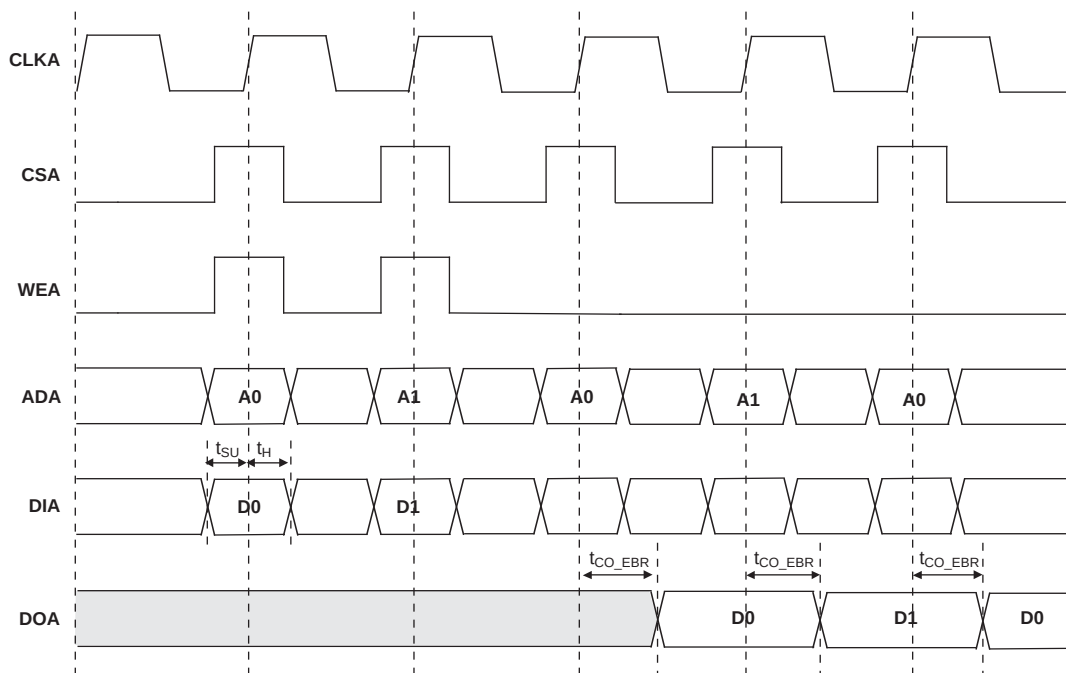
LatticeECP2/M Internal Switching Characteristics¹

Over Recommended Operating Conditions

Parameter	Description	-7		-6		-5		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
PFU/PFF Logic Mode Timing								
t _{LUT4_PFU}	LUT4 delay (A to D inputs to F output)	—	0.180	—	0.198	—	0.216	ns
t _{LUT6_PFU}	LUT6 delay (A to D inputs to OFX output)	—	0.304	—	0.331	—	0.358	ns
t _{LSR_PFU}	Set/Reset to output of PFU (Asynchronous)	—	0.600	—	0.655	—	0.711	ns
t _{SUM_PFU}	Clock to Mux (M0,M1) Input Setup Time	0.128	—	0.129	—	0.129	—	ns
t _{HM_PFU}	Clock to Mux (M0,M1) Input Hold Time	-0.051	—	-0.049	—	-0.046	—	ns
t _{SUD_PFU}	Clock to D input setup time	0.061	—	0.071	—	0.081	—	ns
t _{HD_PFU}	Clock to D input hold time	0.002	—	0.003	—	0.003	—	ns
t _{CK2Q_PFU}	Clock to Q delay, (D-type Register Configuration)	—	0.285	—	0.309	—	0.333	ns
PFU Dual Port Memory Mode Timing								
t _{CORAM_PFU}	Clock to Output (F Port)	—	0.902	—	1.083	—	1.263	ns
t _{SUDATA_PFU}	Data Setup Time	-0.172	—	-0.205	—	-0.238	—	ns
t _{HDATA_PFU}	Data Hold Time	0.199	—	0.235	—	0.271	—	ns
t _{SUADDR_PFU}	Address Setup Time	-0.245	—	-0.284	—	-0.323	—	ns
t _{HADDR_PFU}	Address Hold Time	0.246	—	0.285	—	0.324	—	ns
t _{SUWREN_PFU}	Write/Read Enable Setup Time	-0.122	—	-0.145	—	-0.168	—	ns
t _{HWREN_PFU}	Write/Read Enable Hold Time	0.132	—	0.156	—	0.180	—	ns
PIC Timing								
PIO Input/Output Buffer Timing								
t _{IN_PIO}	Input Buffer Delay (LVCMOS25)	—	0.613	—	0.681	—	0.749	ns
t _{OUT_PIO}	Output Buffer Delay (LVCMOS25)	—	1.115	—	1.115	—	1.343	ns
IOLOGIC Input/Output Timing								
t _{SUI_PIO}	Input Register Setup Time (Data Before Clock)	0.596	—	0.645	—	0.694	—	ns
t _{HI_PIO}	Input Register Hold Time (Data after Clock)	-0.570	—	-0.614	—	-0.658	—	ns
t _{COO_PIO}	Output Register Clock to Output Delay	—	0.61	—	0.66	—	0.72	ns
t _{SUCE_PIO}	Input Register Clock Enable Setup Time	0.032	—	0.037	—	0.041	—	ns
t _{HCE_PIO}	Input Register Clock Enable Hold Time	-0.022	—	-0.025	—	-0.028	—	ns
t _{SULSR_PIO}	Set/Reset Setup Time	0.184	—	0.201	—	0.217	—	ns
t _{HLSR_PIO}	Set/Reset Hold Time	-0.080	—	-0.086	—	-0.093	—	ns
EBR Timing								
t _{CO_EBR}	Clock (Read) to output from Address or Data	—	2.51	—	2.75	—	2.99	ns
t _{COO_EBR}	Clock (Write) to output from EBR output Register	—	0.33	—	0.36	—	0.39	ns
t _{SUDATA_EBR}	Setup Data to EBR Memory	-0.157	—	-0.181	—	-0.205	—	ns
t _{HDATA_EBR}	Hold Data to EBR Memory	0.173	—	0.195	—	0.217	—	ns
t _{SUADDR_EBR}	Setup Address to EBR Memory	-0.115	—	-0.130	—	-0.145	—	ns
t _{HADDR_EBR}	Hold Address to EBR Memory	0.138	—	0.155	—	0.172	—	ns
t _{SUWREN_EBR}	Setup Write/Read Enable to PFU Memory	-0.128	—	-0.149	—	-0.170	—	ns

Timing Diagrams

Figure 3-9. Read/Write Mode (Normal)



Note: Input data and address are registered at the positive edge of the clock and output data appears after the positive edge of the clock.

Figure 3-10. Read/Write Mode with Input and Output Registers

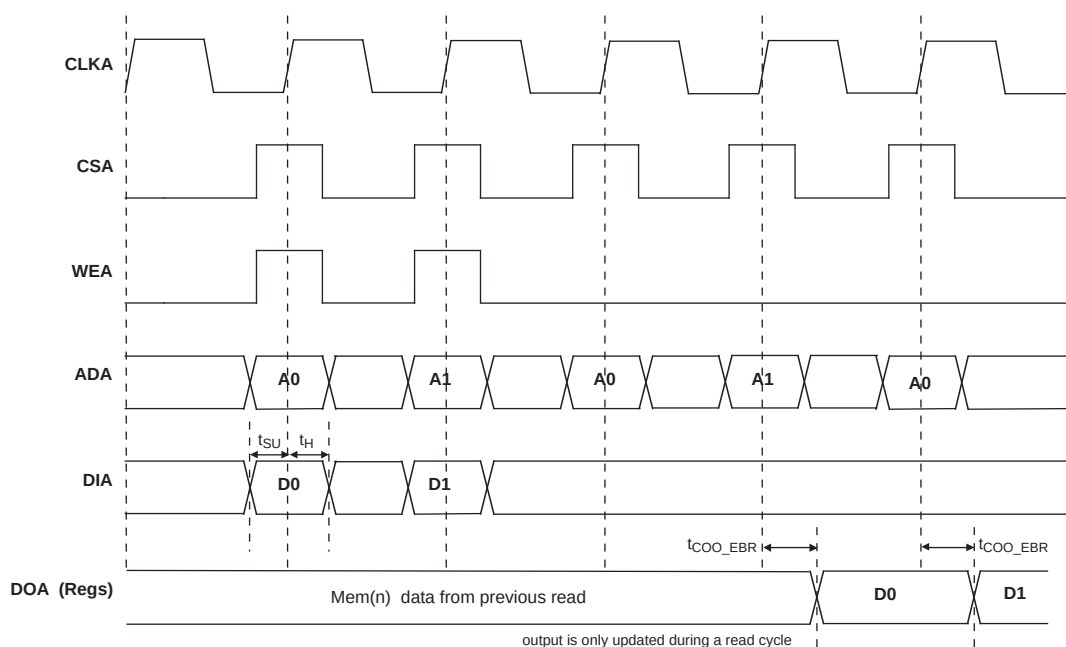
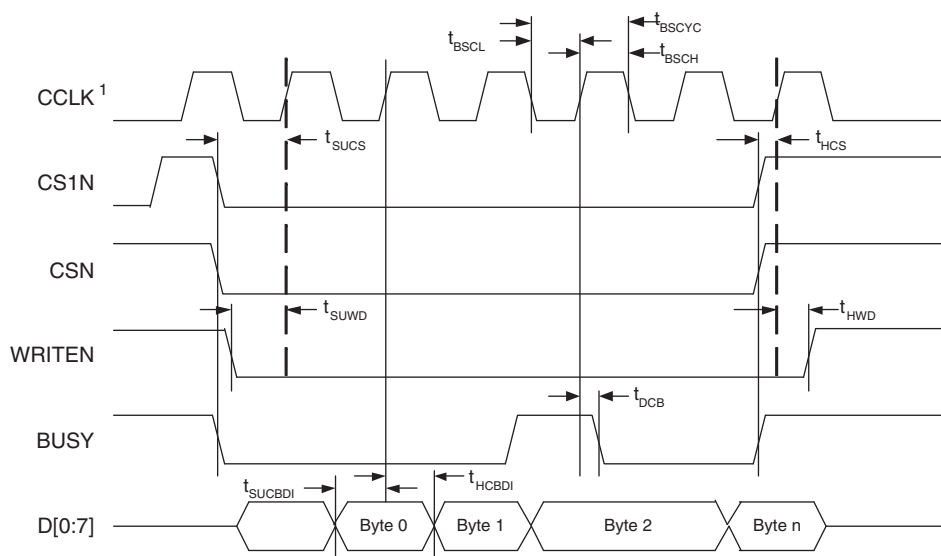


Figure 3-15. sysCONFIG Parallel Port Write Cycle



1. In Master Parallel Mode the FPGA provides CCLK. In Slave Parallel Mode the external device provides CCLK.

Figure 3-16. sysCONFIG Slave Serial Port Timing

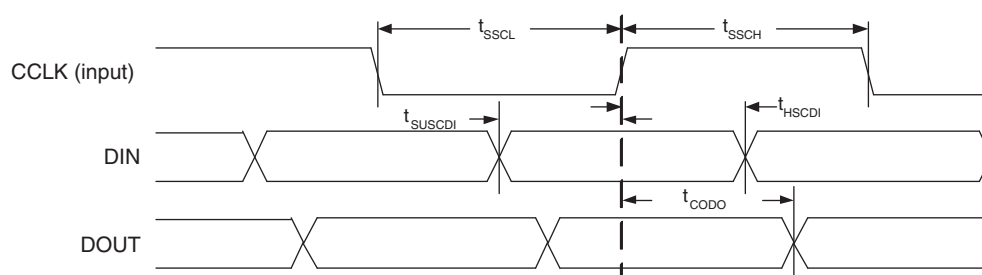
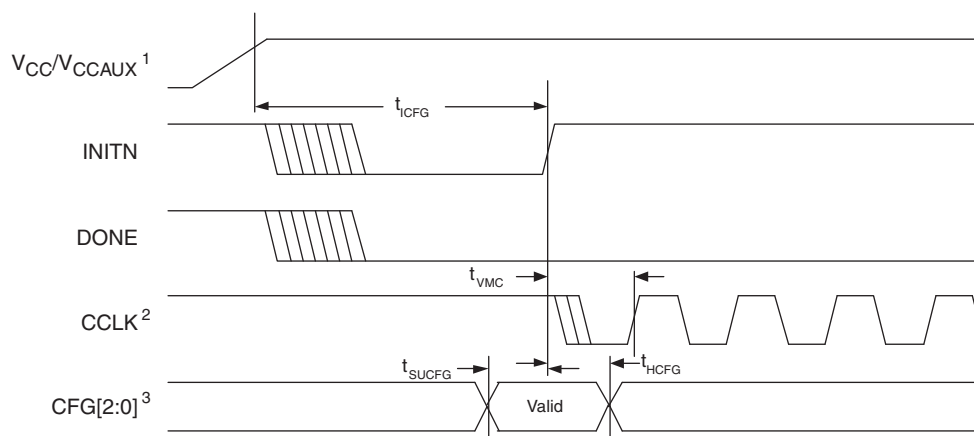


Figure 3-17. Power-On-Reset (POR) Timing



1. Time taken from V_{CC} or V_{CCAUX} , whichever is the last to reach its V_{MIN} .
2. Device is in a Master Mode.
3. The CFG pins are normally static (hard wired).

LFE2-6E/SE and LFE2-12E/SE Logic Signal Connections: 144 TQFP (Cont.)

LFE2-6E/SE					LFE2-12E/12SE				
Pin Number	Pin/Pad Function	Bank	Dual Function	Differential	Pin/Pad Function	Bank	Dual Function	Differential	
91	PR20B	3	RLM0_GPLL_C_IN_A**	C (LVDS)*	PR20B	3	RLM0_GPLL_C_IN_A**	C (LVDS)*	
92	PR20A	3	RLM0_GPLL_T_IN_A**	T (LVDS)*	PR20A	3	RLM0_GPLL_T_IN_A**	T (LVDS)*	
93	RLM0_PLLCAP	3			RLM0_PLLCAP	3			
94	VCC	-			VCC	-			
95	GND	-			GND	-			
96	PR17B	3	RLM0_GDLL_C_IN_A**	C (LVDS)*	PR17B	3	RLM0_GDLL_C_IN_A**	C (LVDS)*	
97	PR17A	3	RLM0_GDLL_T_IN_A**	T (LVDS)*	PR17A	3	RLM0_GDLL_T_IN_A**	T (LVDS)*	
98	PR16B	3	VREF2_3	C	PR16B	3	VREF2_3	C	
99	PR16A	3	VREF1_3	T	PR16A	3	VREF1_3	T	
100	PR15B	3	PCLKC3_0	C (LVDS)*	PR15B	3	PCLKC3_0	C (LVDS)*	
101	PR15A	3	PCLKT3_0	T (LVDS)*	PR15A	3	PCLKT3_0	T (LVDS)*	
102	VCC	-			VCC	-			
103	PR13B	2	PCLKC2_0/RDQ10	C	PR13B	2	PCLKC2_0/RDQ10	C	
104	PR13A	2	PCLKT2_0/RDQ10	T	PR13A	2	PCLKT2_0/RDQ10	T	
105	GND	-			GND	-			
106	VCCIO2	2			VCCIO2	2			
107	PR2B	2	VREF2_2	C (LVDS)*	PR2B	2	VREF2_2	C (LVDS)*	
108	PR2A	2	VREF1_2	T (LVDS)*	PR2A	2	VREF1_2	T (LVDS)*	
109	PT28B	1	VREF2_1	C	PT55B	1	VREF2_1	C	
110	PT28A	1	VREF1_1	T	PT55A	1	VREF1_1	T	
111	PT26B	1		C	PT54B	1		C	
112	PT26A	1		T	PT54A	1		T	
113	PT24B	1		C	PT52B	1		C	
114	PT24A	1		T	PT52A	1		T	
115	PT22B	1		C	PT50B	1		C	
116	PT22A	1		T	PT50A	1		T	
117	VCCIO1	1			VCCIO1	1			
118	PT20B	1		C	PT48B	1		C	
119	PT20A	1		T	PT48A	1		T	
120	GND	-			GND	-			
121	PT18B	1		C	PT44B	1		C	
122	PT18A	1		T	PT44A	1		T	
123	PT16A	1			PT40B	1		C	
124	NC	1			PT40A	1		T	
125	PT14B	1		C	PT34B	1		C	
126	PT14A	1		T	PT34A	1		T	
127	NC	1			NC	1			
128	VCC	-			VCC	-			
129	PT12B	1	PCLKC1_0	C	PT30B	1	PCLKC1_0	C	
130	PT12A	1	PCLKT1_0	T	PT30A	1	PCLKT1_0	T	
131	PT10B	0	PCLKC0_0	C	PT28B	0	PCLKC0_0	C	
132	XRES	0			XRES	0			
133	GND	-			GND	-			
134	PT10A	0	PCLKT0_0	T	PT28A	0	PCLKT0_0	T	
135	VCC	-			VCC	-			

LFE2-6E/SE and LFE2-12E/SE Logic Signal Connections: 256 fpBGA (Cont.)

LFE2-6E/SE					LFE2-12E/SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
D5	PT2B	0	VREF2_0	C	PT2B	0	VREF2_0	C
E5	PT2A	0	VREF1_0	T	PT2A	0	VREF1_0	T
G7	VCC	-			VCC	-		
G9	VCC	-			VCC	-		
H7	VCC	-			VCC	-		
J10	VCC	-			VCC	-		
K10	VCC	-			VCC	-		
K8	VCC	-			VCC	-		
G8	VCCAUX	-			VCCAUX	-		
H10	VCCAUX	-			VCCAUX	-		
J7	VCCAUX	-			VCCAUX	-		
K9	VCCAUX	-			VCCAUX	-		
C5	VCCIO0	0			VCCIO0	0		
E7	VCCIO0	0			VCCIO0	0		
C12	VCCIO1	1			VCCIO1	1		
E10	VCCIO1	1			VCCIO1	1		
E14	VCCIO2	2			VCCIO2	2		
G12	VCCIO2	2			VCCIO2	2		
K12	VCCIO3	3			VCCIO3	3		
M14	VCCIO3	3			VCCIO3	3		
M10	VCCIO4	4			VCCIO4	4		
P12	VCCIO4	4			VCCIO4	4		
M7	VCCIO5	5			VCCIO5	5		
P5	VCCIO5	5			VCCIO5	5		
K5	VCCIO6	6			VCCIO6	6		
M3	VCCIO6	6			VCCIO6	6		
E3	VCCIO7	7			VCCIO7	7		
G5	VCCIO7	7			VCCIO7	7		
T15	VCCIO8	8			VCCIO8	8		
A1	GND	-			GND	-		
A16	GND	-			GND	-		
B12	GND	-			GND	-		
B5	GND	-			GND	-		
C8	GND	-			GND	-		
E15	GND	-			GND	-		
E2	GND	-			GND	-		
H14	GND	-			GND	-		
H8	GND	-			GND	-		
H9	GND	-			GND	-		
J3	GND	-			GND	-		
J8	GND	-			GND	-		
J9	GND	-			GND	-		
M15	GND	-			GND	-		
M2	GND	-			GND	-		
P9	GND	-			GND	-		

LFE2-12E/SE and LFE2-20E/SE Logic Signal Connections: 484 fpBGA (Cont.)

LFE2-12E/12SE					LFE2-20E/20SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential	
T7	PL29B	6	LDQ28	C	PL43B	6	LDQ42	C	
T6	PL26B	6	LDQ28	C (LVDS)*	PL40B	6	LDQ42	C (LVDS)*	
AA2	PL31A	6	LDQ28	T	PL45A	6	LDQ42	T	
VCCIO	VCCIO6	6			VCCIO6	6			
Y1	PL28A	6	LDQS28	T (LVDS)*	PL42A	6	LDQS42	T (LVDS)*	
AA1	PL31B	6	LDQ28	C	PL45B	6	LDQ42	C	
W1	PL28B	6	LDQ28	C (LVDS)*	PL42B	6	LDQ42	C (LVDS)*	
V3	PL30B	6	LDQ28	C (LVDS)*	PL44B	6	LDQ42	C (LVDS)*	
GNDIO	GNDIO6	-			GNDIO	-			
V4	PL30A	6	LDQ28	T (LVDS)*	PL44A	6	LDQ42	T (LVDS)*	
U5	TDI	-			TDI	-			
U7	TCK	-			TCK	-			
V6	TDO	-			TDO	-			
V5	TMS	-			TMS	-			
T8	VCCJ	-			VCCJ	-			
W4	PB3A	5	BDQ6	T	PB3A	5	BDQ6	T	
Y3	PB2A	5	VREF2_5/BDQ6	T	PB2A	5	VREF2_5/BDQ6	T	
W3	PB3B	5	BDQ6	C	PB3B	5	BDQ6	C	
Y2	PB2B	5	VREF1_5/BDQ6	C	PB2B	5	VREF1_5/BDQ6	C	
AB3	PB5A	5	BDQ6	T	PB5A	5	BDQ6	T	
VCCIO	VCCIO5	5			VCCIO5	5			
W5	PB4A	5	BDQ6	T	PB4A	5	BDQ6	T	
AB2	PB5B	5	BDQ6	C	PB5B	5	BDQ6	C	
W6	PB4B	5	BDQ6	C	PB4B	5	BDQ6	C	
AB5	PB7A	5	BDQ6	T	PB7A	5	BDQ6	T	
GNDIO	GNDIO5	-			GNDIO	-			
Y4	PB6A	5	BDQS6	T	PB6A	5	BDQS6	T	
AB4	PB7B	5	BDQ6	C	PB7B	5	BDQ6	C	
AA3	PB6B	5	BDQ6	C	PB6B	5	BDQ6	C	
AB6	PB9A	5	BDQ6	T	PB9A	5	BDQ6	T	
VCCIO	VCCIO5	5			VCCIO5	5			
AA5	PB8A	5	BDQ6	T	PB8A	5	BDQ6	T	
AA6	PB9B	5	BDQ6	C	PB9B	5	BDQ6	C	
Y5	PB8B	5	BDQ6	C	PB8B	5	BDQ6	C	
GNDIO	GNDIO5	-			GNDIO	-			
-	-	-			VCCIO5	5			
Y6	PB12A	5	BDQ15	T	PB21A	5	BDQ24	T	
W7	PB11A	5	BDQ15	T	PB20A	5	BDQ24	T	
Y7	PB12B	5	BDQ15	C	PB21B	5	BDQ24	C	
W8	PB11B	5	BDQ15	C	PB20B	5	BDQ24	C	
U8	PB14A	5	BDQ15	T	PB23A	5	BDQ24	T	
VCCIO	VCCIO5	5			VCCIO5	5			
AA7	PB13A	5	BDQ15	T	PB22A	5	BDQ24	T	
U9	PB14B	5	BDQ15	C	PB23B	5	BDQ24	C	

LFE2-12E/SE and LFE2-20E/SE Logic Signal Connections: 484 fpBGA
(Cont.)

LFE2-12E/12SE					LFE2-20E/20SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
AB7	PB13B	5	BDQ15	C	PB22B	5	BDQ24	C
Y8	PB16A	5	BDQ15	T	PB25A	5	BDQ24	T
GNDIO	GNDIO5	-			GNDIO	-		
W9	PB15A	5	BDQS15	T	PB24A	5	BDQS24	T
AA8	PB16B	5	BDQ15	C	PB25B	5	BDQ24	C
V9	PB15B	5	BDQ15	C	PB24B	5	BDQ24	C
AB8	PB18A	5	BDQ15	T	PB27A	5	BDQ24	T
VCCIO	VCCIO5	5			VCCIO5	5		
W10	PB17A	5	BDQ15	T	PB26A	5	BDQ24	T
AA9	PB18B	5	BDQ15	C	PB27B	5	BDQ24	C
V10	PB17B	5	BDQ15	C	PB26B	5	BDQ24	C
GNDIO	GNDIO5	-			GNDIO	-		
Y10	PB21A	5	BDQ24	T	PB30A	5	BDQ33	T
AB9	PB20A	5	BDQ24	T	PB29A	5	BDQ33	T
AA10	PB21B	5	BDQ24	C	PB30B	5	BDQ33	C
AB10	PB20B	5	BDQ24	C	PB29B	5	BDQ33	C
AB11	PB23A	5	BDQ24	T	PB32A	5	BDQ33	T
U10	PB22A	5	BDQ24	T	PB31A	5	BDQ33	T
VCCIO	VCCIO5	5			VCCIO5	5		
AA11	PB23B	5	BDQ24	C	PB32B	5	BDQ33	C
U11	PB22B	5	BDQ24	C	PB31B	5	BDQ33	C
GNDIO	GNDIO5	-			GNDIO5	-		
AB12	PB25A	5	BDQ24	T	PB34A	5	BDQ33	T
Y11	PB24A	5	BDQS24	T	PB33A	5	BDQS33	T
AA12	PB25B	5	BDQ24	C	PB34B	5	BDQ33	C
W11	PB24B	5	BDQ24	C	PB33B	5	BDQ33	C
AB13	PB26A	5	PCLKT5_0/BDQ24	T	PB35A	5	PCLKT5_0/BDQ33	T
VCCIO	VCCIO5	5			VCCIO5	5		
AB14	PB26B	5	PCLKC5_0/BDQ24	C	PB35B	5	PCLKC5_0/BDQ33	C
GNDIO	GNDIO5	-			GNDIO5	-		
Y12	PB32A	4	BDQ33	T	PB41A	4	BDQ42	T
W12	PB32B	4	BDQ33	C	PB41B	4	BDQ42	C
VCCIO	VCCIO4	4			VCCIO4	4		
U12	PB31A	4	PCLKT4_0/BDQ33	T	PB40A	4	PCLKT4_0/BDQ42	T
V12	PB31B	4	PCLKC4_0/BDQ33	C	PB40B	4	PCLKC4_0/BDQ42	C
U13	PB34A	4	BDQ33	T	PB43A	4	BDQ42	T
GNDIO	GNDIO4	-			GNDIO4	-		
AA13	PB33A	4	BDQS33	T	PB42A	4	BDQS42	T
U14	PB34B	4	BDQ33	C	PB43B	4	BDQ42	C
Y13	PB33B	4	BDQ33	C	PB42B	4	BDQ42	C
AB16	PB36A	4	BDQ33	T	PB45A	4	BDQ42	T
VCCIO	VCCIO4	4			VCCIO4	4		
AB15	PB35A	4	BDQ33	T	PB44A	4	BDQ42	T
AB17	PB36B	4	BDQ33	C	PB45B	4	BDQ42	C

LFE2-12E/SE and LFE2-20E/SE Logic Signal Connections: 484 fpBGA (Cont.)

LFE2-12E/12SE					LFE2-20E/20SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
F19	PR5A	2		T	PR7A	2	RDQ8	T
D20	PR4A	2		T (LVDS)*	PR6A	2	RDQ8	T (LVDS)*
F18	PR3B	2		C	PR5B	2	RDQ8	C
VCCIO	VCCIO2	2			VCCIO2	2		
C21	NC	-			PR4B	2	RDQ8	C (LVDS)*
F16	PR3A	2		T	PR5A	2	RDQ8	T
C22	NC	-			PR4A	2	RDQ8	T (LVDS)*
-	-	-			GNDIO	-		
D19	PR2B	2	VREF2_2	C (LVDS)*	PR2B	2	VREF2_2	C (LVDS)*
E19	PR2A	2	VREF1_2	T (LVDS)*	PR2A	2	VREF1_2	T (LVDS)*
B21	PT55B	1	VREF2_1	C	PT64B	1	VREF2_1	C
B22	PT55A	1	VREF1_1	T	PT64A	1	VREF1_1	T
GNDIO	GNDIO1	-			GNDIO1	-		
D18	PT53B	1		C	PT62B	1		C
C20	PT54B	1		C	PT63B	1		C
E18	PT53A	1		T	PT62A	1		T
C19	PT54A	1		T	PT63A	1		T
VCCIO	VCCIO1	1			VCCIO1	1		
D17	PT51B	1		C	PT60B	1		C
B20	PT52B	1		C	PT61B	1		C
C18	PT51A	1		T	PT60A	1		T
A19	PT52A	1		T	PT61A	1		T
GNDIO	GNDIO1	-			GNDIO1	-		
A18	PT49B	1		C	PT58B	1		C
A21	PT50B	1		C	PT59B	1		C
B18	PT49A	1		T	PT58A	1		T
A20	PT50A	1		T	PT59A	1		T
VCCIO	VCCIO1	1			VCCIO1	1		
D16	PT47B	1		C	PT56B	1		C
G16	PT48B	1		C	PT57B	1		C
E16	PT47A	1		T	PT56A	1		T
G15	PT48A	1		T	PT57A	1		T
C17	PT46B	1		C	PT55B	1		C
GNDIO	GNDIO1	-			GNDIO1	-		
C16	PT46A	1		T	PT55A	1		T
A17	PT44B	1		C	PT53B	1		C
B17	PT45B	1		C	PT54B	1		C
A16	PT44A	1		T	PT53A	1		T
VCCIO	VCCIO1	1			VCCIO1	1		
B16	PT45A	1		T	PT54A	1		T
E15	PT42B	1		C	PT51B	1		C
C15	PT43B	1		C	PT52B	1		C
F15	PT42A	1		T	PT51A	1		T
D15	PT43A	1		T	PT52A	1		T

LFE2-50E/SE and LFE2-70E/SE Logic Signal Connections: 672 fpBGA
(Cont.)

LFE2-50E/SE					LFE2-70E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential	
AA14	PB38B	5	BDQ42	C	PB47B	5	BDQ51	C	
AE10	PB39A	5	BDQ42	T	PB48A	5	BDQ51	T	
AF10	PB39B	5	BDQ42	C	PB48B	5	BDQ51	C	
W14	PB40A	5	BDQ42	T	PB49A	5	BDQ51	T	
AB13	PB40B	5	BDQ42	C	PB49B	5	BDQ51	C	
VCCIO	VCCIO5	5			VCCIO5	5			
Y14	PB41A	5	BDQ42	T	PB50A	5	BDQ51	T	
AB14	PB41B	5	BDQ42	C	PB50B	5	BDQ51	C	
GND	GNDIO5	-			GNDIO5	-			
AE11	PB42A	5	BDQS42	T	PB51A	5	BDQS51	T	
AF11	PB42B	5	BDQ42	C	PB51B	5	BDQ51	C	
AD14	PB43A	5	BDQ42	T	PB52A	5	BDQ51	T	
AA15	PB43B	5	BDQ42	C	PB52B	5	BDQ51	C	
AE12	PB44A	5	PCLKT5_0/BDQ42	T	PB53A	5	PCLKT5_0/BDQ51	T	
AF12	PB44B	5	PCLKC5_0/BDQ42	C	PB53B	5	PCLKC5_0/BDQ51	C	
VCCIO	VCCIO5	5			VCCIO5	5			
GND	GNDIO5	-			GNDIO5	-			
AD15	PB49A	4	PCLKT4_0/BDQ51	T	PB58A	4	PCLKT4_0/BDQ60	T	
VCCIO	VCCIO4	4			VCCIO4	4			
AC15	PB49B	4	PCLKC4_0/BDQ51	C	PB58B	4	PCLKC4_0/BDQ60	C	
AE13	PB50A	4	BDQ51	T	PB59A	4	BDQ60	T	
AF13	PB50B	4	BDQ51	C	PB59B	4	BDQ60	C	
AB17	PB51A	4	BDQS51	T	PB60A	4	BDQS60	T	
GND	GNDIO4	-			GNDIO4	-			
Y15	PB51B	4	BDQ51	C	PB60B	4	BDQ60	C	
AE14	PB52A	4	BDQ51	T	PB61A	4	BDQ60	T	
AF14	PB52B	4	BDQ51	C	PB61B	4	BDQ60	C	
AA16	PB53A	4	BDQ51	T	PB62A	4	BDQ60	T	
VCCIO	VCCIO4	4			VCCIO4	4			
W15	PB53B	4	BDQ51	C	PB62B	4	BDQ60	C	
AC17	PB54A	4	BDQ51	T	PB63A	4	BDQ60	T	
AB16	PB54B	4	BDQ51	C	PB63B	4	BDQ60	C	
AE15	PB55A	4	BDQ51	T	PB64A	4	BDQ60	T	
GND	GNDIO4	-			GNDIO4	-			
AF15	PB55B	4	BDQ51	C	PB64B	4	BDQ60	C	
AE16	PB56A	4	BDQ60	T	PB65A	4	BDQ69	T	
AF16	PB56B	4	BDQ60	C	PB65B	4	BDQ69	C	
Y16	PB57A	4	BDQ60	T	PB66A	4	BDQ69	T	
AB18	PB57B	4	BDQ60	C	PB66B	4	BDQ69	C	
AD17	PB58A	4	BDQ60	T	PB67A	4	BDQ69	T	
AD18	PB58B	4	BDQ60	C	PB67B	4	BDQ69	C	
VCCIO	VCCIO4	4			VCCIO4	4			
AC18	PB59A	4	BDQ60	T	PB68A	4	BDQ69	T	
AD19	PB59B	4	BDQ60	C	PB68B	4	BDQ69	C	
GND	GNDIO4	-			GNDIO4	-			
AC19	PB60A	4	BDQS60	T	PB69A	4	BDQS69	T	

LFE2-50E/SE and LFE2-70E/SE Logic Signal Connections: 672 fpBGA (Cont.)

LFE2-50E/SE					LFE2-70E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential	
U24	PR63B	3	RLM0_GPLL_C_IN_A**/RDQ67	C (LVDS)*	PR76B	3	RLM0_GPLL_C_IN_A**/RDQ80	C (LVDS)*	
U25	PR63A	3	RLM0_GPLL_T_IN_A**/RDQ67	T (LVDS)*	PR76A	3	RLM0_GPLL_T_IN_A**/RDQ80	T (LVDS)*	
R20	RLM0_PLLCAP	3			RLM0_PLLCAP	3			
P18	VCCPLL	3			VCCPLL	-			
T19	PR61B	3	RLM0_GDLLC_FB_A/RDQ58	C	PR74B	3	RLM0_GDLLC_FB_A/RDQ71	C	
U20	PR61A	3	RLM0_GDLLT_FB_A/RDQ58	T	PR74A	3	RLM0_GDLLT_FB_A/RDQ71	T	
GND	GNDIO3	-			GNDIO3	-			
T25	PR60B	3	RLM0_GDLLC_IN_A**/RDQ58	C (LVDS)*	PR73B	3	RLM0_GDLLC_IN_A**/RDQ71	C (LVDS)*	
T26	PR60A	3	RLM0_GDLLT_IN_A**/RDQ58	T (LVDS)*	PR73A	3	RLM0_GDLLT_IN_A**/RDQ71	T (LVDS)*	
T20	PR59B	3	RDQ58	C	PR72B	3	RDQ71	C	
T22	PR59A	3	RDQ58	T	PR72A	3	RDQ71	T	
VCCIO	VCCIO3	3			VCCIO3	3			
R26	PR58B	3	RDQ58	C (LVDS)*	PR71B	3	RDQ71	C (LVDS)*	
R25	PR58A	3	RDQS58	T (LVDS)*	PR71A	3	RDQS71	T (LVDS)*	
R22	PR57B	3	RDQ58	C	PR70B	3	RDQ71	C	
GND	GNDIO3	-			GNDIO3	-			
T21	PR57A	3	RDQ58	T	PR70A	3	RDQ71	T	
P26	PR56B	3	RDQ58	C (LVDS)*	PR69B	3	RDQ71	C (LVDS)*	
P25	PR56A	3	RDQ58	T (LVDS)*	PR69A	3	RDQ71	T (LVDS)*	
R24	PR55B	3	RDQ58	C	PR68B	3	RDQ71	C	
VCCIO	VCCIO3	3			VCCIO3	3			
R23	PR55A	3	RDQ58	T	PR68A	3	RDQ71	T	
P20	PR54B	3	RDQ58	C (LVDS)*	PR67B	3	RDQ71	C (LVDS)*	
R19	PR54A	3	RDQ58	T (LVDS)*	PR67A	3	RDQ71	T (LVDS)*	
P21	PR53B	3	RDQ50	C	PR66B	3	RDQ63	C	
GND	GNDIO3	-			GNDIO3	-			
P19	PR53A	3	RDQ50	T	PR66A	3	RDQ63	T	
P23	PR52B	3	RDQ50	C (LVDS)*	PR65B	3	RDQ63	C (LVDS)*	
P22	PR52A	3	RDQ50	T (LVDS)*	PR65A	3	RDQ63	T (LVDS)*	
N22	PR51B	3	RDQ50	C	PR64B	3	RDQ63	C	
VCCIO	VCCIO3	3			VCCIO3	3			
R21	PR51A	3	RDQ50	T	PR64A	3	RDQ63	T	
N26	PR50B	3	RDQ50	C (LVDS)*	PR63B	3	RDQ63	C (LVDS)*	
N25	PR50A	3	RDQS50	T (LVDS)*	PR63A	3	RDQS63	T (LVDS)*	
GND	GNDIO3	-			GNDIO3	-			
N19	PR49B	3	RDQ50	C	PR62B	3	RDQ63	C	
N20	PR49A	3	RDQ50	T	PR62A	3	RDQ63	T	
M26	PR48B	3	RDQ50	C (LVDS)*	PR61B	3	RDQ63	C (LVDS)*	
M25	PR48A	3	RDQ50	T (LVDS)*	PR61A	3	RDQ63	T (LVDS)*	
VCCIO	VCCIO3	3			VCCIO3	3			
N18	PR47B	3	VREF2_3/RDQ50	C	PR60B	3	VREF2_3/RDQ63	C	
N21	PR47A	3	VREF1_3/RDQ50	T	PR60A	3	VREF1_3/RDQ63	T	
L26	PR46B	3	PCLKC3_0/RDQ50	C (LVDS)*	PR59B	3	PCLKC3_0/RDQ63	C (LVDS)*	
L25	PR46A	3	PCLKT3_0/RDQ50	T (LVDS)*	PR59A	3	PCLKT3_0/RDQ63	T (LVDS)*	
N24	PR44B	2	PCLKC2_0/RDQ41	C	PR57B	2	PCLKC2_0/RDQ54	C	
M23	PR44A	2	PCLKT2_0/RDQ41	T	PR57A	2	PCLKT2_0/RDQ54	T	

LFE2-70E/SE Logic Signal Connections: 900 fpBGA (Cont.)

LFE2-70E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential
Y10	VCC	-		
Y11	VCC	-		
Y12	VCC	-		
Y13	VCC	-		
Y18	VCC	-		
Y19	VCC	-		
Y20	VCC	-		
J13	VCCIO0	0		
J14	VCCIO0	0		
K12	VCCIO0	0		
K13	VCCIO0	0		
K14	VCCIO0	0		
K15	VCCIO0	0		
J17	VCCIO1	1		
J18	VCCIO1	1		
J20	VCCIO1	1		
K17	VCCIO1	1		
K18	VCCIO1	1		
K20	VCCIO1	1		
L21	VCCIO2	2		
M21	VCCIO2	2		
M22	VCCIO2	2		
N21	VCCIO2	2		
N22	VCCIO2	2		
R21	VCCIO2	2		
U21	VCCIO3	3		
U22	VCCIO3	3		
V21	VCCIO3	3		
V22	VCCIO3	3		
W21	VCCIO3	3		
Y22	VCCIO3	3		
AA16	VCCIO4	4		
AA17	VCCIO4	4		
AA18	VCCIO4	4		
AA19	VCCIO4	4		
AB17	VCCIO4	4		
AB18	VCCIO4	4		
AA12	VCCIO5	5		
AA13	VCCIO5	5		
AA14	VCCIO5	5		
AB12	VCCIO5	5		
AB13	VCCIO5	5		
AB14	VCCIO5	5		

LFE2M20E/SE and LFE2M35E/SE Logic Signal Connections: 484 fpBGA (Cont.)

LFE2M20E/SE					LFE2M35E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential	
F15	NC	-			NC	-			
F14	NC	-			NC	-			
F13	NC	-			NC	-			
G12	NC	-			NC	-			
G13	NC	-			NC	-			

* Supports true LVDS. Other differential signals must be emulated with external resistors.

** These dedicated input pins can be used for GPLLs or GDLLs within the respective quadrant.

***For density migration, board design must take into account that these sysCONFIG pins are dual function for the lower density devices (ECP2M20 and ECP2M35). They can be either sysCONFIG pins or general purpose I/Os. These pins are dedicated sysCONFIG pins for the higher density devices (ECP2M50, ECP2M70 and ECP2M100).

****Due to packaging bond out option, this DQS does not have all the necessary DQ pins bonded out for a full 8-bit data width.

Note: VCCIO and GND pads are used to determine the average DC current drawn by I/Os between GND/VCCIO connections, or between the last GND/VCCIO in an I/O bank and the end of an I/O bank. The substrate pads listed in the Pin Table do not necessarily have a one to one connection with a package ball or pin.

LFE2M100E/SE Logic Signal Connections: 900 fpBGA (Cont.)

LFE2M100E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential
D19	PT93B	1		C
E18	PT93A	1		T
D18	PT92B	1		C
C17	PT92A	1		T
A17	PT91B	1		C
B17	PT91A	1		T
GNDIO	GNDIO1	-		
VCCIO	VCCIO1	1		
J18	PT75B	1		C
J19	PT75A	1		T
H17	PT74B	1		C
J17	PT74A	1		T
F18	PT73B	1		C
F17	PT73A	1		T
GNDIO	GNDIO1	-		
A16	PT72B	1		C
B16	PT72A	1		T
G17	PT71B	1		C
G16	PT71A	1		T
VCCIO	VCCIO1	1		
H16	PT70B	1		C
F16	PT70A	1		T
J16	PT69B	1		C
G15	PT69A	1		T
GNDIO	GNDIO1	-		
C16	PT68B	1		C
D16	PT68A	1		T
J15	PT67B	1		C
H15	PT67A	1		T
VCCIO	VCCIO1	1		
A15	PT66B	1	VREF2_1	C
B15	PT66A	1	VREF1_1	T
F15	PT65B	1	PCLKC1_0	C
E16	PT65A	1	PCLKT1_0	T
C15	PT64B	0	PCLKC0_0	C
GNDIO	GNDIO0	-		
D15	PT64A	0	PCLKT0_0	T
C14	PT63B	0	VREF2_0	C
E15	PT63A	0	VREF1_0	T
G14	PT62B	0		C
VCCIO	VCCIO0	0		
J14	PT62A	0		T
F14	PT61B	0		C

LFE2M100E/SE Logic Signal Connections: 900 fpBGA (Cont.)

LFE2M100E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential
AE23	NC	-		
AE5	NC	-		
AE6	NC	-		
AE7	NC	-		
AF20	NC	-		
AF23	NC	-		
AF5	NC	-		
AG23	NC	-		
AG26	NC	-		
D10	NC	-		
E10	NC	-		
E11	NC	-		
F10	NC	-		
F20	NC	-		
F23	NC	-		
F8	NC	-		
G10	NC	-		
G20	NC	-		
G21	NC	-		
G7	NC	-		
G8	NC	-		
G9	NC	-		
H19	NC	-		
H20	NC	-		
H21	NC	-		
H22	NC	-		
H6	NC	-		
H8	NC	-		
H9	NC	-		
J10	NC	-		
J20	NC	-		
J21	NC	-		
J9	NC	-		
K9	NC	-		
R9	NC	-		
U22	NC	-		
W9	NC	-		
N13	VCCPLL	-		
N18	VCCPLL	-		
V13	VCCPLL	-		

LFE2M70E/SE and LFE2M100E/SE Logic Signal Connections: 1152 fpBGA (Cont.)

LFE2M70E/SE				LFE2M100E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
AG23	VCCIO4	4			VCCIO4	4		
AK21	VCCIO4	4			VCCIO4	4		
AM19	VCCIO4	4			VCCIO4	4		
AM23	VCCIO4	4			VCCIO4	4		
AC14	VCCIO5	5			VCCIO5	5		
AC15	VCCIO5	5			VCCIO5	5		
AG12	VCCIO5	5			VCCIO5	5		
AG16	VCCIO5	5			VCCIO5	5		
AK14	VCCIO5	5			VCCIO5	5		
AM12	VCCIO5	5			VCCIO5	5		
AM16	VCCIO5	5			VCCIO5	5		
AA12	VCCIO6	6			VCCIO6	6		
AB3	VCCIO6	6			VCCIO6	6		
AB8	VCCIO6	6			VCCIO6	6		
AE3	VCCIO6	6			VCCIO6	6		
AE7	VCCIO6	6			VCCIO6	6		
AH3	VCCIO6	6			VCCIO6	6		
W3	VCCIO6	6			VCCIO6	6		
W8	VCCIO6	6			VCCIO6	6		
Y12	VCCIO6	6			VCCIO6	6		
G3	VCCIO7	7			VCCIO7	7		
K3	VCCIO7	7			VCCIO7	7		
K7	VCCIO7	7			VCCIO7	7		
N3	VCCIO7	7			VCCIO7	7		
N8	VCCIO7	7			VCCIO7	7		
P12	VCCIO7	7			VCCIO7	7		
R12	VCCIO7	7			VCCIO7	7		
T3	VCCIO7	7			VCCIO7	7		
T8	VCCIO7	7			VCCIO7	7		
AD28	VCCIO8	8			VCCIO8	8		
AG32	VCCIO8	8			VCCIO8	8		
AB12	VCCAUX	-			VCCAUX	-		
AB13	VCCAUX	-			VCCAUX	-		
AB22	VCCAUX	-			VCCAUX	-		
AB23	VCCAUX	-			VCCAUX	-		
AC13	VCCAUX	-			VCCAUX	-		
AC22	VCCAUX	-			VCCAUX	-		
M13	VCCAUX	-			VCCAUX	-		
M22	VCCAUX	-			VCCAUX	-		
N12	VCCAUX	-			VCCAUX	-		
N13	VCCAUX	-			VCCAUX	-		
N22	VCCAUX	-			VCCAUX	-		
N23	VCCAUX	-			VCCAUX	-		
A1	GND	-			GND	-		
A10	GND	-			GND	-		
A13	GND	-			GND	-		
A22	GND	-			GND	-		
A25	GND	-			GND	-		
A34	GND	-			GND	-		

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2-35E-5FN484C	331	1.2V	-5	Lead-Free fpBGA	484	COM	35
LFE2-35E-6FN484C	331	1.2V	-6	Lead-Free fpBGA	484	COM	35
LFE2-35E-7FN484C	331	1.2V	-7	Lead-Free fpBGA	484	COM	35
LFE2-35E-5FN672C	450	1.2V	-5	Lead-Free fpBGA	672	COM	35
LFE2-35E-6FN672C	450	1.2V	-6	Lead-Free fpBGA	672	COM	35
LFE2-35E-7FN672C	450	1.2V	-7	Lead-Free fpBGA	672	COM	35

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2-50E-5FN484C	339	1.2V	-5	Lead-Free fpBGA	484	COM	50
LFE2-50E-6FN484C	339	1.2V	-6	Lead-Free fpBGA	484	COM	50
LFE2-50E-7FN484C	339	1.2V	-7	Lead-Free fpBGA	484	COM	50
LFE2-50E-5FN672C	500	1.2V	-5	Lead-Free fpBGA	672	COM	50
LFE2-50E-6FN672C	500	1.2V	-6	Lead-Free fpBGA	672	COM	50
LFE2-50E-7FN672C	500	1.2V	-7	Lead-Free fpBGA	672	COM	50

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2-70E-5FN672C	500	1.2V	-5	Lead-Free fpBGA	672	COM	70
LFE2-70E-6FN672C	500	1.2V	-6	Lead-Free fpBGA	672	COM	70
LFE2-70E-7FN672C	500	1.2V	-7	Lead-Free fpBGA	672	COM	70
LFE2-70E-5FN900C	583	1.2V	-5	Lead-Free fpBGA	900	COM	70
LFE2-70E-6FN900C	583	1.2V	-6	Lead-Free fpBGA	900	COM	70
LFE2-70E-7FN900C	583	1.2V	-7	Lead-Free fpBGA	900	COM	70

Industrial

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2-6E-5TN144I	90	1.2V	-5	Lead-Free TQFP	144	IND	6
LFE2-6E-6TN144I	90	1.2V	-6	Lead-Free TQFP	144	IND	6
LFE2-6E-5FN256I	190	1.2V	-5	Lead-Free fpBGA	256	IND	6
LFE2-6E-6FN256I	190	1.2V	-6	Lead-Free fpBGA	256	IND	6

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2-12E-5TN144I	93	1.2V	-5	Lead-Free TQFP	144	IND	12
LFE2-12E-6TN144I	93	1.2V	-6	Lead-Free TQFP	144	IND	12
LFE2-12E-5QN208I	131	1.2V	-5	Lead-Free PQFP	208	IND	12
LFE2-12E-6QN208I	131	1.2V	-6	Lead-Free PQFP	208	IND	12
LFE2-12E-5FN256I	193	1.2V	-5	Lead-Free fpBGA	256	IND	12
LFE2-12E-6FN256I	193	1.2V	-6	Lead-Free fpBGA	256	IND	12
LFE2-12E-5FN484I	297	1.2V	-5	Lead-Free fpBGA	484	IND	12
LFE2-12E-6FN484I	297	1.2V	-6	Lead-Free fpBGA	484	IND	12