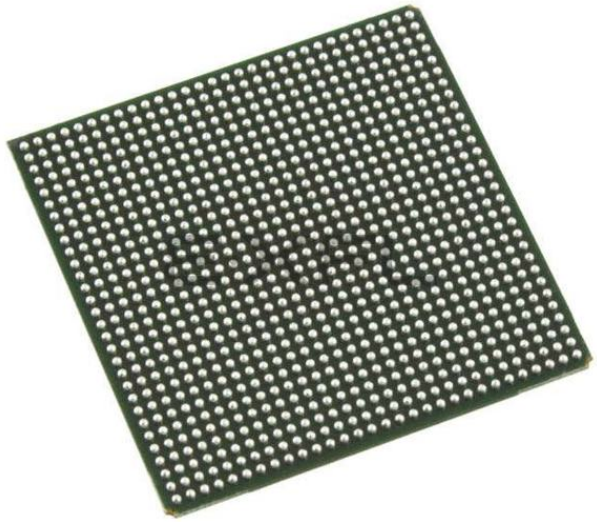
Lattice Semiconductor Corporation - LFE2M100E-6FN900I Datasheet



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Understanding Embedded - FPGAs (Field Programmable Gate Array)

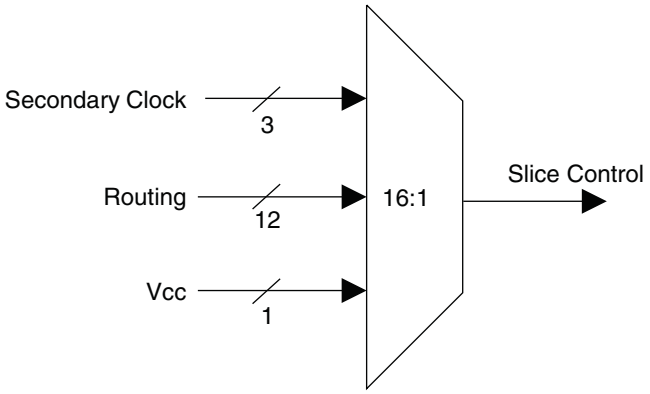
Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	11875
Number of Logic Elements/Cells	95000
Total RAM Bits	5435392
Number of I/O	416
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	900-BBGA
Supplier Device Package	900-FPBGA (31x31)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfe2m100e-6fn900i

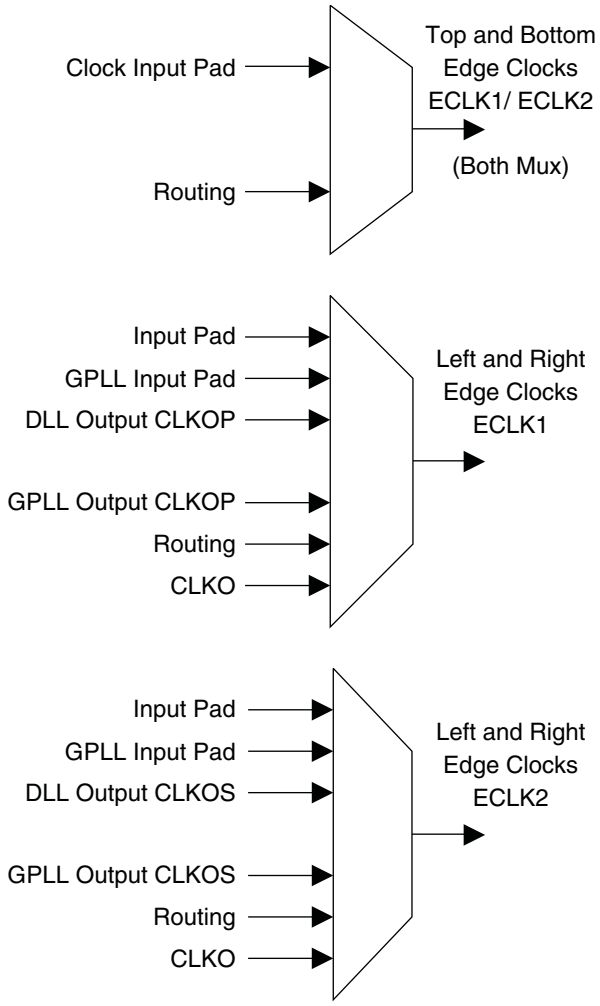
Figure 2-18. Slice0 through Slice2 Control Selection



Edge Clock Routing

LatticeECP2/M devices have a number of high-speed edge clocks that are intended for use with the PIOs in the implementation of high-speed interfaces. There are eight edge clocks per device: two edge clocks per edge. Different PLL and DLL outputs are routed to the two muxes on the left and right sides of the device. In addition, the CLKO signal (generated from the DLLDELA block) is routed to all the edge clock muxes on the left and right sides of the device. Figure 2-19 shows the selection muxes for these clocks.

Figure 2-19. Edge Clock Mux Connections



IPexpress™

The user can access the sysDSP block via the IPexpress tool, which provides the option to configure each DSP module (or group of modules) or by direct HDL instantiation. In addition, Lattice has partnered with The MathWorks® to support instantiation in the Simulink® tool, a graphical simulation environment. Simulink works with Diamond to dramatically shorten the DSP design cycle in Lattice FPGAs.

Optimized DSP Functions

Lattice provides a library of optimized DSP IP functions. Some of the IP cores planned for the LatticeECP2/M DSP include the Bit Correlator, Fast Fourier Transform, Finite Impulse Response (FIR) Filter, Reed-Solomon Encoder/Decoder, Turbo Encoder/Decoder and Convolutional Encoder/Decoder. Please contact Lattice to obtain the latest list of available DSP IP cores.

Resources Available in the LatticeECP2/M Family

Table 2-9 shows the maximum number of multipliers for each member of the LatticeECP2/M family. Table 2-10 shows the maximum available EBR RAM Blocks in each LatticeECP2/M device. EBR blocks, together with Distributed RAM can be used to store variables locally for fast DSP operations.

Table 2-9. Maximum Number of DSP Blocks in the LatticeECP2/M Family

Device	DSP Block	9x9 Multiplier	18x18 Multiplier	36x36 Multiplier
ECP2-6	3	24	12	3
ECP2-12	6	48	24	6
ECP2-20	7	56	28	7
ECP2-35	8	64	32	8
ECP2-50	18	144	72	18
ECP2-70	22	176	88	22
ECP2M20	6	48	24	6
ECP2M35	8	64	32	8
ECP2M50	22	176	88	22
ECP2M70	24	192	96	24
ECP2M100	42	336	168	42

Table 2-10. Embedded SRAM in the LatticeECP2/M Family

Device	EBR SRAM Block	Total EBR SRAM (Kbits)
ECP2-6	3	55
ECP2-12	12	221
ECP2-20	15	277
ECP2-35	18	332
ECP2-50	21	387
ECP2-70	60	1106
ECP2M20	66	1217
ECP2M35	114	2101
ECP2M50	225	4147
ECP2M70	246	4534
ECP2M100	288	5308

LatticeECP2/M DSP Performance

Table 2-11 lists the maximum performance in millions of MAC operations per second (MMAC) for each member of the LatticeECP2/M family.

Table 2-11. DSP Performance

Device	DSP Block	DSP Performance GMAC
ECP2-6	3	3.9
ECP2-12	6	7.8
ECP2-20	7	9.1
ECP2-35	8	10.4
ECP2-50	18	23.4
ECP2-70	22	28.6
ECP2M20	6	7.8
ECP2M35	8	10.4
ECP2M50	22	28.6
ECP2M70	24	31.2
ECP2M100	42	54.6

For further information about the sysDSP block, please see the list of additional technical information at the end of this data sheet.

Programmable I/O Cells (PIC)

Each PIC contains two PIOs connected to their respective sysI/O buffers as shown in Figure 2-28. The PIO Block supplies the output data (DO) and the tri-state control signal (TO) to the sysI/O buffer and receives input from the buffer. Table 2-12 provides the PIO signal list.

sets of single-ended input buffers (both ratioed and referenced). One of the referenced input buffers can also be configured as a differential input.

The two pads in the pair are described as “true” and “comp”, where the true pad is associated with the positive side of the differential input buffer and the comp (complementary) pad is associated with the negative side of the differential input buffer.

3. **Left and Right (Banks 2, 3, 6 and 7) sysI/O Buffer Pairs (50% Differential and 100% Single-Ended Outputs)**
   The sysI/O buffer pairs in the left and right banks of the device consist of two single-ended output drivers, two sets of single-ended input buffers (both ratioed and referenced) and one differential output driver. One of the referenced input buffers can also be configured as a differential input. In these banks the two pads in the pair are described as “true” and “comp”, where the true pad is associated with the positive side of the differential I/O, and the comp (complementary) pad is associated with the negative side of the differential I/O.

   LVDS differential output drivers are available on 50% of the buffer pairs on the left and right banks.

4. **Bank 8 sysI/O Buffer Pairs (Single-Ended Outputs, Only on Shared Pins When Not Used by Configuration)**
   The sysI/O buffers in Bank 8 consist of single-ended output drivers and single-ended input buffers (both ratioed and referenced). The referenced input buffer can also be configured as a differential input.

   The two pads in the pair are described as “true” and “comp”, where the true pad is associated with the positive side of the differential input buffer and the comp (complementary) pad is associated with the negative side of the differential input buffer.

In LatticeECP2 devices, only the I/Os on the bottom banks have programmable PCI clamps. In LatticeECP2M devices, the I/Os on the left and bottom banks have programmable PCI clamps.

Typical sysI/O I/O Behavior During Power-up

The internal power-on-reset (POR) signal is deactivated when V_{CC}, V_{CCIO8} and V_{CCAUX} have reached satisfactory levels. After the POR signal is deactivated, the FPGA core logic becomes active. It is the user’s responsibility to ensure that all other V_{CCIO} banks are active with valid input logic levels to properly control the output logic states of all the I/O banks that are critical to the application. For more information about controlling the output logic state with valid input logic levels during power-up in LatticeECP2/M devices, see the list of additional technical documentation at the end of this data sheet.

The V_{CC} and V_{CCAUX} supply the power to the FPGA core fabric, whereas the V_{CCIO} supplies power to the I/O buffers. In order to simplify system design while providing consistent and predictable I/O behavior, it is recommended that the I/O buffers be powered-up prior to the FPGA core fabric. V_{CCIO} supplies should be powered-up before or together with the V_{CC} and V_{CCAUX} supplies.

Prior to and throughout programming of the FPGA, the I/O of the device have a weak-pullup resistor to V_{CCIO} on the input buffer and the output buffer is tri-stated. A pullup to V_{CCIO} is present on the input until the user programs the input differently in the FPGA design. See the DC Electrical Characteristics table of this data sheet. The pullup value will be between 20-30K ohms based on the V_{CCIO} voltage supplied on the board. This pullup will also remain active if the design does not use a particular I/O.

Supported sysI/O Standards

The LatticeECP2/M sysI/O buffer supports both single-ended and differential standards. Single-ended standards can be further subdivided into LVCMOS, LVTTL and other standards. The buffers support the LVTTL, LVCMOS 1.2V, 1.5V, 1.8V, 2.5V and 3.3V standards. In the LVCMOS and LVTTL modes, the buffer has individual configuration options for drive strength, bus maintenance (weak pull-up, weak pull-down, or a bus-keeper latch) and open drain. Other single-ended standards supported include SSTL and HSTL. Differential standards supported include LVDS, MLVDS, BLVDS, LVPECL, RSDS, differential SSTL and differential HSTL. Tables 2-13 and 2-14 show the I/

LatticeECP2M Supply Current (Standby)[1, 2, 3, 4]

Over Recommended Operating Conditions

Symbol	Parameter	Device	Typ.[5]	Units
I_{CC}	Core Power Supply Current	ECP2M20	25	mA
		ECP2M35	50	mA
		ECP2M50	85	mA
		ECP2M70	100	mA
		ECP2M100	100	mA
I_{CCAUX}	Auxiliary Power Supply Current	ECP2M20	24	mA
		ECP2M35	24	mA
		ECP2M50	24	mA
		ECP2M70	24	mA
		ECP2M100	24	mA
I_{CCGPLL}	GPLL Power Supply Current (per GPLL)	All Devices	0.5	mA
I_{CCSPLL}	GPLL Power Supply Current (per SPLL)	All Devices	0.5	mA
I_{CCIO}	Bank Power Supply Current (Per Bank)	ECP2M20	2	mA
		ECP2M35	2	mA
		ECP2M50	2	mA
		ECP2M70	2	mA
		ECP2M100	2	mA
I_{CCJ}	V_{CCJ} Power Supply Current	All Devices	3	mA

1. For further information about supply current, please see the list of additional technical documentation at the end of this data sheet.
2. Assumes all outputs are tristated, all inputs are configured as LVCMOS and held at the V_{CCIO} or GND.
3. Frequency 0MHz.
4. Pattern represents a “blank” configuration data file.
5. T_J = 25°C, power supplies at normal voltage.

RSDS

The LatticeECP2/M devices support differential RSDS standard. This standard is emulated using complementary LVCMOS outputs in conjunction with a parallel resistor across the driver outputs. The RSDS input standard is supported by the LVDS differential input buffer. The scheme shown in Figure 3-4 is one possible solution for RSDS standard implementation. Resistor values in Figure 3-4 are industry standard values for 1% resistors.

Figure 3-4. RSDS (Reduced Swing Differential Signaling)

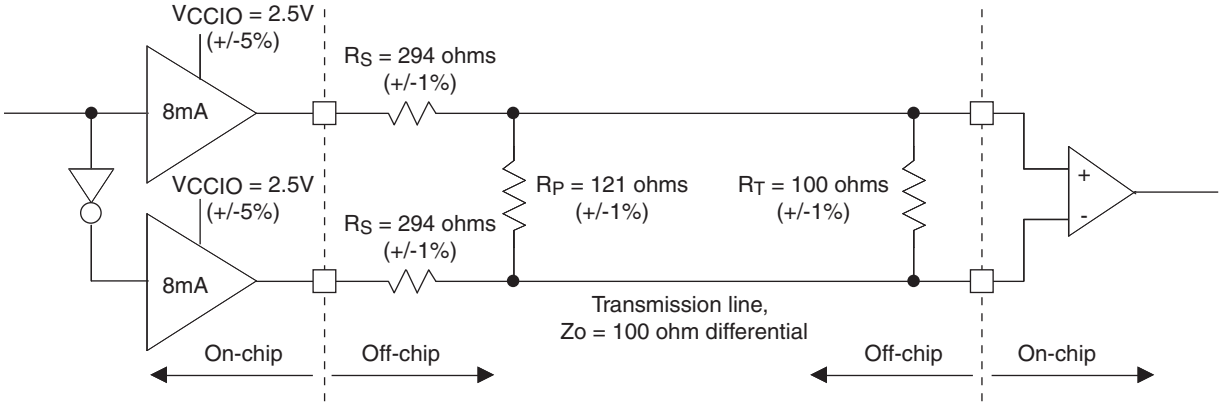


Table 3-5. RSDS DC Conditions[1]

Over Recommended Operating Conditions

Parameter	Description	Typical	Units
V_{CCIO}	Output Driver Supply (+/-5%)	2.50	V
Z_{OUT}	Driver Impedance	20	Ω
R_S	Driver Series Resistor (+/-1%)	294	Ω
R_P	Driver Parallel Resistor (+/-1%)	121	Ω
R_T	Receiver Termination (+/-1%)	100	Ω
V_{OH}	Output High Voltage	1.35	V
V_{OL}	Output Low Voltage	1.15	V
V_{OD}	Output Differential Voltage	0.20	V
V_{CM}	Output Common Mode Voltage	1.25	V
Z_{BACK}	Back Impedance	101.5	Ω
I_{DC}	DC Output Current	3.66	mA

1. For input buffer, see LVDS table.

LFE2-6E/SE and LFE2-12E/SE Logic Signal Connections: 256 fpBGA (Cont.)

LFE2-6E/SE					LFE2-12E/SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
F15	PR11B	2	RDQ10	C	PR11B	2	RDQ10	C
G11	PR12B	2	RDQ10	C (LVDS)*	PR12B	2	RDQ10	C (LVDS)*
F14	PR11A	2	RDQ10	T	PR11A	2	RDQ10	T
VCCIO	VCCIO2	2			VCCIO2	2		
F12	PR12A	2	RDQ10	T (LVDS)*	PR12A	2	RDQ10	T (LVDS)*
G14	PR10B	2	RDQ10	C (LVDS)*	PR10B	2	RDQ10	C (LVDS)*
G13	PR10A	2	RDQS10	T (LVDS)*	PR10A	2	RDQS10	T (LVDS)*
GND	GNDIO2	-			GNDIO2	-		
F16	PR8B	2	RDQ10	C (LVDS)*	PR8B	2	RDQ10	C (LVDS)*
F9	PR9B	2	RDQ10	C	PR9B	2	RDQ10	C
E16	PR8A	2	RDQ10	T (LVDS)*	PR8A	2	RDQ10	T (LVDS)*
F10	PR9A	2	RDQ10	T	PR9A	2	RDQ10	T
VCCIO	VCCIO2	2			VCCIO2	2		
D16	PR7B	2	RDQ10	C	PR7B	2	RDQ10	C
D15	PR7A	2	RDQ10	T	PR7A	2	RDQ10	T
C15	PR4B	2		C (LVDS)*	PR4B	2		C (LVDS)*
C16	PR5B	2		C	PR5B	2		C
GND	GNDIO2	-			GNDIO2	-		
D14	PR4A	2		T (LVDS)*	PR4A	2		T (LVDS)*
B16	PR5A	2		T	PR5A	2		T
F13	PR2B	2	VREF2_2	C (LVDS)*	PR2B	2	VREF2_2	C (LVDS)*
VCCIO	VCCIO2	2			VCCIO2	2		
E13	PR2A	2	VREF1_2	T (LVDS)*	PR2A	2	VREF1_2	T (LVDS)*
F11	PT28B	1	VREF2_1	C	PT55B	1	VREF2_1	C
E11	PT28A	1	VREF1_1	T	PT55A	1	VREF1_1	T
GND	GNDIO1	-			GNDIO1	-		
A15	PT27B	1		C	PT54B	1		C
E12	PT26B	1		C	PT53B	1		C
B15	PT27A	1		T	PT54A	1		T
VCCIO	VCCIO1	1			VCCIO1	1		
D12	PT26A	1		T	PT53A	1		T
B14	PT25B	1		C	PT52B	1		C
C14	PT24B	1		C	PT51B	1		C
A14	PT25A	1		T	PT52A	1		T
D13	PT24A	1		T	PT51A	1		T
C13	PT23B	1		C	PT50B	1		C
GND	GNDIO1	-			GNDIO1	-		
A13	PT22B	1		C	PT49B	1		C
B13	PT23A	1		T	PT50A	1		T
VCCIO	VCCIO1	1			VCCIO1	1		
A12	PT22A	1		T	PT49A	1		T
B11	PT21B	1		C	PT48B	1		C
D11	PT20B	1		C	PT47B	1		C
A11	PT21A	1		T	PT48A	1		T
C11	PT20A	1		T	PT47A	1		T

LFE2-20E/SE Logic Signal Connections: 256 fpBGA (Cont.)

LFE2-20E/SE					
Ball Number	Ball Number	Ball/Pad Function	Bank	Dual Function	Differential
A5	A5	PT36B	0		C
A3	A3	PT35B	0		C
A4	A4	PT36A	0		T
VCCIO	VCCIO	VCCIO0	0		
B3	B3	PT35A	0		T
A2	A2	PT34B	0		C
C7	C7	PT33B	0		C
B2	B2	PT34A	0		T
D7	D7	PT33A	0		T
D6	D6	PT32B	0		C
GND	GND	GNDIO0	-		
F7	F7	PT31B	0		C
C6	C6	PT32A	0		T
VCCIO	VCCIO	VCCIO0	0		
F6	F6	PT31A	0		T
C4	C4	PT30B	0		C
B4	B4	PT30A	0		T
-	GND	GNDIO0	0		
-	VCC	VCCIO	0		
D5	D5	PT2B	0	VREF2_0	C
E5	E5	PT2A	0	VREF1_0	T
G7	G7	VCC	-		
G9	G9	VCC	-		
H7	H7	VCC	-		
J10	J10	VCC	-		
K10	K10	VCC	-		
K8	K8	VCC	-		
G8	G8	VCCAUX	-		
H10	H10	VCCAUX	-		
J7	J7	VCCAUX	-		
K9	K9	VCCAUX	-		
C5	C5	VCCIO0	0		
E7	E7	VCCIO0	0		
C12	C12	VCCIO1	1		
E10	E10	VCCIO1	1		
E14	E14	VCCIO2	2		
G12	G12	VCCIO2	2		
K12	K12	VCCIO3	3		
M14	M14	VCCIO3	3		
M10	M10	VCCIO4	4		
P12	P12	VCCIO4	4		
M7	M7	VCCIO5	5		

LFE2-12E/SE and LFE2-20E/SE Logic Signal Connections: 484 fpBGA (Cont.)

LFE2-12E/12SE					LFE2-20E/20SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
T7	PL29B	6	LDQ28	C	PL43B	6	LDQ42	C
T6	PL26B	6	LDQ28	C (LVDS)*	PL40B	6	LDQ42	C (LVDS)*
AA2	PL31A	6	LDQ28	T	PL45A	6	LDQ42	T
VCCIO	VCCIO6	6			VCCIO6	6		
Y1	PL28A	6	LDQS28	T (LVDS)*	PL42A	6	LDQS42	T (LVDS)*
AA1	PL31B	6	LDQ28	C	PL45B	6	LDQ42	C
W1	PL28B	6	LDQ28	C (LVDS)*	PL42B	6	LDQ42	C (LVDS)*
V3	PL30B	6	LDQ28	C (LVDS)*	PL44B	6	LDQ42	C (LVDS)*
GNDIO	GNDIO6	-			GNDIO	-		
V4	PL30A	6	LDQ28	T (LVDS)*	PL44A	6	LDQ42	T (LVDS)*
U5	TDI	-			TDI	-		
U7	TCK	-			TCK	-		
V6	TDO	-			TDO	-		
V5	TMS	-			TMS	-		
T8	VCCJ	-			VCCJ	-		
W4	PB3A	5	BDQ6	T	PB3A	5	BDQ6	T
Y3	PB2A	5	VREF2_5/BDQ6	T	PB2A	5	VREF2_5/BDQ6	T
W3	PB3B	5	BDQ6	C	PB3B	5	BDQ6	C
Y2	PB2B	5	VREF1_5/BDQ6	C	PB2B	5	VREF1_5/BDQ6	C
AB3	PB5A	5	BDQ6	T	PB5A	5	BDQ6	T
VCCIO	VCCIO5	5			VCCIO5	5		
W5	PB4A	5	BDQ6	T	PB4A	5	BDQ6	T
AB2	PB5B	5	BDQ6	C	PB5B	5	BDQ6	C
W6	PB4B	5	BDQ6	C	PB4B	5	BDQ6	C
AB5	PB7A	5	BDQ6	T	PB7A	5	BDQ6	T
GNDIO	GNDIO5	-			GNDIO	-		
Y4	PB6A	5	BDQS6	T	PB6A	5	BDQS6	T
AB4	PB7B	5	BDQ6	C	PB7B	5	BDQ6	C
AA3	PB6B	5	BDQ6	C	PB6B	5	BDQ6	C
AB6	PB9A	5	BDQ6	T	PB9A	5	BDQ6	T
VCCIO	VCCIO5	5			VCCIO5	5		
AA5	PB8A	5	BDQ6	T	PB8A	5	BDQ6	T
AA6	PB9B	5	BDQ6	C	PB9B	5	BDQ6	C
Y5	PB8B	5	BDQ6	C	PB8B	5	BDQ6	C
GNDIO	GNDIO5	-			GNDIO	-		
-	-	-			VCCIO5	5		
Y6	PB12A	5	BDQ15	T	PB21A	5	BDQ24	T
W7	PB11A	5	BDQ15	T	PB20A	5	BDQ24	T
Y7	PB12B	5	BDQ15	C	PB21B	5	BDQ24	C
W8	PB11B	5	BDQ15	C	PB20B	5	BDQ24	C
U8	PB14A	5	BDQ15	T	PB23A	5	BDQ24	T
VCCIO	VCCIO5	5			VCCIO5	5		
AA7	PB13A	5	BDQ15	T	PB22A	5	BDQ24	T
U9	PB14B	5	BDQ15	C	PB23B	5	BDQ24	C

LFE2-12E/SE and LFE2-20E/SE Logic Signal Connections: 484 fpBGA (Cont.)

LFE2-12E/12SE					LFE2-20E/20SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
R8	VCCIO6	6			VCCIO6	6		
J8	VCCIO7	7			VCCIO7	7		
K7	VCCIO7	7			VCCIO7	7		
L7	VCCIO7	7			VCCIO7	7		
M7	VCCIO7	7			VCCIO7	7		
P15	VCCIO8	8			VCCIO8	8		
R15	VCCIO8	8			VCCIO8	8		
C5	VCCAUX	-			VCCAUX	-		
D11	VCCAUX	-			VCCAUX	-		
E17	VCCAUX	-			VCCAUX	-		
E6	VCCAUX	-			VCCAUX	-		
F13	VCCAUX	-			VCCAUX	-		
G18	VCCAUX	-			VCCAUX	-		
G5	VCCAUX	-			VCCAUX	-		
K5	VCCAUX	-			VCCAUX	-		
M17	VCCAUX	-			VCCAUX	-		
P17	VCCAUX	-			VCCAUX	-		
R5	VCCAUX	-			VCCAUX	-		
V11	VCCAUX	-			VCCAUX	-		
V13	VCCAUX	-			VCCAUX	-		
V15	VCCAUX	-			VCCAUX	-		
V7	VCCAUX	-			VCCAUX	-		
V8	VCCAUX	-			VCCAUX	-		
A1	GND	-			GND	-		
A22	GND	-			GND	-		
AA19	GND	-			GND	-		
AA4	GND	-			GND	-		
AB1	GND	-			GND	-		
AB22	GND	-			GND	-		
B19	GND	-			GND	-		
B4	GND	-			GND	-		
C14	GND	-			GND	-		
C9	GND	-			GND	-		
D2	GND	-			GND	-		
D21	GND	-			GND	-		
F17	GND	-			GND	-		
F6	GND	-			GND	-		
H10	GND	-			GND	-		
H11	GND	-			GND	-		
H12	GND	-			GND	-		
H13	GND	-			GND	-		
J14	GND	-			GND	-		
J20	GND	-			GND	-		
J3	GND	-			GND	-		

LFE2-12E/SE and LFE2-20E/SE Logic Signal Connections: 484 fpBGA (Cont.)

LFE2-12E/12SE					LFE2-20E/20SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
J9	GND	-			GND	-		
K10	GND	-			GND	-		
K11	GND	-			GND	-		
K12	GND	-			GND	-		
K13	GND	-			GND	-		
K15	GND	-			GND	-		
K8	GND	-			GND	-		
L10	GND	-			GND	-		
L11	GND	-			GND	-		
L12	GND	-			GND	-		
L13	GND	-			GND	-		
L15	GND	-			GND	-		
L8	GND	-			GND	-		
M10	GND	-			GND	-		
M11	GND	-			GND	-		
M12	GND	-			GND	-		
M13	GND	-			GND	-		
M15	GND	-			GND	-		
M8	GND	-			GND	-		
N10	GND	-			GND	-		
N11	GND	-			GND	-		
N12	GND	-			GND	-		
N13	GND	-			GND	-		
N15	GND	-			GND	-		
N8	GND	-			GND	-		
P14	GND	-			GND	-		
P20	GND	-			GND	-		
P3	GND	-			GND	-		
P9	GND	-			GND	-		
R10	GND	-			GND	-		
R11	GND	-			GND	-		
R12	GND	-			GND	-		
R13	GND	-			GND	-		
U17	GND	-			GND	-		
U6	GND	-			GND	-		
W2	GND	-			GND	-		
W21	GND	-			GND	-		
Y14	GND	-			GND	-		
Y9	GND	-			GND	-		
H6	NC	-			NC	-		
J6	NC	-			NC	-		
H3	NC	-			NC	-		
H2	NC	-			NC	-		
H17	NC	-			NC	-		

LFE2-20E/SE and LFE2-35E/SE Logic Signal Connections: 672 fpBGA (Cont.)

LFE2-20E/20SE					LFE2-35E/35SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
C20	PT57B	1		C	PT66B	1		C
D20	PT57A	1		T	PT66A	1		T
A22	PT56B	1		C	PT65B	1		C
A21	PT56A	1		T	PT65A	1		T
GND	GNDIO1	-			GNDIO1	-		
E19	NC	-			NC	-		
C19	NC	-			NC	-		
VCCIO	VCCIO1	1			VCCIO1	1		
B21	NC	-			NC	-		
B20	NC	-			NC	-		
D19	NC	-			NC	-		
B19	NC	-			NC	-		
GND	GNDIO1	-			GNDIO1	-		
G17	NC	-			NC	-		
E18	NC	-			NC	-		
G19	NC	-			NC	-		
F17	NC	-			NC	-		
VCCIO	VCCIO1	1			VCCIO1	1		
A20	NC	-			NC	-		
A19	NC	-			NC	-		
E17	NC	-			NC	-		
D18	NC	-			NC	-		
B18	PT55B	1		C	PT55B	1		C
GND	GNDIO1	-			GNDIO1	-		
A18	PT55A	1		T	PT55A	1		T
E16	PT54B	1		C	PT54B	1		C
G16	PT54A	1		T	PT54A	1		T
F16	PT53B	1		C	PT53B	1		C
VCCIO	VCCIO1	1			VCCIO1	1		
H18	PT53A	1		T	PT53A	1		T
A17	PT52B	1		C	PT52B	1		C
B17	PT52A	1		T	PT52A	1		T
C18	PT51B	1		C	PT51B	1		C
B16	PT51A	1		T	PT51A	1		T
C17	PT50B	1		C	PT50B	1		C
GND	GNDIO1	-			GNDIO1	-		
D17	PT50A	1		T	PT50A	1		T
E15	PT49B	1		C	PT49B	1		C
VCCIO	VCCIO1	1			VCCIO1	1		
G15	PT49A	1		T	PT49A	1		T
A16	PT48B	1		C	PT48B	1		C
B15	PT48A	1		T	PT48A	1		T
D15	PT47B	1		C	PT47B	1		C
F15	PT47A	1		T	PT47A	1		T
A14	PT46B	1		C	PT46B	1		C
B14	PT46A	1		T	PT46A	1		T

LFE2-70E/SE Logic Signal Connections: 900 fpBGA (Cont.)

LFE2-70E/SE				
Ball Number	**Ball/Pad Function**	**Bank**	**Dual Function**	**Differential**
E27	NC	-		
E28	NC	-		
E29	NC	-		
E3	NC	-		
E30	NC	-		
E4	NC	-		
E5	NC	-		
E6	NC	-		
F25	NC	-		
F5	NC	-		
F6	NC	-		
G6	NC	-		
G7	NC	-		
K10	NC	-		
K9	NC	-		
N27	NC	-		
N4	NC	-		
R1	NC	-		
R2	NC	-		
V27	NC	-		
V4	NC	-		
P22	VCCPLL	-		
P8	VCCPLL	-		
T22	VCCPLL	-		
Y7	VCCPLL	-		

* Supports true LVDS. Other differential signals must be emulated with external resistors.
** These dedicated input pins can be used for GPLLs or GDLLs within the respective quadrant.
***Due to packaging bond out option, this DQS does not have all the necessary DQ pins bonded out for a full 8-bit data width.

Note: VCCIO and GND pads are used to determine the average DC current drawn by I/Os between GND/VCCIO connections, or between the last GND/VCCIO in an I/O bank and the end of an I/O bank. The substrate pads listed in the Pin Table do not necessarily have a one to one connection with a package ball or pin.

LFE2M-20E/SE and LFE2M-35E/SE Logic Signal Connections: 256 fpBGA (Cont.)

LFE2M20E/SE					LFE2M35E/SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
A7	URC_SQ_HDOUTP3	12		T	URC_SQ_HDOUTP3	12		T
C6	URC_SQ_VCCTX3	12			URC_SQ_VCCTX3	12		
B4	URC_SQ_HDINN3	12		C	URC_SQ_HDINN3	12		C
B3	URC_SQ_VCCIB3	12			URC_SQ_VCCIB3	12		
A4	URC_SQ_HDINP3	12		T	URC_SQ_HDINP3	12		T
C3	URC_SQ_VCCRX3	12			URC_SQ_VCCRX3	12		
GNDIO	GNDIO1	-			GNDIO1	-		
VCCIO	VCCIO1	1			VCCIO1	1		
GNDIO	GNDIO0	-			GNDIO0	-		
VCCIO	VCCIO0	0			VCCIO0	0		
G10	VCCPLL	-			VCCPLL	-		
G7	VCC	-			VCC	-		
G9	VCC	-			VCC	-		
H7	VCC	-			VCC	-		
J10	VCC	-			VCC	-		
K10	VCC	-			VCC	-		
K8	VCC	-			VCC	-		
E7	VCCIO0	0			VCCIO0	0		
VCCIO	VCCIO0	0			VCCIO0	0		
E10	VCCIO1	1			VCCIO1	1		
VCCIO	VCCIO1	1			VCCIO1	1		
E14	VCCIO2	2			VCCIO2	2		
G12	VCCIO2	2			VCCIO2	2		
VCCIO	VCCIO2	2			VCCIO2	2		
K12	VCCIO3	3			VCCIO3	3		
M14	VCCIO3	3			VCCIO3	3		
VCCIO	VCCIO3	3			VCCIO3	3		
M10	VCCIO4	4			VCCIO4	4		
P12	VCCIO4	4			VCCIO4	4		
VCCIO	VCCIO4	4			VCCIO4	4		
M7	VCCIO5	5			VCCIO5	5		
P5	VCCIO5	5			VCCIO5	5		
VCCIO	VCCIO5	5			VCCIO5	5		
K5	VCCIO6	6			VCCIO6	6		
M3	VCCIO6	6			VCCIO6	6		
VCCIO	VCCIO6	6			VCCIO6	6		
E3	VCCIO7	7			VCCIO7	7		
G5	VCCIO7	7			VCCIO7	7		
VCCIO	VCCIO7	7			VCCIO7	7		
T15	VCCIO8	8			VCCIO8	8		
VCCIO	VCCIO8	8			VCCIO8	8		
G8	VCCAUX	-			VCCAUX	-		
H10	VCCAUX	-			VCCAUX	-		
J7	VCCAUX	-			VCCAUX	-		
K9	VCCAUX	-			VCCAUX	-		
A1	GND	-			GND	-		
A15	GND	-			GND	-		
A16	GND	-			GND	-		

LFE2M50E/SE Logic Signal Connections: 484 fpBGA (Cont.)

LFE2M50E/SE				
Ball Number	**Ball/Pad Function**	**Bank**	**Dual Function**	**Differential**
M19	PR50A	3	RDQ52	T (LVDS)*
M18	PR49B	3	RDQ52	C
VCCIO	VCCIO3	3		
L16	PR49A	3	RDQ52	T
L22	PR48B	3	RDQ52	C (LVDS)*
L21	PR48A	3	RDQ52	T (LVDS)*
GNDIO	GNDIO3	-		
K22	PR46B	3	RLM3_SPLLC_FB_A	C
VCCIO	VCCIO3	3		
K21	PR46A	3	RLM3_SPLLT_FB_A	T
L17	PR45B	3	RLM3_SPLLC_IN_A	C (LVDS)*
L18	PR45A	3	RLM3_SPLLT_IN_A	T (LVDS)*
GNDIO	GNDIO3	-		
L20	PR44B	3		C
L19	PR44A	3		T
K16	PR43B	3		C (LVDS)*
K17	PR43A	3		T (LVDS)*
VCCIO	VCCIO3	3		
J16	PR42B	3	VREF2_3	C
K18	PR42A	3	VREF1_3	T
J22	PR41B	3	PCLKC3_0	C (LVDS)*
J21	PR41A	3	PCLKT3_0	T (LVDS)*
H22	PR39B	2	PCLKC2_0/RDQ36	C
H21	PR39A	2	PCLKT2_0/RDQ36	T
GNDIO	GNDIO2	-		
J17	PR38B	2	RDQ36	C (LVDS)*
J18	PR38A	2	RDQ36	T (LVDS)*
J20	PR37B	2	RDQ36	C
J19	PR37A	2	RDQ36	T
VCCIO	VCCIO2	2		
H16	PR36B	2	RDQ36	C (LVDS)*
H17	PR36A	2	RDQS36	T (LVDS)*
G22	PR35B	2	RDQ36	C
GNDIO	GNDIO2	-		
G21	PR35A	2	RDQ36	T
H20	PR34B	2	RDQ36	C (LVDS)*
H19	PR34A	2	RDQ36	T (LVDS)*
G16	PR33B	2	RUM3_SPLLC_FB_A/RDQ36	C
VCCIO	VCCIO2	2		
H18	PR33A	2	RUM3_SPLLT_FB_A/RDQ36	T
F22	PR32B	2	RUM3_SPLLC_IN_A/RDQ36	C (LVDS)*
F21	PR32A	2	RUM3_SPLLT_IN_A/RDQ36	T (LVDS)*
G20	PR30B	2	RDQ27	C

LFE2M50E/SE and LFE2M70E/SE Logic Signal Connections: 900 fpBGA (Cont.)

LFE2M50E/SE					LFE2M70E/SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
K13	VCCIO0	0			VCCIO0	0		
D17	VCCIO1	1			VCCIO1	1		
E22	VCCIO1	1			VCCIO1	1		
E25	VCCIO1	1			VCCIO1	1		
F19	VCCIO1	1			VCCIO1	1		
K18	VCCIO1	1			VCCIO1	1		
K19	VCCIO1	1			VCCIO1	1		
F28	VCCIO2	2			VCCIO2	2		
J25	VCCIO2	2			VCCIO2	2		
K28	VCCIO2	2			VCCIO2	2		
M21	VCCIO2	2			VCCIO2	2		
M24	VCCIO2	2			VCCIO2	2		
N21	VCCIO2	2			VCCIO2	2		
N28	VCCIO2	2			VCCIO2	2		
P21	VCCIO2	2			VCCIO2	2		
R25	VCCIO2	2			VCCIO2	2		
AA28	VCCIO3	3			VCCIO3	3		
AB25	VCCIO3	3			VCCIO3	3		
AE28	VCCIO3	3			VCCIO3	3		
T25	VCCIO3	3			VCCIO3	3		
U21	VCCIO3	3			VCCIO3	3		
V21	VCCIO3	3			VCCIO3	3		
V28	VCCIO3	3			VCCIO3	3		
W21	VCCIO3	3			VCCIO3	3		
W24	VCCIO3	3			VCCIO3	3		
AA18	VCCIO4	4			VCCIO4	4		
AA19	VCCIO4	4			VCCIO4	4		
AE19	VCCIO4	4			VCCIO4	4		
AF22	VCCIO4	4			VCCIO4	4		
AG17	VCCIO4	4			VCCIO4	4		
AG25	VCCIO4	4			VCCIO4	4		
AA12	VCCIO5	5			VCCIO5	5		
AA13	VCCIO5	5			VCCIO5	5		
AE12	VCCIO5	5			VCCIO5	5		
AF9	VCCIO5	5			VCCIO5	5		
AG14	VCCIO5	5			VCCIO5	5		
AG6	VCCIO5	5			VCCIO5	5		
AA3	VCCIO6	6			VCCIO6	6		
AB6	VCCIO6	6			VCCIO6	6		
AE3	VCCIO6	6			VCCIO6	6		
T6	VCCIO6	6			VCCIO6	6		
U10	VCCIO6	6			VCCIO6	6		
V10	VCCIO6	6			VCCIO6	6		
V3	VCCIO6	6			VCCIO6	6		
W10	VCCIO6	6			VCCIO6	6		
W7	VCCIO6	6			VCCIO6	6		
F3	VCCIO7	7			VCCIO7	7		
J6	VCCIO7	7			VCCIO7	7		

LFE2M100E/SE Logic Signal Connections: 900 fpBGA (Cont.)

LFE2M100E/SE				
Ball Number	**Ball/Pad Function**	**Bank**	**Dual Function**	**Differential**
AJ2	LLC_SQ_HDINN3	14		C
AH4	LLC_SQ_VCCTX3	14		
AK5	LLC_SQ_HDOUTP3	14		T
AK4	LLC_SQ_VCCOB3	14		
AJ5	LLC_SQ_HDOUTN3	14		C
AH5	LLC_SQ_VCCTX2	14		
AJ6	LLC_SQ_HDOUTN2	14		C
AH6	LLC_SQ_VCCOB2	14		
AK6	LLC_SQ_HDOUTP2	14		T
AH2	LLC_SQ_VCCRX2	14		
AJ3	LLC_SQ_HDINN2	14		C
AH3	LLC_SQ_VCCIB2	14		
AK3	LLC_SQ_HDINP2	14		T
AH7	LLC_SQ_VCCP	14		
AG7	LLC_SQ_REFCLKP	14		T
AF7	LLC_SQ_REFCLKN	14		C
AJ7	LLC_SQ_VCCAUX33	14		
AK11	LLC_SQ_HDINP1	14		T
AH11	LLC_SQ_VCCIB1	14		
AJ11	LLC_SQ_HDINN1	14		C
AH12	LLC_SQ_VCCRX1	14		
AK8	LLC_SQ_HDOUTP1	14		T
AH8	LLC_SQ_VCCOB1	14		
AJ8	LLC_SQ_HDOUTN1	14		C
AH9	LLC_SQ_VCCTX1	14		
AJ9	LLC_SQ_HDOUTN0	14		C
AK10	LLC_SQ_VCCOB0	14		
AK9	LLC_SQ_HDOUTP0	14		T
AH10	LLC_SQ_VCCTX0	14		
AJ12	LLC_SQ_HDINN0	14		C
AJ13	LLC_SQ_VCCIB0	14		
AK12	LLC_SQ_HDINP0	14		T
AH13	LLC_SQ_VCCRX0	14		
AF10	PB30A	5	BDQ33	T
AE8	PB30B	5	BDQ33	C
AE11	PB31A	5	BDQ33	T
VCCIO	VCCIO5	5		
AD9	PB31B	5	BDQ33	C
AE10	PB32A	5	BDQ33	T
AD10	PB32B	5	BDQ33	C
AE13	PB33A	5	BDQS33	T
GNDIO	GNDIO5	-		
AC12	PB33B	5	BDQ33	C

LFE2M100E/SE Logic Signal Connections: 900 fpBGA (Cont.)

LFE2M100E/SE				
Ball Number	**Ball/Pad Function**	**Bank**	**Dual Function**	**Differential**
AB27	PR97A	3	RDQ99	T (LVDS)*
VCCIO	VCCIO3	3		
Y24	PR96B	3	RDQ99	C
Y25	PR96A	3	RDQ99	T
AA29	PR95B	3	RDQ99	C (LVDS)*
Y28	PR95A	3	RDQ99	T (LVDS)*
Y30	PR93B	3	RDQ90	C
Y29	PR93A	3	RDQ90	T
GNDIO	GNDIO3	-		
VCCIO	VCCIO3	3		
W22	PR83B	3	RDQ81	C (LVDS)*
V22	PR83A	3	RDQ81	T (LVDS)*
Y27	PR82B	3	RDQ81	C
VCCIO	VCCIO3	3		
Y26	PR82A	3	RDQ81	T
W30	PR81B	3	RDQ81	C (LVDS)*
W29	PR81A	3	RDQS81	T (LVDS)*
GNDIO	GNDIO3	-		
W25	PR80B	3	RDQ81	C
W26	PR80A	3	RDQ81	T
U29	PR79B	3	RDQ81	C (LVDS)*
V29	PR79A	3	RDQ81	T (LVDS)*
VCCIO	VCCIO3	3		
V30	PR78B	3	RDQ81	C
U30	PR78A	3	RDQ81	T
W27	PR77B	3	RDQ81	C (LVDS)*
W28	PR77A	3	RDQ81	T (LVDS)*
V24	PR75B	3	RDQ72	C
V25	PR75A	3	RDQ72	T
GNDIO	GNDIO3	-		
U28	PR74B	3	RDQ72	C (LVDS)*
U27	PR74A	3	RDQ72	T (LVDS)*
U23	PR73B	3	RDQ72	C
V23	PR73A	3	RDQ72	T
VCCIO	VCCIO3	3		
V26	PR72B	3	RDQ72	C (LVDS)*
U26	PR72A	3	RDQS72	T (LVDS)*
U25	PR71B	3	RDQ72	C
GNDIO	GNDIO3	-		
U24	PR71A	3	RDQ72	T
T30	PR70B	3	RDQ72	C (LVDS)*
R30	PR70A	3	RDQ72	T (LVDS)*
T23	PR69B	3	RDQ72	C

LFE2M70E/SE and LFE2M100E/SE Logic Signal Connections: 1152 fpBGA (Cont.)

LFE2M70E/SE				LFE2M100E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
GNDIO	GNDIO5	-			GNDIO5	-		
AE16	PB42B	5	BDQ42	C	PB51B	5	BDQ51	C
AF15	PB44A	5	BDQ42	T	PB53A	5	BDQ51	T
VCCIO	VCCIO5	5			VCCIO5	5		
AD16	PB44B	5	BDQ42	C	PB53B	5	BDQ51	C
AK17	PB45A	5	BDQ42	T	PB54A	5	BDQ51	T
AH16	PB45B	5	BDQ42	C	PB54B	5	BDQ51	C
AN16	PB46A	5	BDQ42	T	PB55A	5	BDQ51	T
GNDIO	GNDIO5	-			GNDIO5	-		
AP16	PB46B	5	BDQ42	C	PB55B	5	BDQ51	C
AL17	PB47A	5	BDQ51	T	PB56A	5	BDQ60	T
AM17	PB47B	5	BDQ51	C	PB56B	5	BDQ60	C
AN17	PB48A	5	BDQ51	T	PB57A	5	BDQ60	T
AP17	PB48B	5	BDQ51	C	PB57B	5	BDQ60	C
AD17	PB49A	5	BDQ51	T	PB58A	5	BDQ60	T
AE17	PB49B	5	BDQ51	C	PB58B	5	BDQ60	C
VCCIO	VCCIO5	5			VCCIO5	5		
AL18	PB50A	5	BDQ51	T	PB59A	5	BDQ60	T
AM18	PB50B	5	BDQ51	C	PB59B	5	BDQ60	C
GNDIO	GNDIO5	-			GNDIO5	-		
AP18	PB51A	5	BDQS51	T	PB60A	5	BDQS60	T
AN18	PB51B	5	BDQ51	C	PB60B	5	BDQ60	C
AG17	PB52A	5	VREF2_5/BDQ51	T	PB61A	5	VREF2_5/BDQ60	T
AJ17	PB52B	5	VREF1_5/BDQ51	C	PB61B	5	VREF1_5/BDQ60	C
AF17	PB53A	5	PCLKT5_0/BDQ51	T	PB62A	5	PCLKT5_0/BDQ60	T
AH17	PB53B	5	PCLKC5_0/BDQ51	C	PB62B	5	PCLKC5_0/BDQ60	C
VCCIO	VCCIO5	5			VCCIO5	5		
GNDIO	GNDIO5	-			GNDIO5	-		
AF18	PB58A	4	PCLKT4_0/BDQ60	T	PB67A	4	PCLKT4_0/BDQ69	T
VCCIO	VCCIO4	4			VCCIO4	4		
AD18	PB58B	4	PCLKC4_0/BDQ60	C	PB67B	4	PCLKC4_0/BDQ69	C
AP19	PB59A	4	VREF2_4/BDQ60	T	PB68A	4	VREF2_4/BDQ69	T
AN19	PB59B	4	VREF1_4/BDQ60	C	PB68B	4	VREF1_4/BDQ69	C
AP20	PB60A	4	BDQS60	T	PB69A	4	BDQS69	T
GNDIO	GNDIO4	-			GNDIO4	-		
AM20	PB60B	4	BDQ60	C	PB69B	4	BDQ69	C
AN20	PB61A	4	BDQ60	T	PB70A	4	BDQ69	T
AM21	PB61B	4	BDQ60	C	PB70B	4	BDQ69	C
AG18	PB62A	4	BDQ60	T	PB71A	4	BDQ69	T
VCCIO	VCCIO4	4			VCCIO4	4		
AE18	PB62B	4	BDQ60	C	PB71B	4	BDQ69	C
AJ18	PB63A	4	BDQ60	T	PB72A	4	BDQ69	T
AH18	PB63B	4	BDQ60	C	PB72B	4	BDQ69	C
AK18	PB64A	4	BDQ60	T	PB73A	4	BDQ69	T
GNDIO	GNDIO4	-			GNDIO4	-		
AK19	PB64B	4	BDQ60	C	PB73B	4	BDQ69	C
AP21	PB65A	4	BDQ69	T	PB74A	4	BDQ78	T
AN21	PB65B	4	BDQ69	C	PB74B	4	BDQ78	C
AL20	PB66A	4	BDQ69	T	PB75A	4	BDQ78	T

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2M100E-5FN1152I	520	1.2V	-5	Lead-Free fpBGA	1152	Ind	100
LFE2M100E-6FN1152I	520	1.2V	-6	Lead-Free fpBGA	1152	Ind	100
LFE2M100E-5FN900I	416	1.2V	-5	Lead-Free fpBGA	900	Ind	100
LFE2M100E-6FN900I	416	1.2V	-6	Lead-Free fpBGA	900	Ind	100

LatticeECP2M S-Series Devices, Conventional Packaging

Commercial

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2M20SE-5F484C	304	1.2V	-5	fpBGA	484	Com	20
LFE2M20SE-6F484C	304	1.2V	-6	fpBGA	484	Com	20
LFE2M20SE-7F484C	304	1.2V	-7	fpBGA	484	Com	20
LFE2M20SE-5F256C	140	1.2V	-5	fpBGA	256	Com	20
LFE2M20SE-6F256C	140	1.2V	-6	fpBGA	256	Com	20
LFE2M20SE-7F256C	140	1.2V	-7	fpBGA	256	Com	20

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2M35SE-5F672C	410	1.2V	-5	fpBGA	672	Com	35
LFE2M35SE-6F672C	410	1.2V	-6	fpBGA	672	Com	35
LFE2M35SE-7F672C	410	1.2V	-7	fpBGA	672	Com	35
LFE2M35SE-5F484C	303	1.2V	-5	fpBGA	484	Com	35
LFE2M35SE-6F484C	303	1.2V	-6	fpBGA	484	Com	35
LFE2M35SE-7F484C	303	1.2V	-7	fpBGA	484	Com	35
LFE2M35SE-5F256C	140	1.2V	-5	fpBGA	256	Com	35
LFE2M35SE-6F256C	140	1.2V	-6	fpBGA	256	Com	35
LFE2M35SE-7F256C	140	1.2V	-7	fpBGA	256	Com	35

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2M50SE-5F900C	410	1.2V	-5	fpBGA	900	Com	50
LFE2M50SE-6F900C	410	1.2V	-6	fpBGA	900	Com	50
LFE2M50SE-7F900C	410	1.2V	-7	fpBGA	900	Com	50
LFE2M50SE-5F672C	372	1.2V	-5	fpBGA	672	Com	50
LFE2M50SE-6F672C	372	1.2V	-6	fpBGA	672	Com	50
LFE2M50SE-7F672C	372	1.2V	-7	fpBGA	672	Com	50
LFE2M50SE-5F484C	270	1.2V	-5	fpBGA	484	Com	50
LFE2M50SE-6F484C	270	1.2V	-6	fpBGA	484	Com	50
LFE2M50SE-7F484C	270	1.2V	-7	fpBGA	484	Com	50