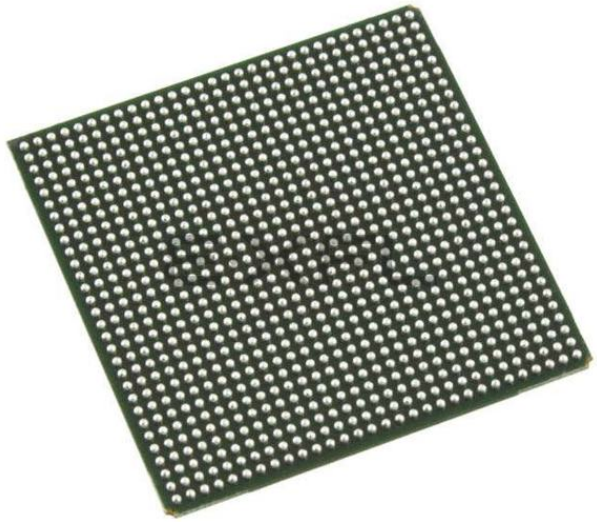
Lattice Semiconductor Corporation - LFE2M100SE-7FN900C Datasheet



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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	11875
Number of Logic Elements/Cells	95000
Total RAM Bits	5435392
Number of I/O	416
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	900-BBGA
Supplier Device Package	900-FPBGA (31x31)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfe2m100se-7fn900c

BLVDS

The LatticeECP2/M devices support the BLVDS standard. This standard is emulated using complementary LVCMOS outputs in conjunction with a parallel external resistor across the driver outputs. BLVDS is intended for use when multi-drop and bi-directional multi-point differential signaling is required. The scheme shown in Figure 3-2 is one possible solution for bi-directional multi-point differential signals.

Figure 3-2. BLVDS Multi-point Output Example

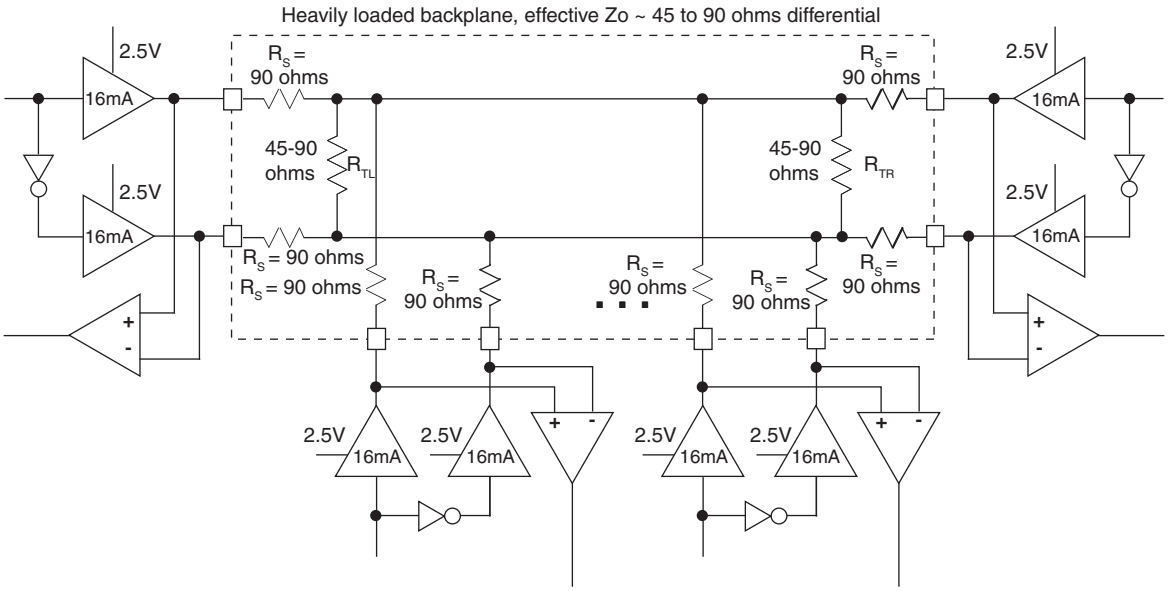


Table 3-3. BLVDS DC Conditions[1]

Over Recommended Operating Conditions

Parameter	Description	Typical		Units
		Zo = 45Ω	Zo = 90Ω	
V_{CCIO}	Output Driver Supply (+/- 5%)	2.50	2.50	V
Z_{OUT}	Driver Impedance	10.00	10.00	Ω
R_S	Driver Series Resistor (+/- 1%)	90.00	90.00	Ω
R_{TL}	Driver Parallel Resistor (+/- 1%)	45.00	90.00	Ω
R_{TR}	Receiver Termination (+/- 1%)	45.00	90.00	Ω
V_{OH}	Output High Voltage	1.38	1.48	V
V_{OL}	Output Low Voltage	1.12	1.02	V
V_{OD}	Output Differential Voltage	0.25	0.46	V
V_{CM}	Output Common Mode Voltage	1.25	1.25	V
I_{DC}	DC Output Current	11.24	10.20	mA

1. For input buffer, see LVDS table.

LatticeECP2/M Internal Switching Characteristics[1]

Over Recommended Operating Conditions

Parameter	Description	-7		-6		-5		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
PFU/PFF Logic Mode Timing								
t_{LUT4_PFU}	LUT4 delay (A to D inputs to F output)	—	0.180	—	0.198	—	0.216	ns
t_{LUT6_PFU}	LUT6 delay (A to D inputs to OFX output)	—	0.304	—	0.331	—	0.358	ns
t_{LSR_PFU}	Set/Reset to output of PFU (Asynchronous)	—	0.600	—	0.655	—	0.711	ns
t_{SUM_PFU}	Clock to Mux (M0,M1) Input Setup Time	0.128	—	0.129	—	0.129	—	ns
t_{HM_PFU}	Clock to Mux (M0,M1) Input Hold Time	-0.051	—	-0.049	—	-0.046	—	ns
t_{SUD_PFU}	Clock to D input setup time	0.061	—	0.071	—	0.081	—	ns
t_{HD_PFU}	Clock to D input hold time	0.002	—	0.003	—	0.003	—	ns
t_{CK2Q_PFU}	Clock to Q delay, (D-type Register Configuration)	—	0.285	—	0.309	—	0.333	ns
PFU Dual Port Memory Mode Timing								
t_{CORAM_PFU}	Clock to Output (F Port)	—	0.902	—	1.083	—	1.263	ns
t_{SUDATA_PFU}	Data Setup Time	-0.172	—	-0.205	—	-0.238	—	ns
t_{HDATA_PFU}	Data Hold Time	0.199	—	0.235	—	0.271	—	ns
t_{SUADDR_PFU}	Address Setup Time	-0.245	—	-0.284	—	-0.323	—	ns
t_{HADDR_PFU}	Address Hold Time	0.246	—	0.285	—	0.324	—	ns
t_{SUWREN_PFU}	Write/Read Enable Setup Time	-0.122	—	-0.145	—	-0.168	—	ns
t_{HWREN_PFU}	Write/Read Enable Hold Time	0.132	—	0.156	—	0.180	—	ns
PIC Timing								
PIO Input/Output Buffer Timing								
t_{IN_PIO}	Input Buffer Delay (LVCMOS25)	—	0.613	—	0.681	—	0.749	ns
t_{OUT_PIO}	Output Buffer Delay (LVCMOS25)	—	1.115	—	1.115	—	1.343	ns
IOLOGIC Input/Output Timing								
t_{SUI_PIO}	Input Register Setup Time (Data Before Clock)	0.596	—	0.645	—	0.694	—	ns
t_{HI_PIO}	Input Register Hold Time (Data after Clock)	-0.570	—	-0.614	—	-0.658	—	ns
t_{COO_PIO}	Output Register Clock to Output Delay	—	0.61	—	0.66	—	0.72	ns
t_{SUCE_PIO}	Input Register Clock Enable Setup Time	0.032	—	0.037	—	0.041	—	ns
t_{HCE_PIO}	Input Register Clock Enable Hold Time	-0.022	—	-0.025	—	-0.028	—	ns
t_{SULSR_PIO}	Set/Reset Setup Time	0.184	—	0.201	—	0.217	—	ns
t_{HLSR_PIO}	Set/Reset Hold Time	-0.080	—	-0.086	—	-0.093	—	ns
EBR Timing								
t_{CO_EBR}	Clock (Read) to output from Address or Data	—	2.51	—	2.75	—	2.99	ns
t_{COO_EBR}	Clock (Write) to output from EBR output Register	—	0.33	—	0.36	—	0.39	ns
t_{SUDATA_EBR}	Setup Data to EBR Memory	-0.157	—	-0.181	—	-0.205	—	ns
t_{HDATA_EBR}	Hold Data to EBR Memory	0.173	—	0.195	—	0.217	—	ns
t_{SUADDR_EBR}	Setup Address to EBR Memory	-0.115	—	-0.130	—	-0.145	—	ns
t_{HADDR_EBR}	Hold Address to EBR Memory	0.138	—	0.155	—	0.172	—	ns
t_{SUWREN_EBR}	Setup Write/Read Enable to PFU Memory	-0.128	—	-0.149	—	-0.170	—	ns

LatticeECP2/M sysCONFIG Port Timing Specifications (Continued)

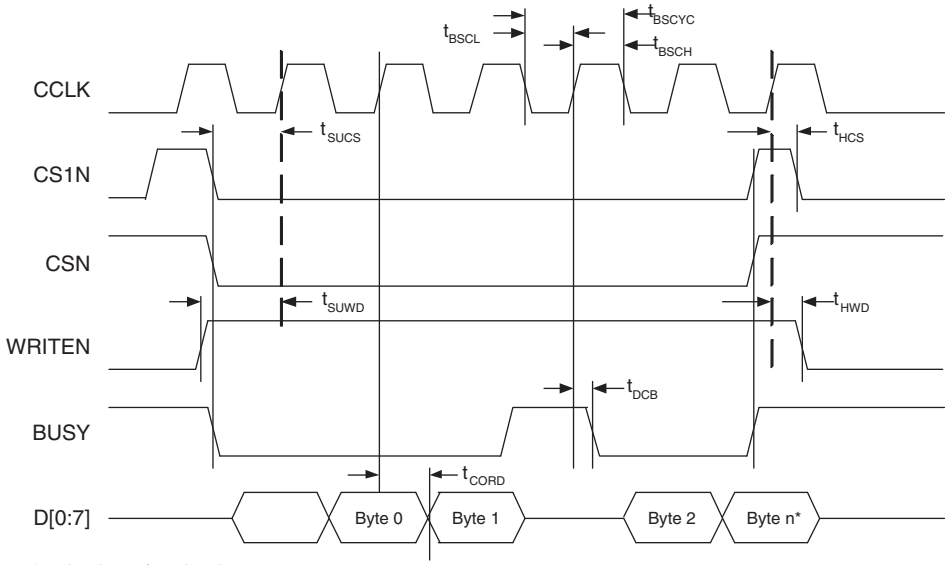
Over Recommended Operating Conditions

Parameter	Description	Min.	Max.	Units
f_{MAXSPI}	Max. CCLK Frequency - SPI Flash Read Opcode (0x03) (SPIFASTN = 1)	—	20	MHz
	Max. CCLK Frequency - SPI Flash Fast Read Opcode (0x0B) (SPIFASTN = 0)	—	50	MHz
	Max. CCLK Frequency - Encrypted Bitstream	—	10	MHz
t_{SUSPI}	SOSPI Data Setup Time Before CCLK	7	—	ns
t_{HSPI}	SOSPI Data Hold Time After CCLK	2	—	ns
t_{SUMCDI}	DI Setup to CCLK	7	—	ns
t_{HMCDI}	DI Hold from CCLK	1	—	ns

1. Re-toggling the PROGRAMN pin is not permitted until the INITN pin is high. Avoid consecutive toggling of the PROGRAMN.
2. For SED (Soft Error Detect), the SEDCLKIN operating frequency must be at least 20MHz. SEDCLKIN is derived from Master Clock Frequency that has a +/-30% variation..

Parameter	Min.	Max.	Units
Master Clock Frequency	Selected value - 30%	Selected value + 30%	MHz
Duty Cycle	40	60	%

Figure 3-14. sysCONFIG Parallel Port Read Cycle



*n = last byte of read cycle.

Signal Descriptions

Signal Name	I/O	Description
General Purpose		
P[Edge] [Row/Column Number*]_[A/B]	I/O	[Edge] indicates the edge of the device on which the pad is located. Valid edge designations are L (Left), B (Bottom), R (Right), T (Top). [Row/Column Number] indicates the PFU row or the column of the device on which the PIC exists. When Edge is T (Top) or B (Bottom), only need to specify Row Number. When Edge is L (Left) or R (Right), only need to specify Column Number. [A/B] indicates the PIO within the PIC to which the pad is connected. Some of these user-programmable pins are shared with special function pins. These pins, when not used as special purpose pins, can be programmed as I/Os for user logic. During configuration the user-programmable I/Os are tri-stated with an internal pull-up resistor enabled. If any pin is not used (or not bonded to a package pin), it is also tri-stated with an internal pull-up resistor enabled after configuration. See "Typical sysI/O I/O Behavior During Power-up" for more information about I/O behavior during power-up.
GSRN	I	Global RESET signal (active low). Any I/O pin can be GSRN.
NC	—	No connect.
GND	—	Ground. Dedicated pins.
V_{CC}	—	Power supply pins for core logic. Dedicated pins.
V_{CCAUX}	—	Auxiliary power supply pin. This dedicated pin powers all the differential and referenced input buffers.
V_{CCIOx}	—	Dedicated power supply pins for I/O bank x.
V_{CCPLL}	—	PLL supply pins. Should be tied to V_{CC} even when the corresponding PLL is unused.
V_{REF1_x}, V_{REF2_x}	—	Reference supply pins for I/O bank x. Pre-determined pins in each bank are assigned as V_{REF} inputs. When not used, they may be used as I/O pins.
XRES[4]	—	10K ohm +/-1% resistor must be connected between this pad and ground.
PLLCAP[4]	—	External capacitor connection for PLL.
PLL, DLL and Clock Functions (Used as user programmable I/O pins when not in use for PLL or clock pins)		
[LOC][num]_V_{CCPLL}	—	Power supply pin for PLL: LUM, LLM, RUM, RLM, num = row from center.
[LOC][num]_GPLL[T, C]_IN_A	I	General Purpose PLL (GPLL) input pads: LUM, LLM, RUM, RLM, num = row from center, T = true and C = complement, index A,B,C...at each side.
[LOC][num]_GPLL[T, C]_FB_A	I	Optional feedback GPLL input pads: LUM, LLM, RUM, RLM, num = row from center, T = true and C = complement, index A,B,C...at each side.
[LOC][num]_SPLL[T, C]_IN_A[5]	I	Secondary PLL (SPLL) input pads: LUM, LLM, RUM, RLM, num = row from center, T = true and C = complement, index A,B,C...at each side.
[LOC][num]_SPLL[T, C]_FB_A[5]	I	Optional feedback (SPLL) input pads: LUM, LLM, RUM, RLM, num = row from center, T = true and C = complement, index A,B,C...at each side.
[LOC][num]_DLL[T, C]_IN_A	I	DLL input pads: LUM, LLM, RUM, RLM, num = row from center, T = true and C = complement, index A,B,C...at each side.
[LOC][num]_DLL[T, C]_FB_A	I	Optional feedback (DLL) input pads: LUM, LLM, RUM, RLM, num = row from center, T = true and C = complement, index A,B,C...at each side.
PCLK[T, C]_[n:0]_[3:0]	I	Primary Clock pads, T = true and C = complement, n per side, indexed by bank and 0,1,2,3 within bank.

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LatticeECP2 Pin Information Summary, LFE2-6 and LFE2-12 (Cont.)

Pin Type		LFE2-6		LFE2-12			
		144 TQFP	256 fpBGA	144 TQFP	208 PQFP	256 fpBGA	484 fpBGA
Available DDR-Interfaces per I/O Bank[1]	Bank0	0	0	0	0	0	0
	Bank1	0	0	0	0	0	0
	Bank2	0	1	0	0	1	1
	Bank3	0	0	0	0	0	0
	Bank4	0	2	0	0	2	3
	Bank5	0	1	0	0	1	3
	Bank6	0	1	0	0	1	1
	Bank7	0	1	0	0	1	1
	Bank8	0	0	0	0	0	0
PCI Capable I/Os per Bank	Bank0	0	0	0	0	0	0
	Bank1	0	0	0	0	0	0
	Bank2	0	0	0	0	0	0
	Bank3	0	0	0	0	0	0
	Bank4	18	32	18	19	32	46
	Bank5	8	14	10	18	17	46
	Bank6	0	0	0	0	0	0
	Bank7	0	0	0	0	0	0
	Bank8	0	0	0	0	0	0

1. Minimum requirement to implement a fully functional 8-bit wide DDR bus. Available DDR interface consists of at least 12 I/Os (1 DQS + 1 DQSB + 8 DQs + 1 DM + Bank VREF1).

LFE2-6E/SE and LFE2-12E/SE Logic Signal Connections: 144 TQFP

LFE2-6E/SE					LFE2-12E/12SE			
Pin Number	Pin/Pad Function	Bank	Dual Function	Differential	Pin/Pad Function	Bank	Dual Function	Differential
1	PL2A	7	VREF2_7	T (LVDS)*	PL2A	7	VREF2_7	T (LVDS)*
2	PL2B	7	VREF1_7	C (LVDS)*	PL2B	7	VREF1_7	C (LVDS)*
3	PL4A	7		T (LVDS)*	PL4A	7		T (LVDS)*
4	PL4B	7		C (LVDS)*	PL4B	7		C (LVDS)*
5	PL6A	7	LDQ10	T (LVDS)*	PL6A	7	LDQ10	T (LVDS)*
6	VCCAUX	-			VCCAUX	-		
7	PL6B	7	LDQ10	C (LVDS)*	PL6B	7	LDQ10	C (LVDS)*
8	PL8A	7	LDQ10	T (LVDS)*	PL8A	7	LDQ10	T (LVDS)*
9	VCCIO7	7			VCCIO7	7		
10	PL8B	7	LDQ10	C (LVDS)*	PL8B	7	LDQ10	C (LVDS)*
11	GND	-			GND	-		
12	PL12A	7	LDQ10	T (LVDS)*	PL12A	7	LDQ10	T (LVDS)*
13	PL12B	7	LDQ10	C (LVDS)*	PL12B	7	LDQ10	C (LVDS)*
14	PL13A	7	PCLKT7_0/LDQ10	T	PL13A	7	PCLKT7_0/LDQ10	T
15	PL13B	7	PCLKC7_0/LDQ10	C	PL13B	7	PCLKC7_0/LDQ10	C
16	VCC	-			VCC	-		
17	PL15A	6	PCLKT6_0	T (LVDS)*	PL15A	6	PCLKT6_0	T (LVDS)*
18	PL15B	6	PCLKC6_0	C (LVDS)*	PL15B	6	PCLKC6_0	C (LVDS)*
19	PL16A	6	VREF2_6	T	PL16A	6	VREF2_6	T
20	PL16B	6	VREF1_6	C	PL16B	6	VREF1_6	C
21	GND	-			GND	-		
22	VCC	-			VCC	-		
23	PL18A	6	LLM0_GDLLT_FB_A	T	PL18A	6	LLM0_GDLLT_FB_A	T
24	PL18B	6	LLM0_GDLLC_FB_A	C	PL18B	6	LLM0_GDLLC_FB_A	C
25	LLM0_PLLCAP	6			LLM0_PLLCAP	6		
26	PL20A	6	LLM0_GPLLT_IN_A**	T (LVDS)*	PL20A	6	LLM0_GPLLT_IN_A**	T (LVDS)*
27	PL20B	6	LLM0_GPLLC_IN_A**	C (LVDS)*	PL20B	6	LLM0_GPLLC_IN_A**	C (LVDS)*
28	PL22A	6			PL22A	6		
29	VCC	-			VCC	-		
30	GND	-			GND	-		
31	VCCIO6	6			VCCIO6	6		
32	TCK	-			TCK	-		
33	TDI	-			TDI	-		
34	TDO	-			TDO	-		
35	VCCJ	-			VCCJ	-		
36	TMS	-			TMS	-		
37	PB2A	5	VREF2_5/BDQ6	T	PB2A	5	VREF2_5/BDQ6	T
38	PB2B	5	VREF1_5/BDQ6	C	PB2B	5	VREF1_5/BDQ6	C
39	VCCAUX	-			VCCAUX	-		
40	PB4A	5	BDQ6	T	PB6A	5	BDQS6	T
41	PB4B	5	BDQ6	C	PB6B	5	BDQ6	C
42	VCCIO5	5			VCCIO5	5		
43	PB6A	5	BDQS6	T	PB12A	5	BDQ15	T
44	PB6B	5	BDQ6	C	PB12B	5	BDQ15	C
45	NC	5			PB16A	5	BDQ15	T

LFE2-6E/SE and LFE2-12E/SE Logic Signal Connections: 256 fpBGA

LFE2-6E/SE					LFE2-12E/SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
C3	PL2A	7	VREF2_7	T (LVDS)*	PL2A	7	VREF2_7	T (LVDS)*
C2	PL2B	7	VREF1_7	C (LVDS)*	PL2B	7	VREF1_7	C (LVDS)*
VCCIO	VCCIO7	7			VCCIO7	7		
-	-	-			-	-		
D3	PL5A	7		T	PL5A	7		T
D4	PL4A	7		T (LVDS)*	PL4A	7		T (LVDS)*
D2	PL5B	7		C	PL5B	7		C
GND	GNDIO7	-			GNDIO7	-		
E4	PL4B	7		C (LVDS)*	PL4B	7		C (LVDS)*
B1	PL7A	7	LDQ10	T	PL7A	7	LDQ10	T
C1	PL7B	7	LDQ10	C	PL7B	7	LDQ10	C
F5	PL9A	7	LDQ10	T	PL9A	7	LDQ10	T
VCCIO	VCCIO7	7			VCCIO7	7		
F4	PL8A	7	LDQ10	T (LVDS)*	PL8A	7	LDQ10	T (LVDS)*
G6	PL9B	7	LDQ10	C	PL9B	7	LDQ10	C
G4	PL8B	7	LDQ10	C (LVDS)*	PL8B	7	LDQ10	C (LVDS)*
D1	PL10A	7	LDQS10	T (LVDS)*	PL10A	7	LDQS10	T (LVDS)*
GND	GNDIO7	-			GNDIO7	-		
E1	PL10B	7	LDQ10	C (LVDS)*	PL10B	7	LDQ10	C (LVDS)*
F3	PL11A	7	LDQ10	T	PL11A	7	LDQ10	T
G3	PL11B	7	LDQ10	C	PL11B	7	LDQ10	C
VCCIO	VCCIO7	7			VCCIO7	7		
F2	PL12A	7	LDQ10	T (LVDS)*	PL12A	7	LDQ10	T (LVDS)*
F1	PL12B	7	LDQ10	C (LVDS)*	PL12B	7	LDQ10	C (LVDS)*
GND	GNDIO7	-			GNDIO7	-		
G2	PL13A	7	PCLKT7_0/LDQ10	T	PL13A	7	PCLKT7_0/LDQ10	T
G1	PL13B	7	PCLKC7_0/LDQ10	C	PL13B	7	PCLKC7_0/LDQ10	C
H6	PL15A	6	PCLKT6_0	T (LVDS)*	PL15A	6	PCLKT6_0	T (LVDS)*
VCCIO	VCCIO6	6			VCCIO6	6		
H5	PL15B	6	PCLKC6_0	C (LVDS)*	PL15B	6	PCLKC6_0	C (LVDS)*
H4	PL16A	6	VREF2_6	T	PL16A	6	VREF2_6	T
GND	GNDIO6	-			GNDIO6	-		
H3	PL16B	6	VREF1_6	C	PL16B	6	VREF1_6	C
H2	PL17A	6	LLM0_GDLLT_IN_A**	T (LVDS)*	PL17A	6	LLM0_GDLLT_IN_A**	T (LVDS)*
H1	PL17B	6	LLM0_GDLLC_IN_A**	C (LVDS)*	PL17B	6	LLM0_GDLLC_IN_A**	C (LVDS)*
G10	VCC	-			VCC	-		
J4	PL18A	6	LLM0_GDLLT_FB_A	T	PL18A	6	LLM0_GDLLT_FB_A	T
J5	PL18B	6	LLM0_GDLLC_FB_A	C	PL18B	6	LLM0_GDLLC_FB_A	C
J6	LLM0_PLLCAP	6			LLM0_PLLCAP	6		
K4	PL20A	6	LLM0_GPLLT_IN_A**	T (LVDS)*	PL20A	6	LLM0_GPLLT_IN_A**	T (LVDS)*
GND	GNDIO6	-			GNDIO6	-		
J1	PL21A	6	LLM0_GPLLT_FB_A	T	PL21A	6	LLM0_GPLLT_FB_A	T
K3	PL20B	6	LLM0_GPLLC_IN_A**	C (LVDS)*	PL20B	6	LLM0_GPLLC_IN_A**	C (LVDS)*
VCCIO	VCCIO6	6			VCCIO6	6		
J2	PL21B	6	LLM0_GPLLC_FB_A	C	PL21B	6	LLM0_GPLLC_FB_A	C

LFE2-6E/SE and LFE2-12E/SE Logic Signal Connections: 256 fpBGA (Cont.)

LFE2-6E/SE					LFE2-12E/SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
M8	PB8B	5	PCLKC5_0/BDQ6	C	PB26B	5	PCLKC5_0/BDQ24	C
GND	GNDIO5	-			GNDIO5	-		
P7	PB13A	4	PCLKT4_0/BDQ15	T	PB31A	4	PCLKT4_0/BDQ33	T
R8	PB13B	4	PCLKC4_0/BDQ15	C	PB31B	4	PCLKC4_0/BDQ33	C
VCCIO	VCCIO4	4			VCCIO4	4		
T5	PB14A	4	BDQ15	T	PB32A	4	BDQ33	T
T6	PB14B	4	BDQ15	C	PB32B	4	BDQ33	C
T8	PB15A	4	BDQS15	T	PB33A	4	BDQS33	T
GND	GNDIO4	-			GNDIO4	-		
R7	PB16A	4	BDQ15	T	PB34A	4	BDQ33	T
T9	PB15B	4	BDQ15	C	PB33B	4	BDQ33	C
T7	PB16B	4	BDQ15	C	PB34B	4	BDQ33	C
L8	PB17A	4	BDQ15	T	PB35A	4	BDQ33	T
VCCIO	VCCIO4	4			VCCIO4	4		
P8	PB18A	4	BDQ15	T	PB36A	4	BDQ33	T
L9	PB17B	4	BDQ15	C	PB35B	4	BDQ33	C
N8	PB18B	4	BDQ15	C	PB36B	4	BDQ33	C
R9	PB19A	4	BDQ15	T	PB37A	4	BDQ33	T
GND	GNDIO4	-			GNDIO4	-		
R10	PB19B	4	BDQ15	C	PB37B	4	BDQ33	C
-	-	-			VCCIO	4		
-	-	-			GNDIO4	4		
N9	PB20A	4	BDQ24	T	PB47A	4	BDQ51	T
T10	PB21A	4	BDQ24	T	PB48A	4	BDQ51	T
M9	PB20B	4	BDQ24	C	PB47B	4	BDQ51	C
R11	PB21B	4	BDQ24	C	PB48B	4	BDQ51	C
P10	PB22A	4	BDQ24	T	PB49A	4	BDQ51	T
N11	PB23A	4	BDQ24	T	PB50A	4	BDQ51	T
VCCIO	VCCIO4	4			VCCIO4	4		
N10	PB22B	4	BDQ24	C	PB49B	4	BDQ51	C
P11	PB23B	4	BDQ24	C	PB50B	4	BDQ51	C
T11	PB24A	4	BDQS24	T	PB51A	4	BDQS51	T
GND	GNDIO4	-			GNDIO4	-		
M11	PB25A	4	BDQ24	T	PB52A	4	BDQ51	T
T12	PB24B	4	BDQ24	C	PB51B	4	BDQ51	C
L11	PB25B	4	BDQ24	C	PB52B	4	BDQ51	C
T13	PB26A	4	BDQ24	T	PB53A	4	BDQ51	T
R13	PB27A	4	BDQ24	T	PB54A	4	BDQ51	T
VCCIO	VCCIO4	4			VCCIO4	4		
T14	PB26B	4	BDQ24	C	PB53B	4	BDQ51	C
P13	PB27B	4	BDQ24	C	PB54B	4	BDQ51	C
GND	GNDIO4	-			GNDIO4	-		
N12	PB28A	4	VREF2_4/BDQ24	T	PB55A	4	VREF2_4/BDQ51	T
M12	PB28B	4	VREF1_4/BDQ24	C	PB55B	4	VREF1_4/BDQ51	C
R15	CFG2	8			CFG2	8		

LFE2-20E/SE Logic Signal Connections: 256 fpBGA (Cont.)

LFE2-20E/SE					
Ball Number	Ball Number	Ball/Pad Function	Bank	Dual Function	Differential
J13	J13	PR28B	3	RLM0_GDLLC_FB_A/RDQ25	C
J12	J12	PR28A	3	RLM0_GDLLT_FB_A/RDQ25	T
H12	H12	PR27B	3	RLM0_GDLLC_IN_A**/RDQ25	C (LVDS)*
GND	GND	GNDIO3	-		
H13	H13	PR27A	3	RLM0_GDLLT_IN_A**/RDQ25	T (LVDS)*
H15	H15	PR22B	3	VREF2_3/RDQ25	C
VCCIO	VCCIO	VCCIO3	3		
H16	H16	PR22A	3	VREF1_3/RDQ25	T
H11	H11	PR21B	3	PCLKC3_0/RDQ25	C (LVDS)*
J11	J11	PR21A	3	PCLKT3_0/RDQ25	T (LVDS)*
G16	G16	PR19B	2	PCLKC2_0/RDQ16	C
GND	GND	GNDIO2	-		
G15	G15	PR19A	2	PCLKT2_0/RDQ16	T
F15	F15	PR17B	2	RDQ16	C
G11	G11	PR18B	2	RDQ16	C (LVDS)*
F14	F14	PR17A	2	RDQ16	T
VCCIO	VCCIO	VCCIO2	2		
F12	F12	PR18A	2	RDQ16	T (LVDS)*
G14	G14	PR16B	2	RDQ16	C (LVDS)*
G13	G13	PR16A	2	RDQS16	T (LVDS)*
GND	GND	GNDIO2	-		
F16	F16	PR14B	2	RDQ16	C (LVDS)*
F9	F9	PR15B	2	RDQ16	C
E16	E16	PR14A	2	RDQ16	T (LVDS)*
F10	F10	PR15A	2	RDQ16	T
VCCIO	VCCIO	VCCIO2	2		
D16	D16	PR13B	2	RDQ16	C
D15	D15	PR13A	2	RDQ16	T
C15	C15	PR6B	2	RDQ8	C (LVDS)*
C16	C16	PR7B	2	RDQ8	C
GND	GND	GNDIO2	-		
D14	D14	PR6A	2	RDQ8	T (LVDS)*
B16	B16	PR7A	2	RDQ8	T
F13	F13	PR2B	2	VREF2_2	C (LVDS)*
VCCIO	VCCIO	VCCIO2	2		
E13	E13	PR2A	2	VREF1_2	T (LVDS)*
F11	F11	PT64B	1	VREF2_1	C
E11	E11	PT64A	1	VREF1_1	T
GND	GND	GNDIO1	-		
A15	A15	PT63B	1		C
E12	E12	PT62B	1		C
B15	B15	PT63A	1		T

LFE2-20E/SE Logic Signal Connections: 256 fpBGA (Cont.)

LFE2-20E/SE					
Ball Number	Ball Number	Ball/Pad Function	Bank	Dual Function	Differential
P5	P5	VCCIO5	5		
K5	K5	VCCIO6	6		
M3	M3	VCCIO6	6		
E3	E3	VCCIO7	7		
G5	G5	VCCIO7	7		
T15	T15	VCCIO8	8		
A1	A1	GND	-		
A16	A16	GND	-		
B12	B12	GND	-		
B5	B5	GND	-		
C8	C8	GND	-		
E15	E15	GND	-		
E2	E2	GND	-		
H14	H14	GND	-		
H8	H8	GND	-		
H9	H9	GND	-		
J3	J3	GND	-		
J8	J8	GND	-		
J9	J9	GND	-		
M15	M15	GND	-		
M2	M2	GND	-		
P9	P9	GND	-		
R12	R12	GND	-		
R5	R5	GND	-		
T1	T1	GND	-		
T16	T16	GND	-		

* Supports true LVDS. Other differential signals must be emulated with external resistors.
** These dedicated input pins can be used for GPLLs or GDLLs within the respective quadrant.

Note: VCCIO and GND pads are used to determine the average DC current drawn by I/Os between GND/VCCIO connections, or between the last GND/VCCIO in an I/O bank and the end of an I/O bank. The substrate pads listed in the Pin Table do not necessarily have a one to one connection with a package ball or pin.

LFE2-12E/SE and LFE2-20E/SE Logic Signal Connections: 484 fpBGA (Cont.)

LFE2-12E/12SE					LFE2-20E/20SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
M6	PL15B	6	PCLKC6_0	C (LVDS)*	PL21B	6	PCLKC6_0/LDQ25	C (LVDS)*
M3	PL16A	6	VREF2_6	T	PL22A	6	VREF2_6/LDQ25	T
GNDIO	GNDIO6	-			-	-		
M4	PL16B	6	VREF1_6	C	PL22B	6	VREF1_6/LDQ25	C
-	-	-			VCCIO6	6		
N1	NC	-			PL24A	6	LDQ25	T
M2	NC	-			PL23A	6	LDQ25	T (LVDS)*
N2	NC	-			PL24B	6	LDQ25	C
M1	NC	-			PL23B	6	LDQ25	C (LVDS)*
-	-	-			GNDIO	-		
N3	NC	-			PL25A	6	LDQS25	T (LVDS)*
N5	NC	-			PL26A	6	LDQ25	T
N4	NC	-			PL25B	6	LDQ25	C (LVDS)*
-	-	-			VCCIO6	6		
P5	NC	-			PL26B	6	LDQ25	C
P1	PL17A	6	LLM0_GDLLT_IN_A**	T (LVDS)*	PL27A	6	LLM0_GDLLT_IN_A**/LDQ25	T (LVDS)*
P2	PL17B	6	LLM0_GDLLC_IN_A**	C (LVDS)*	PL27B	6	LLM0_GDLLC_IN_A**/LDQ25	C (LVDS)*
P4	PL18A	6	LLM0_GDLLT_FB_A	T	PL28A	6	LLM0_GDLLT_FB_A/LDQ25	T
-	-	-			GNDIO	-		
R4	PL18B	6	LLM0_GDLLC_FB_A	C	PL28B	6	LLM0_GDLLC_FB_A/LDQ25	C
P6	LLM0_PLLCAP	6			LLM0_PLLCAP	6		
R1	PL20A	6	LLM0_GPLLT_IN_A**	T (LVDS)*	PL30A	6	LLM0_GPLLT_IN_A**/LDQ34	T (LVDS)*
GNDIO	GNDIO6	-			-	-		
R3	PL21A	6	LLM0_GPLLT_FB_A	T	PL31A	6	LLM0_GPLLT_FB_A/LDQ34	T
R2	PL20B	6	LLM0_GPLLC_IN_A**	C (LVDS)*	PL30B	6	LLM0_GPLLC_IN_A/LDQ34	C (LVDS)*
T4	PL21B	6	LLM0_GPLLC_FB_A	C	PL31B	6	LLM0_GPLLC_FB_A/LDQ34	C
T5	PL23A	6		T	PL33A	6	LDQ34	T
VCCIO	VCCIO6	6			VCCIO6	6		
T1	PL22A	6		T (LVDS)*	PL32A	6	LDQ34	T (LVDS)*
T3	PL23B	6		C	PL33B	6	LDQ34	C
T2	PL22B	6		C (LVDS)*	PL32B	6	LDQ34	C (LVDS)*
GNDIO	GNDIO6	-			GNDIO6	-		
-	-	-			VCCIO6	6		
V1	PL25A	6	LDQ28	T	PL39A	6	LDQ42	T
-	-	-			GNDIO	-		
V2	PL25B	6	LDQ28	C	PL39B	6	LDQ42	C
U1	PL24A	6	LDQ28	T (LVDS)*	PL38A	6	LDQ42	T (LVDS)*
U3	PL27A	6	LDQ28	T	PL41A	6	LDQ42	T
VCCIO	VCCIO6	6			VCCIO6	6		
U2	PL24B	6	LDQ28	C (LVDS)*	PL38B	6	LDQ42	C (LVDS)*
U4	PL27B	6	LDQ28	C	PL41B	6	LDQ42	C
R6	PL26A	6	LDQ28	T (LVDS)*	PL40A	6	LDQ42	T (LVDS)*
R7	PL29A	6	LDQ28	T	PL43A	6	LDQ42	T
GNDIO	GNDIO6	-			GNDIO	-		

LFE2-20E/SE and LFE2-35E/SE Logic Signal Connections: 672 fpBGA (Cont.)

LFE2-20E/20SE					LFE2-35E/35SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
GND	GNDIO5	-			GNDIO5	-		
W10	PB11A	5	BDQ15	T	PB11A	5	BDQ15	T
Y10	PB11B	5	BDQ15	C	PB11B	5	BDQ15	C
W11	PB12A	5	BDQ15	T	PB12A	5	BDQ15	T
AA10	PB12B	5	BDQ15	C	PB12B	5	BDQ15	C
AC8	PB13A	5	BDQ15	T	PB13A	5	BDQ15	T
AD8	PB13B	5	BDQ15	C	PB13B	5	BDQ15	C
VCCIO	VCCIO5	5			VCCIO5	5		
AB8	PB14A	5	BDQ15	T	PB14A	5	BDQ15	T
AB10	PB14B	5	BDQ15	C	PB14B	5	BDQ15	C
GND	GNDIO5	-			GNDIO5	-		
AE6	PB15A	5	BDQS15	T	PB15A	5	BDQS15	T
AF6	PB15B	5	BDQ15	C	PB15B	5	BDQ15	C
AA11	PB16A	5	BDQ15	T	PB16A	5	BDQ15	T
AC9	PB16B	5	BDQ15	C	PB16B	5	BDQ15	C
AB9	PB17A	5	BDQ15	T	PB17A	5	BDQ15	T
AD9	PB17B	5	BDQ15	C	PB17B	5	BDQ15	C
VCCIO	VCCIO5	5			VCCIO5	5		
Y11	PB18A	5	BDQ15	T	PB18A	5	BDQ15	T
AB11	PB18B	5	BDQ15	C	PB18B	5	BDQ15	C
AE7	PB19A	5	BDQ15	T	PB19A	5	BDQ15	T
AF7	PB19B	5	BDQ15	C	PB19B	5	BDQ15	C
GND	GNDIO5	-			GNDIO5	-		
AC10	PB20A	5	BDQ24	T	PB20A	5	BDQ24	T
AD10	PB20B	5	BDQ24	C	PB20B	5	BDQ24	C
AA12	PB21A	5	BDQ24	T	PB21A	5	BDQ24	T
W12	PB21B	5	BDQ24	C	PB21B	5	BDQ24	C
AB12	PB22A	5	BDQ24	T	PB22A	5	BDQ24	T
VCCIO	VCCIO5	5			VCCIO5	5		
Y12	PB22B	5	BDQ24	C	PB22B	5	BDQ24	C
AD12	PB23A	5	BDQ24	T	PB23A	5	BDQ24	T
AC12	PB23B	5	BDQ24	C	PB23B	5	BDQ24	C
AC13	PB24A	5	BDQS24	T	PB24A	5	BDQS24	T
GND	GNDIO5	-			GNDIO5	-		
AA13	PB24B	5	BDQ24	C	PB24B	5	BDQ24	C
AD13	PB25A	5	BDQ24	T	PB25A	5	BDQ24	T
AC14	PB25B	5	BDQ24	C	PB25B	5	BDQ24	C
AE8	PB26A	5	BDQ24	T	PB26A	5	BDQ24	T
VCCIO	VCCIO5	5			VCCIO5	5		
AF8	PB26B	5	BDQ24	C	PB26B	5	BDQ24	C
AB15	PB27A	5	BDQ24	T	PB27A	5	BDQ24	T
Y13	PB27B	5	BDQ24	C	PB27B	5	BDQ24	C
AE9	PB28A	5	BDQ24	T	PB28A	5	BDQ24	T
GND	GNDIO5	-			GNDIO5	-		
AF9	PB28B	5	BDQ24	C	PB28B	5	BDQ24	C
W13	PB29A	5	BDQ33	T	PB29A	5	BDQ33	T

LFE2M20E/SE and LFE2M35E/SE Logic Signal Connections: 484 fpBGA (Cont.)

LFE2M20E/SE					LFE2M35E/SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
AB6	PB17A	5	PCLKT5_0/BDQ15	T	PB35A	5	PCLKT5_0/BDQ33	T
AB7	PB17B	5	PCLKC5_0/BDQ15	C	PB35B	5	PCLKC5_0/BDQ33	C
VCCIO	VCCIO5	5			VCCIO5	5		
GNDIO	GNDIO5	-			GNDIO5	-		
AA8	PB22A	4	PCLKT4_0/BDQ24	T	PB40A	4	PCLKT4_0/BDQ42	T
VCCIO	VCCIO4	4			VCCIO4	4		
AB8	PB22B	4	PCLKC4_0/BDQ24	C	PB40B	4	PCLKC4_0/BDQ42	C
AA9	PB23A	4	VREF2_4/BDQ24	T	PB41A	4	VREF2_4/BDQ42	T
Y9	PB23B	4	VREF1_4/BDQ24	C	PB41B	4	VREF1_4/BDQ42	C
AB9	PB24A	4	BDQS24****	T	PB42A	4	BDQS42****	T
GNDIO	GNDIO4	-			GNDIO4	-		
AB10	PB24B	4	BDQ24	C	PB42B	4	BDQ42	C
AA10	PB25A	4	BDQ24	T	PB43A	4	BDQ42	T
Y11	PB25B	4	BDQ24	C	PB43B	4	BDQ42	C
VCCIO	VCCIO4	4			VCCIO4	4		
GNDIO	GNDIO4	-			GNDIO4	-		
V10	PB29A	4	BDQ33	T	PB47A	4	BDQ51	T
U11	PB29B	4	BDQ33	C	PB47B	4	BDQ51	C
V11	PB30A	4	BDQ33	T	PB48A	4	BDQ51	T
W11	PB30B	4	BDQ33	C	PB48B	4	BDQ51	C
AA11	PB31A	4	BDQ33	T	PB49A	4	BDQ51	T
AB11	PB31B	4	BDQ33	C	PB49B	4	BDQ51	C
VCCIO	VCCIO4	4			VCCIO4	4		
T11	PB32A	4	BDQ33	T	PB50A	4	BDQ51	T
U12	PB32B	4	BDQ33	C	PB50B	4	BDQ51	C
GNDIO	GNDIO4	-			GNDIO4	-		
AA12	PB33A	4	BDQS33	T	PB51A	4	BDQS51	T
Y12	PB33B	4	BDQ33	C	PB51B	4	BDQ51	C
V12	PB34A	4	BDQ33	T	PB52A	4	BDQ51	T
W12	PB34B	4	BDQ33	C	PB52B	4	BDQ51	C
AB12	PB35A	4	BDQ33	T	PB53A	4	BDQ51	T
AA13	PB35B	4	BDQ33	C	PB53B	4	BDQ51	C
VCCIO	VCCIO4	4			VCCIO4	4		
T12	PB36A	4	BDQ33	T	PB54A	4	BDQ51	T
U13	PB36B	4	BDQ33	C	PB54B	4	BDQ51	C
V13	PB37A	4	BDQ33	T	PB55A	4	BDQ51	T
T13	PB37B	4	BDQ33	C	PB55B	4	BDQ51	C
GNDIO	GNDIO4	-			GNDIO4	-		
AB13	PB38A	4	BDQ42	T	PB56A	4	BDQ60	T
AB14	PB38B	4	BDQ42	C	PB56B	4	BDQ60	C
U14	PB39A	4	BDQ42	T	PB57A	4	BDQ60	T
T14	PB39B	4	BDQ42	C	PB57B	4	BDQ60	C
AA14	PB40A	4	BDQ42	T	PB58A	4	BDQ60	T
VCCIO	VCCIO4	4			VCCIO4	4		
Y14	PB40B	4	BDQ42	C	PB58B	4	BDQ60	C
W14	PB41A	4	BDQ42	T	PB59A	4	BDQ60	T
V14	PB41B	4	BDQ42	C	PB59B	4	BDQ60	C
AB15	PB42A	4	BDQS42	T	PB60A	4	BDQS60	T

LFE2M35E/SE and LFE2M50E/SE Logic Signal Connections: 672 fpBGA (Cont.)

LFE2M35E/SE					LFE2M50E/SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
AA14	PB42B	4	BDQ42	C	PB51B	4	BDQ51	C
VCCIO	VCCIO4	4			VCCIO4	4		
GNDIO	GNDIO4	-			GNDIO4	-		
W17	PB65A	4	BDQ69	T	PB56A	4	BDQ60	T
AA19	PB65B	4	BDQ69	C	PB56B	4	BDQ60	C
AC15	PB48A	4	BDQ51	T	PB57A	4	BDQ60	T
Y18	PB68B	4	BDQ69	C	PB57B	4	BDQ60	C
AB15	PB49A	4	BDQ51	T	PB58A	4	BDQ60	T
AC16	PB49B	4	BDQ51	C	PB58B	4	BDQ60	C
VCCIO	VCCIO4	4			VCCIO4	4		
AA17	PB60A	4	BDQS60****	T	PB59A	4	BDQ60	T
AB16	PB50B	4	BDQ51	C	PB59B	4	BDQ60	C
GNDIO	GNDIO4	-			GNDIO4	-		
AA15	PB51A	4	BDQS51****	T	PB60A	4	BDQS60	T
W16	PB59B	4	BDQ60	C	PB60B	4	BDQ60	C
Y15	PB52A	4	BDQ51	T	PB61A	4	BDQ60	T
AC17	PB52B	4	BDQ51	C	PB61B	4	BDQ60	C
AA18	PB61A	4	BDQ60	T	PB62A	4	BDQ60	T
Y17	PB61B	4	BDQ60	C	PB62B	4	BDQ60	C
-	-	-			VCCIO4	4		
GNDIO	GNDIO4	-			-	-		
W15	PB54A	4	BDQ51	T	PB63A	4	BDQ60	T
AB17	PB54B	4	BDQ51	C	PB63B	4	BDQ60	C
GNDIO	GNDIO4	-			GNDIO4	-		
VCCIO	VCCIO4	4			VCCIO4	4		
V17	PB73A	4	BDQ69	T	PB72A	4	BDQ69	T
AA20	PB73B	4	BDQ69	C	PB72B	4	BDQ69	C
GNDIO	GNDIO4	-			GNDIO4	-		
AD13	VCC	-			LRC_SQ_VCCRX3	13		
AF14	PB47A	4	BDQ51	T	LRC_SQ_HDINP3	13		T
AE13	NC	-			LRC_SQ_VCCIB3	13		
AE14	PB41A	4	VREF2_4/BDQ42	T	LRC_SQ_HDINN3	13		C
AD16	VCC	-			LRC_SQ_VCCTX3	13		
AF17	PB51B	4	BDQ51	C	LRC_SQ_HDOUTP3	13		T
AF16	NC	-			LRC_SQ_VCCOB3	13		
AE17	PB50A	4	BDQ51	T	LRC_SQ_HDOUTN3	13		C
AD17	VCC	-			LRC_SQ_VCCTX2	13		
AE18	PB53B	4	BDQ51	C	LRC_SQ_HDOUTN2	13		C
AD18	NC	-			LRC_SQ_VCCOB2	13		
AF18	PB53A	4	BDQ51	T	LRC_SQ_HDOUTP2	13		T
AD14	VCC	-			LRC_SQ_VCCRX2	13		
AE15	PB48B	4	BDQ51	C	LRC_SQ_HDINN2	13		C
AD15	NC	-			LRC_SQ_VCCIB2	13		
AF15	PB47B	4	BDQ51	C	LRC_SQ_HDINP2	13		T
AD19	VCC	-			LRC_SQ_VCCP	13		
AC19	PB57B	4	BDQ60	C	LRC_SQ_REFCLKP	13		T
AB19	PB59A	4	BDQ60	T	LRC_SQ_REFCLKN	13		C
AE19	VCCAUX	-			LRC_SQ_VCCAUX33	13		

LFE2M50E/SE and LFE2M70E/SE Logic Signal Connections: 900 fpBGA (Cont.)

LFE2M50E/SE					LFE2M70E/SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
AH12	VCC	-			LLC_SQ_VCCRX1	14		
AK8	PB16A	5	BDQ15	T	LLC_SQ_HDOUTP1	14		T
AH8	NC	-			LLC_SQ_VCCOB1	14		
AJ8	PB16B	5	BDQ15	C	LLC_SQ_HDOUTN1	14		C
AH9	VCC	-			LLC_SQ_VCCTX1	14		
AJ9	PB17B	5	BDQ15	C	LLC_SQ_HDOUTN0	14		C
AK10	NC	-			LLC_SQ_VCCOB0	14		
AK9	PB17A	5	BDQ15	T	LLC_SQ_HDOUTP0	14		T
AH10	VCC	-			LLC_SQ_VCCTX0	14		
AJ12	PB19B	5	BDQ15	C	LLC_SQ_HDINN0	14		C
AJ13	NC	-			LLC_SQ_VCCIB0	14		
AK12	PB19A	5	BDQ15	T	LLC_SQ_HDINP0	14		T
AH13	VCC	-			LLC_SQ_VCCRX0	14		
AF10	PB3A	5	BDQ6	T	PB30A	5	BDQ33	T
AE8	PB3B	5	BDQ6	C	PB30B	5	BDQ33	C
AE11	PB4A	5	BDQ6	T	PB31A	5	BDQ33	T
VCCIO	VCCIO5	5			VCCIO5	5		
AD9	PB4B	5	BDQ6	C	PB31B	5	BDQ33	C
AE10	PB5A	5	BDQ6	T	PB32A	5	BDQ33	T
AD10	PB5B	5	BDQ6	C	PB32B	5	BDQ33	C
AE13	PB6A	5	BDQS6	T	PB33A	5	BDQS33	T
GNDIO	GNDIO5	-			GNDIO5	-		
AC12	PB6B	5	BDQ6	C	PB33B	5	BDQ33	C
AG2	PB7A	5	BDQ6	T	PB34A	5	BDQ33	T
AG3	PB7B	5	BDQ6	C	PB34B	5	BDQ33	C
AD13	PB8A	5	BDQ6	T	PB35A	5	BDQ33	T
VCCIO	VCCIO5	5			VCCIO5	5		
AC13	PB8B	5	BDQ6	C	PB35B	5	BDQ33	C
AE14	PB9A	5	BDQ6	T	PB36A	5	BDQ33	T
AC14	PB9B	5	BDQ6	C	PB36B	5	BDQ33	C
AF3	PB10A	5	BDQ6	T	PB37A	5	BDQ33	T
GNDIO	GNDIO5	-			GNDIO5	-		
AF4	PB10B	5	BDQ6	C	PB37B	5	BDQ33	C
VCCIO	VCCIO5	5			-	-		
AG4	PB20A	5	BDQ24	T	PB38A	5	BDQ42	T
AG5	PB20B	5	BDQ24	C	PB38B	5	BDQ42	C
GNDIO	GNDIO5	-			-	-		
VCCIO	VCCIO5	5			-	-		
AD11	PB24A	5	BDQS24****	T	PB39A	5	BDQ42	T
AF13	PB24B	5	BDQ24	C	PB39B	5	BDQ42	C
AF12	PB25A	5	BDQ24	T	PB40A	5	BDQ42	T
-	-	-			VCCIO5	5		
AD14	PB25B	5	BDQ24	C	PB40B	5	BDQ42	C
AG8	PB26A	5	BDQ24	T	PB41A	5	BDQ42	T
AF8	PB26B	5	BDQ24	C	PB41B	5	BDQ42	C
AE15	PB27A	5	BDQ24	T	PB42A	5	BDQS42****	T
-	-	-			GNDIO5	-		
VCCIO	VCCIO5	5			-	-		

LFE2M50E/SE and LFE2M70E/SE Logic Signal Connections: 900 fpBGA (Cont.)

LFE2M50E/SE					LFE2M70E/SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
L13	VCC	-			VCC	-		
L18	VCC	-			VCC	-		
L19	VCC	-			VCC	-		
M11	VCC	-			VCC	-		
M12	VCC	-			VCC	-		
M13	VCC	-			VCC	-		
M14	VCC	-			VCC	-		
M15	VCC	-			VCC	-		
M16	VCC	-			VCC	-		
M17	VCC	-			VCC	-		
M18	VCC	-			VCC	-		
M19	VCC	-			VCC	-		
M20	VCC	-			VCC	-		
N11	VCC	-			VCC	-		
N12	VCC	-			VCC	-		
N19	VCC	-			VCC	-		
N20	VCC	-			VCC	-		
P12	VCC	-			VCC	-		
P19	VCC	-			VCC	-		
R12	VCC	-			VCC	-		
R19	VCC	-			VCC	-		
T12	VCC	-			VCC	-		
T19	VCC	-			VCC	-		
U12	VCC	-			VCC	-		
U19	VCC	-			VCC	-		
V11	VCC	-			VCC	-		
V12	VCC	-			VCC	-		
V19	VCC	-			VCC	-		
V20	VCC	-			VCC	-		
W11	VCC	-			VCC	-		
W12	VCC	-			VCC	-		
W13	VCC	-			VCC	-		
W14	VCC	-			VCC	-		
W15	VCC	-			VCC	-		
W16	VCC	-			VCC	-		
W17	VCC	-			VCC	-		
W18	VCC	-			VCC	-		
W19	VCC	-			VCC	-		
W20	VCC	-			VCC	-		
Y12	VCC	-			VCC	-		
Y13	VCC	-			VCC	-		
Y18	VCC	-			VCC	-		
Y19	VCC	-			VCC	-		
D14	VCCIO0	0			VCCIO0	0		
E6	VCCIO0	0			VCCIO0	0		
E9	VCCIO0	0			VCCIO0	0		
F12	VCCIO0	0			VCCIO0	0		
K12	VCCIO0	0			VCCIO0	0		

LFE2M100E/SE Logic Signal Connections: 900 fpBGA (Cont.)

LFE2M100E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential
M19	VCC	-		
M20	VCC	-		
N11	VCC	-		
N12	VCC	-		
N19	VCC	-		
N20	VCC	-		
P12	VCC	-		
P19	VCC	-		
R12	VCC	-		
R19	VCC	-		
T12	VCC	-		
T19	VCC	-		
U12	VCC	-		
U19	VCC	-		
V11	VCC	-		
V12	VCC	-		
V19	VCC	-		
V20	VCC	-		
W11	VCC	-		
W12	VCC	-		
W13	VCC	-		
W14	VCC	-		
W15	VCC	-		
W16	VCC	-		
W17	VCC	-		
W18	VCC	-		
W19	VCC	-		
W20	VCC	-		
Y12	VCC	-		
Y13	VCC	-		
Y18	VCC	-		
Y19	VCC	-		
D14	VCCIO0	0		
E6	VCCIO0	0		
E9	VCCIO0	0		
F12	VCCIO0	0		
K12	VCCIO0	0		
K13	VCCIO0	0		
D17	VCCIO1	1		
E22	VCCIO1	1		
E25	VCCIO1	1		
F19	VCCIO1	1		
K18	VCCIO1	1		

LFE2M70E/SE and LFE2M100E/SE Logic Signal Connections: 1152 fpBGA (Cont.)

LFE2M70E/SE				LFE2M100E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
AN29	LRC_SQ_VCCRX2	13			LRC_SQ_VCCRX2	13		
AM28	LRC_SQ_HDINN2	13		C	LRC_SQ_HDINN2	13		C
AL27	LRC_SQ_VCCIB2	13			LRC_SQ_VCCIB2	13		
AM29	LRC_SQ_HDINP2	13		T	LRC_SQ_HDINP2	13		T
AL29	LRC_SQ_VCCP	13			LRC_SQ_VCCP	13		
AL30	LRC_SQ_REFCLKP	13		T	LRC_SQ_REFCLKP	13		T
AK30	LRC_SQ_REFCLKN	13		C	LRC_SQ_REFCLKN	13		C
AK29	LRC_SQ_VCCAUX33	13			LRC_SQ_VCCAUX33	13		
AM30	LRC_SQ_HDINP1	13		T	LRC_SQ_HDINP1	13		T
AL31	LRC_SQ_VCCIB1	13			LRC_SQ_VCCIB1	13		
AM31	LRC_SQ_HDINN1	13		C	LRC_SQ_HDINN1	13		C
AN30	LRC_SQ_VCCRX1	13			LRC_SQ_VCCRX1	13		
AP30	LRC_SQ_HDOUTP1	13		T	LRC_SQ_HDOUTP1	13		T
AL32	LRC_SQ_VCCOB1	13			LRC_SQ_VCCOB1	13		
AP31	LRC_SQ_HDOUTN1	13		C	LRC_SQ_HDOUTN1	13		C
AN31	LRC_SQ_VCCTX1	13			LRC_SQ_VCCTX1	13		
AP32	LRC_SQ_HDOUTN0	13		C	LRC_SQ_HDOUTN0	13		C
AM34	LRC_SQ_VCCOB0	13			LRC_SQ_VCCOB0	13		
AP33	LRC_SQ_HDOUTP0	13		T	LRC_SQ_HDOUTP0	13		T
AN32	LRC_SQ_VCCTX0	13			LRC_SQ_VCCTX0	13		
AM32	LRC_SQ_HDINN0	13		C	LRC_SQ_HDINN0	13		C
AN34	LRC_SQ_VCCIB0	13			LRC_SQ_VCCIB0	13		
AM33	LRC_SQ_HDINP0	13		T	LRC_SQ_HDINP0	13		T
AN33	LRC_SQ_VCCRX0	13			LRC_SQ_VCCRX0	13		
AH28	CFG2	8			CFG2	8		
AD24	CFG1	8			CFG1	8		
AJ29	CFG0	8			CFG0	8		
AF25	PROGRAMN	8			PROGRAMN	8		
AJ28	CCLK	8			CCLK	8		
AE25	INITN	8			INITN	8		
AK31	DONE	8			DONE	8		
GNDIO	GNDIO8	-			GNDIO8	-		
AE24	WRITEN***	8			WRITEN***	8		
AJ30	CS1N***	8			CS1N***	8		
AD25	CSN***	8			CSN***	8		
AG29	D0/SPIFASTN***	8			D0/SPIFASTN***	8		
VCCIO	VCCIO8	8			VCCIO8	8		
AG28	D1***	8			D1***	8		
AG30	D2***	8			D2***	8		
AH29	D3***	8			D3***	8		
GNDIO	GNDIO8	-			GNDIO8	-		
AF26	D4***	8			D4***	8		
AH30	D5***	8			D5***	8		
AE26	D6***	8			D6***	8		
AJ31	D7/SPID0***	8			D7/SPID0***	8		
VCCIO	VCCIO8	8			VCCIO8	8		
AG27	DI/CSSPI0N***	8			DI/CSSPI0N***	8		
AK32	DOUT/CSON/ CSSPI1N***	8			DOUT/CSON/ CSSPI1N***	8		
AK33	BUSY/SISPI***	8			BUSY/SISPI***	8		

LFE2M70E/SE and LFE2M100E/SE Logic Signal Connections: 1152 fpBGA (Cont.)

LFE2M70E/SE				LFE2M100E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
AG23	VCCIO4	4			VCCIO4	4		
AK21	VCCIO4	4			VCCIO4	4		
AM19	VCCIO4	4			VCCIO4	4		
AM23	VCCIO4	4			VCCIO4	4		
AC14	VCCIO5	5			VCCIO5	5		
AC15	VCCIO5	5			VCCIO5	5		
AG12	VCCIO5	5			VCCIO5	5		
AG16	VCCIO5	5			VCCIO5	5		
AK14	VCCIO5	5			VCCIO5	5		
AM12	VCCIO5	5			VCCIO5	5		
AM16	VCCIO5	5			VCCIO5	5		
AA12	VCCIO6	6			VCCIO6	6		
AB3	VCCIO6	6			VCCIO6	6		
AB8	VCCIO6	6			VCCIO6	6		
AE3	VCCIO6	6			VCCIO6	6		
AE7	VCCIO6	6			VCCIO6	6		
AH3	VCCIO6	6			VCCIO6	6		
W3	VCCIO6	6			VCCIO6	6		
W8	VCCIO6	6			VCCIO6	6		
Y12	VCCIO6	6			VCCIO6	6		
G3	VCCIO7	7			VCCIO7	7		
K3	VCCIO7	7			VCCIO7	7		
K7	VCCIO7	7			VCCIO7	7		
N3	VCCIO7	7			VCCIO7	7		
N8	VCCIO7	7			VCCIO7	7		
P12	VCCIO7	7			VCCIO7	7		
R12	VCCIO7	7			VCCIO7	7		
T3	VCCIO7	7			VCCIO7	7		
T8	VCCIO7	7			VCCIO7	7		
AD28	VCCIO8	8			VCCIO8	8		
AG32	VCCIO8	8			VCCIO8	8		
AB12	VCCAUX	-			VCCAUX	-		
AB13	VCCAUX	-			VCCAUX	-		
AB22	VCCAUX	-			VCCAUX	-		
AB23	VCCAUX	-			VCCAUX	-		
AC13	VCCAUX	-			VCCAUX	-		
AC22	VCCAUX	-			VCCAUX	-		
M13	VCCAUX	-			VCCAUX	-		
M22	VCCAUX	-			VCCAUX	-		
N12	VCCAUX	-			VCCAUX	-		
N13	VCCAUX	-			VCCAUX	-		
N22	VCCAUX	-			VCCAUX	-		
N23	VCCAUX	-			VCCAUX	-		
A1	GND	-			GND	-		
A10	GND	-			GND	-		
A13	GND	-			GND	-		
A22	GND	-			GND	-		
A25	GND	-			GND	-		
A34	GND	-			GND	-		

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2M100SE-5FN1152C	520	1.2V	-5	Lead-Free fpBGA	1152	Com	100
LFE2M100SE-6FN1152C	520	1.2V	-6	Lead-Free fpBGA	1152	Com	100
LFE2M100SE-7FN1152C	520	1.2V	-7	Lead-Free fpBGA	1152	Com	100
LFE2M100SE-5FN900C	416	1.2V	-5	Lead-Free fpBGA	900	Com	100
LFE2M100SE-6FN900C	416	1.2V	-6	Lead-Free fpBGA	900	Com	100
LFE2M100SE-7FN900C	416	1.2V	-7	Lead-Free fpBGA	900	Com	100