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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

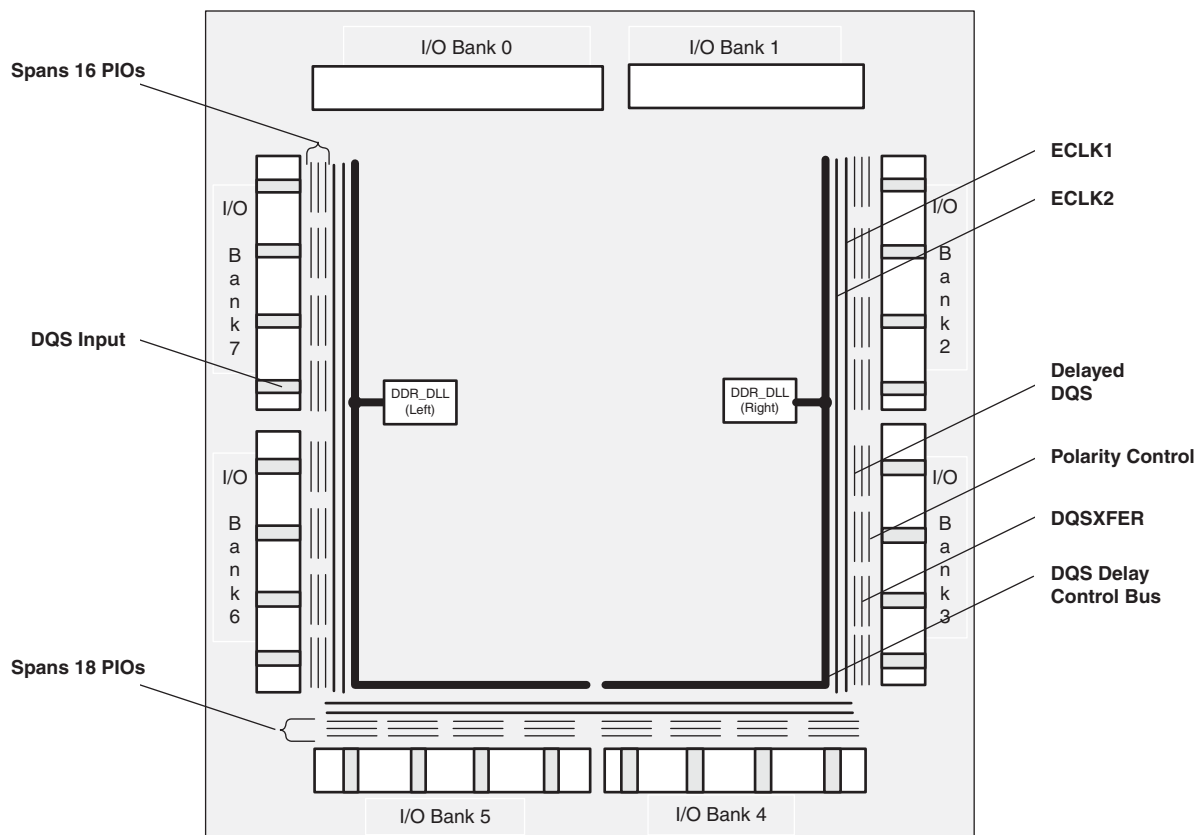
Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	2375
Number of Logic Elements/Cells	19000
Total RAM Bits	1246208
Number of I/O	304
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	484-BBGA
Supplier Device Package	484-FPBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfe2m20e-5f484i

Figure 2-35. Edge Clock, DLL Calibration and DQS Local Bus Distribution



Note: Bank 8 is not shown.

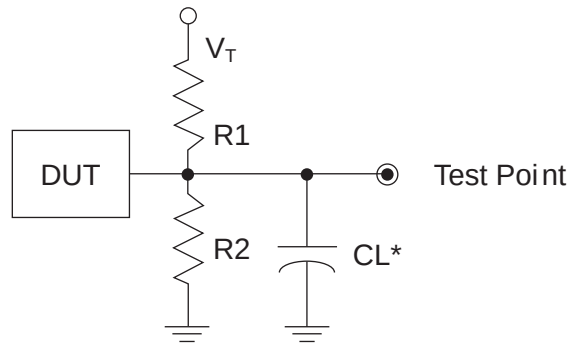
LatticeECP2/M Family Timing Adders^{1, 2, 3}
Over Recommended Operating Conditions

Buffer Type	Description	-7	-6	-5	Units
Input Adjusters					
LVDS25	LVDS	-0.04	-0.02	0.00	ns
BLVDS25	BLVDS	-0.04	-0.09	-0.15	ns
MLVDS	LVDS	-0.15	-0.15	-0.15	ns
RSDS	RSDS	-0.15	-0.15	-0.15	ns
LVPECL33	LVPECL	0.16	0.15	0.13	ns
HSTL18_I	HSTL_18 class I	0.01	-0.01	-0.04	ns
HSTL18_II	HSTL_18 class II	0.01	-0.01	-0.04	ns
HSTL18D_I	Differential HSTL 18 class I	0.01	-0.01	-0.04	ns
HSTL18D_II	Differential HSTL 18 class II	0.01	-0.01	-0.04	ns
HSTL15_I	HSTL_15 class I	0.01	-0.01	-0.04	ns
HSTL15D_I	Differential HSTL 15 class I	0.01	-0.01	-0.04	ns
SSTL33_I	SSTL_3 class I	-0.03	-0.07	-0.10	ns
SSTL33_II	SSTL_3 class II	-0.03	-0.07	-0.10	ns
SSTL33D_I	Differential SSTL_3 class I	-0.03	-0.07	-0.10	ns
SSTL33D_II	Differential SSTL_3 class II	-0.03	-0.07	-0.10	ns
SSTL25_I	SSTL_2 class I	-0.04	-0.07	-0.10	ns
SSTL25_II	SSTL_2 class II	-0.04	-0.07	-0.10	ns
SSTL25D_I	Differential SSTL_2 class I	-0.04	-0.07	-0.10	ns
SSTL25D_II	Differential SSTL_2 class II	-0.04	-0.07	-0.10	ns
SSTL18_I	SSTL_18 class I	-0.01	-0.04	-0.07	ns
SSTL18_II	SSTL_18 class II	-0.01	-0.04	-0.07	ns
SSTL18D_I	Differential SSTL_18 class I	-0.01	-0.04	-0.07	ns
SSTL18D_II	Differential SSTL_18 class II	-0.01	-0.04	-0.07	ns
LVTTTL33	LVTTTL	-0.16	-0.16	-0.16	ns
LVC MOS33	LVC MOS 3.3	-0.08	-0.12	-0.16	ns
LVC MOS25	LVC MOS 2.5	0.00	0.00	0.00	ns
LVC MOS18	LVC MOS 1.8	-0.16	-0.17	-0.17	ns
LVC MOS15	LVC MOS 1.5	-0.14	-0.14	-0.14	ns
LVC MOS12	LVC MOS 1.2	-0.04	-0.01	0.01	ns
PCI33	PCI	-0.08	-0.12	-0.16	ns
Output Adjusters					
LVDS25E	LVDS 2.5 E ⁴	0.25	0.19	0.13	ns
LVDS25	LVDS 2.5	0.10	0.13	0.17	ns
BLVDS25	BLVDS 2.5	0.00	-0.01	-0.03	ns
MLVDS	MLVDS 2.5 ⁴	0.00	-0.01	-0.03	ns
RSDS	RSDS 2.5 ⁴	0.25	0.19	0.13	ns
LVPECL33	LVPECL 3.3 ⁴	-0.02	-0.04	-0.06	ns
HSTL18_I	HSTL_18 class I 8mA drive	-0.19	-0.22	-0.25	ns
HSTL18_II	HSTL_18 class II	-0.30	-0.34	-0.37	ns
HSTL18D_I	Differential HSTL 18 class I 8mA drive	-0.19	-0.22	-0.25	ns
HSTL18D_II	Differential HSTL 18 class II	-0.30	-0.34	-0.37	ns

Switching Test Conditions

Figure 3-22 shows the output test load that is used for AC testing. The specific values for resistance, capacitance, voltage, and other test conditions are shown in Table 3-19.

Figure 3-22. Output Test Load, LVTTTL and LVCMOS Standards



*CL Includes Test Fixture and Probe Capacitance

Table 3-19. Test Fixture Required Components, Non-Terminated Interfaces

Test Condition	R ₁	R ₂	C _L	Timing Ref.	V _T
LVTTTL and other LVCMOS settings (L → H, H → L)	∞	∞	0pF	LVCMOS 3.3 = 1.5V	—
				LVCMOS 2.5 = V _{CCIO} /2	—
				LVCMOS 1.8 = V _{CCIO} /2	—
				LVCMOS 1.5 = V _{CCIO} /2	—
				LVCMOS 1.2 = V _{CCIO} /2	—
LVCMOS 2.5 I/O (Z → H)	∞	1MΩ		V _{CCIO} /2	—
LVCMOS 2.5 I/O (Z → L)	1MΩ	∞		V _{CCIO} /2	V _{CCIO}
LVCMOS 2.5 I/O (H → Z)	∞	100		V _{OH} - 0.10	—
LVCMOS 2.5 I/O (L → Z)	100	∞		V _{OL} + 0.10	V _{CCIO}

Note: Output test conditions for all other interfaces are determined by the respective standards.

LatticeECP2 Pin Information Summary, LFE2-20 and LFE2-35 (Cont.)

Pin Type		LFE2-20				LFE2-35	
		208 PQFP	256 fpBGA	484 fpBGA	672 fpBGA	484 fpBGA	672 fpBGA
Available DDR-Interfaces per I/O Bank ¹	Bank0	0	0	0	0	0	0
	Bank1	0	0	0	0	0	0
	Bank2	0	1	2	2	2	3
	Bank3	0	0	0	2	0	2
	Bank4	0	2	3	3	3	3
	Bank5	0	1	3	4	3	4
	Bank6	0	1	2	3	1	3
	Bank7	0	1	2	2	2	3
	Bank8	0	0	0	0	0	0
PCI Capable I/Os per Bank	Bank0	0	0	0	0	0	0
	Bank1	0	0	0	0	0	0
	Bank2	0	0	0	0	0	0
	Bank3	0	0	0	0	0	0
	Bank4	19	32	46	50	46	54
	Bank5	18	17	46	68	46	68
	Bank6	0	0	0	0	0	0
	Bank7	0	0	0	0	0	0
	Bank8	0	0	0	0	0	0

1. Minimum requirement to implement a fully functional 8-bit wide DDR bus. Available DDR interface consists of at least 12 I/Os (1 DQS + 1 DQSB + 8 DQs + 1 DM + Bank VREF1).

LatticeECP2M Power Supply and NC (Cont.)

Signal	672 fpBGA	900 fpBGA
GND ¹	A13, A19, A2, A25, AA2, AA25, AB18, AB22, AB5, AB9, AE1, AE11, AE16, AE22, AE26, AE6, AF13, AF19, AF2, AF25, B1, B11, B16, B22, B26, B6, E18, E22, E5, E9, F2, F25, G11, G16, J22, J5, K11, K13, K14, K16, L10, L11, L16, L17, L2, L20, L25, L7, M13, M14, N10, N12, N13, N14, N15, N17, P10, P12, P13, P14, P15, P17, R13, R14, T10, T11, T16, T17, T2, T20, T25, T7, U11, U13, U14, U16, V22, V5, Y11, Y16	LFE2M50: A1, A13, A18, A24, A30, A7, AA14, AA15, AA16, AA17, AA24, AA27, AA4, AB24, AB7, AD12, AD19, AD27, AE22, AE27, AE4, AE9, AF14, AF17, AF25, AF6, AJ10, AJ21, AJ27, AJ4, AK1, AK13, AK18, AK24, AK30, AK7, B10, B21, B27, B4, D25, D6, E14, E17, F22, F27, F4, F9, G12, G19, J24, J7, K14, K15, K16, K17, K27, K4, L14, L15, L16, L17, M23, M8, N14, N15, N16, N17, N27, N4, P11, P13, P14, P15, P16, P17, P18, P20, R10, R11, R13, R14, R15, R16, R17, R18, R20, R21, R24, R7, T10, T11, T13, T14, T15, T16, T17, T18, T20, T21, T24, T7, U11, U13, U14, U15, U16, U17, U18, U20, V14, V15, V16, V17, V27, V4, W23, W8, Y14, Y15, Y16, Y17 LFE2M70/LFE2M100: A1, A13, A18, A24, A30, A7, AA14, AA15, AA16, AA17, AA24, AA27, AA4, AB24, AB7, AD12, AD19, AD27, AE22, AE27, AE4, AE9, AF14, AF17, AF25, AF6, AJ10, AJ21, AJ27, AJ4, AK1, AK13, AK18, AK24, AK30, AK7, B10, B21, B27, B4, D25, D6, E14, E17, F22, F27, F4, F9, G12, G19, J24, J7, K14, K15, K16, K17, K27, K4, L14, L15, L16, L17, M23, M8, N14, N15, N16, N17, N27, N4, P11, P13, P14, P15, P16, P17, P18, P20, R10, R11, R13, R14, R15, R16, R17, R18, R20, R21, R24, R7, T10, T11, T13, T14, T15, T16, T17, T18, T20, T21, T24, T7, U11, U13, U14, U15, U16, U17, U18, U20, V14, V15, V16, V17, V27, V4, W23, W8, Y14, Y15, Y16, Y17
NC ²	LFE2M35: AB3, AB4, AC1, AC2, AD15, AD18, AD20, AD23, AE13, AE25, AF16, AF22, B4, B5, C26, D20, D21, D22, D23, D24, D25, D26, E20, E21, E25, E26, F20, G20, K10, K17, R4, U10, U23, V10, W7, N7, V7 LFE2M50: AB3, AB4, AC1, AC2, B4, B5, C26, D20, D21, D22, D23, D24, D25, D26, E20, E21, E25, E26, F20, G20, K10, K17, R4, U10, U23, V10, W7, AB21, AC20, AC21, AC22, AC23, AC25, AD26, W20	LFE2M50: G5, G4, K7, K8, E1, F2, F1, G3, G2, G1, L9, L7, K6, K5, L8, L6, AA1, AA2, Y3, AB1, Y9, Y8, Y7, AA7, AB2, AB3, AA5, AA6, AB4, AB5, AA8, AA9, AJ1, AK4, AH6, AH3, AH11, AH8, AK10, AJ13, AB26, AB27, Y24, Y25, AA29, Y28, Y30, Y29, W22, V22, Y27, Y26, W30, W29, W25, W26, L24, L23, D30, D29, K24, K25, J27, K26, J26, H26, H27, G26, H23, H24, D28, E28, J18, J19, H17, J17, F18, F17, B13, A10, C8, C11, C3, C6, A4, B1, AA26, AB11, AB12, AB13, AB14, AB15, AB16, AB17, AB19, AB20, AB21, AC11, AC21, AC22, AD21, AD22, AE23, AF20, AF23, AG23, AG26, F20, F23, G10, G20, G21, H19, H20, H21, H22, J20, J21, R9, U22, W9 LFE2M70/LFE2M100: AA26, AB10, AB11, AB12, AB13, AB14, AB15, AB16, AB17, AB19, AB20, AB21, AB9, AC10, AC11, AC21, AC22, AC8, AC9, AD21, AD22, AD4, AD5, AD6, AD7, AD8, AE23, AE5, AE6, AE7, AF20, AF23, AF5, AG23, AG26, D10, E10, E11, F10, F20, F23, F8, G10, G20, G21, G7, G8, G9, H19, H20, H21, H22, H6, H8, H9, J10, J20, J21, J9, K9, R9, U22, W9

1. All grounds must be electrically connected at the board level. For fpBGA packages, the total number of GND balls is less than the actual number of GND logic connections from the die to the common package GND plane.
2. NC pins should not be connected to any active signals, VCC or GND.
3. For package migration across device densities, the designer must comprehend the package pin requirements for the SERDES blocks. Specifically, the SERDES power pins of the largest density device must be accounted to accommodate migration to other smaller devices using the same package. Please refer to TN1160, [LatticeECP2/M Density Migration](#) for more details.

LFE2-6E/SE and LFE2-12E/SE Logic Signal Connections: 256 fpBGA (Cont.)

LFE2-6E/SE					LFE2-12E/SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
N14	CFG1	8			CFG1	8		
N13	PROGRAMN	8			PROGRAMN	8		
N15	CFG0	8			CFG0	8		
P15	PR30B	8	WRITEN	C	PR30B	8	WRITEN	C
L12	INITN	8			INITN	8		
N16	PR29B	8	CSN	C	PR29B	8	CSN	C
GND	GNDIO8	-			GNDIO8	-		
R14	CCLK	8			CCLK	8		
P14	PR30A	8	CS1N	T	PR30A	8	CS1N	T
M13	DONE	8			DONE	8		
R16	PR28B	8	D1	C	PR28B	8	D1	C
VCCIO	VCCIO8	8			VCCIO8	8		
M16	PR29A	8	D0/SPIFASTN	T	PR29A	8	D0/SPIFASTN	T
P16	PR28A	8	D2	T	PR28A	8	D2	T
L15	PR27B	8	D3	C	PR27B	8	D3	C
GND	GNDIO8	-			GNDIO8	-		
L14	PR26A	8	D6	T	PR26A	8	D6	T
L16	PR27A	8	D4	T	PR27A	8	D4	T
L10	PR25B	8	D7/SPID0	C	PR25B	8	D7/SPID0	C
L13	PR26B	8	D5	C	PR26B	8	D5	C
VCCIO	VCCIO8	8			VCCIO8	8		
K11	PR25A	8	DI/CSSPI0N	T	PR25A	8	DI/CSSPI0N	T
K14	PR24B	8	DOU/CSON	C	PR24B	8	DOU/CSON	C
K13	PR24A	8	BUSY/SISPI	T	PR24A	8	BUSY/SISPI	T
GND	GNDIO8	-			GNDIO8	-		
K15	PR21B	3	RLM0_GPLL_C_FB_A	C	PR21B	3	RLM0_GPLL_C_FB_A	C
VCCIO	VCCIO3	3			VCCIO3	3		
K16	PR21A	3	RLM0_GPLL_T_FB_A	T	PR21A	3	RLM0_GPLL_T_FB_A	T
GND	GNDIO3	-			GNDIO3	-		
J16	PR20B	3	RLM0_GPLL_C_IN_A**	C (LVDS)*	PR20B	3	RLM0_GPLL_C_IN_A**	C (LVDS)*
J15	PR20A	3	RLM0_GPLL_T_IN_A**	T (LVDS)*	PR20A	3	RLM0_GPLL_T_IN_A**	T (LVDS)*
J14	RLM0_PLLCAP	3			RLM0_PLLCAP	3		
J13	PR18B	3	RLM0_GDLL_C_FB_A	C	PR18B	3	RLM0_GDLL_C_FB_A	C
J12	PR18A	3	RLM0_GDLL_T_FB_A	T	PR18A	3	RLM0_GDLL_T_FB_A	T
H12	PR17B	3	RLM0_GDLL_C_IN_A**	C (LVDS)*	PR17B	3	RLM0_GDLL_C_IN_A**	C (LVDS)*
GND	GNDIO3	-			GNDIO3	-		
H13	PR17A	3	RLM0_GDLL_T_IN_A**	T (LVDS)*	PR17A	3	RLM0_GDLL_T_IN_A**	T (LVDS)*
H15	PR16B	3	VREF2_3	C	PR16B	3	VREF2_3	C
VCCIO	VCCIO3	3			VCCIO3	3		
H16	PR16A	3	VREF1_3	T	PR16A	3	VREF1_3	T
H11	PR15B	3	PCLKC3_0	C (LVDS)*	PR15B	3	PCLKC3_0	C (LVDS)*
J11	PR15A	3	PCLKT3_0	T (LVDS)*	PR15A	3	PCLKT3_0	T (LVDS)*
G16	PR13B	2	PCLKC2_0/RDQ10	C	PR13B	2	PCLKC2_0/RDQ10	C
GND	GNDIO2	-			GNDIO2	-		
G15	PR13A	2	PCLKT2_0/RDQ10	T	PR13A	2	PCLKT2_0/RDQ10	T

LFE2-12E/SE and LFE2-20E/SE Logic Signal Connections: 484 fpBGA

LFE2-12E/12SE					LFE2-20E/20SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential	
E4	PL2A	7	VREF2_7	T (LVDS)*	PL2A	7	VREF2_7	T (LVDS)*	
E5	PL2B	7	VREF1_7	C (LVDS)*	PL2B	7	VREF1_7	C (LVDS)*	
-	-	-			GNDIO7	-			
E3	NC	-			PL4A	7	LDQ8	T (LVDS)*	
F4	PL3A	7		T	PL5A	7	LDQ8	T	
F3	NC	-			PL4B	7	LDQ8	C (LVDS)*	
F5	PL3B	7		C	PL5B	7	LDQ8	C	
VCCIO	VCCIO7	7			VCCIO7	7			
E2	PL4A	7		T (LVDS)*	PL6A	7	LDQ8	T (LVDS)*	
G6	PL5A	7		T	PL7A	7	LDQ8	T	
E1	PL4B	7		C (LVDS)*	PL6B	7	LDQ8	C (LVDS)*	
G7	PL5B	7		C	PL7B	7	LDQ8	C	
GNDIO	GNDIO7	-			GNDIO7	-			
F1	NC	-			PL9A	7	LDQ8	T	
H4	NC	-			PL8A	7	LDQS8	T (LVDS)*	
F2	NC	-			PL9B	7	LDQ8	C	
-	-	-			VCCIO7	7			
H5	NC	-			PL8B	7	LDQ8	C (LVDS)*	
G1	NC	-			PL11A	7	LDQ8	T	
G3	NC	-			PL10A	7	LDQ8	T (LVDS)*	
G2	NC	-			PL11B	7	LDQ8	C	
-	-	-			GNDIO	-			
G4	NC	-			PL10B	7	LDQ8	C (LVDS)*	
J4	PL7A	7	LDQ10	T	PL13A	7	LDQ16	T	
H1	PL6A	7	LDQ10		PL12A	7	LDQ16	T (LVDS)*	
J5	PL7B	7	LDQ10	C	PL13B	7	LDQ16	C	
L6	PL9A	7	LDQ10	T	PL15A	7	LDQ16	T	
VCCIO	VCCIO7	7			VCCIO7	7			
J2	PL8A	7	LDQ10	T (LVDS)*	PL14A	7	LDQ16	T (LVDS)*	
L5	PL9B	7	LDQ10	C	PL15B	7	LDQ16	C	
J1	PL8B	7	LDQ10	C (LVDS)*	PL14B	7	LDQ16	C (LVDS)*	
K3	PL10A	7	LDQS10	T (LVDS)*	PL16A	7	LDQS16	T (LVDS)*	
GNDIO	GNDIO7	-			GNDIO	-			
K4	PL10B	7	LDQ10	C (LVDS)*	PL16B	7	LDQ16	C (LVDS)*	
K2	PL11A	7	LDQ10	T	PL17A	7	LDQ16	T	
VCCIO	VCCIO7	7			VCCIO7	7			
K1	PL11B	7	LDQ10	C	PL17B	7	LDQ16	C	
L4	PL12A	7	LDQ10	T (LVDS)*	PL18A	7	LDQ16	T (LVDS)*	
GNDIO	GNDIO7	-			GNDIO	-			
L3	PL12B	7	LDQ10	C (LVDS)*	PL18B	7	LDQ16	C (LVDS)*	
L2	PL13A	7	PCLKT7_0/LDQ10	T	PL19A	7	PCLKT7_0/LDQ16	T	
L1	PL13B	7	PCLKC7_0/LDQ10	C	PL19B	7	PCLKC7_0/LDQ16	C	
M5	PL15A	6	PCLKT6_0	T (LVDS)*	PL21A	6	PCLKT6_0/LDQ25	T (LVDS)*	
VCCIO	VCCIO6	6			-	-			

LFE2-12E/SE and LFE2-20E/SE Logic Signal Connections: 484 fpBGA (Cont.)

LFE2-12E/12SE					LFE2-20E/20SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
A6	PT21A	0		T	PT30A	0		T
GNDIO	GNDIO0	-			GNDIO0	-		
C7	PT17B	0		C	PT26B	0		C
D10	PT18B	0		C	PT27B	0		C
C6	PT17A	0		T	PT26A	0		T
E10	PT18A	0		T	PT27A	0		T
VCCIO	VCCIO0	0			VCCIO0	0		
F10	PT15B	0		C	PT24B	0		C
B6	PT16B	0		C	PT25B	0		C
D9	PT15A	0		T	PT24A	0		T
B5	PT16A	0		T	PT25A	0		T
GNDIO	GNDIO0	-			GNDIO0	-		
A5	PT13B	0		C	PT22B	0		C
F9	PT14B	0		C	PT23B	0		C
A4	PT13A	0		T	PT22A	0		T
E9	PT14A	0		T	PT23A	0		T
VCCIO	VCCIO0	0			VCCIO0	0		
G8	PT11B	0		C	PT20B	0		C
A3	PT12B	0		C	PT21B	0		C
E8	PT11A	0		T	PT20A	0		T
A2	PT12A	0		T	PT21A	0		T
GNDIO	GNDIO0	-			GNDIO0	-		
-	-	-			VCCIO0	0		
C3	PT10B	0		C	PT10B	0		C
B3	PT10A	0		T	PT10A	0		T
-	-	-			GNDIO0	-		
E7	PT8B	0		C	PT8B	0		C
F8	PT9B	0		C	PT9B	0		C
F7	PT8A	0		T	PT8A	0		T
D7	PT9A	0		T	PT9A	0		T
VCCIO	VCCIO0	0			VCCIO0	0		
D4	PT6B	0		C	PT6B	0		C
D5	PT7B	0		C	PT7B	0		C
C4	PT6A	0		T	PT6A	0		T
D6	PT7A	0		T	PT7A	0		T
GNDIO	GNDIO0	-			GNDIO	-		
J7	PT4B	0		C	PT4B	0		C
B2	PT5B	0		C	PT5B	0		C
H7	PT4A	0		T	PT4A	0		T
B1	PT5A	0		T	PT5A	0		T
VCCIO	VCCIO0	0			VCCIO0	0		
D1	PT2B	0	VREF2_0	C	PT2B	0	VREF2_0	C
D3	PT3B	0		C	PT3B	0		C
C1	PT2A	0	VREF1_0	T	PT2A	0	VREF1_0	T

LFE2-20E/SE and LFE2-35E/SE Logic Signal Connections: 672 fpBGA (Cont.)

LFE2-20E/20SE					LFE2-35E/35SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential	
AE17	PB51B	4	BDQ51	C	PB51B	4	BDQ51	C	
AB19	PB52A	4	BDQ51	T	PB52A	4	BDQ51	T	
AE19	PB52B	4	BDQ51	C	PB52B	4	BDQ51	C	
AF17	PB53A	4	BDQ51	T	PB53A	4	BDQ51	T	
AE18	PB53B	4	BDQ51	C	PB53B	4	BDQ51	C	
VCCIO	VCCIO4	4			VCCIO4	4			
W16	PB54A	4	BDQ51	T	PB54A	4	BDQ51	T	
AA17	PB54B	4	BDQ51	C	PB54B	4	BDQ51	C	
AF18	PB55A	4	BDQ51	T	PB55A	4	BDQ51	T	
AF19	PB55B	4	BDQ51	C	PB55B	4	BDQ51	C	
GND	GNDIO4	-			GNDIO4	-			
AA19	NC	-			PB56A	4	BDQ60	T	
W17	NC	-			PB56B	4	BDQ60	C	
Y19	NC	-			PB57A	4	BDQ60	T	
Y17	NC	-			PB57B	4	BDQ60	C	
AF20	NC	-			NC	-			
VCCIO	VCCIO4	4			VCCIO4	4			
AE20	NC	-			NC	-			
AA20	NC	-			NC	-			
W18	NC	-			NC	-			
AD20	NC	-			NC	-			
GND	GNDIO4	-			GNDIO4	-			
AE21	NC	-			NC	-			
AF21	NC	-			NC	-			
AF22	NC	-			NC	-			
VCCIO	VCCIO4	4			VCCIO4	4			
GND	GNDIO4	-			GNDIO4	-			
AE22	PB56A	4	BDQ60	T	PB65A	4	BDQ69	T	
AD22	PB56B	4	BDQ60	C	PB65B	4	BDQ69	C	
AF23	PB57A	4	BDQ60	T	PB66A	4	BDQ69	T	
AE23	PB57B	4	BDQ60	C	PB66B	4	BDQ69	C	
AD23	PB58A	4	BDQ60	T	PB67A	4	BDQ69	T	
AC23	PB58B	4	BDQ60	C	PB67B	4	BDQ69	C	
VCCIO	VCCIO4	4			VCCIO4	4			
AB20	PB59A	4	BDQ60	T	PB68A	4	BDQ69	T	
AC20	PB59B	4	BDQ60	C	PB68B	4	BDQ69	C	
GND	GNDIO4	-			GNDIO4	-			
AB21	PB60A	4	BDQS60	T	PB69A	4	BDQS69	T	
AC22	PB60B	4	BDQ60	C	PB69B	4	BDQ69	C	
W19	PB61A	4	BDQ60	T	PB70A	4	BDQ69	T	
AA21	PB61B	4	BDQ60	C	PB70B	4	BDQ69	C	
AF24	PB62A	4	BDQ60	T	PB71A	4	BDQ69	T	
AE24	PB62B	4	BDQ60	C	PB71B	4	BDQ69	C	
VCCIO	VCCIO4	4			VCCIO4	4			
Y20	PB63A	4	BDQ60	T	PB72A	4	BDQ69	T	
AB22	PB63B	4	BDQ60	C	PB72B	4	BDQ69	C	

LFE2-70E/SE Logic Signal Connections: 900 fpBGA

LFE2-70E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential
VCCIO	VCCIO7	7		
F4	PL2A	7	VREF2_7	T (LVDS)*
F3	PL2B	7	VREF1_7	C (LVDS)*
H4	PL3A	7		T
G5	PL3B	7		C
GND	GNDIO7	-		
D2	PL4A	7		T (LVDS)*
D1	PL4B	7		C (LVDS)*
E2	PL5A	7		T
VCCIO	VCCIO7	7		
E1	PL5B	7		C
GND	GNDIO7	-		
VCCIO	VCCIO7	7		
F1	PL14A	7	LUM1_SPLLT_IN_A/LDQ12	T (LVDS)*
F2	PL14B	7	LUM1_SPLLC_IN_A/LDQ12	C (LVDS)*
G1	PL15A	7	LUM1_SPLLT_FB_A/LDQ12	T
G2	PL15B	7	LUM1_SPLLC_FB_A/LDQ12	C
GND	GNDIO7	-		
H8	PL18A	7	LDQ21	T
H6	PL18B	7	LDQ21	C
VCCIO	VCCIO7	7		
G4	PL19A	7	LDQ21	T (LVDS)*
G3	PL19B	7	LDQ21	C (LVDS)*
H7	PL20A	7	LDQ21	T
H5	PL20B	7	LDQ21	C
GND	GNDIO7	-		
H2	PL21A	7	LDQS21	T (LVDS)*
H1	PL21B	7	LDQ21	C (LVDS)*
J6	PL22A	7	LDQ21	T
VCCIO	VCCIO7	7		
J8	PL22B	7	LDQ21	C
J2	PL23A	7	LDQ21	T (LVDS)*
J1	PL23B	7	LDQ21	C (LVDS)*
J5	PL24A	7	LDQ21	T
GND	GNDIO7	-		
J7	PL24B	7	LDQ21	C
J4	PL25A	7	LDQ29	T (LVDS)*
J3	PL25B	7	LDQ29	C (LVDS)*
K6	PL26A	7	LDQ29	T
K8	PL26B	7	LDQ29	C
VCCIO	VCCIO7	7		
K2	PL27A	7	LDQ29	T (LVDS)*

LFE2M20E/SE and LFE2M35E/SE Logic Signal Connections: 484 fpBGA (Cont.)

LFE2M20E/SE					LFE2M35E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential	
L4	PL24B	7	LDQ22	C (LVDS)*	PL34B	7	LDQ32	C (LVDS)*	
M1	PL25A	7	PCLKT7_0/LDQ22	T	PL35A	7	PCLKT7_0/LDQ32	T	
GNDIO	GNDIO7	-			GNDIO7	-			
M2	PL25B	7	PCLKC7_0/LDQ22	C	PL35B	7	PCLKC7_0/LDQ32	C	
M6	PL27A	6	PCLKT6_0	T (LVDS)*	PL37A	6	PCLKT6_0	T (LVDS)*	
M5	PL27B	6	PCLKC6_0	C (LVDS)*	PL37B	6	PCLKC6_0	C (LVDS)*	
M3	PL28A	6	VREF2_6	T	PL38A	6	VREF2_6	T	
M4	PL28B	6	VREF1_6	C	PL38B	6	VREF1_6	C	
VCCIO	VCCIO6	6			VCCIO6	6			
N7	PL31A	6	LLM1_SPLLT_IN_A	T (LVDS)*	PL41A	6	LLM2_SPLLT_IN_A	T (LVDS)*	
GNDIO	GNDIO6	-			GNDIO6	-			
N6	PL31B	6	LLM1_SPLLC_IN_A	C (LVDS)*	PL41B	6	LLM2_SPLLC_IN_A	C (LVDS)*	
N1	PL32A	6	LLM1_SPLLT_FB_A	T	PL42A	6	LLM2_SPLLT_FB_A	T	
N2	PL32B	6	LLM1_SPLLC_FB_A	C	PL42B	6	LLM2_SPLLC_FB_A	C	
VCCIO	VCCIO6	6			VCCIO6	6			
GNDIO	GNDIO6	-			GNDIO6	-			
P6	PL38A	6	LDQS38****	T (LVDS)*	PL48A	6	LDQS48****	T (LVDS)*	
N5	PL38B	6	LDQ38	C (LVDS)*	PL48B	6	LDQ48	C (LVDS)*	
P1	PL39A	6	LDQ38	T	PL49A	6	LDQ48	T	
VCCIO	VCCIO6	6			VCCIO6	6			
P2	PL39B	6	LDQ38	C	PL49B	6	LDQ48	C	
P3	PL40A	6	LDQ38	T (LVDS)*	PL50A	6	LDQ48	T (LVDS)*	
P4	PL40B	6	LDQ38	C (LVDS)*	PL50B	6	LDQ48	C (LVDS)*	
P5	PL41A	6	LDQ38	T	PL51A	6	LDQ48	T	
GNDIO	GNDIO6	-			GNDIO6	-			
P7	PL41B	6	LDQ38	C	PL51B	6	LDQ48	C	
R1	PL42A	6	LLM0_GPLLT_IN_A**	T (LVDS)*	PL57A	6	LLM0_GPLLT_IN_A**/LDQS57****	T (LVDS)*	
GNDIO	GNDIO6	-			GNDIO6	-			
R2	PL42B	6	LLM0_GPLLC_IN_A**	C (LVDS)*	PL57B	6	LLM0_GPLLC_IN_A**/LDQ57	C (LVDS)*	
R3	PL43A	6	LLM0_GPLLT_FB_A	T	PL58A	6	LLM0_GPLLT_FB_A/LDQ57	T	
R4	PL43B	6	LLM0_GPLLC_FB_A	C	PL58B	6	LLM0_GPLLC_FB_A/LDQ57	C	
VCCIO	VCCIO6	6			VCCIO6	6			
R6	PL44A	6	LLM0_GDLT_IN_A**	T (LVDS)*	PL59A	6	LLM0_GDLT_IN_A**/LDQ57	T (LVDS)*	
R5	PL44B	6	LLM0_GDLLC_IN_A**	C (LVDS)*	PL59B	6	LLM0_GDLLC_IN_A**/LDQ57	C (LVDS)*	
T1	PL45A	6	LLM0_GDLT_FB_A	T	PL60A	6	LLM0_GDLT_FB_A/LDQ57	T	
T2	PL45B	6	LLM0_GDLLC_FB_A	C	PL60B	6	LLM0_GDLLC_FB_A/LDQ57	C	
GNDIO	GNDIO6	-			GNDIO6	-			
R7	LLM0_PLLCAP	6			LLM0_PLLCAP	6			
T6	PL47A	6	LDQ51	T (LVDS)*	PL62A	6	LDQ66	T (LVDS)*	
T7	PL47B	6	LDQ51	C (LVDS)*	PL62B	6	LDQ66	C (LVDS)*	
U1	PL48A	6	LDQ51	T	PL63A	6	LDQ66	T	
U2	PL48B	6	LDQ51	C	PL63B	6	LDQ66	C	
VCCIO	VCCIO6	6			VCCIO6	6			
T3	PL49A	6	LDQ51	T (LVDS)*	PL64A	6	LDQ66	T (LVDS)*	
U3	PL49B	6	LDQ51	C (LVDS)*	PL64B	6	LDQ66	C (LVDS)*	
U6	PL50A	6	LDQ51	T	NC	-			
U5	PL50B	6	LDQ51	C	PL65B	6	LDQ66	C	
GNDIO	GNDIO6	-			GNDIO6	-			

LFE2M50E/SE Logic Signal Connections: 484 fpBGA (Cont.)

LFE2M50E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential
T1	PL65A	6	LLM0_GDLLT_FB_A	T
T2	PL65B	6	LLM0_GDLLC_FB_A	C
GNDIO	GNDIO6	-		
R7	LLM0_PLLCAP	6		
T6	PL67A	6	LDQ71	T (LVDS)*
T7	PL67B	6	LDQ71	C (LVDS)*
U1	PL68A	6	LDQ71	T
U2	PL68B	6	LDQ71	C
VCCIO	VCCIO6	6		
T3	PL69A	6	LDQ71	T (LVDS)*
U3	PL69B	6	LDQ71	C (LVDS)*
U6	PL70A	6	LDQ71	T
U5	PL70B	6	LDQ71	C
GNDIO	GNDIO6	-		
V5	PL71A	6	LDQS71	T (LVDS)*
U4	PL71B	6	LDQ71	C (LVDS)*
V1	PL72A	6	LDQ71	T
VCCIO	VCCIO6	6		
V3	PL72B	6	LDQ71	C
W1	PL73A	6	LDQ71	T (LVDS)*
Y1	PL73B	6	LDQ71	C (LVDS)*
AA1	PL74A	6	LDQ71	T
GNDIO	GNDIO6	-		
AA2	PL74B	6	LDQ71	C
V4	TCK	-		
Y2	TDI	-		
Y3	TMS	-		
W3	TDO	-		
W4	VCCJ	-		
W5	PB2A	5	BDQ6	T
Y4	PB2B	5	BDQ6	C
W6	PB3A	5	BDQ6	T
V6	PB3B	5	BDQ6	C
AA3	PB4A	5	BDQ6	T
AB2	PB4B	5	BDQ6	C
VCCIO	VCCIO5	5		
T8	PB5A	5	BDQ6	T
U7	PB5B	5	BDQ6	C
GNDIO	GNDIO5	-		
U8	PB6A	5	BDQS6	T
T9	PB6B	5	BDQ6	C
V8	PB7A	5	BDQ6	T
W8	PB7B	5	BDQ6	C

LFE2M35E/SE and LFE2M50E/SE Logic Signal Connections: 672 fpBGA

LFE2M35E/SE					LFE2M50E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential	
C2	PL2A	7	LDQ6	T (LVDS)*	PL2A	7	LDQ6	T*	
C1	PL2B	7	LDQ6	C (LVDS)*	PL2B	7	LDQ6	C*	
F6	PL3A	7	LDQ6	T	PL3A	7	LDQ6	T	
H9	PL3B	7	LDQ6	C	PL3B	7	LDQ6	C	
D3	PL4A	7	LDQ6	T (LVDS)*	PL4A	7	LDQ6	T*	
VCCIO	VCCIO7	7			VCCIO7	7			
D2	PL4B	7	LDQ6	C (LVDS)*	PL4B	7	LDQ6	C*	
F5	PL5A	7	LDQ6	T	PL5A	7	LDQ6	T	
H8	PL5B	7	LDQ6	C	PL5B	7	LDQ6	C	
E3	PL6A	7	LDQS6	T (LVDS)*	PL6A	7	LDQS6	T*	
GNDIO	GNDIO7	-			GNDIO7	-			
E2	PL6B	7	LDQ6	C (LVDS)*	PL6B	7	LDQ6	C*	
J9	PL7A	7	LDQ6	T	PL7A	7	LDQ6	T	
E4	PL7B	7	LDQ6	C	PL7B	7	LDQ6	C	
VCCIO	VCCIO7	7			VCCIO7	7			
E1	PL8A	7	LDQ6	T (LVDS)*	PL8A	7	LDQ6	T*	
D1	PL8B	7	LDQ6	C (LVDS)*	PL8B	7	LDQ6	C*	
J8	PL9A	7	VREF2_7/LDQ6	T	PL9A	7	VREF2_7/LDQ6	T	
F4	PL9B	7	VREF1_7/LDQ6	C	PL9B	7	VREF1_7/LDQ6	C	
GNDIO	GNDIO7	-			GNDIO7	-			
-	-	-			VCCIO7	7			
F3	PL11A	7	LUM0_SPLLT_IN_A/LDQ15	T (LVDS)*	PL11A	7	LUM0_SPLLT_IN_A	T*	
F1	PL11B	7	LUM0_SPLLC_IN_A/LDQ15	C (LVDS)*	PL11B	7	LUM0_SPLLC_IN_A	C*	
G6	PL12A	7	LUM0_SPLLT_FB_A/LDQ15	T	PL12A	7	LUM0_SPLLT_FB_A	T	
K9	PL12B	7	LUM0_SPLLC_FB_A/LDQ15	C	PL12B	7	LUM0_SPLLC_FB_A	C	
-	-	-			GNDIO7	-			
G5	PL13A	7	LDQ15	T (LVDS)*	PL13A	7		T*	
VCCIO	VCCIO7	7			-	-			
G4	PL13B	7	LDQ15	C (LVDS)*	PL13B	7		C*	
H5	PL14A	7	LDQ15	T	PL14A	7		T	
-	-	-			VCCIO7	7			
H6	PL14B	7	LDQ15	C	PL14B	7		C	
GNDIO	GNDIO7	-			GNDIO7	-			
J7	PL16A	7	LDQ15	T	PL19A	7		T	
H4	PL16B	7	LDQ15	C	PL19B	7		C	
H3	PL17A	7	LDQ15	T (LVDS)*	PL20A	7		T*	
VCCIO	VCCIO7	7			VCCIO7	7			
G3	PL17B	7	LDQ15	C (LVDS)*	PL20B	7		C*	
GNDIO	GNDIO7	-			GNDIO7	-			
G1	PL19A	7	LDQ23	T (LVDS)*	PL23A	7	LDQ27	T*	
H1	PL19B	7	LDQ23	C (LVDS)*	PL23B	7	LDQ27	C*	
J3	PL20A	7	LDQ23	T	PL24A	7	LDQ27	T	
J4	PL20B	7	LDQ23	C	PL24B	7	LDQ27	C	
VCCIO	VCCIO7	7			VCCIO7	7			
H2	PL21A	7	LDQ23	T (LVDS)*	PL25A	7	LDQ27	T*	
J2	PL21B	7	LDQ23	C (LVDS)*	PL25B	7	LDQ27	C*	
K7	PL22A	7	LDQ23	T	PL26A	7	LDQ27	T	
J6	PL22B	7	LDQ23	C	PL26B	7	LDQ27	C	

LFE2M35E/SE and LFE2M50E/SE Logic Signal Connections: 672 fpBGA (Cont.)

LFE2M35E/SE					LFE2M50E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential	
AF4	PB17B	5	BDQ15	C	PB17B	5	BDQ15	C	
VCCIO	VCCIO5	5			VCCIO5	5			
AF5	PB18A	5	BDQ15	T	PB18A	5	BDQ15	T	
AF6	PB18B	5	BDQ15	C	PB18B	5	BDQ15	C	
Y12	PB19A	5	BDQ15	T	PB19A	5	BDQ15	T	
GNDIO	GNDIO5	-			GNDIO5	-			
AB11	PB19B	5	BDQ15	C	PB19B	5	BDQ15	C	
-	-	-			VCCIO5	5			
-	-	-			GNDIO5	-			
AD7	PB20A	5	BDQ24	T	PB29A	5	BDQ33	T	
AF7	PB20B	5	BDQ24	C	PB29B	5	BDQ33	C	
AD8	PB21A	5	BDQ24	T	PB30A	5	BDQ33	T	
AA12	PB21B	5	BDQ24	C	PB30B	5	BDQ33	C	
AE8	PB22A	5	BDQ24	T	PB31A	5	BDQ33	T	
VCCIO	VCCIO5	5			VCCIO5	5			
AF8	PB22B	5	BDQ24	C	PB31B	5	BDQ33	C	
AD9	PB23A	5	BDQ24	T	PB32A	5	BDQ33	T	
AC10	PB23B	5	BDQ24	C	PB32B	5	BDQ33	C	
AC11	PB24A	5	BDQS24	T	PB33A	5	BDQS33	T	
GNDIO	GNDIO5	-			GNDIO5	-			
AB12	PB24B	5	BDQ24	C	PB33B	5	BDQ33	C	
AD10	PB25A	5	BDQ24	T	PB34A	5	BDQ33	T	
Y13	PB25B	5	BDQ24	C	PB34B	5	BDQ33	C	
AF9	PB26A	5	BDQ24	T	PB35A	5	BDQ33	T	
VCCIO	VCCIO5	5			VCCIO5	5			
AE9	PB26B	5	BDQ24	C	PB35B	5	BDQ33	C	
AF10	PB27A	5	BDQ24	T	PB36A	5	BDQ33	T	
AE10	PB27B	5	BDQ24	C	PB36B	5	BDQ33	C	
AD11	PB28A	5	BDQ24	T	PB37A	5	BDQ33	T	
GNDIO	GNDIO5	-			GNDIO5	-			
AF11	PB28B	5	BDQ24	C	PB37B	5	BDQ33	C	
VCCIO	VCCIO5	5			VCCIO5	5			
GNDIO	GNDIO5	-			GNDIO5	-			
AA13	PB33A	5	BDQS33****	T	PB42A	5	BDQS42****	T	
AB13	PB33B	5	BDQ33	C	PB42B	5	BDQ42	C	
W14	PB34A	5	VREF2_5/BDQ33	T	PB43A	5	VREF2_5/BDQ42	T	
AC12	PB34B	5	VREF1_5/BDQ33	C	PB43B	5	VREF1_5/BDQ42	C	
AF12	PB35A	5	PCLKT5_0/BDQ33	T	PB44A	5	PCLKT5_0/BDQ42	T	
AD12	PB35B	5	PCLKC5_0/BDQ33	C	PB44B	5	PCLKC5_0/BDQ42	C	
VCCIO	VCCIO5	5			VCCIO5	5			
GNDIO	GNDIO5	-			GNDIO5	-			
AC13	PB40A	4	PCLKT4_0/BDQ42	T	PB49A	4	PCLKT4_0/BDQ51	T	
VCCIO	VCCIO4	4			VCCIO4	4			
Y14	PB40B	4	PCLKC4_0/BDQ42	C	PB49B	4	PCLKC4_0/BDQ51	C	
AB20	PB57A	4	BDQ60	T	PB50A	4	VREF2_4/BDQ51	T	
AC14	PB41B	4	VREF1_4/BDQ42	C	PB50B	4	VREF1_4/BDQ51	C	
AB14	PB42A	4	BDQS42****	T	PB51A	4	BDQS51****	T	
GNDIO	GNDIO4	-			GNDIO4	-			

LFE2M100E/SE Logic Signal Connections: 900 fpBGA

LFE2M100E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential
D2	PL9A	7	VREF2_7	T
D3	PL9B	7	VREF1_7	C
GNDIO	GNDIO7	-		
J8	PL11A	7	LUM0_SPLLT_IN_A/LDQ15	T (LVDS)*
H7	PL11B	7	LUM0_SPLLC_IN_A/LDQ15	C (LVDS)*
E3	PL12A	7	LUM0_SPLLT_FB_A/LDQ15	T
E4	PL12B	7	LUM0_SPLLC_FB_A/LDQ15	C
G6	PL13A	7	LDQ15	T (LVDS)*
F5	PL13B	7	LDQ15	C (LVDS)*
E2	PL14A	7	LDQ15	T
D1	PL14B	7	LDQ15	C
GNDIO	GNDIO7	-		
G5	PL15A	7	LDQS15	T (LVDS)*
G4	PL15B	7	LDQ15	C (LVDS)*
K7	PL16A	7	LDQ15	T
K8	PL16B	7	LDQ15	C
E1	PL17A	7	LDQ15	T (LVDS)*
F2	PL17B	7	LDQ15	C (LVDS)*
F1	PL18A	7	LDQ15	T
GNDIO	GNDIO7	-		
G3	PL18B	7	LDQ15	C
GNDIO	GNDIO7	-		
H5	PL25A	7	LDQ23	T (LVDS)*
H4	PL25B	7	LDQ23	C (LVDS)*
J5	PL26A	7	LDQ23	T
J4	PL26B	7	LDQ23	C
GNDIO	GNDIO7	-		
G2	PL28A	7	LDQ32	T (LVDS)*
G1	PL28B	7	LDQ32	C (LVDS)*
L9	PL29A	7	LDQ32	T
L7	PL29B	7	LDQ32	C
K6	PL30A	7	LDQ32	T (LVDS)*
K5	PL30B	7	LDQ32	C (LVDS)*
L8	PL31A	7	LDQ32	T
L6	PL31B	7	LDQ32	C
GNDIO	GNDIO7	-		
H3	PL32A	7	LDQS32	T (LVDS)*
H2	PL32B	7	LDQ32	C (LVDS)*
N8	PL33A	7	LDQ32	T
M9	PL33B	7	LDQ32	C
J3	PL34A	7	LDQ32	T (LVDS)*
-	-	-		

LFE2M100E/SE Logic Signal Connections: 900 fpBGA (Cont.)

LFE2M100E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential
AG2	PB34A	5	BDQ33	T
AG3	PB34B	5	BDQ33	C
AD13	PB35A	5	BDQ33	T
VCCIO	VCCIO5	5		
AC13	PB35B	5	BDQ33	C
AE14	PB36A	5	BDQ33	T
AC14	PB36B	5	BDQ33	C
AF3	PB37A	5	BDQ33	T
GNDIO	GNDIO5	-		
AF4	PB37B	5	BDQ33	C
-	-	-		
AG4	PB38A	5	BDQ42	T
AG5	PB38B	5	BDQ42	C
GNDIO	GNDIO5	-		
-	-	-		
AD11	PB48A	5	BDQ51	T
AF13	PB48B	5	BDQ51	C
AF12	PB49A	5	BDQ51	T
VCCIO	VCCIO5	5		
AD14	PB49B	5	BDQ51	C
AG8	PB50A	5	BDQ51	T
AF8	PB50B	5	BDQ51	C
AE15	PB51A	5	BDQS51****	T
GNDIO	GNDIO5	-		
-	-	-		
AC15	PB51B	5	BDQ51	C
VCCIO	VCCIO5	5		
GNDIO	GNDIO5	-		
AD15	PB56A	5	BDQ60	T
AF15	PB56B	5	BDQ60	C
AG10	PB57A	5	BDQ60	T
AG9	PB57B	5	BDQ60	C
AH14	PB58A	5	BDQ60	T
AG12	PB58B	5	BDQ60	C
VCCIO	VCCIO5	5		
AG15	PB59A	5	BDQ60	T
AG13	PB59B	5	BDQ60	C
GNDIO	GNDIO5	-		
AF16	PB60A	5	BDQS60	T
AH15	PB60B	5	BDQ60	C
AC16	PB61A	5	VREF2_5/BDQ60	T
AE16	PB61B	5	VREF1_5/BDQ60	C
AG11	PB62A	5	PCLKT5_0/BDQ60	T

LFE2M70E/SE and LFE2M100E/SE Logic Signal Connections: 1152 fpBGA (Cont.)

LFE2M70E/SE				LFE2M100E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
P31	NC	-			PR39B	2		C (LVDS)*
P32	NC	-			PR39A	2		T (LVDS)*
R25	NC	-			PR38B	2		C
-	-	-			VCCIO2	2		
T24	NC	-			PR38A	2		T
N34	NC	-			PR37B	2		C (LVDS)*
N33	NC	-			PR37A	2		T (LVDS)*
GNDIO	GNDIO2	-			GNDIO2	-		
M34	PR31B	2	RDQ28	C	PR35B	2	RDQ32	C
M33	PR31A	2	RDQ28	T	PR35A	2	RDQ32	T
-	-	-			GNDIO2	-		
R24	PR30B	2	RDQ28	C (LVDS)*	PR34B	2	RDQ32	C (LVDS)*
P24	PR30A	2	RDQ28	T (LVDS)*	PR34A	2	RDQ32	T (LVDS)*
N30	PR29B	2	RDQ28	C	PR33B	2	RDQ32	C
M29	PR29A	2	RDQ28	T	PR33A	2	RDQ32	T
VCCIO	VCCIO2	2			VCCIO2	2		
N28	PR28B	2	RDQ28	C (LVDS)*	PR32B	2	RDQ32	C (LVDS)*
N29	PR28A	2	RDQS28	T (LVDS)*	PR32A	2	RDQS32	T (LVDS)*
N24	PR27B	2	RDQ28	C	PR31B	2	RDQ32	C
GNDIO	GNDIO2	-			GNDIO2	-		
N25	PR27A	2	RDQ28	T	PR31A	2	RDQ32	T
M28	PR26B	2	RDQ28	C (LVDS)*	PR30B	2	RDQ32	C (LVDS)*
M27	PR26A	2	RDQ28	T (LVDS)*	PR30A	2	RDQ32	T (LVDS)*
L27	PR25B	2	RDQ28	C	PR29B	2	RDQ32	C
VCCIO	VCCIO2	2			VCCIO2	2		
M26	PR25A	2	RDQ28	T	PR29A	2	RDQ32	T
M32	PR24B	2	RDQ28	C (LVDS)*	PR28B	2	RDQ32	C (LVDS)*
M31	PR24A	2	RDQ28	T (LVDS)*	PR28A	2	RDQ32	T (LVDS)*
GNDIO	GNDIO2	-			GNDIO2	-		
-	-	-			VCCIO2	2		
L34	PR22B	2		C	PR22B	2	RDQ23	C
L33	PR22A	2		T	PR22A	2	RDQ23	T
L32	PR21B	2		C (LVDS)*	PR21B	2	RDQ23	C (LVDS)*
L31	PR21A	2		T (LVDS)*	PR21A	2	RDQ23	T (LVDS)*
VCCIO	VCCIO2	2			VCCIO2	2		
L28	PR20B	2		C	PR20B	2	RDQ23	C
L29	PR20A	2		T	PR20A	2	RDQ23	T
M30	PR19B	2		C (LVDS)*	PR19B	2	RDQ23	C (LVDS)*
L30	PR19A	2		T (LVDS)*	PR19A	2	RDQ23	T (LVDS)*
K34	PR18B	2	RDQ15	C	PR18B	2	RDQ15	C
K33	PR18A	2	RDQ15	T	PR18A	2	RDQ15	T
GNDIO	GNDIO2	-			GNDIO2	-		
K30	PR17B	2	RDQ15	C (LVDS)*	PR17B	2	RDQ15	C (LVDS)*
K29	PR17A	2	RDQ15	T (LVDS)*	PR17A	2	RDQ15	T (LVDS)*
J34	PR16B	2	RDQ15	C	PR16B	2	RDQ15	C
J33	PR16A	2	RDQ15	T	PR16A	2	RDQ15	T
VCCIO	VCCIO2	2			VCCIO2	2		
J32	PR15B	2	RDQ15	C (LVDS)*	PR15B	2	RDQ15	C (LVDS)*
J31	PR15A	2	RDQS15	T (LVDS)*	PR15A	2	RDQS15	T (LVDS)*

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2-35SE-5F484C	331	1.2V	-5	fpBGA	484	Com	35
LFE2-35SE-6F484C	331	1.2V	-6	fpBGA	484	Com	35
LFE2-35SE-7F484C	331	1.2V	-7	fpBGA	484	Com	35
LFE2-35SE-5F672C	450	1.2V	-5	fpBGA	672	Com	35
LFE2-35SE-6F672C	450	1.2V	-6	fpBGA	672	Com	35
LFE2-35SE-7F672C	450	1.2V	-7	fpBGA	672	Com	35

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2-50SE-5F484C	339	1.2V	-5	fpBGA	484	Com	50
LFE2-50SE-6F484C	339	1.2V	-6	fpBGA	484	Com	50
LFE2-50SE-7F484C	339	1.2V	-7	fpBGA	484	Com	50
LFE2-50SE-5F672C	500	1.2V	-5	fpBGA	672	Com	50
LFE2-50SE-6F672C	500	1.2V	-6	fpBGA	672	Com	50
LFE2-50SE-7F672C	500	1.2V	-7	fpBGA	672	Com	50

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2-70SE-5F672C	500	1.2V	-5	fpBGA	672	Com	70
LFE2-70SE-6F672C	500	1.2V	-6	fpBGA	672	Com	70
LFE2-70SE-7F672C	500	1.2V	-7	fpBGA	672	Com	70
LFE2-70SE-5F900C	583	1.2V	-5	fpBGA	900	Com	70
LFE2-70SE-6F900C	583	1.2V	-6	fpBGA	900	Com	70
LFE2-70SE-7F900C	583	1.2V	-7	fpBGA	900	Com	70

Industrial

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2-6SE-5T144I	90	1.2V	-5	TQFP	144	Ind	6
LFE2-6SE-6T144I	90	1.2V	-6	TQFP	144	Ind	6
LFE2-6SE-5F256I	190	1.2V	-5	fpBGA	256	Ind	6
LFE2-6SE-6F256I	190	1.2V	-6	fpBGA	256	Ind	6

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2-12SE-5T144I	93	1.2V	-5	TQFP	144	Ind	12
LFE2-12SE-6T144I	93	1.2V	-6	TQFP	144	Ind	12
LFE2-12SE-5Q208I	131	1.2V	-5	PQFP	208	Ind	12
LFE2-12SE-6Q208I	131	1.2V	-6	PQFP	208	Ind	12
LFE2-12SE-5F256I	193	1.2V	-5	fpBGA	256	Ind	12
LFE2-12SE-6F256I	193	1.2V	-6	fpBGA	256	Ind	12
LFE2-12SE-5F484I	297	1.2V	-5	fpBGA	484	Ind	12
LFE2-12SE-6F484I	297	1.2V	-6	fpBGA	484	Ind	12

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2-20SE-5QN208I	131	1.2V	-5	Lead-Free PQFP	208	Ind	20
LFE2-20SE-6QN208I	131	1.2V	-6	Lead-Free PQFP	208	Ind	20
LFE2-20SE-5FN256I	193	1.2V	-5	Lead-Free fpBGA	256	Ind	20
LFE2-20SE-6FN256I	193	1.2V	-6	Lead-Free fpBGA	256	Ind	20
LFE2-20SE-5FN484I	331	1.2V	-5	Lead-Free fpBGA	484	Ind	20
LFE2-20SE-6FN484I	331	1.2V	-6	Lead-Free fpBGA	484	Ind	20
LFE2-20SE-5FN672I	402	1.2V	-5	Lead-Free fpBGA	672	Ind	20
LFE2-20SE-6FN672I	402	1.2V	-6	Lead-Free fpBGA	672	Ind	20

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2-35SE-5FN484I	331	1.2V	-5	Lead-Free fpBGA	484	Ind	35
LFE2-35SE-6FN484I	331	1.2V	-6	Lead-Free fpBGA	484	Ind	35
LFE2-35SE-5FN672I	450	1.2V	-5	Lead-Free fpBGA	672	Ind	35
LFE2-35SE-6FN672I	450	1.2V	-6	Lead-Free fpBGA	672	Ind	35

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2-50SE-5FN484I	339	1.2V	-5	Lead-Free fpBGA	484	Ind	50
LFE2-50SE-6FN484I	339	1.2V	-6	Lead-Free fpBGA	484	Ind	50
LFE2-50SE-5FN672I	500	1.2V	-5	Lead-Free fpBGA	672	Ind	50
LFE2-50SE-6FN672I	500	1.2V	-6	Lead-Free fpBGA	672	Ind	50

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2-70SE-5FN672I	500	1.2V	-5	Lead-Free fpBGA	672	Ind	70
LFE2-70SE-6FN672I	500	1.2V	-6	Lead-Free fpBGA	672	Ind	70
LFE2-70SE-5FN900I	583	1.2V	-5	Lead-Free fpBGA	900	Ind	70
LFE2-70SE-6FN900I	583	1.2V	-6	Lead-Free fpBGA	900	Ind	70

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2M100SE-5FN1152C	520	1.2V	-5	Lead-Free fpBGA	1152	Com	100
LFE2M100SE-6FN1152C	520	1.2V	-6	Lead-Free fpBGA	1152	Com	100
LFE2M100SE-7FN1152C	520	1.2V	-7	Lead-Free fpBGA	1152	Com	100
LFE2M100SE-5FN900C	416	1.2V	-5	Lead-Free fpBGA	900	Com	100
LFE2M100SE-6FN900C	416	1.2V	-6	Lead-Free fpBGA	900	Com	100
LFE2M100SE-7FN900C	416	1.2V	-7	Lead-Free fpBGA	900	Com	100