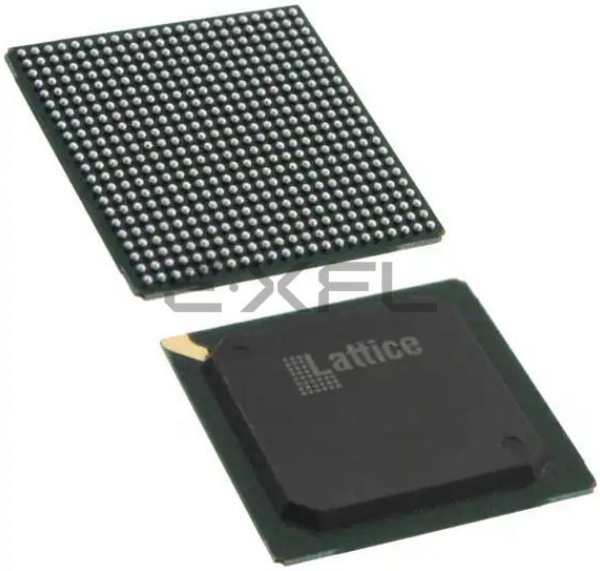
Lattice Semiconductor Corporation - LFE2M20E-6F484I Datasheet



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Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	2375
Number of Logic Elements/Cells	19000
Total RAM Bits	1246208
Number of I/O	304
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	484-BBGA
Supplier Device Package	484-FPBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfe2m20e-6f484i

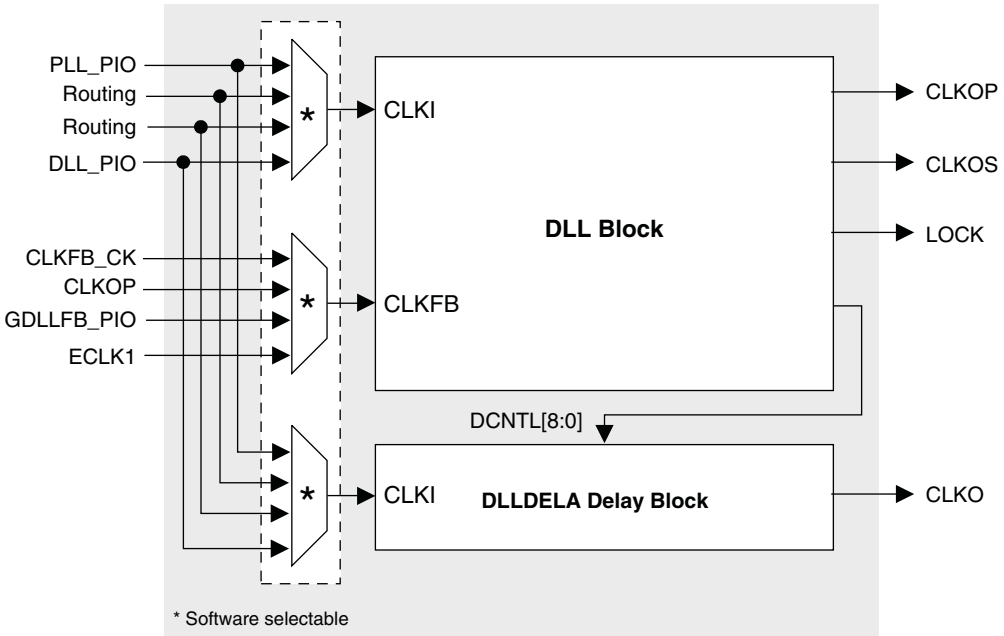
Table 2-5. DLL Signals

Signal	I/O	Description
CLKI	I	Clock input from external pin or routing
CLKFB	I	DLL feed input from DLL output, clock net, routing or external pin
RSTN	I	Active low synchronous reset
ALUHOLD	I	Active high freezes the ALU
UDDCNTL	I	Synchronous enable signal (hold high for two cycles) from routing
DCNTL[8:0]	O	Encoded digital control signals for PIC INDEL and slave delay calibration
CLKOP	O	The primary clock output
CLKOS	O	The secondary clock output with fine phase shift and/or division by 2 or by 4
LOCK	O	Active high phase lock indicator

DLLDELA Delay Block

Closely associated with each DLL is a DLLDELA block. This is a delay block consisting of a delay line with taps and a selection scheme that selects one of the taps. The DCNTL[8:0] bus controls the delay of the CLKO signal. Typically this is the delay setting that the DLL uses to achieve phase alignment. This results in the delay providing a calibrated 90° phase shift that is useful in centering a clock in the middle of a data cycle for source synchronous data. The CLKO signal feeds the edge clock network. Figure 2-7 shows the connections between the DLL block and the DLLDELA delay block. For more information, please see the list of additional technical documentation at the end of this data sheet.

Figure 2-7. DLLDELA Delay Block

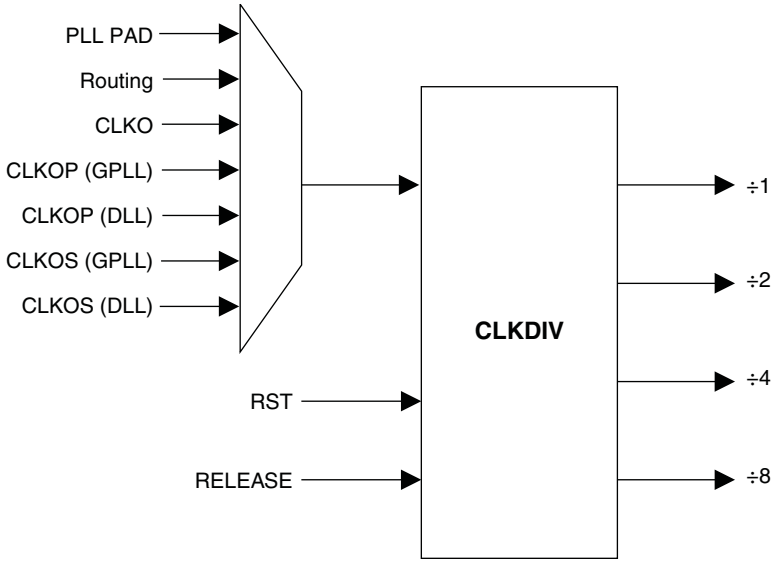


PLL/DLL Cascading

LatticeECP2/M devices have been designed to allow certain combinations of PLL (GPLL and SPLL) and DLL cascading. The allowable combinations are:

- PLL to PLL supported
- PLL to DLL supported

Figure 2-9. Clock Divider Connections



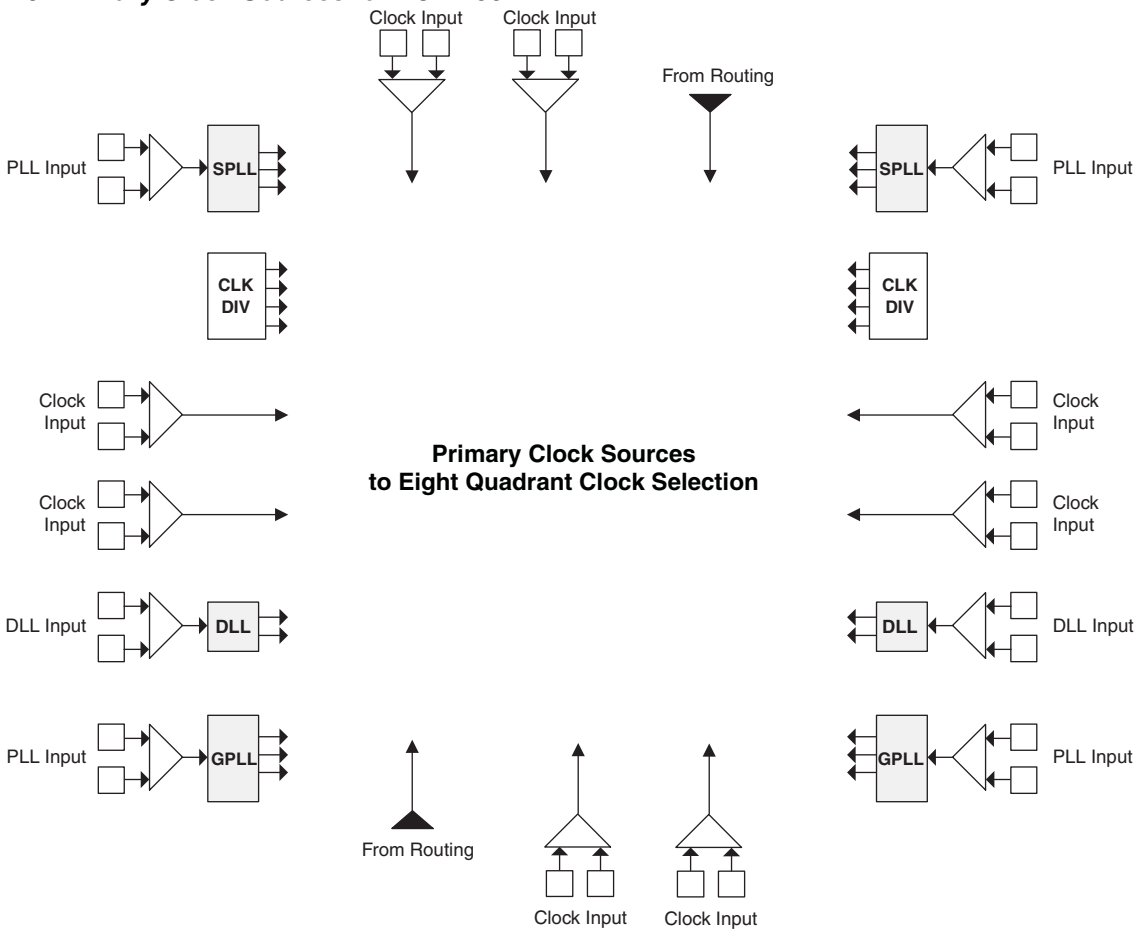
Clock Distribution Network

LatticeECP2/M devices have eight quadrant-based primary clocks and eight flexible region-based secondary clocks/control signals. Two high performance edge clocks are available on each edge of the device to support high speed interfaces. These clock inputs are selected from external I/Os, the sysCLOCK PLLs, DLLs or routing. These clock inputs are fed throughout the chip via a clock distribution system.

Primary Clock Sources

LatticeECP2/M devices derive clocks from five primary sources: PLL (GPLL and SPLL) outputs, DLL outputs, CLKDIV outputs, dedicated clock inputs and routing. LatticeECP2/M devices have two to eight sysCLOCK PLLs and two DLLs, located on the left and right sides of the device. There are eight dedicated clock inputs, two on each side of the device, with the exception of the LatticeECP2M 256-fpBGA package devices which have six dedicated clock inputs on the device. Figure 2-10 shows the primary clock sources.

Figure 2-10. Primary Clock Sources for ECP2-50

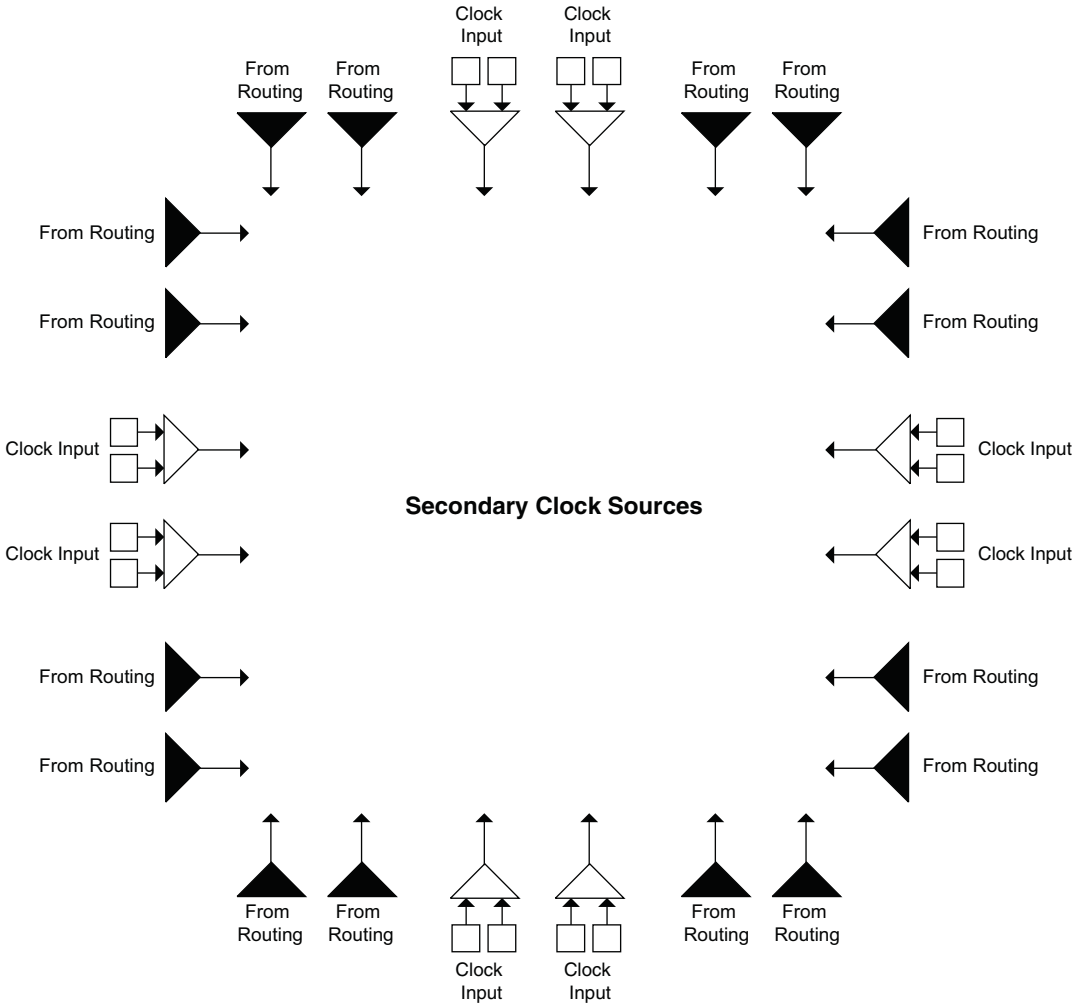


Note: This diagram shows sources for the ECP2-50 device. Smaller LatticeECP2 devices have fewer SPLLs. All LatticeECP2M devices have six SPLLs.

Secondary Clock/Control Sources

LatticeECP2/M devices derive secondary clocks (SC0 through SC7) from eight dedicated clock input pads and the rest from routing. Figure 2-11 shows the secondary clock sources.

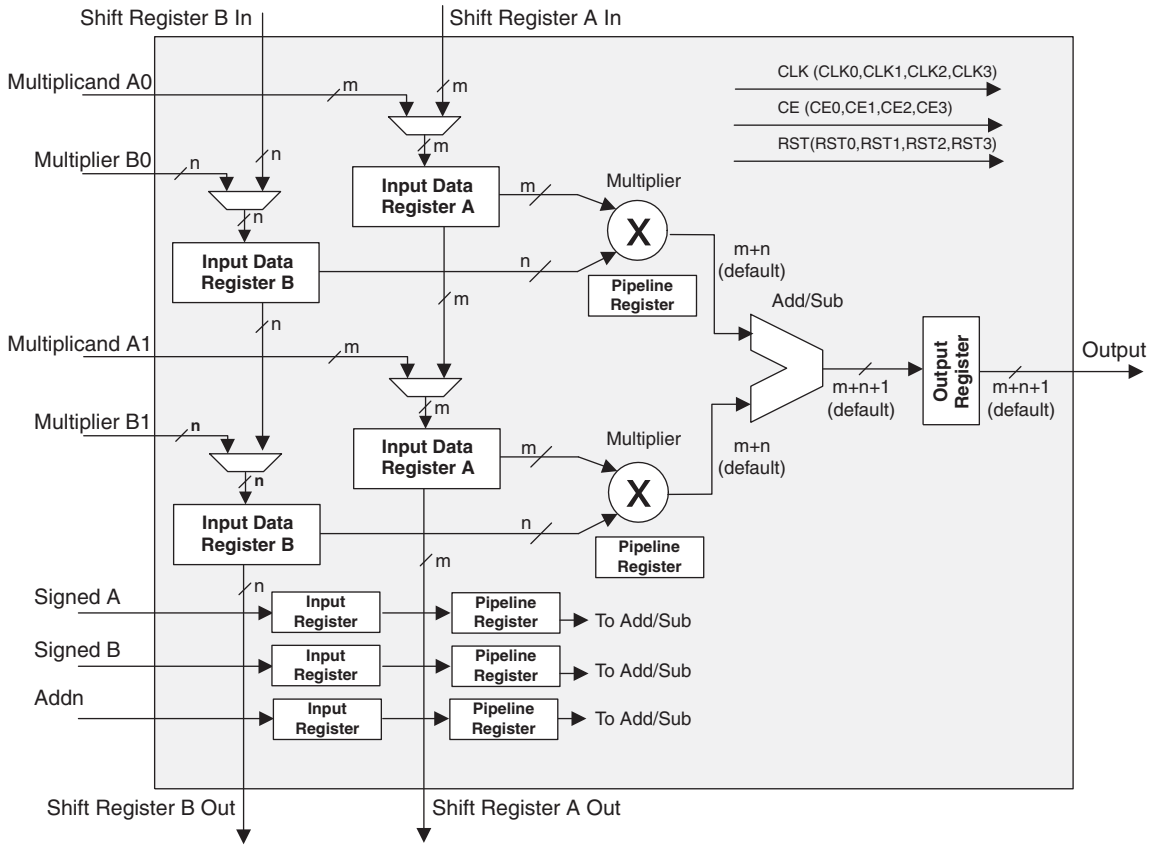
Figure 2-11. Secondary Clock Sources



MULTADDSUB sysDSP Element

In this case, the operands A0 and B0 are multiplied and the result is added/subtracted with the result of the multiplier operation of operands A1 and A2. The user can enable the input, output and pipeline registers. Figure 2-25 shows the MULTADDSUB sysDSP element.

Figure 2-25. MULTADDSUB



LFE2-12E/SE and LFE2-20E/SE Logic Signal Connections: 208 PQFP (Cont.)

LFE2-12E/SE					LFE2-20E/SE			
Pin Number	Pin/Pad Function	Bank	Dual Function	Differential	Pin/Pad Function	Bank	Dual Function	Differential
46	PL28B	6	LDQ28	C (LVDS)*	PL42B	6	LDQ42	C (LVDS)*
47	PL30A	6	LDQ28		PL44A	6	LDQ42	
48	TCK	-			TCK	-		
49	TDI	-			TDI	-		
50	TDO	-			TDO	-		
51	VCCJ	-			VCCJ	-		
52	TMS	-			TMS	-		
53	PB2A	5	VREF2_5/BDQ6	T	PB2A	5	VREF2_5/BDQ6	T
54	PB2B	5	VREF1_5/BDQ6	C	PB2B	5	VREF1_5/BDQ6	C
55	VCCIO5	5			VCCIO5	5		
56	PB6A	5	BDQS6	T	PB6A	5	BDQS6	T
57	PB6B	5	BDQ6	C	PB6B	5	BDQ6	C
58	PB8A	5	BDQ6	T	PB8A	5	BDQ6	T
59	PB8B	5	BDQ6	C	PB8B	5	BDQ6	C
60	GND	-			GND	-		
61	PB12A	5	BDQ15	T	PB12A	5	BDQ15	T
62	PB12B	5	BDQ15	C	PB12B	5	BDQ15	C
63	VCCIO5	5			VCCIO5	5		
64	PB16A	5	BDQ15	T	PB16A	5	BDQ15	T
65	PB16B	5	BDQ15	C	PB16B	5	BDQ15	C
66	PB18A	5	BDQ15	T	PB18A	5	BDQ15	T
67	PB18B	5	BDQ15	C	PB18B	5	BDQ15	C
68	GND	-			GND	-		
69	PB20A	5	BDQ24	T	PB30A	5	BDQ33	T
70	VCCAUX	-			VCCAUX	-		
71	PB20B	5	BDQ24	C	PB30B	5	BDQ33	C
72	PB22A	5	BDQ24	T	PB32A	5	BDQ33	T
73	PB22B	5	BDQ24	C	PB32B	5	BDQ33	C
74	VCC	-			VCC	-		
75	PB26A	5	PCLKT5_0/BDQ24	T	PB35A	5	PCLKT5_0/BDQ33	T
76	PB26B	5	PCLKC5_0/BDQ24	C	PB35B	5	PCLKC5_0/BDQ33	C
77	GND	-			GND	-		
78	PB31A	4	PCLKT4_0/BDQ33	T	PB40A	4	PCLKT4_0/BDQ42	T
79	PB31B	4	PCLKC4_0/BDQ33	C	PB40B	4	PCLKC4_0/BDQ42	C
80	VCC	-			VCC	-		
81	GND	-			GND	-		
82	PB34A	4	BDQ33	T	PB42A	4	BDQS42	T
83	PB34B	4	BDQ33	C	PB42B	4	BDQ42	C
84	PB36A	4	BDQ33	T	PB44A	4	BDQ42	T
85	PB36B	4	BDQ33	C	PB44B	4	BDQ42	C
86	VCCAUX	-			VCCAUX	-		
87	PB40A	4	BDQ42	T	PB50A	4	BDQ51	T
88	PB40B	4	BDQ42	C	PB50B	4	BDQ51	C
89	GND	-			GND	-		
90	PB42A	4	BDQS42	T	PB52A	4	BDQ51	T
91	PB42B	4	BDQ42	C	PB52B	4	BDQ51	C

LFE2-12E/SE and LFE2-20E/SE Logic Signal Connections: 484 fpBGA (Cont.)

LFE2-12E/12SE					LFE2-20E/20SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
H16	NC	-			NC	-		
H20	NC	-			NC	-		
H18	NC	-			NC	-		
K6	NC	-			NC	-		
J16	NC	-			NC	-		
N18	VCC	-			VCC	-		
N6	VCC	-			VCC	-		

* Supports true LVDS. Other differential signals must be emulated with external resistors.
** These dedicated input pins can be used for GPLLs or GDLLs within the respective quadrant.

Note: VCCIO and GND pads are used to determine the average DC current drawn by I/Os between GND/VCCIO connections, or between the last GND/VCCIO in an I/O bank and the end of an I/O bank. The substrate pads listed in the Pin Table do not necessarily have a one to one connection with a package ball or pin.

LFE2-20E/SE and LFE2-35E/SE Logic Signal Connections: 672 fpBGA (Cont.)

LFE2-20E/20SE					LFE2-35E/35SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
AE17	PB51B	4	BDQ51	C	PB51B	4	BDQ51	C
AB19	PB52A	4	BDQ51	T	PB52A	4	BDQ51	T
AE19	PB52B	4	BDQ51	C	PB52B	4	BDQ51	C
AF17	PB53A	4	BDQ51	T	PB53A	4	BDQ51	T
AE18	PB53B	4	BDQ51	C	PB53B	4	BDQ51	C
VCCIO	VCCIO4	4			VCCIO4	4		
W16	PB54A	4	BDQ51	T	PB54A	4	BDQ51	T
AA17	PB54B	4	BDQ51	C	PB54B	4	BDQ51	C
AF18	PB55A	4	BDQ51	T	PB55A	4	BDQ51	T
AF19	PB55B	4	BDQ51	C	PB55B	4	BDQ51	C
GND	GNDIO4	-			GNDIO4	-		
AA19	NC	-			PB56A	4	BDQ60	T
W17	NC	-			PB56B	4	BDQ60	C
Y19	NC	-			PB57A	4	BDQ60	T
Y17	NC	-			PB57B	4	BDQ60	C
AF20	NC	-			NC	-		
VCCIO	VCCIO4	4			VCCIO4	4		
AE20	NC	-			NC	-		
AA20	NC	-			NC	-		
W18	NC	-			NC	-		
AD20	NC	-			NC	-		
GND	GNDIO4	-			GNDIO4	-		
AE21	NC	-			NC	-		
AF21	NC	-			NC	-		
AF22	NC	-			NC	-		
VCCIO	VCCIO4	4			VCCIO4	4		
GND	GNDIO4	-			GNDIO4	-		
AE22	PB56A	4	BDQ60	T	PB65A	4	BDQ69	T
AD22	PB56B	4	BDQ60	C	PB65B	4	BDQ69	C
AF23	PB57A	4	BDQ60	T	PB66A	4	BDQ69	T
AE23	PB57B	4	BDQ60	C	PB66B	4	BDQ69	C
AD23	PB58A	4	BDQ60	T	PB67A	4	BDQ69	T
AC23	PB58B	4	BDQ60	C	PB67B	4	BDQ69	C
VCCIO	VCCIO4	4			VCCIO4	4		
AB20	PB59A	4	BDQ60	T	PB68A	4	BDQ69	T
AC20	PB59B	4	BDQ60	C	PB68B	4	BDQ69	C
GND	GNDIO4	-			GNDIO4	-		
AB21	PB60A	4	BDQS60	T	PB69A	4	BDQS69	T
AC22	PB60B	4	BDQ60	C	PB69B	4	BDQ69	C
W19	PB61A	4	BDQ60	T	PB70A	4	BDQ69	T
AA21	PB61B	4	BDQ60	C	PB70B	4	BDQ69	C
AF24	PB62A	4	BDQ60	T	PB71A	4	BDQ69	T
AE24	PB62B	4	BDQ60	C	PB71B	4	BDQ69	C
VCCIO	VCCIO4	4			VCCIO4	4		
Y20	PB63A	4	BDQ60	T	PB72A	4	BDQ69	T
AB22	PB63B	4	BDQ60	C	PB72B	4	BDQ69	C

LFE2-20E/SE and LFE2-35E/SE Logic Signal Connections: 672 fpBGA (Cont.)

LFE2-20E/20SE					LFE2-35E/35SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
Y21	PB64A	4	VREF2_4/BDQ60	T	PB73A	4	VREF2_4/BDQ69	T
AB23	PB64B	4	VREF1_4/BDQ60	C	PB73B	4	VREF1_4/BDQ69	C
GND	GNDIO4	-			GNDIO4	-		
AD24	CFG2	8			CFG2	8		
W20	CFG1	8			CFG1	8		
AC24	CFG0	8			CFG0	8		
V19	PROGRAMN	8			PROGRAMN	8		
AA22	CCLK	8			CCLK	8		
AB24	INITN	8			INITN	8		
AD25	DONE	8			DONE	8		
GND	GNDIO8	-			GNDIO8	-		
W21	PR44B	8	WRITEN	C	PR58B	8	WRITEN	C
Y22	PR44A	8	CS1N	T	PR58A	8	CS1N	T
AC25	PR43B	8	CSN	C	PR57B	8	CSN	C
AB25	PR43A	8	D0/SPIFASTN	T	PR57A	8	D0/SPIFASTN	T
VCCIO	VCCIO8	8			VCCIO8	8		
AD26	PR42B	8	D1	C	PR56B	8	D1	C
AC26	PR42A	8	D2	T	PR56A	8	D2	T
Y23	PR41B	8	D3	C	PR55B	8	D3	C
GND	GNDIO8	-			GNDIO8	-		
W22	PR41A	8	D4	T	PR55A	8	D4	T
AA25	PR40B	8	D5	C	PR54B	8	D5	C
AB26	PR40A	8	D6	T	PR54A	8	D6	T
W23	PR39B	8	D7/SPID0	C	PR53B	8	D7/SPID0	C
VCCIO	VCCIO8	8			VCCIO8	8		
V22	PR39A	8	DI/CSSPI0N	T	PR53A	8	DI/CSSPI0N	T
Y24	PR38B	8	DOUT/CSON	C	PR52B	8	DOUT/CSON	C
Y25	PR38A	8	BUSY/SISPI	T	PR52A	8	BUSY/SISPI	T
W24	PR37B	3	RDQ34	C	PR51B	3	RDQ48	C
GND	GNDIO3	-			GNDIO3	-		
V23	PR37A	3	RDQ34	T	PR51A	3	RDQ48	T
AA26	PR36B	3	RDQ34	C (LVDS)*	PR50B	3	RDQ48	C (LVDS)*
Y26	PR36A	3	RDQ34	T (LVDS)*	PR50A	3	RDQ48	T (LVDS)*
U21	PR35B	3	RDQ34	C	PR49B	3	RDQ48	C
VCCIO	VCCIO3	3			VCCIO3	3		
U19	PR35A	3	RDQ34	T	PR49A	3	RDQ48	T
W25	PR34B	3	RDQ34	C (LVDS)*	PR48B	3	RDQ48	C (LVDS)*
W26	PR34A	3	RDQS34	T (LVDS)*	PR48A	3	RDQS48	T (LVDS)*
GND	GNDIO3	-			GNDIO3	-		
V24	PR33B	3	RDQ34	C	PR47B	3	RDQ48	C
V25	PR33A	3	RDQ34	T	PR47A	3	RDQ48	T
V26	PR32B	3	RDQ34	C (LVDS)*	PR46B	3	RDQ48	C (LVDS)*
U26	PR32A	3	RDQ34	T (LVDS)*	PR46A	3	RDQ48	T (LVDS)*
VCCIO	VCCIO3	3			VCCIO3	3		
U22	PR31B	3	RLM0_GPLLC_FB_A/RDQ34	C	PR45B	3	RLM0_GPLLC_FB_A/RDQ48	C
U23	PR31A	3	RLM0_GPLLT_FB_A/RDQ34	T	PR45A	3	RLM0_GPLLT_FB_A/RDQ48	T

LFE2-50E/SE and LFE2-70E/SE Logic Signal Connections: 672 fpBGA (Cont.)

LFE2-50E/SE					LFE2-70E/SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
L23	VCCIO2	2			VCCIO2	2		
M17	VCCIO2	2			VCCIO2	2		
M18	VCCIO2	2			VCCIO2	2		
AA23	VCCIO3	3			VCCIO3	3		
R17	VCCIO3	3			VCCIO3	3		
R18	VCCIO3	3			VCCIO3	3		
T23	VCCIO3	3			VCCIO3	3		
V20	VCCIO3	3			VCCIO3	3		
AC16	VCCIO4	4			VCCIO4	4		
AC21	VCCIO4	4			VCCIO4	4		
U15	VCCIO4	4			VCCIO4	4		
V15	VCCIO4	4			VCCIO4	4		
Y18	VCCIO4	4			VCCIO4	4		
AC11	VCCIO5	5			VCCIO5	5		
AC6	VCCIO5	5			VCCIO5	5		
U12	VCCIO5	5			VCCIO5	5		
V12	VCCIO5	5			VCCIO5	5		
Y9	VCCIO5	5			VCCIO5	5		
AA4	VCCIO6	6			VCCIO6	6		
R10	VCCIO6	6			VCCIO6	6		
R9	VCCIO6	6			VCCIO6	6		
T4	VCCIO6	6			VCCIO6	6		
V7	VCCIO6	6			VCCIO6	6		
F4	VCCIO7	7			VCCIO7	7		
J7	VCCIO7	7			VCCIO7	7		
L4	VCCIO7	7			VCCIO7	7		
M10	VCCIO7	7			VCCIO7	7		
M9	VCCIO7	7			VCCIO7	7		
AE25	VCCIO8	8			VCCIO8	8		
V18	VCCIO8	8			VCCIO8	8		
J10	VCCAUX	-			VCCAUX	-		
J11	VCCAUX	-			VCCAUX	-		
J16	VCCAUX	-			VCCAUX	-		
J17	VCCAUX	-			VCCAUX	-		
K18	VCCAUX	-			VCCAUX	-		
K9	VCCAUX	-			VCCAUX	-		
L18	VCCAUX	-			VCCAUX	-		
L9	VCCAUX	-			VCCAUX	-		
T18	VCCAUX	-			VCCAUX	-		
T9	VCCAUX	-			VCCAUX	-		
U18	VCCAUX	-			VCCAUX	-		
U9	VCCAUX	-			VCCAUX	-		
V10	VCCAUX	-			VCCAUX	-		
V11	VCCAUX	-			VCCAUX	-		
V16	VCCAUX	-			VCCAUX	-		
V17	VCCAUX	-			VCCAUX	-		

LFE2-70E/SE Logic Signal Connections: 900 fpBGA (Cont.)

LFE2-70E/SE				
Ball Number	**Ball/Pad Function**	**Bank**	**Dual Function**	**Differential**
W18	GND	-		
W19	GND	-		
Y14	GND	-		
Y15	GND	-		
Y16	GND	-		
Y17	GND	-		
A2	NC	-		
A3	NC	-		
A4	NC	-		
A5	NC	-		
AB28	NC	-		
AC4	NC	-		
AD23	NC	-		
AE1	NC	-		
AE2	NC	-		
AE29	NC	-		
AE3	NC	-		
AE30	NC	-		
AE4	NC	-		
AE5	NC	-		
AE6	NC	-		
AF1	NC	-		
AF2	NC	-		
AF23	NC	-		
AF26	NC	-		
AF27	NC	-		
AF28	NC	-		
AF29	NC	-		
AF3	NC	-		
AF30	NC	-		
AF4	NC	-		
AF5	NC	-		
AG1	NC	-		
AG13	NC	-		
AG16	NC	-		
AG18	NC	-		
AG2	NC	-		
AG26	NC	-		
AG27	NC	-		
AG28	NC	-		
AG29	NC	-		
AG3	NC	-		
AG30	NC	-		

LFE2M20E/SE and LFE2M35E/SE Logic Signal Connections: 484 fpBGA (Cont.)

LFE2M20E/SE					LFE2M35E/SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
E13	PT28B	1		C	PT46B	1		C
D12	PT28A	1		T	PT46A	1		T
GNDIO	GNDIO1	-			GNDIO1	-		
A9	PT27B	1		C	PT45B	1		C
A8	PT27A	1		T	PT45A	1		T
A7	PT26B	1		C	PT44B	1		C
A6	PT26A	1		T	PT44A	1		T
VCCIO	VCCIO1	1			VCCIO1	1		
E12	PT25B	1		C	PT43B	1		C
F12	PT25A	1		T	PT43A	1		T
A5	PT24B	1		C	PT42B	1		C
A4	PT24A	1		T	PT42A	1		T
GNDIO	GNDIO1	-			GNDIO1	-		
B7	PT23B	1		C	PT41B	1		C
B8	PT23A	1		T	PT41A	1		T
G11	PT22B	1		C	PT40B	1		C
E11	PT22A	1		T	PT40A	1		T
VCCIO	VCCIO1	1			VCCIO1	1		
D11	PT21B	1	VREF2_1	C	PT39B	1	VREF2_1	C
D10	PT21A	1	VREF1_1	T	PT39A	1	VREF1_1	T
F11	PT20A	1	PCLKT1_0	T	PT38A	1	PCLKT1_0	T
G10	PT20B	1	PCLKC1_0	C	PT38B	1	PCLKC1_0	C
G9	PT19B	0	PCLKC0_0	C	PT37B	0	PCLKC0_0	C
GNDIO	GNDIO0	-			GNDIO0	-		
F9	PT19A	0	PCLKT0_0	T	PT37A	0	PCLKT0_0	T
C9	PT18B	0	VREF2_0	C	PT36B	0	VREF2_0	C
D9	PT18A	0	VREF1_0	T	PT36A	0	VREF1_0	T
A2	PT17B	0		C	PT35B	0		C
VCCIO	VCCIO0	0			VCCIO0	0		
A3	PT17A	0		T	PT35A	0		T
B3	PT16B	0		C	PT34B	0		C
C4	PT16A	0		T	PT34A	0		T
E10	PT15B	0		C	PT33B	0		C
F10	PT15A	0		T	PT33A	0		T
C7	PT14B	0		C	PT32B	0		C
GNDIO	GNDIO0	-			GNDIO0	-		
B6	PT14A	0		T	PT32A	0		T
C6	PT13B	0		C	PT31B	0		C
VCCIO	VCCIO0	0			VCCIO0	0		
C5	PT13A	0		T	PT31A	0		T
C8	PT12B	0		C	PT30B	0		C
D8	PT12A	0		T	PT30A	0		T
E8	PT11B	0		C	PT29B	0		C
E9	PT11A	0		T	PT29A	0		T
-	-	-			GNDIO0	-		
-	-	-			VCCIO0	0		
F8	PT10B	0		C	PT10B	0		C
G8	PT10A	0		T	PT10A	0		T

LFE2M20E/SE and LFE2M35E/SE Logic Signal Connections: 484 fpBGA (Cont.)

LFE2M20E/SE					LFE2M35E/SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
G18	VCCIO2	2			VCCIO2	2		
J15	VCCIO2	2			VCCIO2	2		
K19	VCCIO2	2			VCCIO2	2		
N19	VCCIO3	3			VCCIO3	3		
P15	VCCIO3	3			VCCIO3	3		
T18	VCCIO3	3			VCCIO3	3		
V21	VCCIO3	3			VCCIO3	3		
AA18	VCCIO4	4			VCCIO4	4		
R14	VCCIO4	4			VCCIO4	4		
V16	VCCIO4	4			VCCIO4	4		
W13	VCCIO4	4			VCCIO4	4		
AA5	VCCIO5	5			VCCIO5	5		
R9	VCCIO5	5			VCCIO5	5		
V7	VCCIO5	5			VCCIO5	5		
W10	VCCIO5	5			VCCIO5	5		
N4	VCCIO6	6			VCCIO6	6		
P8	VCCIO6	6			VCCIO6	6		
T5	VCCIO6	6			VCCIO6	6		
V2	VCCIO6	6			VCCIO6	6		
E2	VCCIO7	7			VCCIO7	7		
G5	VCCIO7	7			VCCIO7	7		
J8	VCCIO7	7			VCCIO7	7		
K4	VCCIO7	7			VCCIO7	7		
AA22	VCCIO8	8			VCCIO8	8		
U19	VCCIO8	8			VCCIO8	8		
H11	VCCAUX	-			VCCAUX	-		
H12	VCCAUX	-			VCCAUX	-		
L15	VCCAUX	-			VCCAUX	-		
L8	VCCAUX	-			VCCAUX	-		
M15	VCCAUX	-			VCCAUX	-		
M8	VCCAUX	-			VCCAUX	-		
R11	VCCAUX	-			VCCAUX	-		
R12	VCCAUX	-			VCCAUX	-		
A1	GND	-			GND	-		
A10	GND	-			GND	-		
A16	GND	-			GND	-		
A22	GND	-			GND	-		
AA19	GND	-			GND	-		
AA4	GND	-			GND	-		
AB1	GND	-			GND	-		
AB22	GND	-			GND	-		
B13	GND	-			GND	-		
B19	GND	-			GND	-		
B4	GND	-			GND	-		
D16	GND	-			GND	-		
D2	GND	-			GND	-		
D21	GND	-			GND	-		
D7	GND	-			GND	-		

LFE2M50E/SE Logic Signal Connections: 484 fpBGA (Cont.)

LFE2M50E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential
D9	PT45A	0	VREF1_0	T
A2	PT44B	0		C
VCCIO	VCCIO0	0		
A3	PT44A	0		T
B3	PT43B	0		C
C4	PT43A	0		T
E10	PT42B	0		C
F10	PT42A	0		T
C7	PT41B	0		C
GNDIO	GNDIO0	-		
B6	PT41A	0		T
C6	PT40B	0		C
VCCIO	VCCIO0	0		
C5	PT40A	0		T
C8	PT39B	0		C
D8	PT39A	0		T
E8	PT38B	0		C
E9	PT38A	0		T
GNDIO	GNDIO0	-		
VCCIO	VCCIO0	0		
F8	PT10B	0		C
GNDIO	GNDIO0	-		
G8	PT10A	0		T
F7	PT9B	0		C
G7	PT9A	0		T
C3	PT8B	0		C
VCCIO	VCCIO0	0		
D4	PT8A	0		T
F6	PT7B	0		C
E6	PT7A	0		T
E5	PT6B	0		C
D6	PT6A	0		T
D3	PT5B	0		C
GNDIO	GNDIO0	-		
E3	PT5A	0		T
D5	PT4B	0		C
VCCIO	VCCIO0	0		
E4	PT4A	0		T
C2	PT3B	0		C
B2	PT3A	0		T
B1	PT2B	0		C
C1	PT2A	0		T
J10	VCC	-		

LFE2M35E/SE and LFE2M50E/SE Logic Signal Connections: 672 fpBGA (Cont.)

LFE2M35E/SE					LFE2M50E/SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
N23	PR37A	3	PCLKT3_0	T (LVDS)*	PR41A	3	PCLKT3_0	T*
N24	PR35B	2	PCLKC2_0/RDQ32	C	PR39B	2	PCLKC2_0/RDQ36	C
N25	PR35A	2	PCLKT2_0/RDQ32	T	PR39A	2	PCLKT2_0/RDQ36	T
GNDIO	GNDIO2	-			GNDIO2	-		
M22	PR34B	2	RDQ32	C (LVDS)*	PR38B	2	RDQ36	C*
M24	PR34A	2	RDQ32	T (LVDS)*	PR38A	2	RDQ36	T*
M23	PR33B	2	RDQ32	C	PR37B	2	RDQ36	C
N26	PR33A	2	RDQ32	T	PR37A	2	RDQ36	T
VCCIO	VCCIO2	2			VCCIO2	2		
L22	PR32B	2	RDQ32	C (LVDS)*	PR36B	2	RDQ36	C*
L24	PR32A	2	RDQS32	T (LVDS)*	PR36A	2	RDQS36	T*
L23	PR31B	2	RDQ32	C	PR35B	2	RDQ36	C
GNDIO	GNDIO2	-			GNDIO2	-		
M20	PR31A	2	RDQ32	T	PR35A	2	RDQ36	T
M26	PR30B	2	RDQ32	C (LVDS)*	PR34B	2	RDQ36	C*
L26	PR30A	2	RDQ32	T (LVDS)*	PR34A	2	RDQ36	T*
K22	PR29B	2	RUM1_SPLLC_FB_A/RDQ32	C	PR33B	2	RUM3_SPLLC_FB_A/RDQ36	C
VCCIO	VCCIO2	2			VCCIO2	2		
M19	PR29A	2	RUM1_SPLLT_FB_A/RDQ32	T	PR33A	2	RUM3_SPLLT_FB_A/RDQ36	T
K25	PR28B	2	RUM1_SPLLC_IN_A/RDQ32	C (LVDS)*	PR32B	2	RUM3_SPLLC_IN_A/RDQ36	C*
K26	PR28A	2	RUM1_SPLLT_IN_A/RDQ32	T (LVDS)*	PR32A	2	RUM3_SPLLT_IN_A/RDQ36	T*
K24	PR26B	2	RDQ23	C	PR30B	2	RDQ27	C
K23	PR26A	2	RDQ23	T	PR30A	2	RDQ27	T
GNDIO	GNDIO2	-			GNDIO2	-		
L19	PR25B	2	RDQ23	C (LVDS)*	PR29B	2	RDQ27	C*
K21	PR25A	2	RDQ23	T (LVDS)*	PR29A	2	RDQ27	T*
J23	PR24B	2	RDQ23	C	PR28B	2	RDQ27	C
J24	PR24A	2	RDQ23	T	PR28A	2	RDQ27	T
VCCIO	VCCIO2	2			VCCIO2	2		
K20	PR23B	2	RDQ23	C (LVDS)*	PR27B	2	RDQ27	C*
J21	PR23A	2	RDQS23	T (LVDS)*	PR27A	2	RDQS27	T*
H21	PR22B	2	RDQ23	C	PR26B	2	RDQ27	C
GNDIO	GNDIO2	-			GNDIO2	-		
K18	PR22A	2	RDQ23	T	PR26A	2	RDQ27	T
H22	PR21B	2	RDQ23	C (LVDS)*	PR25B	2	RDQ27	C*
J20	PR21A	2	RDQ23	T (LVDS)*	PR25A	2	RDQ27	T*
J25	PR20B	2	RDQ23	C	PR24B	2	RDQ27	C
VCCIO	VCCIO2	2			VCCIO2	2		
J26	PR20A	2	RDQ23	T	PR24A	2	RDQ27	T
G21	PR19B	2	RDQ23	C (LVDS)*	PR23B	2	RDQ27	C*
J19	PR19A	2	RDQ23	T (LVDS)*	PR23A	2	RDQ27	T*
GNDIO	GNDIO2	-			GNDIO2	-		
H23	PR18B	2	RDQ15	C	PR21B	2		C
H24	PR18A	2	RDQ15	T	PR21A	2		T
H25	PR17B	2	RDQ15	C (LVDS)*	PR20B	2		C*
H26	PR17A	2	RDQ15	T (LVDS)*	PR20A	2		T*
VCCIO	VCCIO2	2			VCCIO2	2		
G22	PR16B	2	RDQ15	C	PR19B	2		C

LFE2M35E/SE and LFE2M50E/SE Logic Signal Connections: 672 fpBGA (Cont.)

LFE2M35E/SE					LFE2M50E/SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
L16	GND	-			GND	-		
L17	GND	-			GND	-		
L2	GND	-			GND	-		
L20	GND	-			GND	-		
L25	GND	-			GND	-		
L7	GND	-			GND	-		
M13	GND	-			GND	-		
M14	GND	-			GND	-		
N10	GND	-			GND	-		
N12	GND	-			GND	-		
N13	GND	-			GND	-		
N14	GND	-			GND	-		
N15	GND	-			GND	-		
N17	GND	-			GND	-		
P10	GND	-			GND	-		
P12	GND	-			GND	-		
P13	GND	-			GND	-		
P14	GND	-			GND	-		
P15	GND	-			GND	-		
P17	GND	-			GND	-		
R13	GND	-			GND	-		
R14	GND	-			GND	-		
T10	GND	-			GND	-		
T11	GND	-			GND	-		
T16	GND	-			GND	-		
T17	GND	-			GND	-		
T2	GND	-			GND	-		
T20	GND	-			GND	-		
T25	GND	-			GND	-		
T7	GND	-			GND	-		
U11	GND	-			GND	-		
U13	GND	-			GND	-		
U14	GND	-			GND	-		
U16	GND	-			GND	-		
V22	GND	-			GND	-		
V5	GND	-			GND	-		
Y11	GND	-			GND	-		
Y16	GND	-			GND	-		
AB3	NC	-			NC	-		
AB4	NC	-			NC	-		
AC1	NC	-			NC	-		
AC2	NC	-			NC	-		
B4	NC	-			NC	-		
B5	NC	-			NC	-		
C26	NC	-			NC	-		
D20	NC	-			NC	-		
D21	NC	-			NC	-		
D22	NC	-			NC	-		

LFE2M50E/SE and LFE2M70E/SE Logic Signal Connections: 900 fpBGA (Cont.)

LFE2M50E/SE					LFE2M70E/SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
Y22	PR60B	3		C	PR81B	3	RDQ82	C
Y23	PR60A	3		T	PR81A	3	RDQ82	T
AB26	NC	-			PR80B	3	RDQ82	C (LVDS)*
AB27	NC	-			PR80A	3	RDQ82	T (LVDS)*
-	-	-			VCCIO3	3		
Y24	NC	-			PR79B	3	RDQ82	C
Y25	NC	-			PR79A	3	RDQ82	T
AA29	NC	-			PR78B	3	RDQ82	C (LVDS)*
Y28	NC	-			PR78A	3	RDQ82	T (LVDS)*
Y30	NC	-			PR76B	3	RDQ73	C
Y29	NC	-			PR76A	3	RDQ73	T
-	-	-			GNDIO3	-		
-	-	-			-	-		
W22	NC	-			PR75B	3	RDQ73	C (LVDS)*
V22	NC	-			PR75A	3	RDQ73	T (LVDS)*
Y27	NC	-			PR74B	3	RDQ73	C
-	-	-			VCCIO3	3		
Y26	NC	-			PR74A	3	RDQ73	T
W30	NC	-			PR73B	3	RDQ73	C (LVDS)*
W29	NC	-			PR73A	3	RDQS73	T (LVDS)*
-	-	-			GNDIO3	-		
W25	NC	-			PR72B	3	RDQ73	C
W26	NC	-			PR72A	3	RDQ73	T
U29	PR59B	3		C (LVDS)*	PR71B	3	RDQ73	C (LVDS)*
V29	PR59A	3		T (LVDS)*	PR71A	3	RDQ73	T (LVDS)*
VCCIO	VCCIO3	3			VCCIO3	3		
V30	PR58B	3		C	PR70B	3	RDQ73	C
U30	PR58A	3		T	PR70A	3	RDQ73	T
W27	PR57B	3		C (LVDS)*	PR69B	3	RDQ73	C (LVDS)*
W28	PR57A	3		T (LVDS)*	PR69A	3	RDQ73	T (LVDS)*
V24	PR55B	3	RDQ52	C	PR67B	3	RDQ64	C
V25	PR55A	3	RDQ52	T	PR67A	3	RDQ64	T
GNDIO	GNDIO3	-			GNDIO3	-		
U28	PR54B	3	RDQ52	C (LVDS)*	PR66B	3	RDQ64	C (LVDS)*
U27	PR54A	3	RDQ52	T (LVDS)*	PR66A	3	RDQ64	T (LVDS)*
U23	PR53B	3	RDQ52	C	PR65B	3	RDQ64	C
V23	PR53A	3	RDQ52	T	PR65A	3	RDQ64	T
VCCIO	VCCIO3	3			VCCIO3	3		
V26	PR52B	3	RDQ52	C (LVDS)*	PR64B	3	RDQ64	C (LVDS)*
U26	PR52A	3	RDQS52	T (LVDS)*	PR64A	3	RDQS64	T (LVDS)*
U25	PR51B	3	RDQ52	C	PR63B	3	RDQ64	C
GNDIO	GNDIO3	-			GNDIO3	-		
U24	PR51A	3	RDQ52	T	PR63A	3	RDQ64	T
T30	PR50B	3	RDQ52	C (LVDS)*	PR62B	3	RDQ64	C (LVDS)*
R30	PR50A	3	RDQ52	T (LVDS)*	PR62A	3	RDQ64	T (LVDS)*
T23	PR49B	3	RDQ52	C	PR61B	3	RDQ64	C
VCCIO	VCCIO3	3			VCCIO3	3		
T22	PR49A	3	RDQ52	T	PR61A	3	RDQ64	T

LFE2M70E/SE and LFE2M100E/SE Logic Signal Connections: 1152 fpBGA (Cont.)

LFE2M70E/SE				LFE2M100E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
W30	PR53A	3	RDQ55	T (LVDS)*	PR61A	3	RDQ63	T (LVDS)*
VCCIO	VCCIO3	3			VCCIO3	3		
U27	PR52B	3	VREF2_3/RDQ55	C	PR60B	3	VREF2_3/RDQ63	C
V29	PR52A	3	VREF1_3/RDQ55	T	PR60A	3	VREF1_3/RDQ63	T
V31	PR51B	3	PCLKC3_0/RDQ55	C (LVDS)*	PR59B	3	PCLKC3_0/RDQ63	C (LVDS)*
V32	PR51A	3	PCLKT3_0/RDQ55	T (LVDS)*	PR59A	3	PCLKT3_0/RDQ63	T (LVDS)*
V33	PR49B	2	PCLKC2_0/RDQ46	C	PR57B	2	PCLKC2_0/RDQ54	C
V34	PR49A	2	PCLKT2_0/RDQ46	T	PR57A	2	PCLKT2_0/RDQ54	T
GNDIO	GNDIO2	-			GNDIO2	-		
U24	PR48B	2	RDQ46	C (LVDS)*	PR56B	2	RDQ54	C (LVDS)*
U25	PR48A	2	RDQ46	T (LVDS)*	PR56A	2	RDQ54	T (LVDS)*
V30	PR47B	2	RDQ46	C	PR55B	2	RDQ54	C
Y32	PR47A	2	RDQ46	T	PR55A	2	RDQ54	T
VCCIO	VCCIO2	2			VCCIO2	2		
U28	PR46B	2	RDQ46	C (LVDS)*	PR54B	2	RDQ54	C (LVDS)*
U29	PR46A	2	RDQS46	T (LVDS)*	PR54A	2	RDQS54	T (LVDS)*
U33	PR45B	2	RDQ46	C	PR53B	2	RDQ54	C
GNDIO	GNDIO2	-			GNDIO2	-		
U34	PR45A	2	RDQ46	T	PR53A	2	RDQ54	T
T30	PR44B	2	RDQ46	C (LVDS)*	PR52B	2	RDQ54	C (LVDS)*
U30	PR44A	2	RDQ46	T (LVDS)*	PR52A	2	RDQ54	T (LVDS)*
T29	PR43B	2	RUM3_SPLLC_FB_A/RDQ46	C	PR51B	2	RUM3_SPLLC_FB_A/RDQ54	C
VCCIO	VCCIO2	2			VCCIO2	2		
T28	PR43A	2	RUM3_SPLLT_FB_A/RDQ46	T	PR51A	2	RUM3_SPLLT_FB_A/RDQ54	T
U31	PR42B	2	RUM3_SPLLC_IN_A/RDQ46	C (LVDS)*	PR50B	2	RUM3_SPLLC_IN_A/RDQ54	C (LVDS)*
U32	PR42A	2	RUM3_SPLLT_IN_A/RDQ46	T (LVDS)*	PR50A	2	RUM3_SPLLT_IN_A/RDQ54	T (LVDS)*
T33	PR40B	2	RDQ37	C	PR48B	2	RDQ45	C
T34	PR40A	2	RDQ37	T	PR48A	2	RDQ45	T
GNDIO	GNDIO2	-			GNDIO2	-		
R27	PR39B	2	RDQ37	C (LVDS)*	PR47B	2	RDQ45	C (LVDS)*
R28	PR39A	2	RDQ37	T (LVDS)*	PR47A	2	RDQ45	T (LVDS)*
R29	PR38B	2	RDQ37	C	PR46B	2	RDQ45	C
R30	PR38A	2	RDQ37	T	PR46A	2	RDQ45	T
VCCIO	VCCIO2	2			VCCIO2	2		
R33	PR37B	2	RDQ37	C (LVDS)*	PR45B	2	RDQ45	C (LVDS)*
R34	PR37A	2	RDQS37	T (LVDS)*	PR45A	2	RDQS45	T (LVDS)*
R32	PR36B	2	RDQ37	C	PR44B	2	RDQ45	C
GNDIO	GNDIO2	-			GNDIO2	-		
R31	PR36A	2	RDQ37	T	PR44A	2	RDQ45	T
P34	PR35B	2	RDQ37	C (LVDS)*	PR43B	2	RDQ45	C (LVDS)*
P33	PR35A	2	RDQ37	T (LVDS)*	PR43A	2	RDQ45	T (LVDS)*
R26	PR34B	2	RDQ37	C	PR42B	2	RDQ45	C
VCCIO	VCCIO2	2			VCCIO2	2		
T25	PR34A	2	RDQ37	T	PR42A	2	RDQ45	T
P28	PR33B	2	RDQ37	C (LVDS)*	PR41B	2	RDQ45	C (LVDS)*
P27	PR33A	2	RDQ37	T (LVDS)*	PR41A	2	RDQ45	T (LVDS)*
P30	NC	-			PR40B	2		C
-	-	-			GNDIO2	-		
P29	NC	-			PR40A	2		T

LFE2M70E/SE and LFE2M100E/SE Logic Signal Connections: 1152 fpBGA (Cont.)

LFE2M70E/SE				LFE2M100E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
AB16	GND	-			GND	-		
AB17	GND	-			GND	-		
AB18	GND	-			GND	-		
AB19	GND	-			GND	-		
AB26	GND	-			GND	-		
AB31	GND	-			GND	-		
AB4	GND	-			GND	-		
AB9	GND	-			GND	-		
AC16	GND	-			GND	-		
AC17	GND	-			GND	-		
AC18	GND	-			GND	-		
AC19	GND	-			GND	-		
AD27	GND	-			GND	-		
AE27	GND	-			GND	-		
AE31	GND	-			GND	-		
AE4	GND	-			GND	-		
AE8	GND	-			GND	-		
AF12	GND	-			GND	-		
AF16	GND	-			GND	-		
AF19	GND	-			GND	-		
AF23	GND	-			GND	-		
AG31	GND	-			GND	-		
AH31	GND	-			GND	-		
AH4	GND	-			GND	-		
AJ14	GND	-			GND	-		
AJ21	GND	-			GND	-		
AK27	GND	-			GND	-		
AK8	GND	-			GND	-		
AL10	GND	-			GND	-		
AL16	GND	-			GND	-		
AL19	GND	-			GND	-		
AL2	GND	-			GND	-		
AL25	GND	-			GND	-		
AL33	GND	-			GND	-		
AP1	GND	-			GND	-		
AP10	GND	-			GND	-		
AP13	GND	-			GND	-		
AP22	GND	-			GND	-		
AP25	GND	-			GND	-		
AP34	GND	-			GND	-		
D10	GND	-			GND	-		
D16	GND	-			GND	-		
D19	GND	-			GND	-		
D2	GND	-			GND	-		
D25	GND	-			GND	-		
D33	GND	-			GND	-		
E27	GND	-			GND	-		
E8	GND	-			GND	-		
F14	GND	-			GND	-		

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2M100E-5FN1152C	520	1.2V	-5	Lead-Free fpBGA	1152	COM	100
LFE2M100E-6FN1152C	520	1.2V	-6	Lead-Free fpBGA	1152	COM	100
LFE2M100E-7FN1152C	520	1.2V	-7	Lead-Free fpBGA	1152	COM	100
LFE2M100E-5FN900C	416	1.2V	-5	Lead-Free fpBGA	900	COM	100
LFE2M100E-6FN900C	416	1.2V	-6	Lead-Free fpBGA	900	COM	100
LFE2M100E-7FN900C	416	1.2V	-7	Lead-Free fpBGA	900	COM	100

Industrial

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2M20E-5FN484I	304	1.2V	-5	Lead-Free fpBGA	484	IND	20
LFE2M20E-6FN484I	304	1.2V	-6	Lead-Free fpBGA	484	IND	20
LFE2M20E-5FN256I	140	1.2V	-5	Lead-Free fpBGA	256	IND	20
LFE2M20E-6FN256I	140	1.2V	-6	Lead-Free fpBGA	256	IND	20

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2M35E-5FN672I	410	1.2V	-5	Lead-Free fpBGA	672	IND	35
LFE2M35E-6FN672I	410	1.2V	-6	Lead-Free fpBGA	672	IND	35
LFE2M35E-5FN484I	303	1.2V	-5	Lead-Free fpBGA	484	IND	35
LFE2M35E-6FN484I	303	1.2V	-6	Lead-Free fpBGA	484	IND	35
LFE2M35E-5FN256I	140	1.2V	-5	Lead-Free fpBGA	256	IND	35
LFE2M35E-6FN256I	140	1.2V	-6	Lead-Free fpBGA	256	IND	35

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2M50E-5FN900I	410	1.2V	-5	Lead-Free fpBGA	900	Ind	50
LFE2M50E-6FN900I	410	1.2V	-6	Lead-Free fpBGA	900	Ind	50
LFE2M50E-5FN672I	372	1.2V	-5	Lead-Free fpBGA	672	Ind	50
LFE2M50E-6FN672I	372	1.2V	-6	Lead-Free fpBGA	672	Ind	50
LFE2M50E-5FN484I	270	1.2V	-5	Lead-Free fpBGA	484	Ind	50
LFE2M50E-6FN484I	270	1.2V	-6	Lead-Free fpBGA	484	Ind	50

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2M70E-5FN1152I	436	1.2V	-5	Lead-Free fpBGA	1152	Ind	70
LFE2M70E-6FN1152I	436	1.2V	-6	Lead-Free fpBGA	1152	Ind	70
LFE2M70E-5FN900I	416	1.2V	-5	Lead-Free fpBGA	900	Ind	70
LFE2M70E-6FN900I	416	1.2V	-6	Lead-Free fpBGA	900	Ind	70