Lattice Semiconductor Corporation - LFE2M20E-7F484C Datasheet

Welcome to E-XFL.COM

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	2375
Number of Logic Elements/Cells	19000
Total RAM Bits	1246208
Number of I/O	304
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	484-BBGA
Supplier Device Package	484-FPBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfe2m20e-7f484c

sysMEM Memory

LatticeECP2/M devices contains a number of sysMEM Embedded Block RAM (EBR). The EBR consists of an 18-Kbit RAM with dedicated input and output registers.

sysMEM Memory Block

The sysMEM block can implement single port, dual port or pseudo dual port memories. Each block can be used in a variety of depths and widths as shown in Table 2-6. FIFOs can be implemented in sysMEM EBR blocks by implementing support logic with PFUs. The EBR block facilitates parity checking by supporting an optional parity bit for each data byte. EBR blocks provide byte-enable support for configurations with18-bit and 36-bit data widths.

Table 2-6. sysMEM Block Configurations

Memory Mode	Configurations
Single Port	16,384 x 1 8,192 x 2 4,096 x 4 2,048 x 9 1,024 x 18 512 x 36
True Dual Port	16,384 x 1 8,192 x 2 4,096 x 4 2,048 x 9 1,024 x 18
Pseudo Dual Port	16,384 x 1 8,192 x 2 4,096 x 4 2,048 x 9 1,024 x 18 512 x 36

Bus Size Matching

All of the multi-port memory modes support different widths on each of the ports. The RAM bits are mapped LSB word 0 to MSB word 0, LSB word 1 to MSB word 1, and so on. Although the word size and number of words for each port varies, this mapping scheme applies to each port.

RAM Initialization and ROM Operation

If desired, the contents of the RAM can be pre-loaded during device configuration. By preloading the RAM block during the chip configuration cycle and disabling the write controls, the sysMEM block can also be utilized as a ROM.

Memory Cascading

Larger and deeper blocks of RAM can be created using EBR sysMEM Blocks. Typically, the Lattice design tools cascade memory transparently, based on specific design inputs.

Single, Dual and Pseudo-Dual Port Modes

In all the sysMEM RAM modes the input data and address for the ports are registered at the input of the memory array. The output data of the memory is optionally registered at the output.

EBR memory supports two forms of write behavior for single port or dual port operation:

1. Normal – Data on the output appears only during a read cycle. During a write cycle, the data (at the current address) does not appear on the output. This mode is supported for all data widths.

SERDES Power Supply Requirements (LatticeECP2M Family Only)[1]

Over Recommended Operating Conditions

Symbol	Description	Typ.[2]	Units
Standby (Power Down)			
$I_{CCTX-SB}$	V_{CCTX} current (per channel)	10	µA
$I_{CCRX-SB}$	V_{CCRX} current (per channel)	75	µA
$I_{CCIB-SB}$	Input buffer current (per channel)	0	µA
$I_{CCOB-SB}$	Output buffer current (per channel)	0	µA
I_{CCP-SB}	SERDES PLL current (per quad)	30	µA
$I_{CCAX33-SB}$	SERDES termination current (per quad)	10	µA
Operating (Data Rate = 3.125 Gbps)			
$I_{CCTX-OP}$	V_{CCTX} current (per channel)	19	mA
$I_{CCRX-OP}$	V_{CCRX} current (per channel)	34	mA
$I_{CCIB-OP}$	Input buffer current (per channel)	4	mA
$I_{CCOB-OP}$	Output buffer current (per channel)	13	mA
I_{CCP-OP}	SERDES PLL current (per quad)	26	mA
$I_{CCAX33-OP}$	SERDES termination current (per quad)	0.01	mA

1. Equalization enabled, pre-emphasis disabled.
2. T_J = 25°C, power supplies at nominal voltage.

SERDES Power (LatticeECP2M Family Only)

Table 3-1 presents the SERDES power for one channel.

Table 3-1. SERDES Power[1]

Symbol	Description	Typ.[2]	Units
$P_{S-1CH-31}$	SERDES power (one channel @ 3.125 Gbps)	90	mW
$P_{S-1CH-25}$	SERDES power (one channel @ 2.5 Gbps)	87	mW
$P_{S-1CH-12}$	SERDES power (one channel @ 1.25 Gbps)	86	mW
$P_{S-1CH-02}$	SERDES power (one channel @ 250 Mbps)	76	mW

1. One quarter of the total quad power (includes contribution from common circuits, all channels in the quad operating, pre-emphasis disabled, equalization enabled).
2. Typical values measured at 25ºC and 1.2V.

sysI/O Recommended Operating Conditions

Standard	V_{CCIO}			V_{REF} (V)		
	Min.	Typ.	Max.	Min.	Typ.	Max.
LVCMOS 3.3[2]	3.135	3.3	3.465	—	—	—
LVCMOS 2.5[2]	2.375	2.5	2.625	—	—	—
LVCMOS 1.8	1.71	1.8	1.89	—	—	—
LVCMOS 1.5	1.425	1.5	1.575	—	—	—
LVCMOS 1.2[2]	1.14	1.2	1.26	—	—	—
LVTTL[2]	3.135	3.3	3.465	—	—	—
PCI	3.135	3.3	3.465	—	—	—
SSTL18[2] Class I, II	1.71	1.8	1.89	0.833	0.9	0.969
SSTL2[2] Class I, II	2.375	2.5	2.625	1.15	1.25	1.35
SSTL3[2] Class I, II	3.135	3.3	3.465	1.3	1.5	1.7
HSTL[2] 15 Class I	1.425	1.5	1.575	0.68	0.75	0.9
HSTL[2] 18 Class I, II	1.71	1.8	1.89	0.816	0.9	1.08
LVDS[2]	2.375	2.5	2.625	—	—	—
MLVDS25[1]	2.375	2.5	2.625	—	—	—
LVPECL33[1, 2]	3.135	3.3	3.465	—	—	—
BLVDS25[1, 2]	2.375	2.5	2.625	—	—	—
RSDS[1, 2]	2.375	2.5	2.625	—	—	—
SSTL18D_I[2], II[2]	1.71	1.8	1.89	—	—	—
SSTL25D_ I[2], II[2]	2.375	2.5	2.625	—	—	—
SSTL33D_ I[2], II[2]	3.135	3.3	3.465	—	—	—
HSTL15D_ I[2]	1.425	1.5	1.575	—	—	—
HSTL18D_ I[2], II[2]	1.71	1.8	1.89	—	—	—

1. Inputs on chip. Outputs are implemented with the addition of external resistors.
2. Input on this standard does not depend on the value of V_{CCIO}.

LatticeECP2/M External Switching Characteristics[9] (Continued)

Over Recommended Operating Conditions

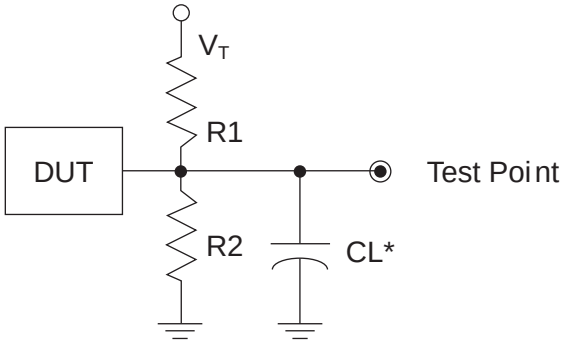
Parameter	Description	Device	-7		-6		-5		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
t_{DIBSPI}	Data Invalid Before Clock (Transmit)	ECP2-20	—	280	—	280	—	280	ps
		ECP2-35	—	280	—	280	—	280	ps
		ECP2-50	—	280	—	280	—	280	ps
		ECP2-70	—	280	—	280	—	280	ps
		ECP2M20	—	230	—	230	—	230	ps
		ECP2M35	—	230	—	230	—	230	ps
		ECP2M50	—	230	—	230	—	230	ps
		ECP2M70	—	230	—	230	—	230	ps
		ECP2M100	—	230	—	230	—	230	ps
XGMII I/O Pin Parameters (312 Mbps)[5]									
$t_{SUXGMII}$	Data Setup Before Read Clock	ECP2/M	480	—	480	—	480	—	ps
t_{HXGMII}	Data Hold After Read Clock	ECP2/M	480	—	480	—	480	—	ps
$t_{DVBCKXGMII}$	Data Valid Before Clock	ECP2/M	960	—	960	—	960	—	ps
$t_{DVACKXGMII}$	Data Valid After Clock	ECP2/M	960	—	960	—	960	—	ps
Primary									
f_{MAX_PRI}[7]	Frequency for Primary Clock Tree	ECP2/M	—	420	—	357	—	311	MHz
t_{W_PRI}	Clock Pulse Width for Primary Clock	ECP2/M	0.95	—	1.19	—	2.00	—	ns
t_{SKEW_PRI}	Primary Clock Skew Within a Bank	ECP2/M	—	300	—	360	—	420	ps
Edge Clock									
f_{MAX_EDGE}[7]	Frequency for Edge Clock	ECP2/M	—	420	—	357	—	311	MHz
t_{W_EDGE}	Clock Pulse Width for Edge Clock	ECP2/M	0.95	—	1.19	—	2.00	—	ns
t_{SKEW_EDGE}	Edge Clock Skew Within an Edge of the Device	ECP2/M	—	300	—	360	—	420	ps

1. General timing numbers based on LVCMOS 2.5, 12mA, 0pf load.
2. DDR timing numbers based on SSTL25 for BGA packages only.
3. DDR2 timing numbers based on SSTL18 for BGA packages only.
4. SPI4.2 and SFI4 timing numbers based on LVDS25 for BGA packages only.
5. XGMII timing numbers based on HSTL class I. A corresponding left/right dedicated clock buffer is used when using the SPI4.2 interface to the left or right edge of the device. For SPI4.2 mode, the software tool will help in selecting the appropriate clock buffer.
6. IP will be used to support DDR and DDR2 memory data rates down to 95MHz. This approach uses a free-running clock and PFU register to sample the data instead of the hardwired DDR memory interface.
7. Using the LVDS I/O standard.
8. ECP2-6 and ECP2-12 do not support SPI4.2
9. The AC numbers do not apply to PCLK6 and PCLK7.
10. Applies to CLKOP only.
11. Please refer to TN1159, LatticeECP2/M Pin Assignment Recommendations for best performance.

Switching Test Conditions

Figure 3-22 shows the output test load that is used for AC testing. The specific values for resistance, capacitance, voltage, and other test conditions are shown in Table 3-19.

Figure 3-22. Output Test Load, LVTTL and LVCMOS Standards



*CL Includes Test Fixture and Probe Capacitance

Table 3-19. Test Fixture Required Components, Non-Terminated Interfaces

Test Condition	R_1	R_2	C_L	Timing Ref.	V_T
LVTTL and other LVCMOS settings (L -> H, H -> L)	∞	∞	0pF	LVCMOS 3.3 = 1.5V	—
				LVCMOS 2.5 = $V_{CCIO}/2$	—
				LVCMOS 1.8 = $V_{CCIO}/2$	—
				LVCMOS 1.5 = $V_{CCIO}/2$	—
				LVCMOS 1.2 = $V_{CCIO}/2$	—
LVCMOS 2.5 I/O (Z -> H)	∞	1MΩ		$V_{CCIO}/2$	—
LVCMOS 2.5 I/O (Z -> L)	1MΩ	∞		$V_{CCIO}/2$	V_{CCIO}
LVCMOS 2.5 I/O (H -> Z)	∞	100		V_{OH} - 0.10	—
LVCMOS 2.5 I/O (L -> Z)	100	∞		V_{OL} + 0.10	V_{CCIO}

Note: Output test conditions for all other interfaces are determined by the respective standards.

Signal Descriptions (Cont.)

Signal Name	I/O	Description
[LOC]_SQ_VCCIBm	—	Input buffer power supply, channel m (1.2V/1.5V). This pin should be left floating if the channel is unused.
[LOC]_SQ_VCCOBm	—	Output buffer power supply, channel m (1.2V/1.5V). This pin should be left floating if the channel is unused.
[LOC]_SQ_HDOUTNm	O	High-speed output, negative channel m
[LOC]_SQ_HDOUTPm	O	High-speed output, positive channel m
[LOC]_SQ_HDINNm	I	High-speed input, negative channel m
[LOC]_SQ_HDINPm	I	High-speed input, positive channel m
[LOC]_SQ_VCCTXm[4]	—	Transmitter power supply, channel m (1.2V). This pin must be tied to 1.2V even if the channel is unused.
[LOC]_SQ_VCCRXm[4]	—	Receiver power supply, channel m (1.2V). This pin must be tied to 1.2V even if the channel is unused.

1. These signals are relevant for LatticeECP2M family.
2. m defines the associated channel in the Quad.
3. These signals are defined in Quads [LOC] indicates the corner SERDES Quad is located: ULC (upper left), URC (upper right), LLC (lower left), LRC (lower right).
4. When placing switching I/Os around these critical pins that are designed to supply the device with the proper reference or supply voltage, care must be given. For more information, refer to TN1159, LatticeECP2/M Pin Assignment Recommendations.
5. There may be SPLLs that do not have dedicated I/Os.

LFE2-35E/SE and LFE2-50E/SE Logic Signal Connections: 484 fpBGA (Cont.)

LFE2-35E/SE					LFE2-50E/SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
C8	PT29B	0		C	PT38B	0		C
D8	PT29A	0		T	PT38A	0		T
GNDIO	GNDIO0	-			GNDIO0	0		
D10	PT27B	0		C	PT36B	0		C
E10	PT27A	0		T	PT36A	0		T
C7	PT26B	0		C	PT35B	0		C
C6	PT26A	0		T	PT35A	0		T
VCCIO	VCCIO0	0			VCCIO	0		
B6	PT25B	0		C	PT34B	0		C
B5	PT25A	0		T	PT34A	0		T
F10	PT24B	0		C	PT33B	0		C
D9	PT24A	0		T	PT33A	0		T
GNDIO	GNDIO0	-			GNDIO0	0		
F9	PT23B	0		C	PT32B	0		C
E9	PT23A	0		T	PT32A	0		T
A5	PT22B	0		C	PT31B	0		C
A4	PT22A	0		T	PT31A	0		T
VCCIO	VCCIO0	0			VCCIO	0		
A3	PT21B	0		C	PT30B	0		C
A2	PT21A	0		T	PT30A	0		T
G8	PT20B	0		C	PT29B	0		C
E8	PT20A	0		T	PT29A	0		T
GNDIO	GNDIO0	-			GNDIO0	0		
VCCIO	VCCIO0	0			VCCIO	0		
C3	PT10B	0		C	PT10B	0		C
B3	PT10A	0		T	PT10A	0		T
GNDIO	GNDIO0	-			GNDIO0	0		
F8	PT9B	0		C	PT9B	0		C
D7	PT9A	0		T	PT9A	0		T
E7	PT8B	0		C	PT8B	0		C
VCCIO	VCCIO0	0			VCCIO	0		
F7	PT8A	0		T	PT8A	0		T
D5	PT7B	0		C	PT7B	0		C
D6	PT7A	0		T	PT7A	0		T
D4	PT6B	0		C	PT6B	0		C
C4	PT6A	0		T	PT6A	0		T
GNDIO	GNDIO0	-			GNDIO0	0		
B2	PT5B	0		C	PT5B	0		C
B1	PT5A	0		T	PT5A	0		T
J7	PT4B	0		C	PT4B	0		C
VCCIO	VCCIO0	0			VCCIO	0		
H7	PT4A	0		T	PT4A	0		T
D3	PT3B	0		C	PT3B	0		C
C2	PT3A	0		T	PT3A	0		T
D1	PT2B	0	VREF2_0	C	PT2B	0	VREF2_0	C
C1	PT2A	0	VREF1_0	T	PT2A	0	VREF1_0	T

LFE2-20E/SE and LFE2-35E/SE Logic Signal Connections: 672 fpBGA (Cont.)

LFE2-20E/20SE					LFE2-35E/35SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
U1	NC	-			PL34A	6	LDQ31	T
V1	NC	-			PL34B	6	LDQ31	C
GND	GNDIO6	-			GNDIO6	-		
P3	NC	-			NC	-		
R3	NC	-			NC	-		
R4	NC	-			NC	-		
U2	NC	-			NC	-		
VCCIO	VCCIO6	6			VCCIO6	6		
V2	NC	-			NC	-		
W2	NC	-			NC	-		
T6	NC	-			PL38A	6	LDQ39	T
R5	NC	-			PL38B	6	LDQ39	C
GND	GNDIO6	-			GNDIO6	-		
R6	PL25A	6	LDQS25***	T (LVDS)*	PL39A	6	LDQS39***	T (LVDS)*
R7	PL25B	6	LDQ25	C (LVDS)*	PL39B	6	LDQ39	C (LVDS)*
W1	PL26A	6	LDQ25	T	PL40A	6	LDQ39	T
VCCIO	VCCIO6	6			VCCIO6	6		
Y2	PL26B	6	LDQ25	C	PL40B	6	LDQ39	C
Y1	PL27A	6	LLM0_GDLLT_IN_A**/LDQ25	T (LVDS)*	PL41A	6	LLM0_GDLLT_IN_A**/LDQ39	T (LVDS)*
AA2	PL27B	6	LLM0_GDLLC_IN_A**/LDQ25	C (LVDS)*	PL41B	6	LLM0_GDLLC_IN_A**/LDQ39	C (LVDS)*
T5	PL28A	6	LLM0_GDLLT_FB_A/LDQ25	T	PL42A	6	LLM0_GDLLT_FB_A/LDQ39	T
GND	GNDIO6	-			GNDIO6	-		
T7	PL28B	6	LLM0_GDLLC_FB_A/LDQ25	C	PL42B	6	LLM0_GDLLC_FB_A/LDQ39	C
R8	VCC	6			VCCPLL	6		
T8	LLM0_PLLCAP	6			LLM0_PLLCAP	6		
U3	PL30A	6	LLM0_GPLLT_IN_A**/LDQ34	T (LVDS)*	PL44A	6	LLM0_GPLLT_IN_A**/LDQ48	T (LVDS)*
U4	PL30B	6	LLM0_GPLLC_IN_A**/LDQ34	C (LVDS)*	PL44B	6	LLM0_GPLLC_IN_A**/LDQ48	C (LVDS)*
V3	PL31A	6	LLM0_GPLLT_FB_A/LDQ34	T	PL45A	6	LLM0_GPLLT_FB_A/LDQ48	T
U5	PL31B	6	LLM0_GPLLC_FB_A/LDQ34	C	PL45B	6	LLM0_GPLLC_FB_A/LDQ48	C
V4	PL32A	6	LDQ34	T (LVDS)*	PL46A	6	LDQ48	T (LVDS)*
VCCIO	VCCIO6	6			VCCIO6	6		
V5	PL32B	6	LDQ34	C (LVDS)*	PL46B	6	LDQ48	C (LVDS)*
Y3	PL33A	6	LDQ34	T	PL47A	6	LDQ48	T
Y4	PL33B	6	LDQ34	C	PL47B	6	LDQ48	C
W3	PL34A	6	LDQS34	T (LVDS)*	PL48A	6	LDQS48	T (LVDS)*
GND	GNDIO6	-			GNDIO6	-		
W4	PL34B	6	LDQ34	C (LVDS)*	PL48B	6	LDQ48	C (LVDS)*
AA1	PL35A	6	LDQ34	T	PL49A	6	LDQ48	T
AB1	PL35B	6	LDQ34	C	PL49B	6	LDQ48	C
VCCIO	VCCIO6	6			VCCIO6	6		
U8	PL36A	6	LDQ34	T (LVDS)*	PL50A	6	LDQ48	T (LVDS)*
U7	PL36B	6	LDQ34	C (LVDS)*	PL50B	6	LDQ48	C (LVDS)*
V8	PL37A	6	LDQ34	T	PL51A	6	LDQ48	T
U6	PL37B	6	LDQ34	C	PL51B	6	LDQ48	C
GND	GNDIO6	-			GNDIO6	-		
W6	PL38A	6	LDQ42	T (LVDS)*	PL52A	6	LDQ56	T (LVDS)*

LFE2-50E/SE and LFE2-70E/SE Logic Signal Connections: 672 fpBGA (Cont.)

LFE2-50E/SE					LFE2-70E/SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
W5	PL71B	6	LDQ75	C (LVDS)*	PL84B	6	LDQ88	C (LVDS)*
AC1	PL72A	6	LDQ75	T	PL85A	6	LDQ88	T
AD1	PL72B	6	LDQ75	C	PL85B	6	LDQ88	C
VCCIO	VCCIO6	6			VCCIO6	6		
Y6	PL73A	6	LDQ75	T (LVDS)*	PL86A	6	LDQ88	T (LVDS)*
Y5	PL73B	6	LDQ75	C (LVDS)*	PL86B	6	LDQ88	C (LVDS)*
AE2	PL74A	6	LDQ75	T	PL87A	6	LDQ88	T
AD2	PL74B	6	LDQ75	C	PL87B	6	LDQ88	C
GND	GNDIO6	-			GNDIO6	-		
AB3	PL75A	6	LDQS75	T (LVDS)*	PL88A	6	LDQS88	T (LVDS)*
AB2	PL75B	6	LDQ75	C (LVDS)*	PL88B	6	LDQ88	C (LVDS)*
W7	PL76A	6	LDQ75	T	PL89A	6	LDQ88	T
VCCIO	VCCIO6	6			VCCIO6	6		
W8	PL76B	6	LDQ75	C	PL89B	6	LDQ88	C
Y7	PL77A	6	LDQ75	T (LVDS)*	PL90A	6	LDQ88	T (LVDS)*
Y8	PL77B	6	LDQ75	C (LVDS)*	PL90B	6	LDQ88	C (LVDS)*
AC2	PL78A	6	LDQ75	T	PL91A	6	LDQ88	T
GND	GNDIO6	-			GNDIO6	-		
AD3	PL78B	6	LDQ75	C	PL91B	6	LDQ88	C
AC3	TCK	-			TCK	-		
AA8	TDI	-			TDI	-		
AB4	TMS	-			TMS	-		
AA5	TDO	-			TDO	-		
AB5	VCCJ	-			VCCJ	-		
AE3	PB2A	5	VREF2_5/BDQ6	T	PB2A	5	VREF2_5/BDQ6	T
AF3	PB2B	5	VREF1_5/BDQ6	C	PB2B	5	VREF1_5/BDQ6	C
AC4	PB3A	5	BDQ6	T	PB3A	5	BDQ6	T
AD4	PB3B	5	BDQ6	C	PB3B	5	BDQ6	C
AE4	PB4A	5	BDQ6	T	PB4A	5	BDQ6	T
AF4	PB4B	5	BDQ6	C	PB4B	5	BDQ6	C
VCCIO	VCCIO5	5			VCCIO5	5		
V9	PB5A	5	BDQ6	T	PB5A	5	BDQ6	T
W9	PB5B	5	BDQ6	C	PB5B	5	BDQ6	C
GND	GNDIO5	-			GNDIO5	-		
AA6	PB6A	5	BDQS6	T	PB6A	5	BDQS6	T
AB6	PB6B	5	BDQ6	C	PB6B	5	BDQ6	C
AC5	PB7A	5	BDQ6	T	PB7A	5	BDQ6	T
AD5	PB7B	5	BDQ6	C	PB7B	5	BDQ6	C
AA7	PB8A	5	BDQ6	T	PB8A	5	BDQ6	T
AB7	PB8B	5	BDQ6	C	PB8B	5	BDQ6	C
VCCIO	VCCIO5	5			VCCIO5	5		
AE5	PB9A	5	BDQ6	T	PB9A	5	BDQ6	T
AF5	PB9B	5	BDQ6	C	PB9B	5	BDQ6	C
AC7	PB10A	5	BDQ6	T	PB10A	5	BDQ6	T
AD7	PB10B	5	BDQ6	C	PB10B	5	BDQ6	C
VCCIO	VCCIO5	5			VCCIO5	5		

LFE2-70E/SE Logic Signal Connections: 900 fpBGA (Cont.)

LFE2-70E/SE				
Ball Number	**Ball/Pad Function**	**Bank**	**Dual Function**	**Differential**
P25	PR51B	2	RDQ54	C
VCCIO	VCCIO2	2		
P23	PR51A	2	RDQ54	T
P27	PR50B	2	RDQ54	C (LVDS)*
P28	PR50A	2	RDQ54	T (LVDS)*
GND	GNDIO2	-		
VCCIO	VCCIO2	2		
N24	PR39B	2	RUM0_SPLLC_FB_A/RDQ37	C
N26	PR39A	2	RUM0_SPLLT_FB_A/RDQ37	T
N23	PR38B	2	RUM0_SPLLC_IN_A/RDQ37	C
N25	PR38A	2	RUM0_SPLLT_IN_A/RDQ37	T
VCCIO	VCCIO2	2		
P29	PR37B	2	RDQ37	C (LVDS)*
P30	PR37A	2	RDQS37	T (LVDS)*
M26	PR36B	2	RDQ37	C
GND	GNDIO2	-		
M24	PR36A	2	RDQ37	T
N29	PR35B	2	RDQ37	C (LVDS)*
N30	PR35A	2	RDQ37	T (LVDS)*
M25	PR34B	2	RDQ37	C
VCCIO	VCCIO2	2		
M23	PR34A	2	RDQ37	T
M27	PR33B	2	RDQ37	C (LVDS)*
M28	PR33A	2	RDQ37	T (LVDS)*
L26	PR32B	2	RDQ29	C
GND	GNDIO2	-		
L24	PR32A	2	RDQ29	T
M29	PR31B	2	RDQ29	C (LVDS)*
M30	PR31A	2	RDQ29	T (LVDS)*
L25	PR30B	2	RDQ29	C
VCCIO	VCCIO2	2		
L23	PR30A	2	RDQ29	T
L27	PR29B	2	RDQ29	C (LVDS)*
L28	PR29A	2	RDQS29	T (LVDS)*
GND	GNDIO2	-		
K24	PR28B	2	RDQ29	C
K26	PR28A	2	RDQ29	T
L29	PR27B	2	RDQ29	C (LVDS)*
L30	PR27A	2	RDQ29	T (LVDS)*
VCCIO	VCCIO2	2		
K23	PR26B	2	RDQ29	C
K25	PR26A	2	RDQ29	T
K27	PR25B	2	RDQ29	C (LVDS)*

LFE2M-20E/SE and LFE2M-35E/SE Logic Signal Connections: 256 fpBGA

LFE2M20E/SE					LFE2M35E/SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
A2	PL2A	7	LDQ6	T (LVDS)*	PL2A	7	LDQ6	T (LVDS)*
B2	PL2B	7	LDQ6	C (LVDS)*	PL2B	7	LDQ6	C(LVDS)*
D3	PL3A	7	LDQ6	T	PL3A	7	LDQ6	T
C2	PL3B	7	LDQ6	C	PL3B	7	LDQ6	C
E4	PL4A	7	LDQ6	T (LVDS)*	PL4A	7	LDQ6	T (LVDS)*
VCCIO	VCCIO7	7			VCCIO7	7		
E5	PL4B	7	LDQ6	C (LVDS)*	PL4B	7	LDQ6	C(LVDS)*
B1	PL5A	7	LDQ6	T	PL5A	7	LDQ6	T
C1	PL5B	7	LDQ6	C	PL5B	7	LDQ6	C
D2	PL6A	7	LDQS6	T (LVDS)*	PL6A	7	LDQS6	T (LVDS)*
GNDIO	GNDIO7	-			GNDIO7	-		
D1	PL6B	7	LDQ6	C (LVDS)*	PL6B	7	LDQ6	C(LVDS)*
E1	PL7A	7	LDQ6	T	PL7A	7	LDQ6	T
F1	PL7B	7	LDQ6	C	PL7B	7	LDQ6	C
VCCIO	VCCIO7	7			VCCIO7	7		
F3	PL8A	7	LDQ6	T (LVDS)*	PL8A	7	LDQ6	T (LVDS)*
F2	PL8B	7	LDQ6	C (LVDS)*	PL8B	7	LDQ6	C(LVDS)*
F6	PL9A	7	VREF2_7/LDQ6	T	PL9A	7	VREF2_7/LDQ6	T
F5	PL9B	7	VREF1_7/LDQ6	C	PL9B	7	VREF1_7/LDQ6	C
GNDIO	GNDIO7	-			GNDIO7	-		
G4	PL11A	7	LUM0_SPLLT_IN_A	T (LVDS)*	PL11A	7	LUM0_SPLLT_IN_A/LDQ15	T (LVDS)*
G3	PL11B	7	LUM0_SPLLC_IN_A	C (LVDS)*	PL11B	7	LUM0_SPLLC_IN_A/LDQ15	C(LVDS)*
G1	PL12A	7	LUM0_SPLLT_FB_A	T	PL12A	7	LUM0_SPLLT_FB_A/LDQ15	T
G2	PL12B	7	LUM0_SPLLC_FB_A	C	PL12B	7	LUM0_SPLLC_FB_A/LDQ15	C
H1	PL13A	7		T (LVDS)*	PL13A	7	LDQ15	T (LVDS)*
VCCIO	VCCIO7	7			VCCIO7	7		
J1	PL13B	7		C (LVDS)*	PL13B	7	LDQ15	C(LVDS)*
H2	PL14A	7		T	PL14A	7	LDQ15	T
H3	PL14B	7		C	PL14B	7	LDQ15	C
GNDIO	GNDIO7	-			GNDIO7	-		
VCCIO	VCCIO7	7			VCCIO7	7		
G6	PL24A	7	LDQ22	T (LVDS)*	PL34A	7	LDQ32	T (LVDS)*
H6	PL24B	7	LDQ22	C (LVDS)*	PL34B	7	LDQ32	C(LVDS)*
J2	PL25A	7	PCLKT7_0/LDQ22	T	PL35A	7	PCLKT7_0/LDQ32	T
GNDIO	GNDIO7	-			GNDIO7	-		
K1	PL25B	7	PCLKC7_0/LDQ22	C	PL35B	7	PCLKC7_0/LDQ32	C
H4	PL27A	6	PCLKT6_0	T (LVDS)*	PL37A	6	PCLKT6_0	T (LVDS)*
H5	PL27B	6	PCLKC6_0	C (LVDS)*	PL37B	6	PCLKC6_0	C(LVDS)*
J4	PL28A	6	VREF2_6	T	PL38A	6	VREF2_6	T
K4	PL28B	6	VREF1_6	C	PL38B	6	VREF1_6	C
VCCIO	VCCIO6	6			VCCIO6	6		
J6	PL31A	6	LLM1_SPLLT_IN_A	T (LVDS)*	PL41A	6	LLM2_SPLLT_IN_A	T (LVDS)*
GNDIO	GNDIO6	-			GNDIO6	-		
J5	PL31B	6	LLM1_SPLLC_IN_A	C (LVDS)*	PL41B	6	LLM2_SPLLC_IN_A	C(LVDS)*
K3	PL32A	6	LLM1_SPLLT_FB_A	T	PL42A	6	LLM2_SPLLT_FB_A	T
K2	PL32B	6	LLM1_SPLLC_FB_A	C	PL42B	6	LLM2_SPLLC_FB_A	C
VCCIO	VCCIO6	6			VCCIO6	6		

LFE2M-20E/SE and LFE2M-35E/SE Logic Signal Connections: 256 fpBGA (Cont.)

LFE2M20E/SE					LFE2M35E/SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
F14	PR24B	2	RDQ22	C (LVDS)*	PR34B	2	RDQ32	C(LVDS)*
F13	PR24A	2	RDQ22	T (LVDS)*	PR34A	2	RDQ32	T (LVDS)*
VCCIO	VCCIO2	2			VCCIO2	2		
GNDIO	GNDIO2	-			GNDIO2	-		
H11	PR14B	2		C	PR14B	2	RDQ15	C
G11	PR14A	2		T	PR14A	2	RDQ15	T
E13	PR13B	2		C (LVDS)*	PR13B	2	RDQ15	C(LVDS)*
F12	PR13A	2		T (LVDS)*	PR13A	2	RDQ15	T (LVDS)*
VCCIO	VCCIO2	2			VCCIO2	2		
F11	PR12B	2	RUM0_SPLLC_FB_A	C	PR12B	2	RUM0_SPLLC_FB_A/RDQ15	C
E12	PR12A	2	RUM0_SPLLT_FB_A	T	PR12A	2	RUM0_SPLLT_FB_A/RDQ15	T
D16	PR11B	2	RUM0_SPLLC_IN_A	C (LVDS)*	PR11B	2	RUM0_SPLLC_IN_A/RDQ15	C(LVDS)*
D15	PR11A	2	RUM0_SPLLT_IN_A	T (LVDS)*	PR11A	2	RUM0_SPLLT_IN_A/RDQ15	T (LVDS)*
C16	PR9B	2	VREF2_2	C	PR9B	2	VREF2_2	C
GNDIO	GNDIO2	-			GNDIO2	-		
B16	PR9A	2	VREF1_2	T	PR9A	2	VREF1_2	T
VCCIO	VCCIO2	2			VCCIO2	2		
F4	XRES	-			XRES	-		
C15	URC_SQ_VCCRX0	12			URC_SQ_VCCRX0	12		
A14	URC_SQ_HDINP0	12		T	URC_SQ_HDINP0	12		T
B15	URC_SQ_VCCIB0	12			URC_SQ_VCCIB0	12		
B14	URC_SQ_HDINN0	12		C	URC_SQ_HDINN0	12		C
C12	URC_SQ_VCCTX0	12			URC_SQ_VCCTX0	12		
A11	URC_SQ_HDOUTP0	12		T	URC_SQ_HDOUTP0	12		T
A12	URC_SQ_VCCOB0	12			URC_SQ_VCCOB0	12		
B11	URC_SQ_HDOUTN0	12		C	URC_SQ_HDOUTN0	12		C
C11	URC_SQ_VCCTX1	12			URC_SQ_VCCTX1	12		
B10	URC_SQ_HDOUTN1	12		C	URC_SQ_HDOUTN1	12		C
C10	URC_SQ_VCCOB1	12			URC_SQ_VCCOB1	12		
A10	URC_SQ_HDOUTP1	12		T	URC_SQ_HDOUTP1	12		T
C14	URC_SQ_VCCRX1	12			URC_SQ_VCCRX1	12		
B13	URC_SQ_HDINN1	12		C	URC_SQ_HDINN1	12		C
C13	URC_SQ_VCCIB1	12			URC_SQ_VCCIB1	12		
A13	URC_SQ_HDINP1	12		T	URC_SQ_HDINP1	12		T
B9	URC_SQ_VCCAUX33	12			URC_SQ_VCCAUX33	12		
D8	URC_SQ_REFCLKN	12		C	URC_SQ_REFCLKN	12		C
D9	URC_SQ_REFCLKP	12		T	URC_SQ_REFCLKP	12		T
C9	URC_SQ_VCCP	12			URC_SQ_VCCP	12		
A5	URC_SQ_HDINP2	12		T	URC_SQ_HDINP2	12		T
C5	URC_SQ_VCCIB2	12			URC_SQ_VCCIB2	12		
B5	URC_SQ_HDINN2	12		C	URC_SQ_HDINN2	12		C
C4	URC_SQ_VCCRX2	12			URC_SQ_VCCRX2	12		
A8	URC_SQ_HDOUTP2	12		T	URC_SQ_HDOUTP2	12		T
C8	URC_SQ_VCCOB2	12			URC_SQ_VCCOB2	12		
B8	URC_SQ_HDOUTN2	12		C	URC_SQ_HDOUTN2	12		C
C7	URC_SQ_VCCTX2	12			URC_SQ_VCCTX2	12		
B7	URC_SQ_HDOUTN3	12		C	URC_SQ_HDOUTN3	12		C
A6	URC_SQ_VCCOB3	12			URC_SQ_VCCOB3	12		

LFE2M20E/SE and LFE2M35E/SE Logic Signal Connections: 484 fpBGA (Cont.)

LFE2M20E/SE					LFE2M35E/SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
L18	PR31A	3	RLM1_SPLLT_IN_A	T (LVDS)*	PR41A	3	RLM2_SPLLT_IN_A	T (LVDS)*
GNDIO	GNDIO3	-			GNDIO3	-		
L20	PR30B	3		C	PR40B	3		C
L19	PR30A	3		T	PR40A	3		T
K16	PR29B	3		C (LVDS)*	PR39B	3		C (LVDS)*
K17	PR29A	3		T (LVDS)*	PR39A	3		T (LVDS)*
VCCIO	VCCIO3	3			VCCIO3	3		
J16	PR28B	3	VREF2_3	C	PR38B	3	VREF2_3	C
K18	PR28A	3	VREF1_3	T	PR38A	3	VREF1_3	T
J22	PR27B	3	PCLKC3_0	C (LVDS)*	PR37B	3	PCLKC3_0	C (LVDS)*
J21	PR27A	3	PCLKT3_0	T (LVDS)*	PR37A	3	PCLKT3_0	T (LVDS)*
H22	PR25B	2	PCLKC2_0/RDQ22	C	PR35B	2	PCLKC2_0/RDQ32	C
H21	PR25A	2	PCLKT2_0/RDQ22	T	PR35A	2	PCLKT2_0/RDQ32	T
GNDIO	GNDIO2	-			GNDIO2	-		
J17	PR24B	2	RDQ22	C (LVDS)*	PR34B	2	RDQ32	C (LVDS)*
J18	PR24A	2	RDQ22	T (LVDS)*	PR34A	2	RDQ32	T (LVDS)*
J20	PR23B	2	RDQ22	C	PR33B	2	RDQ32	C
J19	PR23A	2	RDQ22	T	PR33A	2	RDQ32	T
VCCIO	VCCIO2	2			VCCIO2	2		
H16	PR22B	2	RDQ22	C (LVDS)*	PR32B	2	RDQ32	C (LVDS)*
H17	PR22A	2	RDQS22	T (LVDS)*	PR32A	2	RDQS32	T (LVDS)*
G22	PR21B	2	RDQ22	C	PR31B	2	RDQ32	C
GNDIO	GNDIO2	-			GNDIO2	-		
G21	PR21A	2	RDQ22	T	PR31A	2	RDQ32	T
H20	PR20B	2	RDQ22	C (LVDS)*	PR30B	2	RDQ32	C (LVDS)*
H19	PR20A	2	RDQ22	T (LVDS)*	PR30A	2	RDQ32	T (LVDS)*
G16	PR19B	2	RUM1_SPLLC_FB_A/RDQ22	C	PR29B	2	RUM1_SPLLC_FB_A/RDQ32	C
VCCIO	VCCIO2	2			VCCIO2	2		
H18	PR19A	2	RUM1_SPLLT_FB_A/RDQ22	T	PR29A	2	RUM1_SPLLT_FB_A/RDQ32	T
F22	PR18B	2	RUM1_SPLLC_IN_A/RDQ22	C (LVDS)*	PR28B	2	RUM1_SPLLC_IN_A/RDQ32	C (LVDS)*
F21	PR18A	2	RUM1_SPLLT_IN_A/RDQ22	T (LVDS)*	PR28A	2	RUM1_SPLLT_IN_A/RDQ32	T (LVDS)*
GNDIO	GNDIO2	-			-	-		
G20	PR16B	2		C	PR26B	2	RDQ23	C
VCCIO	VCCIO2	2			-	-		
F20	PR16A	2		T	PR26A	2	RDQ23	T
-	-	-			GNDIO2	-		
G17	PR15B	2		C (LVDS)*	PR25B	2	RDQ23	C (LVDS)*
F17	PR15A	2		T (LVDS)*	PR25A	2	RDQ23	T (LVDS)*
-	-	-			VCCIO2	2		
GNDIO	GNDIO2	-			GNDIO2	-		
E22	PR14B	2		C	PR14B	2	RDQ15	C
D22	PR14A	2		T	PR14A	2	RDQ15	T
E20	PR13B	2		C (LVDS)*	PR13B	2	RDQ15	C (LVDS)*
D20	PR13A	2		T (LVDS)*	PR13A	2	RDQ15	T (LVDS)*
VCCIO	VCCIO2	2			VCCIO2	2		
D19	PR12B	2	RUM0_SPLLC_FB_A	C	PR12B	2	RUM0_SPLLC_FB_A/RDQ15	C
E19	PR12A	2	RUM0_SPLLT_FB_A	T	PR12A	2	RUM0_SPLLT_FB_A/RDQ15	T
F18	PR11B	2	RUM0_SPLLC_IN_A	C (LVDS)*	PR11B	2	RUM0_SPLLC_IN_A/RDQ15	C (LVDS)*

LFE2M50E/SE Logic Signal Connections: 484 fpBGA (Cont.)

LFE2M50E/SE				
Ball Number	**Ball/Pad Function**	**Bank**	**Dual Function**	**Differential**
M19	PR50A	3	RDQ52	T (LVDS)*
M18	PR49B	3	RDQ52	C
VCCIO	VCCIO3	3		
L16	PR49A	3	RDQ52	T
L22	PR48B	3	RDQ52	C (LVDS)*
L21	PR48A	3	RDQ52	T (LVDS)*
GNDIO	GNDIO3	-		
K22	PR46B	3	RLM3_SPLLC_FB_A	C
VCCIO	VCCIO3	3		
K21	PR46A	3	RLM3_SPLLT_FB_A	T
L17	PR45B	3	RLM3_SPLLC_IN_A	C (LVDS)*
L18	PR45A	3	RLM3_SPLLT_IN_A	T (LVDS)*
GNDIO	GNDIO3	-		
L20	PR44B	3		C
L19	PR44A	3		T
K16	PR43B	3		C (LVDS)*
K17	PR43A	3		T (LVDS)*
VCCIO	VCCIO3	3		
J16	PR42B	3	VREF2_3	C
K18	PR42A	3	VREF1_3	T
J22	PR41B	3	PCLKC3_0	C (LVDS)*
J21	PR41A	3	PCLKT3_0	T (LVDS)*
H22	PR39B	2	PCLKC2_0/RDQ36	C
H21	PR39A	2	PCLKT2_0/RDQ36	T
GNDIO	GNDIO2	-		
J17	PR38B	2	RDQ36	C (LVDS)*
J18	PR38A	2	RDQ36	T (LVDS)*
J20	PR37B	2	RDQ36	C
J19	PR37A	2	RDQ36	T
VCCIO	VCCIO2	2		
H16	PR36B	2	RDQ36	C (LVDS)*
H17	PR36A	2	RDQS36	T (LVDS)*
G22	PR35B	2	RDQ36	C
GNDIO	GNDIO2	-		
G21	PR35A	2	RDQ36	T
H20	PR34B	2	RDQ36	C (LVDS)*
H19	PR34A	2	RDQ36	T (LVDS)*
G16	PR33B	2	RUM3_SPLLC_FB_A/RDQ36	C
VCCIO	VCCIO2	2		
H18	PR33A	2	RUM3_SPLLT_FB_A/RDQ36	T
F22	PR32B	2	RUM3_SPLLC_IN_A/RDQ36	C (LVDS)*
F21	PR32A	2	RUM3_SPLLT_IN_A/RDQ36	T (LVDS)*
G20	PR30B	2	RDQ27	C

LFE2M35E/SE and LFE2M50E/SE Logic Signal Connections: 672 fpBGA (Cont.)

LFE2M35E/SE					LFE2M50E/SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
C6	PT12B	0		C	PT12B	0		C
F10	PT12A	0		T	PT12A	0		T
D7	PT11B	0		C	PT11B	0		C
H11	PT11A	0		T	PT11A	0		T
D5	PT10B	0		C	PT10B	0		C
GNDIO	GNDIO0	-			GNDIO0	-		
E6	PT10A	0		T	PT10A	0		T
G10	PT9B	0		C	PT9B	0		C
F9	PT9A	0		T	PT9A	0		T
H10	PT8B	0		C	PT8B	0		C
VCCIO	VCCIO0	0			VCCIO0	0		
E7	PT8A	0		T	PT8A	0		T
B3	PT7B	0		C	PT7B	0		C
C5	PT7A	0		T	PT7A	0		T
B2	PT6B	0		C	PT6B	0		C
C4	PT6A	0		T	PT6A	0		T
G9	PT5B	0		C	PT5B	0		C
GNDIO	GNDIO0	-			GNDIO0	-		
F7	PT5A	0		T	PT5A	0		T
C3	PT4B	0		C	PT4B	0		C
VCCIO	VCCIO0	0			VCCIO0	0		
D4	PT4A	0		T	PT4A	0		T
J10	PT3B	0		C	PT3B	0		C
F8	PT3A	0		T	PT3A	0		T
G8	PT2B	0		C	PT2B	0		C
G7	PT2A	0		T	PT2A	0		T
L12	VCC	-			VCC	-		
L13	VCC	-			VCC	-		
L14	VCC	-			VCC	-		
L15	VCC	-			VCC	-		
M11	VCC	-			VCC	-		
M12	VCC	-			VCC	-		
M15	VCC	-			VCC	-		
M16	VCC	-			VCC	-		
N11	VCC	-			VCC	-		
N16	VCC	-			VCC	-		
P11	VCC	-			VCC	-		
P16	VCC	-			VCC	-		
R11	VCC	-			VCC	-		
R12	VCC	-			VCC	-		
R15	VCC	-			VCC	-		
R16	VCC	-			VCC	-		
T12	VCC	-			VCC	-		
T13	VCC	-			VCC	-		
T14	VCC	-			VCC	-		
T15	VCC	-			VCC	-		
B12	VCCIO0	0			VCCIO0	0		
B7	VCCIO0	0			VCCIO0	0		

LFE2M100E/SE Logic Signal Connections: 900 fpBGA (Cont.)

LFE2M100E/SE				
Ball Number	**Ball/Pad Function**	**Bank**	**Dual Function**	**Differential**
AJ2	LLC_SQ_HDINN3	14		C
AH4	LLC_SQ_VCCTX3	14		
AK5	LLC_SQ_HDOUTP3	14		T
AK4	LLC_SQ_VCCOB3	14		
AJ5	LLC_SQ_HDOUTN3	14		C
AH5	LLC_SQ_VCCTX2	14		
AJ6	LLC_SQ_HDOUTN2	14		C
AH6	LLC_SQ_VCCOB2	14		
AK6	LLC_SQ_HDOUTP2	14		T
AH2	LLC_SQ_VCCRX2	14		
AJ3	LLC_SQ_HDINN2	14		C
AH3	LLC_SQ_VCCIB2	14		
AK3	LLC_SQ_HDINP2	14		T
AH7	LLC_SQ_VCCP	14		
AG7	LLC_SQ_REFCLKP	14		T
AF7	LLC_SQ_REFCLKN	14		C
AJ7	LLC_SQ_VCCAUX33	14		
AK11	LLC_SQ_HDINP1	14		T
AH11	LLC_SQ_VCCIB1	14		
AJ11	LLC_SQ_HDINN1	14		C
AH12	LLC_SQ_VCCRX1	14		
AK8	LLC_SQ_HDOUTP1	14		T
AH8	LLC_SQ_VCCOB1	14		
AJ8	LLC_SQ_HDOUTN1	14		C
AH9	LLC_SQ_VCCTX1	14		
AJ9	LLC_SQ_HDOUTN0	14		C
AK10	LLC_SQ_VCCOB0	14		
AK9	LLC_SQ_HDOUTP0	14		T
AH10	LLC_SQ_VCCTX0	14		
AJ12	LLC_SQ_HDINN0	14		C
AJ13	LLC_SQ_VCCIB0	14		
AK12	LLC_SQ_HDINP0	14		T
AH13	LLC_SQ_VCCRX0	14		
AF10	PB30A	5	BDQ33	T
AE8	PB30B	5	BDQ33	C
AE11	PB31A	5	BDQ33	T
VCCIO	VCCIO5	5		
AD9	PB31B	5	BDQ33	C
AE10	PB32A	5	BDQ33	T
AD10	PB32B	5	BDQ33	C
AE13	PB33A	5	BDQS33	T
GNDIO	GNDIO5	-		
AC12	PB33B	5	BDQ33	C

LFE2M100E/SE Logic Signal Connections: 900 fpBGA (Cont.)

LFE2M100E/SE				
Ball Number	**Ball/Pad Function**	**Bank**	**Dual Function**	**Differential**
AJ30	LRC_SQ_VCCIB0	13		
AK29	LRC_SQ_HDINP0	13		T
AH30	LRC_SQ_VCCRX0	13		
AG27	CFG2	8		
AD25	CFG1	8		
AG28	CFG0	8		
AG30	PROGRAMN	8		
AG29	CCLK	8		
AC24	INITN	8		
AF27	DONE	8		
GNDIO	GNDIO8	-		
AF28	WRITEN***	8		
AE26	CS1N***	8		
AB23	CSN***	8		
AF29	D0/SPIFASTN***	8		
VCCIO	VCCIO8	8		
AF30	D1***	8		
AD26	D2***	8		
AE29	D3***	8		
GNDIO	GNDIO8	-		
AE30	D4***	8		
AD29	D5***	8		
AC25	D6***	8		
AD30	D7/SPID0***	8		
VCCIO	VCCIO8	8		
AA22	DI/CSSPI0N***	8		
AC26	DOUT/CSON/CSSPI1N***	8		
AA23	BUSY/SISPI***	8		
AB22	RLM0_PLLCAP	3		
AC27	PR102B	3	RLM0_GDLLC_FB_A/RDQ99	C
GNDIO	GNDIO3	-		
AC28	PR102A	3	RLM0_GDLLT_FB_A/RDQ99	T
AC29	PR101B	3	RLM0_GDLLC_IN_A**/RDQ99	C (LVDS)*
AC30	PR101A	3	RLM0_GDLLT_IN_A**/RDQ99	T (LVDS)*
AB30	PR100B	3	RLM0_GPLLC_IN_A**/RDQ99	C
VCCIO	VCCIO3	3		
AA30	PR100A	3	RLM0_GPLLT_IN_A**/RDQ99	T
AB29	PR99B	3	RLM0_GPLLC_FB_A/RDQ99	C (LVDS)*
AB28	PR99A	3	RLM0_GPLLT_FB_A/RDQS99	T (LVDS)*
GNDIO	GNDIO3	-		
Y22	PR98B	3	RDQ99	C
Y23	PR98A	3	RDQ99	T
AB26	PR97B	3	RDQ99	C (LVDS)*

LFE2M100E/SE Logic Signal Connections: 900 fpBGA (Cont.)

LFE2M100E/SE				
Ball Number	**Ball/Pad Function**	**Bank**	**Dual Function**	**Differential**
VCCIO	VCCIO3	3		
T22	PR69A	3	RDQ72	T
T29	PR68B	3	RDQ72	C (LVDS)*
T28	PR68A	3	RDQ72	T (LVDS)*
R23	PR66B	3	RLM4_SPLLC_FB_A/RDQ63	C
GNDIO	GNDIO3	-		
-	-	-		
R22	PR66A	3	RLM4_SPLLT_FB_A/RDQ63	T
P30	PR65B	3	RLM4_SPLLC_IN_A/RDQ63	C (LVDS)*
R29	PR65A	3	RLM4_SPLLT_IN_A/RDQ63	T (LVDS)*
T27	PR64B	3	RDQ63	C
VCCIO	VCCIO3	3		
T26	PR64A	3	RDQ63	T
GNDIO	GNDIO3	-		
N30	PR61B	3	RDQ63	C (LVDS)*
N29	PR61A	3	RDQ63	T (LVDS)*
VCCIO	VCCIO3	3		
R27	PR60B	3	VREF2_3/RDQ63	C
R28	PR60A	3	VREF1_3/RDQ63	T
P29	PR59B	3	PCLKC3_0/RDQ63	C (LVDS)*
P28	PR59A	3	PCLKT3_0/RDQ63	T (LVDS)*
M30	PR57B	2	PCLKC2_0/RDQ54	C
M29	PR57A	2	PCLKT2_0/RDQ54	T
GNDIO	GNDIO2	-		
P23	PR56B	2	RDQ54	C (LVDS)*
P24	PR56A	2	RDQ54	T (LVDS)*
R26	PR55B	2	RDQ54	C
P27	PR55A	2	RDQ54	T
VCCIO	VCCIO2	2		
P25	PR54B	2	RDQ54	C (LVDS)*
P26	PR54A	2	RDQS54	T (LVDS)*
K30	PR53B	2	RDQ54	C
GNDIO	GNDIO2	-		
K29	PR53A	2	RDQ54	T
N22	PR52B	2	RDQ54	C (LVDS)*
P22	PR52A	2	RDQ54	T (LVDS)*
J30	PR51B	2	RUM3_SPLLC_FB_A/RDQ54	C
VCCIO	VCCIO2	2		
J29	PR51A	2	RUM3_SPLLT_FB_A/RDQ54	T
N24	PR50B	2	RUM3_SPLLC_IN_A/RDQ54	C (LVDS)*
N23	PR50A	2	RUM3_SPLLT_IN_A/RDQ54	T (LVDS)*
N25	PR48B	2	RDQ45	C
N26	PR48A	2	RDQ45	T

LFE2M70E/SE and LFE2M100E/SE Logic Signal Connections: 1152 fpBGA (Cont.)

LFE2M70E/SE				LFE2M100E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
W30	PR53A	3	RDQ55	T (LVDS)*	PR61A	3	RDQ63	T (LVDS)*
VCCIO	VCCIO3	3			VCCIO3	3		
U27	PR52B	3	VREF2_3/RDQ55	C	PR60B	3	VREF2_3/RDQ63	C
V29	PR52A	3	VREF1_3/RDQ55	T	PR60A	3	VREF1_3/RDQ63	T
V31	PR51B	3	PCLKC3_0/RDQ55	C (LVDS)*	PR59B	3	PCLKC3_0/RDQ63	C (LVDS)*
V32	PR51A	3	PCLKT3_0/RDQ55	T (LVDS)*	PR59A	3	PCLKT3_0/RDQ63	T (LVDS)*
V33	PR49B	2	PCLKC2_0/RDQ46	C	PR57B	2	PCLKC2_0/RDQ54	C
V34	PR49A	2	PCLKT2_0/RDQ46	T	PR57A	2	PCLKT2_0/RDQ54	T
GNDIO	GNDIO2	-			GNDIO2	-		
U24	PR48B	2	RDQ46	C (LVDS)*	PR56B	2	RDQ54	C (LVDS)*
U25	PR48A	2	RDQ46	T (LVDS)*	PR56A	2	RDQ54	T (LVDS)*
V30	PR47B	2	RDQ46	C	PR55B	2	RDQ54	C
Y32	PR47A	2	RDQ46	T	PR55A	2	RDQ54	T
VCCIO	VCCIO2	2			VCCIO2	2		
U28	PR46B	2	RDQ46	C (LVDS)*	PR54B	2	RDQ54	C (LVDS)*
U29	PR46A	2	RDQS46	T (LVDS)*	PR54A	2	RDQS54	T (LVDS)*
U33	PR45B	2	RDQ46	C	PR53B	2	RDQ54	C
GNDIO	GNDIO2	-			GNDIO2	-		
U34	PR45A	2	RDQ46	T	PR53A	2	RDQ54	T
T30	PR44B	2	RDQ46	C (LVDS)*	PR52B	2	RDQ54	C (LVDS)*
U30	PR44A	2	RDQ46	T (LVDS)*	PR52A	2	RDQ54	T (LVDS)*
T29	PR43B	2	RUM3_SPLLC_FB_A/RDQ46	C	PR51B	2	RUM3_SPLLC_FB_A/RDQ54	C
VCCIO	VCCIO2	2			VCCIO2	2		
T28	PR43A	2	RUM3_SPLLT_FB_A/RDQ46	T	PR51A	2	RUM3_SPLLT_FB_A/RDQ54	T
U31	PR42B	2	RUM3_SPLLC_IN_A/RDQ46	C (LVDS)*	PR50B	2	RUM3_SPLLC_IN_A/RDQ54	C (LVDS)*
U32	PR42A	2	RUM3_SPLLT_IN_A/RDQ46	T (LVDS)*	PR50A	2	RUM3_SPLLT_IN_A/RDQ54	T (LVDS)*
T33	PR40B	2	RDQ37	C	PR48B	2	RDQ45	C
T34	PR40A	2	RDQ37	T	PR48A	2	RDQ45	T
GNDIO	GNDIO2	-			GNDIO2	-		
R27	PR39B	2	RDQ37	C (LVDS)*	PR47B	2	RDQ45	C (LVDS)*
R28	PR39A	2	RDQ37	T (LVDS)*	PR47A	2	RDQ45	T (LVDS)*
R29	PR38B	2	RDQ37	C	PR46B	2	RDQ45	C
R30	PR38A	2	RDQ37	T	PR46A	2	RDQ45	T
VCCIO	VCCIO2	2			VCCIO2	2		
R33	PR37B	2	RDQ37	C (LVDS)*	PR45B	2	RDQ45	C (LVDS)*
R34	PR37A	2	RDQS37	T (LVDS)*	PR45A	2	RDQS45	T (LVDS)*
R32	PR36B	2	RDQ37	C	PR44B	2	RDQ45	C
GNDIO	GNDIO2	-			GNDIO2	-		
R31	PR36A	2	RDQ37	T	PR44A	2	RDQ45	T
P34	PR35B	2	RDQ37	C (LVDS)*	PR43B	2	RDQ45	C (LVDS)*
P33	PR35A	2	RDQ37	T (LVDS)*	PR43A	2	RDQ45	T (LVDS)*
R26	PR34B	2	RDQ37	C	PR42B	2	RDQ45	C
VCCIO	VCCIO2	2			VCCIO2	2		
T25	PR34A	2	RDQ37	T	PR42A	2	RDQ45	T
P28	PR33B	2	RDQ37	C (LVDS)*	PR41B	2	RDQ45	C (LVDS)*
P27	PR33A	2	RDQ37	T (LVDS)*	PR41A	2	RDQ45	T (LVDS)*
P30	NC	-			PR40B	2		C
-	-	-			GNDIO2	-		
P29	NC	-			PR40A	2		T

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2M100E-5FN1152I	520	1.2V	-5	Lead-Free fpBGA	1152	Ind	100
LFE2M100E-6FN1152I	520	1.2V	-6	Lead-Free fpBGA	1152	Ind	100
LFE2M100E-5FN900I	416	1.2V	-5	Lead-Free fpBGA	900	Ind	100
LFE2M100E-6FN900I	416	1.2V	-6	Lead-Free fpBGA	900	Ind	100

LatticeECP2M S-Series Devices, Conventional Packaging

Commercial

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2M20SE-5F484C	304	1.2V	-5	fpBGA	484	Com	20
LFE2M20SE-6F484C	304	1.2V	-6	fpBGA	484	Com	20
LFE2M20SE-7F484C	304	1.2V	-7	fpBGA	484	Com	20
LFE2M20SE-5F256C	140	1.2V	-5	fpBGA	256	Com	20
LFE2M20SE-6F256C	140	1.2V	-6	fpBGA	256	Com	20
LFE2M20SE-7F256C	140	1.2V	-7	fpBGA	256	Com	20

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2M35SE-5F672C	410	1.2V	-5	fpBGA	672	Com	35
LFE2M35SE-6F672C	410	1.2V	-6	fpBGA	672	Com	35
LFE2M35SE-7F672C	410	1.2V	-7	fpBGA	672	Com	35
LFE2M35SE-5F484C	303	1.2V	-5	fpBGA	484	Com	35
LFE2M35SE-6F484C	303	1.2V	-6	fpBGA	484	Com	35
LFE2M35SE-7F484C	303	1.2V	-7	fpBGA	484	Com	35
LFE2M35SE-5F256C	140	1.2V	-5	fpBGA	256	Com	35
LFE2M35SE-6F256C	140	1.2V	-6	fpBGA	256	Com	35
LFE2M35SE-7F256C	140	1.2V	-7	fpBGA	256	Com	35

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2M50SE-5F900C	410	1.2V	-5	fpBGA	900	Com	50
LFE2M50SE-6F900C	410	1.2V	-6	fpBGA	900	Com	50
LFE2M50SE-7F900C	410	1.2V	-7	fpBGA	900	Com	50
LFE2M50SE-5F672C	372	1.2V	-5	fpBGA	672	Com	50
LFE2M50SE-6F672C	372	1.2V	-6	fpBGA	672	Com	50
LFE2M50SE-7F672C	372	1.2V	-7	fpBGA	672	Com	50
LFE2M50SE-5F484C	270	1.2V	-5	fpBGA	484	Com	50
LFE2M50SE-6F484C	270	1.2V	-6	fpBGA	484	Com	50
LFE2M50SE-7F484C	270	1.2V	-7	fpBGA	484	Com	50