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Understanding **Embedded - FPGAs (Field Programmable Gate Array)**

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	2375
Number of Logic Elements/Cells	19000
Total RAM Bits	1246208
Number of I/O	304
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (Tj)
Package / Case	484-BBGA
Supplier Device Package	484-FPBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfe2m20se-5fn484c

Architecture Overview

Each LatticeECP2/M device contains an array of logic blocks surrounded by Programmable I/O Cells (PIC). Interspersed between the rows of logic blocks are rows of sysMEM™ Embedded Block RAM (EBR) and rows of sys-DSP™ Digital Signal Processing blocks, as shown in Figure 2-1. In addition, the LatticeECP2M family contains SERDES Quads in one or more of the corners. Figure 2-2 shows the block diagram of ECP2M20 with one quad.

There are two kinds of logic blocks, the Programmable Functional Unit (PFU) and Programmable Functional Unit without RAM (PFF). The PFU contains the building blocks for logic, arithmetic, RAM and ROM functions. The PFF block contains building blocks for logic, arithmetic and ROM functions. Both PFU and PFF blocks are optimized for flexibility, allowing complex designs to be implemented quickly and efficiently. Logic Blocks are arranged in a two-dimensional array. Only one type of block is used per row.

The LatticeECP2/M devices contain one or more rows of sysMEM EBR blocks. sysMEM EBRs are large dedicated 18K fast memory blocks. Each sysMEM block can be configured in a variety of depths and widths of RAM or ROM. In addition, LatticeECP2/M devices contain up to two rows of DSP Blocks. Each DSP block has multipliers and adder/accumulators, which are the building blocks for complex signal processing capabilities.

The LatticeECP2M devices feature up to 16 embedded 3.125Gbps SERDES (Serializer / Deserializer) channels. Each SERDES channel contains independent 8b/10b encoding / decoding, polarity adjust and elastic buffer logic. Each group of four SERDES channels along with its Physical Coding Sub-layer (PCS) block, creates a quad. The functionality of the SERDES/PCS Quads can be controlled by memory cells set during device configuration or by registers that are addressable during device operation. The registers in every quad can be programmed by a soft IP interface, referred to as the SERDES Client Interface (SCI). These quads (up to four) are located at the corners of the devices.

Each PIC block encompasses two PIOs (PIO pairs) with their respective sysI/O buffers. The sysI/O buffers of the LatticeECP2/M devices are arranged in eight banks, allowing the implementation of a wide variety of I/O standards. In addition, a separate I/O bank is provided for the programming interfaces. PIO pairs on the left and right edges of the device can be configured as LVDS transmit/receive pairs. The PIC logic also includes pre-engineered support to aid in the implementation of high speed source synchronous standards such as SPI4.2, along with memory interfaces including DDR2.

The LatticeECP2/M registers in PFU and sysI/O can be configured to be SET or RESET. After power up and the device is configured, it enters into user mode with these registers SET/RESET according to the configuration setting, allowing the device entering to a known state for predictable system function.

Other blocks provided include PLLs, DLLs and configuration functions. The LatticeECP2/M architecture provides two General PLLs (GPLL) and up to six Standard PLLs (SPLL) per device. In addition, each LatticeECP2/M family member provides two DLLs per device. The GPLLs and DLLs blocks are located in pairs at the end of the bottom-most EBR row; the DLL block is located towards the edge of the device. The SPLL blocks are located at the end of the other EBR/DSP rows.

The configuration block that supports features such as configuration bit-stream decryption, transparent updates and dual boot support is located toward the center of this EBR row. The Ball Grid Array (BGA) package devices in the LatticeECP2/M family supports a sysCONFIG™ port located in the corner between banks four and five, which allows for serial or parallel device configuration.

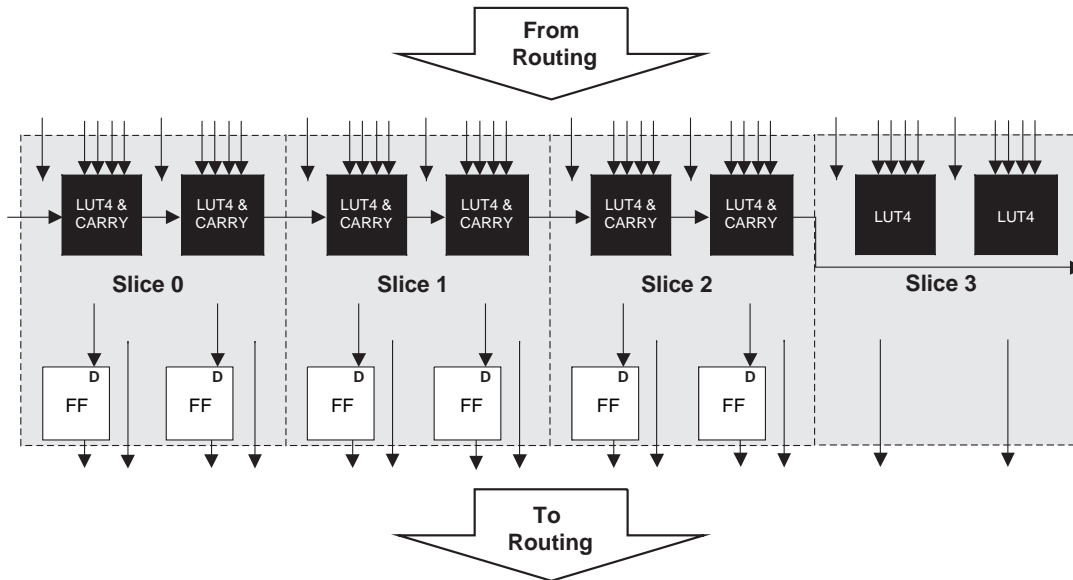
In addition, every device in the family has a JTAG port. This family also provides an on-chip oscillator. The LatticeECP2/M devices use 1.2V as their core voltage.

PFU Blocks

The core of the LatticeECP2/M device consists of PFU blocks, which are provided in two forms, the PFU and PFF. The PFUs can be programmed to perform Logic, Arithmetic, Distributed RAM and Distributed ROM functions. PFF blocks can be programmed to perform Logic, Arithmetic and ROM functions. Except where necessary, the remainder of this data sheet will use the term PFU to refer to both PFU and PFF blocks.

Each PFU block consists of four interconnected slices, numbered 0-3 as shown in Figure 2-3. All the interconnections to and from PFU blocks are from routing. There are 50 inputs and 23 outputs associated with each PFU block.

Figure 2-3. PFU Diagram



Slice

Slice 0 through Slice 2 contain two LUT4s feeding two registers, whereas Slice 3 contains two LUT4s only. For PFUs, Slice 0 and Slice 2 can also be configured as distributed memory, a capability not available in the PFF. Table 2-1 shows the capability of the slices in both PFF and PFU blocks along with the operation modes they enable. In addition, each PFU contains some logic that allows the LUTs to be combined to perform functions such as LUT5, LUT6, LUT7 and LUT8. There is control logic to perform set/reset functions (programmable as synchronous/asynchronous), clock select, chip-select and wider RAM/ROM functions. Figure 2-4 shows an overview of the internal logic of the slice. The registers in the slice can be configured for positive/negative and edge triggered or level sensitive clocks.

Table 2-1. Resources and Modes Available per Slice

Slice	PFU Block		PFF Block	
	Resources	Modes	Resources	Modes
Slice 0	2 LUT4s and 2 Registers	Logic, Ripple, RAM, ROM	2 LUT4s and 2 Registers	Logic, Ripple, ROM
Slice 1	2 LUT4s and 2 Registers	Logic, Ripple, ROM	2 LUT4s and 2 Registers	Logic, Ripple, ROM
Slice 2	2 LUT4s and 2 Registers	Logic, Ripple, RAM, ROM	2 LUT4s and 2 Registers	Logic, Ripple, ROM
Slice 3	2 LUT4s	Logic, ROM	2 LUT4s	Logic, ROM

Slices 0, 1 and 2 have 14 input signals: 13 signals from routing and one from the carry-chain (from the adjacent slice or PFU). There are seven outputs: six to routing and one to carry-chain (to the adjacent PFU). Slice 3 has 13 input signals from routing and four signals to routing. Table 2-2 lists the signals associated with Slice 0 to Slice 2.

DQSXFER

LatticeECP2/M devices provide a DQSXFER signal to the output buffer to assist it in data transfer to DDR memories that require DQS strobe be shifted 90°. This shifted DQS strobe is generated by the DQSDEL block. The DQSXFER signal runs the span of the data bus.

sysI/O Buffer

Each I/O is associated with a flexible buffer referred to as a sysI/O buffer. These buffers are arranged around the periphery of the device in groups referred to as banks. The sysI/O buffers allow users to implement the wide variety of standards that are found in today's systems including LVCMOS, SSTL, HSTL, LVDS and LVPECL.

sysI/O Buffer Banks

LatticeECP2/M devices have nine sysI/O buffer banks: eight banks for user I/Os arranged two per side. The ninth sysI/O buffer bank (Bank 8) is located adjacent to Bank 3 and has dedicated/shared I/Os for configuration. When a shared pin is not used for configuration it is available as a user I/O. Each bank is capable of supporting multiple I/O standards. Each sysI/O bank has its own I/O supply voltage (V_{CCIO}). In addition, each bank, except Bank 8, has voltage references, V_{REF1} and V_{REF2} , which allow it to be completely independent from the others. Bank 8 shares two voltage references, V_{REF1} and V_{REF2} , with Bank 3. Figure 2-37 shows the nine banks and their associated supplies.

In LatticeECP2/M devices, single-ended output buffers and ratioed input buffers (LVTTL, LVCMOS and PCI) are powered using V_{CCIO} . LVTTL, LVCMOS33, LVCMOS25 and LVCMOS12 can also be set as fixed threshold inputs independent of V_{CCIO} .

Each bank can support up to two separate V_{REF} voltages, V_{REF1} and V_{REF2} , that set the threshold for the referenced input buffers. Some dedicated I/O pins in a bank can be configured to be a reference voltage supply pin. Each I/O is individually configurable based on the bank's supply and reference voltages.

LatticeECP2M Supply Current (Standby)^{1, 2, 3, 4}
Over Recommended Operating Conditions

Symbol	Parameter	Device	Typ. ⁵	Units
I _{CC}	Core Power Supply Current	ECP2M20	25	mA
		ECP2M35	50	mA
		ECP2M50	85	mA
		ECP2M70	100	mA
		ECP2M100	100	mA
I _{CCAUX}	Auxiliary Power Supply Current	ECP2M20	24	mA
		ECP2M35	24	mA
		ECP2M50	24	mA
		ECP2M70	24	mA
		ECP2M100	24	mA
I _{CCGPLL}	GPLL Power Supply Current (per GPLL)	All Devices	0.5	mA
I _{CCSPLL}	GPLL Power Supply Current (per SPLL)	All Devices	0.5	mA
I _{CCIO}	Bank Power Supply Current (Per Bank)	ECP2M20	2	mA
		ECP2M35	2	mA
		ECP2M50	2	mA
		ECP2M70	2	mA
		ECP2M100	2	mA
I _{CCJ}	V _{CCJ} Power Supply Current	All Devices	3	mA

1. For further information about supply current, please see the list of additional technical documentation at the end of this data sheet.
2. Assumes all outputs are tristated, all inputs are configured as LVCMOS and held at the V_{CCIO} or GND.
3. Frequency 0MHz.
4. Pattern represents a "blank" configuration data file.
5. T_J = 25°C, power supplies at normal voltage.

SERDES Power Supply Requirements (LatticeECP2M Family Only)¹

Over Recommended Operating Conditions

Symbol	Description	Typ. ²	Units
Standby (Power Down)			
I _{CCTX-SB}	V _{CCTX} current (per channel)	10	μA
I _{CCR_X-SB}	V _{CCR_X} current (per channel)	75	μA
I _{CCIB-SB}	Input buffer current (per channel)	0	μA
I _{CCOB-SB}	Output buffer current (per channel)	0	μA
I _{CCP-SB}	SERDES PLL current (per quad)	30	μA
I _{CCAX33-SB}	SERDES termination current (per quad)	10	μA
Operating (Data Rate = 3.125 Gbps)			
I _{CCTX-OP}	V _{CCTX} current (per channel)	19	mA
I _{CCR_X-OP}	V _{CCR_X} current (per channel)	34	mA
I _{CCIB-OP}	Input buffer current (per channel)	4	mA
I _{CCOB-OP}	Output buffer current (per channel)	13	mA
I _{CCP-OP}	SERDES PLL current (per quad)	26	mA
I _{CCAX33-OP}	SERDES termination current (per quad)	0.01	mA

1. Equalization enabled, pre-emphasis disabled.
2. T_J = 25°C, power supplies at nominal voltage.

SERDES Power (LatticeECP2M Family Only)

Table 3-1 presents the SERDES power for one channel.

Table 3-1. SERDES Power¹

Symbol	Description	Typ. ²	Units
P _{S-1CH-31}	SERDES power (one channel @ 3.125 Gbps)	90	mW
P _{S-1CH-25}	SERDES power (one channel @ 2.5 Gbps)	87	mW
P _{S-1CH-12}	SERDES power (one channel @ 1.25 Gbps)	86	mW
P _{S-1CH-02}	SERDES power (one channel @ 250 Mbps)	76	mW

1. One quarter of the total quad power (includes contribution from common circuits, all channels in the quad operating, pre-emphasis disabled, equalization enabled).
2. Typical values measured at 25°C and 1.2V.

Signal Descriptions

Signal Name	I/O	Description
General Purpose		
P[Edge] [Row/Column Number*]_[A/B]	I/O	<p>[Edge] indicates the edge of the device on which the pad is located. Valid edge designations are L (Left), B (Bottom), R (Right), T (Top).</p> <p>[Row/Column Number] indicates the PFU row or the column of the device on which the PIC exists. When Edge is T (Top) or B (Bottom), only need to specify Row Number. When Edge is L (Left) or R (Right), only need to specify Column Number.</p> <p>[A/B] indicates the PIO within the PIC to which the pad is connected. Some of these user-programmable pins are shared with special function pins. These pins, when not used as special purpose pins, can be programmed as I/Os for user logic. During configuration the user-programmable I/Os are tri-stated with an internal pull-up resistor enabled. If any pin is not used (or not bonded to a package pin), it is also tri-stated with an internal pull-up resistor enabled after configuration. See “Typical sysI/O I/O Behavior During Power-up” for more information about I/O behavior during power-up.</p>
GSRN	I	Global RESET signal (active low). Any I/O pin can be GSRN.
NC	—	No connect.
GND	—	Ground. Dedicated pins.
V _{CC}	—	Power supply pins for core logic. Dedicated pins.
V _{CCAUX}	—	Auxiliary power supply pin. This dedicated pin powers all the differential and referenced input buffers.
V _{CCIOx}	—	Dedicated power supply pins for I/O bank x.
V _{CCPLL}	—	PLL supply pins. Should be tied to V _{CC} even when the corresponding PLL is unused.
V _{REF1_x} , V _{REF2_x}	—	Reference supply pins for I/O bank x. Pre-determined pins in each bank are assigned as V _{REF} inputs. When not used, they may be used as I/O pins.
XRES ⁴	—	10K ohm +/-1% resistor must be connected between this pad and ground.
PLLCAP ⁴	—	External capacitor connection for PLL.
PLL, DLL and Clock Functions (Used as user programmable I/O pins when not in use for PLL or clock pins)		
[LOC][num]_V _{CCPLL}	—	Power supply pin for PLL: LUM, LLM, RUM, RLM, num = row from center.
[LOC][num]_GPLL[T, C]_IN_A	I	General Purpose PLL (GPLL) input pads: LUM, LLM, RUM, RLM, num = row from center, T = true and C = complement, index A,B,C...at each side.
[LOC][num]_GPLL[T, C]_FB_A	I	Optional feedback GPLL input pads: LUM, LLM, RUM, RLM, num = row from center, T = true and C = complement, index A,B,C...at each side.
[LOC][num]_SPLL[T, C]_IN_A ⁵	I	Secondary PLL (SPLL) input pads: LUM, LLM, RUM, RLM, num = row from center, T = true and C = complement, index A,B,C...at each side.
[LOC][num]_SPLL[T, C]_FB_A ⁵	I	Optional feedback (SPLL) input pads: LUM, LLM, RUM, RLM, num = row from center, T = true and C = complement, index A,B,C...at each side.
[LOC][num]_DLL[T, C]_IN_A	I	DLL input pads: LUM, LLM, RUM, RLM, num = row from center, T = true and C = complement, index A,B,C...at each side.
[LOC][num]_DLL[T, C]_FB_A	I	Optional feedback (DLL) input pads: LUM, LLM, RUM, RLM, num = row from center, T = true and C = complement, index A,B,C...at each side.
PCLK[T, C]_[n:0]_[3:0]	I	Primary Clock pads, T = true and C = complement, n per side, indexed by bank and 0,1,2,3 within bank.

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LFE2-20E/SE Logic Signal Connections: 256 fpBGA

LFE2-20E/SE					
Ball Number	Ball Number	Ball/Pad Function	Bank	Dual Function	Differential
C3	C3	PL2A	7	VREF2_7	T (LVDS)*
C2	C2	PL2B	7	VREF1_7	C (LVDS)*
VCCIO	VCCIO	VCCIO7	7		
-	GND	GNDIO7	7		
D3	D3	PL7A	7	LDQ8	T
D4	D4	PL6A	7	LDQ8	T (LVDS)*
D2	D2	PL7B	7	LDQ8	C
GND	GND	GNDIO7	-		
E4	E4	PL6B	7	LDQ8	C (LVDS)*
B1	B1	PL13A	7	LDQ16	T
C1	C1	PL13B	7	LDQ16	C
F5	F5	PL15A	7	LDQ16	T
VCCIO	VCC	VCCIO	7		
F4	F4	PL14A	7	LDQ16	T (LVDS)*
G6	G6	PL15B	7	LDQ16	C
G4	G4	PL14B	7	LDQ16	C (LVDS)*
D1	D1	PL16A	7	LDQS16	T (LVDS)*
GND	GND	GNDIO7	-		
E1	E1	PL16B	7	LDQ16	C (LVDS)*
F3	F3	PL17A	7	LDQ16	T
G3	G3	PL17B	7	LDQ16	C
VCCIO	VCCIO	VCCIO7	7		
F2	F2	PL18A	7	LDQ16	T (LVDS)*
F1	F1	PL18B	7	LDQ16	C (LVDS)*
GND	GND	GNDIO7	-		
G2	G2	PL19A	7	PCLKT7_0/LDQ16	T
G1	G1	PL19B	7	PCLKC7_0/LDQ16	C
H6	H6	PL21A	6	PCLKT6_0/LDQ25	T (LVDS)*
VCCIO	VCCIO	VCCIO6	6		
H5	H5	PL21B	6	PCLKC6_0/LDQ25	C (LVDS)*
H4	H4	PL22A	6	VREF2_6/LDQ25	T
GND	GND	GNDIO6	-		
H3	H3	PL22B	6	VREF1_6/LDQ25	C
H2	H2	PL27A	6	LLM0_GDLLT_IN_A**/LDQ25	T (LVDS)*
H1	H1	PL27B	6	LLM0_GDLLC_IN_A**/LDQ25	C (LVDS)*
G10	G10	VCC	-		
J4	J4	PL28A	6	LLM0_GDLLT_FB_A/LDQ25	T
J5	J5	PL28B	6	LLM0_GDLLC_FB_A/LDQ25	C
J6	J6	LLM0_PLLCAP	6		
K4	K4	PL30A	6	LLM0_GPLLT_IN_A**/LDQ34	T (LVDS)*
GND	GND	GNDIO6	-		

**LFE2-12E/SE and LFE2-20E/SE Logic Signal Connections: 484 fpBGA
 (Cont.)**

LFE2-12E/12SE					LFE2-20E/20SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
R8	VCCIO6	6			VCCIO6	6		
J8	VCCIO7	7			VCCIO7	7		
K7	VCCIO7	7			VCCIO7	7		
L7	VCCIO7	7			VCCIO7	7		
M7	VCCIO7	7			VCCIO7	7		
P15	VCCIO8	8			VCCIO8	8		
R15	VCCIO8	8			VCCIO8	8		
C5	VCCAUX	-			VCCAUX	-		
D11	VCCAUX	-			VCCAUX	-		
E17	VCCAUX	-			VCCAUX	-		
E6	VCCAUX	-			VCCAUX	-		
F13	VCCAUX	-			VCCAUX	-		
G18	VCCAUX	-			VCCAUX	-		
G5	VCCAUX	-			VCCAUX	-		
K5	VCCAUX	-			VCCAUX	-		
M17	VCCAUX	-			VCCAUX	-		
P17	VCCAUX	-			VCCAUX	-		
R5	VCCAUX	-			VCCAUX	-		
V11	VCCAUX	-			VCCAUX	-		
V13	VCCAUX	-			VCCAUX	-		
V15	VCCAUX	-			VCCAUX	-		
V7	VCCAUX	-			VCCAUX	-		
V8	VCCAUX	-			VCCAUX	-		
A1	GND	-			GND	-		
A22	GND	-			GND	-		
AA19	GND	-			GND	-		
AA4	GND	-			GND	-		
AB1	GND	-			GND	-		
AB22	GND	-			GND	-		
B19	GND	-			GND	-		
B4	GND	-			GND	-		
C14	GND	-			GND	-		
C9	GND	-			GND	-		
D2	GND	-			GND	-		
D21	GND	-			GND	-		
F17	GND	-			GND	-		
F6	GND	-			GND	-		
H10	GND	-			GND	-		
H11	GND	-			GND	-		
H12	GND	-			GND	-		
H13	GND	-			GND	-		
J14	GND	-			GND	-		
J20	GND	-			GND	-		
J3	GND	-			GND	-		

**LFE2-35E/SE and LFE2-50E/SE Logic Signal Connections: 484 fpBGA
 (Cont.)**

LFE2-35E/SE					LFE2-50E/SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
D15	PT52A	1		T	PT61A	1		T
E15	PT51B	1		C	PT60B	1		C
F15	PT51A	1		T	PT60A	1		T
GNDIO	GNDIO1	-			GNDIO1	-		
B15	PT49B	1		C	PT58B	1		C
VCCIO	VCCIO1	1			VCCIO	1		
A15	PT49A	1		T	PT58A	1		T
B14	PT48B	1		C	PT57B	1		C
A14	PT48A	1		T	PT57A	1		T
D14	PT46B	1		C	PT55B	1		C
C13	PT46A	1		T	PT55A	1		T
GNDIO	GNDIO1	-			GNDIO1	-		
E14	PT45B	1		C	PT54B	1		C
F14	PT45A	1		T	PT54A	1		T
A13	PT44B	1		C	PT53B	1		C
B13	PT44A	1		T	PT53A	1		T
VCCIO	VCCIO1	1			VCCIO	1		
E13	PT43B	1		C	PT52B	1		C
D13	PT43A	1		T	PT52A	1		T
E12	PT42B	1		C	PT51B	1		C
D12	PT42A	1		T	PT51A	1		T
GNDIO	GNDIO1	-			GNDIO1	-		
A12	PT40B	1		C	PT49B	1		C
A11	PT40A	1		T	PT49A	1		T
VCCIO	VCCIO1	1			VCCIO	1		
B12	PT39B	1	PCLKC1_0	C	PT48B	1	PCLKC1_0	C
C12	PT39A	1	PCLKT1_0	T	PT48A	1	PCLKT1_0	T
F12	XRES	1			XRES	1		
B10	PT37B	0	PCLKC0_0	C	PT46B	0	PCLKC0_0	C
GNDIO	GNDIO0	-			GNDIO0	0		
B11	PT37A	0	PCLKT0_0	T	PT46A	0	PCLKT0_0	T
A10	PT36B	0		C	PT45B	0		C
A9	PT36A	0		T	PT45A	0		T
C11	PT35B	0		C	PT44B	0		C
VCCIO	VCCIO0	0			VCCIO	0		
C10	PT35A	0		T	PT44A	0		T
E11	PT34B	0		C	PT43B	0		C
F11	PT34A	0		T	PT43A	0		T
A8	PT33B	0		C	PT42B	0		C
A7	PT33A	0		T	PT42A	0		T
B8	PT32B	0		C	PT41B	0		C
GNDIO	GNDIO0	-			GNDIO0	0		
B9	PT32A	0		T	PT41A	0		T
VCCIO	VCCIO0	0			VCCIO	0		
B7	PT30B	0		C	PT39B	0		C
A6	PT30A	0		T	PT39A	0		T

**LFE2-20E/SE and LFE2-35E/SE Logic Signal Connections: 672 fpBGA
 (Cont.)**

LFE2-20E/20SE					LFE2-35E/35SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
D4	PT7B	0		C	PT7B	0		C
D3	PT7A	0		T	PT7A	0		T
C2	PT6B	0		C	PT6B	0		C
C1	PT6A	0		T	PT6A	0		T
G8	PT5B	0		C	PT5B	0		C
GND	GNDIO0	-			GNDIO0	-		
G7	PT5A	0		T	PT5A	0		T
E7	PT4B	0		C	PT4B	0		C
VCCIO	VCCIO0	0			VCCIO0	0		
F7	PT4A	0		T	PT4A	0		T
E6	PT3B	0		C	PT3B	0		C
E5	PT3A	0		T	PT3A	0		T
G6	PT2B	0	VREF2_0	C	PT2B	0	VREF2_0	C
G5	PT2A	0	VREF1_0	T	PT2A	0	VREF1_0	T
L12	VCC	-			VCC	-		
L13	VCC	-			VCC	-		
L14	VCC	-			VCC	-		
L15	VCC	-			VCC	-		
M11	VCC	-			VCC	-		
M12	VCC	-			VCC	-		
M15	VCC	-			VCC	-		
M16	VCC	-			VCC	-		
N11	VCC	-			VCC	-		
N16	VCC	-			VCC	-		
P11	VCC	-			VCC	-		
P16	VCC	-			VCC	-		
R11	VCC	-			VCC	-		
R12	VCC	-			VCC	-		
R15	VCC	-			VCC	-		
R16	VCC	-			VCC	-		
T12	VCC	-			VCC	-		
T13	VCC	-			VCC	-		
T14	VCC	-			VCC	-		
T15	VCC	-			VCC	-		
D11	VCCIO0	0			VCCIO0	0		
D6	VCCIO0	0			VCCIO0	0		
G9	VCCIO0	0			VCCIO0	0		
K12	VCCIO0	0			VCCIO0	0		
J12	VCCIO0	0			VCCIO0	0		
D16	VCCIO1	1			VCCIO1	1		
D21	VCCIO1	1			VCCIO1	1		
G18	VCCIO1	1			VCCIO1	1		
J15	VCCIO1	1			VCCIO1	1		
K15	VCCIO1	1			VCCIO1	1		
F23	VCCIO2	2			VCCIO2	2		
J20	VCCIO2	2			VCCIO2	2		

**LFE2-50E/SE and LFE2-70E/SE Logic Signal Connections: 672 fpBGA
 (Cont.)**

LFE2-50E/SE					LFE2-70E/SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
GND	GNDIO5	-			GNDIO5	-		
W10	PB20A	5	BDQ24	T	PB29A	5	BDQ33	T
Y10	PB20B	5	BDQ24	C	PB29B	5	BDQ33	C
W11	PB21A	5	BDQ24	T	PB30A	5	BDQ33	T
AA10	PB21B	5	BDQ24	C	PB30B	5	BDQ33	C
AC8	PB22A	5	BDQ24	T	PB31A	5	BDQ33	T
AD8	PB22B	5	BDQ24	C	PB31B	5	BDQ33	C
VCCIO	VCCIO5	5			VCCIO5	5		
AB8	PB23A	5	BDQ24	T	PB32A	5	BDQ33	T
AB10	PB23B	5	BDQ24	C	PB32B	5	BDQ33	C
GND	GNDIO5	-			GNDIO5	-		
AE6	PB24A	5	BDQS24	T	PB33A	5	BDQS33	T
AF6	PB24B	5	BDQ24	C	PB33B	5	BDQ33	C
AA11	PB25A	5	BDQ24	T	PB34A	5	BDQ33	T
AC9	PB25B	5	BDQ24	C	PB34B	5	BDQ33	C
AB9	PB26A	5	BDQ24	T	PB35A	5	BDQ33	T
AD9	PB26B	5	BDQ24	C	PB35B	5	BDQ33	C
VCCIO	VCCIO5	5			VCCIO5	5		
Y11	PB27A	5	BDQ24	T	PB36A	5	BDQ33	T
AB11	PB27B	5	BDQ24	C	PB36B	5	BDQ33	C
AE7	PB28A	5	BDQ24	T	PB37A	5	BDQ33	T
AF7	PB28B	5	BDQ24	C	PB37B	5	BDQ33	C
GND	GNDIO5	-			GNDIO5	-		
AC10	PB29A	5	BDQ33	T	PB38A	5	BDQ42	T
AD10	PB29B	5	BDQ33	C	PB38B	5	BDQ42	C
AA12	PB30A	5	BDQ33	T	PB39A	5	BDQ42	T
W12	PB30B	5	BDQ33	C	PB39B	5	BDQ42	C
AB12	PB31A	5	BDQ33	T	PB40A	5	BDQ42	T
VCCIO	VCCIO5	5			VCCIO5	5		
Y12	PB31B	5	BDQ33	C	PB40B	5	BDQ42	C
AD12	PB32A	5	BDQ33	T	PB41A	5	BDQ42	T
AC12	PB32B	5	BDQ33	C	PB41B	5	BDQ42	C
AC13	PB33A	5	BDQS33	T	PB42A	5	BDQS42	T
GND	GNDIO5	-			GNDIO5	-		
AA13	PB33B	5	BDQ33	C	PB42B	5	BDQ42	C
AD13	PB34A	5	BDQ33	T	PB43A	5	BDQ42	T
AC14	PB34B	5	BDQ33	C	PB43B	5	BDQ42	C
AE8	PB35A	5	BDQ33	T	PB44A	5	BDQ42	T
VCCIO	VCCIO5	5			VCCIO5	5		
AF8	PB35B	5	BDQ33	C	PB44B	5	BDQ42	C
AB15	PB36A	5	BDQ33	T	PB45A	5	BDQ42	T
Y13	PB36B	5	BDQ33	C	PB45B	5	BDQ42	C
AE9	PB37A	5	BDQ33	T	PB46A	5	BDQ42	T
GND	GNDIO5	-			GNDIO5	-		
AF9	PB37B	5	BDQ33	C	PB46B	5	BDQ42	C
W13	PB38A	5	BDQ42	T	PB47A	5	BDQ51	T

LFE2-70E/SE Logic Signal Connections: 900 fpBGA (Cont.)

LFE2-70E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential
D25	PT99A	1		T
J22	PT98B	1		C
J21	PT98A	1		T
VCCIO	VCCIO1	1		
B25	PT97B	1		C
A25	PT97A	1		T
E24	PT96B	1		C
F24	PT96A	1		T
GND	GNDIO1	-		
F23	PT95B	1		C
H22	PT95A	1		T
D24	PT94B	1		C
C24	PT94A	1		T
VCCIO	VCCIO1	1		
E23	PT93B	1		C
G23	PT93A	1		T
B24	PT92B	1		C
A24	PT92A	1		T
C27	PT91B	1		C
GND	GNDIO1	-		
D27	PT91A	1		T
C26	PT90B	1		C
D26	PT90A	1		T
A27	PT89B	1		C
VCCIO	VCCIO1	1		
B27	PT89A	1		T
A28	PT88B	1		C
B28	PT88A	1		T
A29	PT87B	1		C
B29	PT87A	1		T
GND	GNDIO1	-		
VCCIO	VCCIO1	1		
H21	PT80B	1		C
F22	PT80A	1		T
VCCIO	VCCIO1	1		
B23	PT79B	1		C
A23	PT79A	1		T
G24	PT78B	1		C
E22	PT78A	1		T
GND	GNDIO1	-		
D22	PT77B	1		C
C22	PT77A	1		T
G22	PT76B	1		C

LFE2-70E/SE Logic Signal Connections: 900 fpBGA (Cont.)

LFE2-70E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential
C13	GND	-		
C18	GND	-		
C23	GND	-		
C28	GND	-		
C3	GND	-		
C8	GND	-		
H28	GND	-		
H3	GND	-		
L14	GND	-		
L15	GND	-		
L16	GND	-		
L17	GND	-		
M12	GND	-		
M13	GND	-		
M14	GND	-		
M15	GND	-		
M16	GND	-		
M17	GND	-		
M18	GND	-		
M19	GND	-		
N12	GND	-		
N13	GND	-		
N14	GND	-		
N15	GND	-		
N16	GND	-		
N17	GND	-		
N18	GND	-		
N19	GND	-		
N28	GND	-		
N3	GND	-		
P11	GND	-		
P12	GND	-		
P13	GND	-		
P14	GND	-		
P15	GND	-		
P16	GND	-		
P17	GND	-		
P18	GND	-		
P19	GND	-		
P20	GND	-		
R11	GND	-		
R12	GND	-		
R13	GND	-		

**LFE2M20E/SE and LFE2M35E/SE Logic Signal Connections: 484 fpBGA
 (Cont.)**

LFE2M20E/SE					LFE2M35E/SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
G18	VCCIO2	2			VCCIO2	2		
J15	VCCIO2	2			VCCIO2	2		
K19	VCCIO2	2			VCCIO2	2		
N19	VCCIO3	3			VCCIO3	3		
P15	VCCIO3	3			VCCIO3	3		
T18	VCCIO3	3			VCCIO3	3		
V21	VCCIO3	3			VCCIO3	3		
AA18	VCCIO4	4			VCCIO4	4		
R14	VCCIO4	4			VCCIO4	4		
V16	VCCIO4	4			VCCIO4	4		
W13	VCCIO4	4			VCCIO4	4		
AA5	VCCIO5	5			VCCIO5	5		
R9	VCCIO5	5			VCCIO5	5		
V7	VCCIO5	5			VCCIO5	5		
W10	VCCIO5	5			VCCIO5	5		
N4	VCCIO6	6			VCCIO6	6		
P8	VCCIO6	6			VCCIO6	6		
T5	VCCIO6	6			VCCIO6	6		
V2	VCCIO6	6			VCCIO6	6		
E2	VCCIO7	7			VCCIO7	7		
G5	VCCIO7	7			VCCIO7	7		
J8	VCCIO7	7			VCCIO7	7		
K4	VCCIO7	7			VCCIO7	7		
AA22	VCCIO8	8			VCCIO8	8		
U19	VCCIO8	8			VCCIO8	8		
H11	VCCAUX	-			VCCAUX	-		
H12	VCCAUX	-			VCCAUX	-		
L15	VCCAUX	-			VCCAUX	-		
L8	VCCAUX	-			VCCAUX	-		
M15	VCCAUX	-			VCCAUX	-		
M8	VCCAUX	-			VCCAUX	-		
R11	VCCAUX	-			VCCAUX	-		
R12	VCCAUX	-			VCCAUX	-		
A1	GND	-			GND	-		
A10	GND	-			GND	-		
A16	GND	-			GND	-		
A22	GND	-			GND	-		
AA19	GND	-			GND	-		
AA4	GND	-			GND	-		
AB1	GND	-			GND	-		
AB22	GND	-			GND	-		
B13	GND	-			GND	-		
B19	GND	-			GND	-		
B4	GND	-			GND	-		
D16	GND	-			GND	-		
D2	GND	-			GND	-		
D21	GND	-			GND	-		
D7	GND	-			GND	-		

**LFE2M35E/SE and LFE2M50E/SE Logic Signal Connections: 672 fpBGA
 (Cont.)**

LFE2M35E/SE					LFE2M50E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential	
A12	PT35B	0		C	PT44B	0		C	
VCCIO	VCCIO0	0			VCCIO0	0			
A11	PT35A	0		T	PT44A	0		T	
D12	PT34B	0		C	PT43B	0		C	
H16	PT34A	0		T	PT43A	0		T	
H18	PT33B	0		C	PT42B	0		C	
H15	PT33A	0		T	PT42A	0		T	
A10	PT32B	0		C	PT41B	0		C	
GNDIO	GNDIO0	-			GNDIO0	-			
B10	PT32A	0		T	PT41A	0		T	
D11	PT31B	0		C	PT40B	0		C	
VCCIO	VCCIO0	0			VCCIO0	0			
G14	PT31A	0		T	PT40A	0		T	
E11	PT30B	0		C	PT39B	0		C	
F13	PT30A	0		T	PT39A	0		T	
D10	PT29B	0		C	PT38B	0		C	
H14	PT29A	0		T	PT38A	0		T	
GNDIO	GNDIO0	-			GNDIO0	-			
VCCIO	VCCIO0	0			VCCIO0	0			
A9	PT24B	0		C	PT24B	0		C	
C10	PT23B	0		C	PT23B	0		C	
GNDIO	GNDIO0	-			GNDIO0	-			
E8	PT23A	0		T	PT23A	0		T	
B9	PT22B	0		C	PT22B	0		C	
A8	PT22A	0		T	PT22A	0		T	
VCCIO	VCCIO0	0			VCCIO0	0			
F12	PT21B	0		C	PT21B	0		C	
E10	PT21A	0		T	PT21A	0		T	
G13	PT20B	0		C	PT20B	0		C	
C9	PT20A	0		T	PT20A	0		T	
B8	PT19B	0		C	PT19B	0		C	
GNDIO	GNDIO0	-			GNDIO0	-			
A7	PT19A	0		T	PT19A	0		T	
D9	PT18B	0		C	PT18B	0		C	
H13	PT18A	0		T	PT18A	0		T	
D6	PT17B	0		C	PT17B	0		C	
C7	PT17A	0		T	PT17A	0		T	
VCCIO	VCCIO0	0			VCCIO0	0			
C8	PT16B	0		C	PT16B	0		C	
G12	PT16A	0		T	PT16A	0		T	
D8	PT15B	0		C	PT15B	0		C	
H12	PT15A	0		T	PT15A	0		T	
GNDIO	GNDIO0	-			GNDIO0	-			
A6	PT14B	0		C	PT14B	0		C	
A5	PT14A	0		T	PT14A	0		T	
A4	PT13B	0		C	PT13B	0		C	
A3	PT13A	0		T	PT13A	0		T	
VCCIO	VCCIO0	0			VCCIO0	0			

LFE2M50E/SE and LFE2M70E/SE Logic Signal Connections: 900 fpBGA
(Cont.)

LFE2M50E/SE					LFE2M70E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential	
AA6	NC	-			PL79B	6	LDQ82	C	
AB4	NC	-			PL80A	6	LDQ82	T (LVDS)*	
-	-	-			VCCIO6	6			
AB5	NC	-			PL80B	6	LDQ82	C (LVDS)*	
AA8	NC	-			PL81A	6	LDQ82	T	
AA9	NC	-			PL81B	6	LDQ82	C	
AC1	PL62A	6	LLM0_GPLLT_IN_A**	T (LVDS)*	PL82A	6	LLM0_GPLLT_IN_A**/LDQS82	T (LVDS)*	
GNDIO	GNDIO6	-			GNDIO6	-			
AC2	PL62B	6	LLM0_GPLLC_IN_A**	C (LVDS)*	PL82B	6	LLM0_GPLLC_IN_A**/LDQ82	C (LVDS)*	
AC4	PL63A	6	LLM0_GPLLT_FB_A	T	PL83A	6	LLM0_GPLLT_FB_A/LDQ82	T	
AC3	PL63B	6	LLM0_GPLLC_FB_A	C	PL83B	6	LLM0_GPLLC_FB_A/LDQ82	C	
VCCIO	VCCIO6	6			VCCIO6	6			
AC7	PL64A	6	LLM0_GDLLT_IN_A**	T (LVDS)*	PL84A	6	LLM0_GDLLT_IN_A**/LDQ82	T (LVDS)*	
AC6	PL64B	6	LLM0_GDLLC_IN_A**	C (LVDS)*	PL84B	6	LLM0_GDLLC_IN_A**/LDQ82	C (LVDS)*	
AC5	PL65A	6	LLM0_GDLLT_FB_A	T	PL85A	6	LLM0_GDLLT_FB_A/LDQ82	T	
AD3	PL65B	6	LLM0_GDLLC_FB_A	C	PL85B	6	LLM0_GDLLC_FB_A/LDQ82	C	
GNDIO	GNDIO6	-			GNDIO6	-			
AB8	LLM0_PLLCAP	6			LLM0_PLLCAP	6			
AD2	PL67A	6	LDQ71	T (LVDS)*	PL87A	6		T	
AD1	PL67B	6	LDQ71	C (LVDS)*	PL87B	6		C	
AE2	TCK	-			TCK	-			
AE1	TDI	-			TDI	-			
AF2	TMS	-			TMS	-			
AF1	TDO	-			TDO	-			
AG1	VCCJ	-			VCCJ	-			
AH1	VCC	-			LLC_SQ_VCCRX3	14			
AK2	PB11A	5	BDQ15	T	LLC_SQ_HDINP3	14		T	
AJ1	NC	-			LLC_SQ_VCCIB3	14			
AJ2	PB11B	5	BDQ15	C	LLC_SQ_HDINN3	14		C	
AH4	VCC	-			LLC_SQ_VCCTX3	14			
AK5	PB13A	5	BDQ15	T	LLC_SQ_HDOUTP3	14		T	
AK4	NC	-			LLC_SQ_VCCOB3	14			
AJ5	PB13B	5	BDQ15	C	LLC_SQ_HDOUTN3	14		C	
AH5	VCC	-			LLC_SQ_VCCTX2	14			
AJ6	PB14B	5	BDQ15	C	LLC_SQ_HDOUTN2	14		C	
AH6	NC	-			LLC_SQ_VCCOB2	14			
AK6	PB14A	5	BDQ15	T	LLC_SQ_HDOUTP2	14		T	
AH2	VCC	-			LLC_SQ_VCCRX2	14			
AJ3	PB12B	5	BDQ15	C	LLC_SQ_HDINN2	14		C	
AH3	NC	-			LLC_SQ_VCCIB2	14			
AK3	PB12A	5	BDQ15	T	LLC_SQ_HDINP2	14		T	
AH7	VCC	-			LLC_SQ_VCCP	14			
AG7	PB15A	5	BDQS15	T	LLC_SQ_REFCLKP	14		T	
AF7	PB15B	5	BDQ15	C	LLC_SQ_REFCLKN	14		C	
AJ7	VCCAUX	-			LLC_SQ_VCCAUX33	14			
AK11	PB18A	5	BDQ15	T	LLC_SQ_HDINP1	14		T	
AH11	NC	-			LLC_SQ_VCCIB1	14			
AJ11	PB18B	5	BDQ15	C	LLC_SQ_HDINN1	14		C	

LFE2M100E/SE Logic Signal Connections: 900 fpBGA (Cont.)

LFE2M100E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential
H14	PT61A	0		T
A14	PT60B	0		C
B14	PT60A	0		T
D13	PT59B	0		C
GNDIO	GNDIO0	-		
F13	PT59A	0		T
G13	PT58B	0		C
VCCIO	VCCIO0	0		
J11	PT58A	0		T
D4	PT57B	0		
D5	PT56A	0		
E5	PT55B	0		C
F6	PT55A	0		T
GNDIO	GNDIO0	-		
VCCIO	VCCIO0	0		
F7	PT52B	0		C
D8	PT52A	0		T
GNDIO	GNDIO0	-		
J13	PT50B	0		C
G11	PT50A	0		T
H13	PT49B	0		C
H12	PT49A	0		T
VCCIO	VCCIO0	0		
E8	PT48B	0		C
D9	PT48A	0		T
D12	PT46B	0		C
GNDIO	GNDIO0	-		
E13	PT46A	0		T
VCCIO	VCCIO0	0		
GNDIO	GNDIO0	-		
J12	PT31B	0		C
-	-	-		
VCCIO	VCCIO0	0		
H10	PT31A	0		T
E12	PT30B	0		C
D11	PT30A	0		T
H11	PT29B	0		C
F11	PT29A	0		T
C13	ULC_SQ_VCCR0	11		
A12	ULC_SQ_HDINP0	11		T
B13	ULC_SQ_VCCIB0	11		
B12	ULC_SQ_HDINN0	11		C
C10	ULC_SQ_VCCTX0	11		

LFE2M70E/SE and LFE2M100E/SE Logic Signal Connections: 1152 fpBGA (Cont.)

LFE2M70E/SE				LFE2M100E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
AA25	PR74B	3	RDQ73	C	PR82B	3	RDQ81	C
VCCIO	VCCIO3	3			VCCIO3	3		
AC24	PR74A	3	RDQ73	T	PR82A	3	RDQ81	T
AC33	PR73B	3	RDQ73	C (LVDS)*	PR81B	3	RDQ81	C (LVDS)*
AC34	PR73A	3	RDQS73	T (LVDS)*	PR81A	3	RDQS81	T (LVDS)*
GNDIO	GNDIO3	-			GNDIO3	-		
AB24	PR72B	3	RDQ73	C	PR80B	3	RDQ81	C
Y26	PR72A	3	RDQ73	T	PR80A	3	RDQ81	T
AB33	PR71B	3	RDQ73	C (LVDS)*	PR79B	3	RDQ81	C (LVDS)*
AB34	PR71A	3	RDQ73	T (LVDS)*	PR79A	3	RDQ81	T (LVDS)*
VCCIO	VCCIO3	3			VCCIO3	3		
Y27	PR70B	3	RDQ73	C	PR78B	3	RDQ81	C
AB29	PR70A	3	RDQ73	T	PR78A	3	RDQ81	T
AA34	PR69B	3	RDQ73	C (LVDS)*	PR77B	3	RDQ81	C (LVDS)*
AA33	PR69A	3	RDQ73	T (LVDS)*	PR77A	3	RDQ81	T (LVDS)*
AA31	PR67B	3	RDQ64	C	PR75B	3	RDQ72	C
AA32	PR67A	3	RDQ64	T	PR75A	3	RDQ72	T
GNDIO	GNDIO3	-			GNDIO3	-		
AA28	PR66B	3	RDQ64	C (LVDS)*	PR74B	3	RDQ72	C (LVDS)*
AA29	PR66A	3	RDQ64	T (LVDS)*	PR74A	3	RDQ72	T (LVDS)*
AA30	PR65B	3	RDQ64	C	PR73B	3	RDQ72	C
AB30	PR65A	3	RDQ64	T	PR73A	3	RDQ72	T
VCCIO	VCCIO3	3			VCCIO3	3		
Y28	PR64B	3	RDQ64	C (LVDS)*	PR72B	3	RDQ72	C (LVDS)*
Y29	PR64A	3	RDQS64	T (LVDS)*	PR72A	3	RDQS72	T (LVDS)*
AA24	PR63B	3	RDQ64	C	PR71B	3	RDQ72	C
GNDIO	GNDIO3	-			GNDIO3	-		
Y25	PR63A	3	RDQ64	T	PR71A	3	RDQ72	T
Y31	PR62B	3	RDQ64	C (LVDS)*	PR70B	3	RDQ72	C (LVDS)*
Y30	PR62A	3	RDQ64	T (LVDS)*	PR70A	3	RDQ72	T (LVDS)*
Y24	PR61B	3	RDQ64	C	PR69B	3	RDQ72	C
VCCIO	VCCIO3	3			VCCIO3	3		
W25	PR61A	3	RDQ64	T	PR69A	3	RDQ72	T
Y33	PR60B	3	RDQ64	C (LVDS)*	PR68B	3	RDQ72	C (LVDS)*
Y34	PR60A	3	RDQ64	T (LVDS)*	PR68A	3	RDQ72	T (LVDS)*
W28	PR58B	3	RLM3_SPLL_C_FB_A/RDQ55	C	PR66B	3	RLM4_SPLL_C_FB_A/RDQ63	C
GNDIO	GNDIO3	-			GNDIO3	-		
V26	PR58A	3	RLM3_SPLLT_FB_A/RDQ55	T	PR66A	3	RLM4_SPLLT_FB_A/RDQ63	T
V28	PR57B	3	RLM3_SPLL_C_IN_A/RDQ55	C (LVDS)*	PR65B	3	RLM4_SPLL_C_IN_A/RDQ63	C (LVDS)*
V27	PR57A	3	RLM3_SPLLT_IN_A/RDQ55	T (LVDS)*	PR65A	3	RLM4_SPLLT_IN_A/RDQ63	T (LVDS)*
V25	PR56B	3	RDQ55	C	PR64B	3	RDQ63	C
VCCIO	VCCIO3	3			VCCIO3	3		
W24	PR56A	3	RDQ55	T	PR64A	3	RDQ63	T
W33	PR55B	3	RDQ55	C (LVDS)*	PR63B	3	RDQ63	C (LVDS)*
W34	PR55A	3	RDQS55	T (LVDS)*	PR63A	3	RDQS63	T (LVDS)*
GNDIO	GNDIO3	-			GNDIO3	-		
V24	PR54B	3	RDQ55	C	PR62B	3	RDQ63	C
U26	PR54A	3	RDQ55	T	PR62A	3	RDQ63	T
W29	PR53B	3	RDQ55	C (LVDS)*	PR61B	3	RDQ63	C (LVDS)*

LFE2M70E/SE and LFE2M100E/SE Logic Signal Connections: 1152 fpBGA (Cont.)

LFE2M70E/SE				LFE2M100E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
E5	ULC_SQ_REFCLKN	11		C	ULC_SQ_REFCLKN	11		C
D5	ULC_SQ_REFCLKP	11		T	ULC_SQ_REFCLKP	11		T
D6	ULC_SQ_VCCP	11			ULC_SQ_VCCP	11		
C5	ULC_SQ_HDINP2	11		T	ULC_SQ_HDINP2	11		T
D4	ULC_SQ_VCCIB2	11			ULC_SQ_VCCIB2	11		
C4	ULC_SQ_HDINN2	11		C	ULC_SQ_HDINN2	11		C
B5	ULC_SQ_VCCRX2	11			ULC_SQ_VCCRX2	11		
A5	ULC_SQ_HDOUDP2	11		T	ULC_SQ_HDOUDP2	11		T
D3	ULC_SQ_VCCOB2	11			ULC_SQ_VCCOB2	11		
A4	ULC_SQ_HDOUTN2	11		C	ULC_SQ_HDOUTN2	11		C
B4	ULC_SQ_VCCTX2	11			ULC_SQ_VCCTX2	11		
A3	ULC_SQ_HDOUTN3	11		C	ULC_SQ_HDOUTN3	11		C
C1	ULC_SQ_VCCOB3	11			ULC_SQ_VCCOB3	11		
A2	ULC_SQ_HDOUDP3	11		T	ULC_SQ_HDOUDP3	11		T
B3	ULC_SQ_VCCTX3	11			ULC_SQ_VCCTX3	11		
C3	ULC_SQ_HDINN3	11		C	ULC_SQ_HDINN3	11		C
B1	ULC_SQ_VCCIB3	11			ULC_SQ_VCCIB3	11		
C2	ULC_SQ_HDINP3	11		T	ULC_SQ_HDINP3	11		T
B2	ULC_SQ_VCCRX3	11			ULC_SQ_VCCRX3	11		
AA13	VCC	-			VCC	-		
AA14	VCC	-			VCC	-		
AA15	VCC	-			VCC	-		
AA16	VCC	-			VCC	-		
AA17	VCC	-			VCC	-		
AA18	VCC	-			VCC	-		
AA19	VCC	-			VCC	-		
AA20	VCC	-			VCC	-		
AA21	VCC	-			VCC	-		
AA22	VCC	-			VCC	-		
AB14	VCC	-			VCC	-		
AB15	VCC	-			VCC	-		
AB20	VCC	-			VCC	-		
AB21	VCC	-			VCC	-		
N14	VCC	-			VCC	-		
N15	VCC	-			VCC	-		
N20	VCC	-			VCC	-		
N21	VCC	-			VCC	-		
P13	VCC	-			VCC	-		
P14	VCC	-			VCC	-		
P15	VCC	-			VCC	-		
P16	VCC	-			VCC	-		
P17	VCC	-			VCC	-		
P18	VCC	-			VCC	-		
P19	VCC	-			VCC	-		
P20	VCC	-			VCC	-		
P21	VCC	-			VCC	-		
P22	VCC	-			VCC	-		
R13	VCC	-			VCC	-		
R14	VCC	-			VCC	-		

Date	Version	Section	Change Summary
August 2006 (cont.)	01.1 (cont.)	Pinout Information (cont.)	Added Information on: Available Device Resources per Packaged Device table.
		Ordering Information	Updated ordering part number table to include ECP2-12. Updated topside mark drawing.
September 2006	02.0	Multiple	Added information regarding LatticeECP2M support throughout.
September 2006	02.1	DC and Switching Characteristics	Added Receiver Total Jitter Tolerance Specification table.
			Removed power-up requirements for proper configuration footnote in Recommended Operating Conditions table.
December 2006	02.2	Introduction	LatticeECP2M Selection Guide table has been updated.
		Architecture	Figure 2-16. Per Region Secondary Clock Selection has been updated.
			Figure 2-39. Simplified Channel Block Diagram for SERDES and PCS has been updated.
		DC and Switching	Footnotes have been added to Recommended Operating Conditions.
			DC Electrical Characteristics table has been updated.
			Supply Current (Standby) tables have been updated.
			Initialization Supply Current table have been updated.
Updated timing numbers to include LFE2-12E (rev A 0.08).			
Pinout Information	Updated to include the entire ECP2 device information as well as 256-fpBGA and 484-fpBGA pin information for the ECP2M35E.		
Ordering Information	Updated to include the entire ECP2 and ECP2M device ordering information.		
February 2007	02.3	Architecture	Updated EBR Asynchronous Reset section.
March 2007	02.4	DC and Switching Characteristics	Power-sequencing footnotes have been added to the Recommended Operating Conditions. DDR2 performance has been updated to 266MHz.
March 2007	02.5	Introduction	Added "Security Series" to the LatticeECP2 and LatticeECP2M families.
		Architecture	Enhanced Configuration Option section updated.
		DC and Switching	Recommended Operating Conditions table - footnote 4 updated.
		Ordering Information	"Security Series" ordering part numbers added.
April 2007	02.6	Introduction	LatticeECP2M family table has been updated for user I/O counts.
		Ordering Information	LatticeECP2M family ordering part number section has been updated to add 1152-fpBGA package for the ECP2M70 and ECP2M100.
July 2007	02.7	Architecture	Updated text in Ripple Mode section.
		DC and Switching	ECP2/M Supply Current information has been updated. Typical Building Block Function Performance, External Switching Characteristics, Internal Switching Characteristics, Family Timing Adders, sysCLOCK GPLL Timing, sysCLOCK SPLL Timing, DLL Timing and sysCONFIG Port Timing Specifications have been updated (timing rev. A 0.10). SERDES timing information has been updated. PCI Express timing information has been updated.
		Pinout Information	Added LatticeECP2M20 pinout information.
August 2007	02.8	Introduction	1156-fpBGA package option has been removed from the LatticeECP2M family.
		Architecture	Table 2-16. Selectable Master Clock (CCLK) Frequencies During Configuration table has been updated.
		DC and Switching	Supply Current (Standby) table has been updated.
DSP Function timing has been updated.			