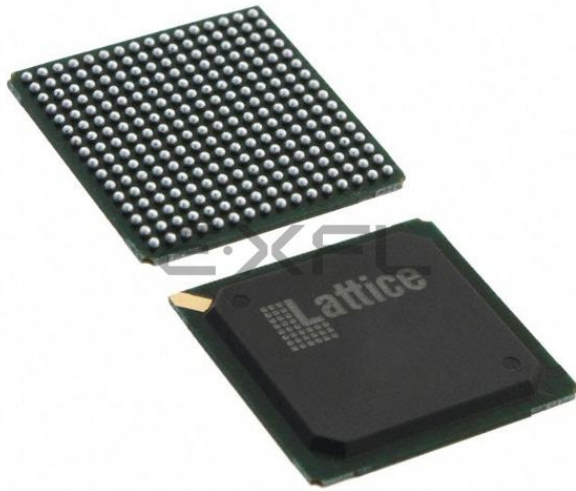




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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	2375
Number of Logic Elements/Cells	19000
Total RAM Bits	1246208
Number of I/O	140
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	256-BGA
Supplier Device Package	256-FPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfe2m20se-6f256c

Features

■ High Logic Density for System Integration

- 6K to 95K LUTs
- 90 to 583 I/Os

■ Embedded SERDES (LatticeECP2M Only)

- Data Rates 250 Mbps to 3.125 Gbps
- Up to 16 channels per device
PCI Express, Ethernet (1GbE, SGMII), OBSAI, CPRI and Serial RapidIO.

■ sysDSP™ Block

- 3 to 42 blocks for high performance multiply and accumulate
- Each block supports
 - One 36x36, four 18x18 or eight 9x9 multipliers

■ Flexible Memory Resources

- 55Kbits to 5308Kbits sysMEM™ Embedded Block RAM (EBR)
 - 18Kbit block
 - Single, pseudo dual and true dual port
 - Byte Enable Mode support
- 12K to 202Kbits distributed RAM
 - Single port and pseudo dual port

■ sysCLOCK Analog PLLs and DLLs

- Two GPLLs and up to six SPLLs per device
 - Clock multiply, divide, phase & delay adjust
 - Dynamic PLL adjustment
- Two general purpose DLLs per device

■ Pre-Engineered Source Synchronous I/O

- DDR registers in I/O cells
- Dedicated gearing logic
- Source synchronous standards support
 - SPI4.2, SFI4 (DDR Mode), XGMII
 - High Speed ADC/DAC devices
- Dedicated DDR and DDR2 memory support
 - DDR1: 400 (200MHz) / DDR2: 533 (266MHz)
- Dedicated DQS support

■ Programmable sysI/O™ Buffer Supports Wide Range Of Interfaces

- LVTTTL and LVCMOS 33/25/18/15/12
- SSTL 3/2/18 I, II
- HSTL15 I and HSTL18 I, II
- PCI and Differential HSTL, SSTL
- LVDS, RSDS, Bus-LVDS, MLVDS, LVPECL

■ Flexible Device Configuration

- 1149.1 Boundary Scan compliant
- Dedicated bank for configuration I/Os
- SPI boot flash interface
- Dual boot images supported
- TransFR™ I/O for simple field updates
- Soft Error Detect macro embedded

■ Optional Bitstream Encryption (LatticeECP2/M “S” Versions Only)

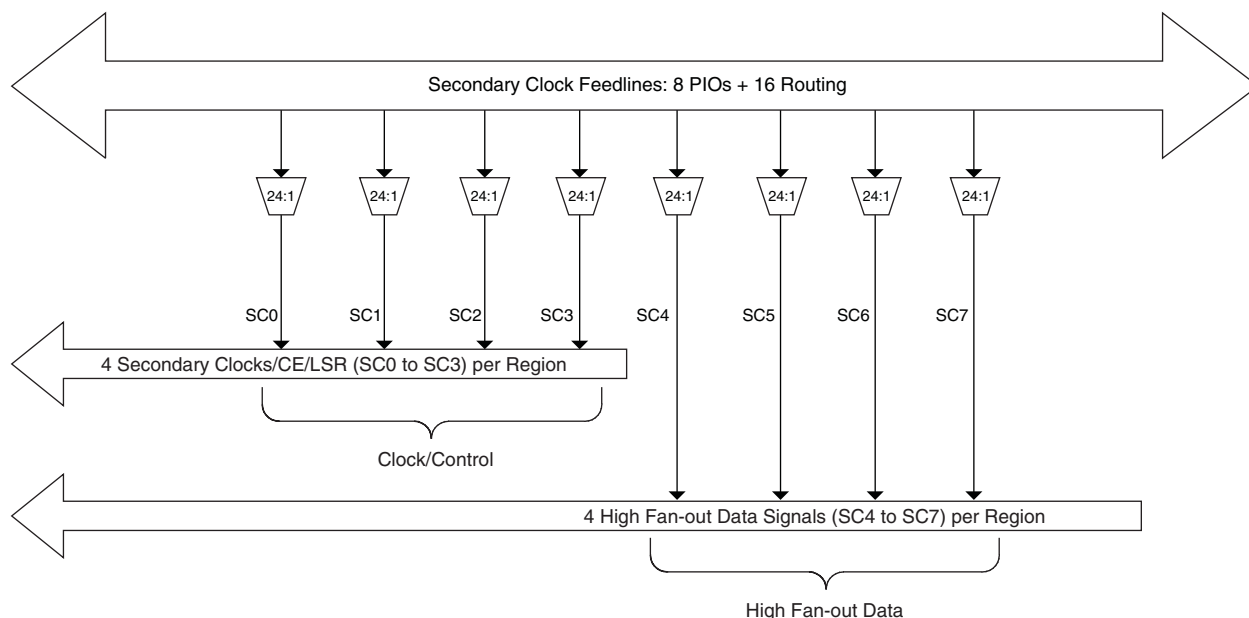
■ System Level Support

- ispTRACY™ internal logic analyzer capability
- On-chip oscillator for initialization & general use
- 1.2V power supply

Table 1-1. LatticeECP2 (Including “S-Series”) Family Selection

Device	ECP2-6	ECP2-12	ECP2-20	ECP2-35	ECP2-50	ECP2-70
LUTs (K)	6	12	21	32	48	68
Distributed RAM (Kbits)	12	24	42	64	96	136
EBR SRAM (Kbits)	55	221	276	332	387	1032
EBR SRAM Blocks	3	12	15	18	21	60
sysDSP Blocks	3	6	7	8	18	22
18x18 Multipliers	12	24	28	32	72	88
GPLL + SPLL + DLL	2+0+2	2+0+2	2+0+2	2+0+2	2+2+2	2+4+2
Maximum Available I/O	190	297	402	450	500	583
Packages and I/O Combinations						
144-pin TQFP (20 x 20 mm)	90	93				
208-pin PQFP (28 x 28 mm)		131	131			
256-ball fpBGA (17 x 17 mm)	190	193	193			
484-ball fpBGA (23 x 23 mm)		297	331	331	339	
672-ball fpBGA (27 x 27 mm)			402	450	500	500
900-ball fpBGA (31 x 31 mm)						583

Figure 2-16. Secondary Clock Selection



Slice Clock Selection

Figure 2-17 shows the clock selections and Figure 2-18 shows the control selections for Slice0 through Slice2. All the primary clocks and the four secondary clocks are routed to this clock selection mux. Other signals can be used as a clock input to the slices via routing. Slice controls are generated from the secondary clocks or other signals connected via routing.

If none of the signals are selected for both clock and control then the default value of the mux output is 1. Slice 3 does not have any registers; therefore it does not have the clock or control muxes.

Figure 2-17. Slice0 through Slice2 Clock Selection

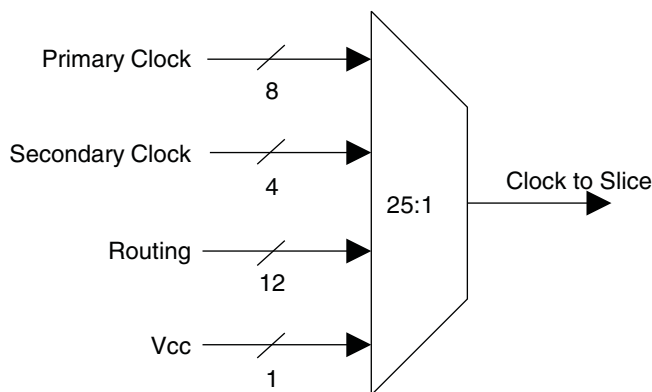


Table 3-13. Periodic Receiver Jitter Tolerance Specification¹

Description	Frequency	Condition	Min.	Typ.	Max.	Units
Periodic	3.125 Gbps	600 mV differential eye	—	—	0.20	UI, p-p
	2.5 Gbps	600 mV differential eye	—	—	0.22	UI, p-p
	1.25 Gbps	600 mV differential eye	—	—	0.20	UI, p-p
	250 Mbps ²	600 mV differential eye	—	—	0.08	UI, p-p

1. Values are measured with PRBS 2⁷-1, all channels operating.

2. Jitter specification is limited by measurement equipment capability.

LatticeECP2/M sysCONFIG Port Timing Specifications

Over Recommended Operating Conditions

Parameter	Description	Min.	Max.	Units
sysCONFIG Byte Data Flow				
t_{SUCBDI}	Byte D[0:7] Setup Time to CCLK	7	—	ns
$t_{HCB DI}$	Byte D[0:7] Hold Time to CCLK	1	—	ns
t_{CODO}	CCLK to DOUT in Flowthrough Mode	—	12	ns
t_{SUCS}	CSN[0:1] Setup Time to CCLK	7	—	ns
t_{HCS}	CSN[0:1] Hold Time to CCLK	1	—	ns
t_{SUWD}	Write Signal Setup Time to CCLK	7	—	ns
t_{HWD}	Write Signal Hold Time to CCLK	1	—	ns
t_{DCB}	CCLK to BUSY Delay Time	—	12	ns
t_{CORD}	CCLK to Out for Read Data	—	12	ns
sysCONFIG Byte Slave Clocking				
t_{BSCH}	Byte Slave CCLK Minimum High Pulse	6	—	ns
t_{BSCL}	Byte Slave CCLK Minimum Low Pulse	9	—	ns
t_{BSCYC}	Byte Slave CCLK Cycle Time	15	—	ns
sysCONFIG Serial (Bit) Data Flow				
t_{SUSCDI}	DI Setup Time to CCLK Slave Mode	7	—	ns
t_{HSCDI}	DI Hold Time to CCLK Slave Mode	1	—	ns
t_{CODO}	CCLK to DOUT in Flowthrough Mode	—	12	ns
sysCONFIG Serial Slave Clocking				
t_{SSCH}	Serial Slave CCLK Minimum High Pulse	6	—	ns
t_{SSCL}	Serial Slave CCLK Minimum Low Pulse	6	—	ns
sysCONFIG POR, Initialization and Wake-up				
t_{ICFG}	Minimum Vcc to INITN High	—	28	ms
t_{VMC}	Time from t_{ICFG} to Valid Master CCLK	—	2	us
t_{PRGMRJ}	PROGRAMN Pin Pulse Rejection	—	8	ns
t_{PRGM}	PROGRAMN Low Time to Start Configuration	25	—	ns
t_{DINIT}	PROGRAMN High to INITN High Delay ¹	—	1.5	ms
$t_{DPPINIT}$	Delay Time from PROGRAMN Low to INITN Low	—	37	ns
$t_{DPPDONE}$	Delay Time from PROGRAMN Low to DONE Low	—	37	ns
t_{IODISS}	User I/O Disable from PROGRAMN Low	—	35	ns
t_{IOENSS}	User I/O Enabled Time from CCLK Edge During Wake-up Sequence	—	25	ns
t_{MWC}	Additional Wake Master Clock Signals after DONE Pin High	120	—	cycles
sysCONFIG SPI Port²				
t_{CFGX}	INITN High to CCLK Low	—	1	μs
t_{CSSPI}	INITN High to CSSPIN Low	—	2	us
t_{CSCCLK}	CCLK Low before CSSPIN Low	0	—	ns
t_{SOCDO}	CCLK Low to Output Valid	—	15	ns
t_{SOE}	CSSPIN[0:1] Active Setup Time	300	—	ns
t_{CSPID}	CSSPIN[0:1] Low to First CCLK Edge Setup Time	300+3cyc	600+6cyc	ns

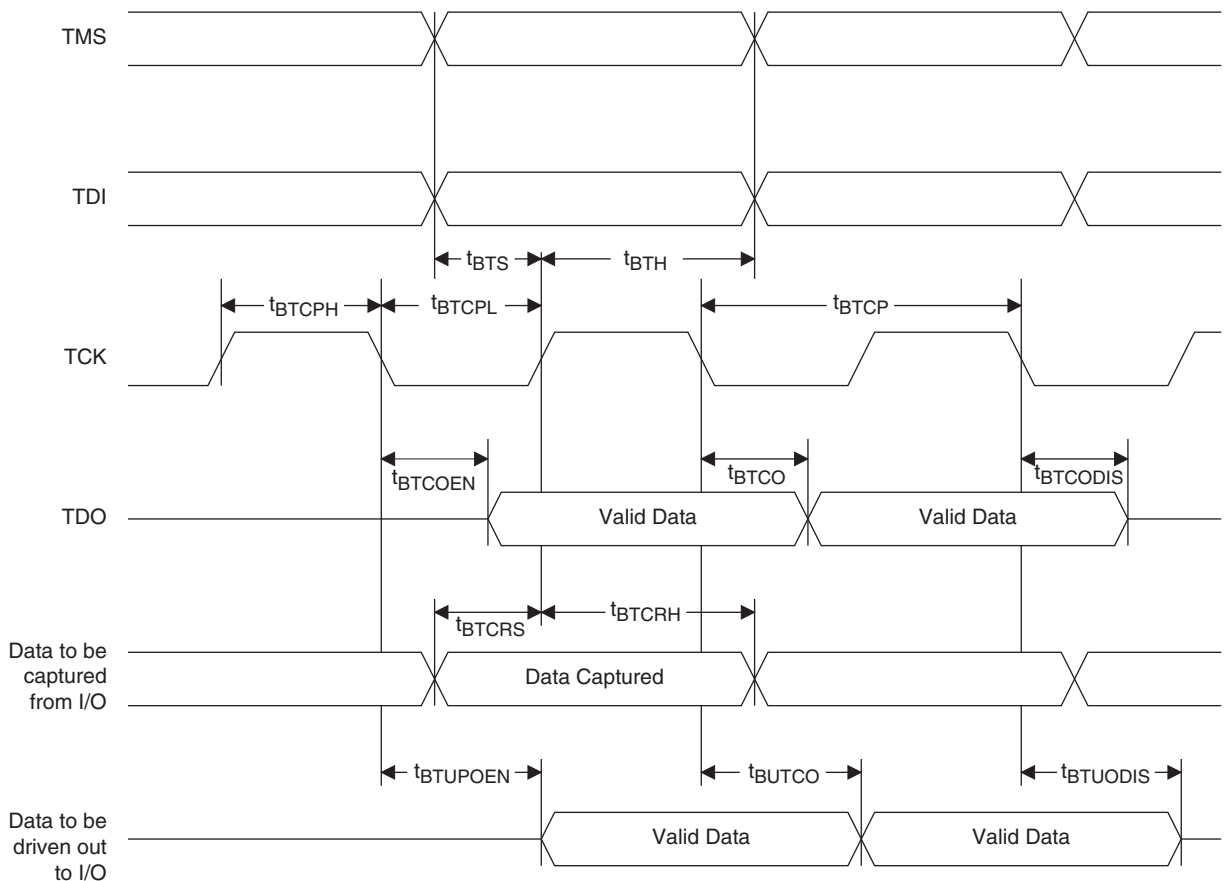
JTAG Port Timing Specifications

Over Recommended Operating Conditions

Symbol	Parameter	Min	Max	Units
f_{MAX}	TCK clock frequency	—	25	MHz
t_{BTCP}	TCK [BSCAN] clock pulse width	40	—	ns
t_{BTCPH}	TCK [BSCAN] clock pulse width high	20	—	ns
t_{BTCPL}	TCK [BSCAN] clock pulse width low	20	—	ns
t_{BTS}	TCK [BSCAN] setup time	8	—	ns
t_{BTH}	TCK [BSCAN] hold time	10	—	ns
t_{BTRF}	TCK [BSCAN] rise/fall time	50	—	mV/ns
t_{BTCO}	TAP controller falling edge of clock to valid output	—	10	ns
$t_{BTCODIS}$	TAP controller falling edge of clock to valid disable	—	10	ns
t_{BTCOEN}	TAP controller falling edge of clock to valid enable	—	10	ns
t_{BTCRS}	BSCAN test capture register setup time	8	—	ns
t_{BTCRH}	BSCAN test capture register hold time	25	—	ns
t_{BUTCO}	BSCAN test update register, falling edge of clock to valid output	—	25	ns
$t_{BTUODIS}$	BSCAN test update register, falling edge of clock to valid disable	—	25	ns
$t_{BTUPOEN}$	BSCAN test update register, falling edge of clock to valid enable	—	25	ns

Timing v.A 0.11

Figure 3-21. JTAG Port Timing Waveforms



Available Device Resources by Package, LatticeECP2

Resource	Device	256 fpBGA	484 fpBGA	672 fpBGA	900 fpBGA
PLL/DLL	ECP2-6	4	—	—	—
	ECP2-12	4	4	—	—
	ECP2-20	4	4	4	—
	ECP2-35	—	4	4	—
	ECP2-50	—	6	6	—
	ECP2-70	—	—	8	8

Available Device Resources by Package, LatticeECP2M

Resource	Device	256 fpBGA	484 fpBGA	672 fpBGA	900 fpBGA	1152 fpBGA
PLL/DLL	ECP2M20	10	10	—	—	—
	ECP2M35	10	10	10	—	—
	ECP2M50	—	10	10	10	—
	ECP2M70	—	—	—	10	10
	ECP2M100	—	—	—	10	10

LatticeECP2M Power Supply and NC (Cont.)

Signal	1152 fpBGA
V _{CC}	AA13, AA14, AA15, AA16, AA17, AA18, AA19, AA20, AA21, AA22, AB14, AB15, AB20, AB21, N14, N15, N20, N21, P13, P14, P15, P16, P17, P18, P19, P20, P21, P22, R13, R14, R21, R22, T14, T21, U14, U21, V14, V21, W14, W21, Y13, Y14, Y21, Y22
V _{CCIO0}	C12, C16, E14, H12, H16, M14, M15
V _{CCIO1}	C19, C23, E21, H19, H23, M20, M21
V _{CCIO2}	G32, K28, K32, N27, N32, P23, R23, T27, T32
V _{CCIO3}	AA23, AB27, AB32, AE28, AE32, AH32, W27, W32, Y23
V _{CCIO4}	AC20, AC21, AG19, AG23, AK21, AM19, AM23
V _{CCIO5}	AC14, AC15, AG12, AG16, AK14, AM12, AM16
V _{CCIO6}	AA12, AB3, AB8, AE3, AE7, AH3, W3, W8, Y12
V _{CCIO7}	G3, K3, K7, N3, N8, P12, R12, T3, T8
V _{CCIO8}	AD28, AG32
V _{CCJ}	AK3
V _{CCAUX}	AB12, AB13, AB22, AB23, AC13, AC22, M13, M22, N12, N13, N22, N23
V _{CCPLL}	R15, R20, Y15, Y20
SERDES Power ³	D7, B9, B8, D9, B7, E7, B6, D8, E6, D6, D4, B5, D3, B4, C1, B3, B1, B2, B33, B34, B32, C34, B31, D32, B30, D31, E29, D29, D27, B29, E28, B28, D26, B27, B26, D28, AL28, AN26, AN27, AL26, AN28, AK28, AN29, AL27, AL29, AK29, AL31, AN30, AL32, AN31, AM34, AN32, AN34, AN33, AN2, AN1, AN3, AM1, AN4, AL3, AN5, AL4, AL6, AK6, AL8, AN6, AK7, AN7, AL9, AN8, AN9, AL7
GND ¹	A1, A10, A13, A22, A25, A34, AB16, AB17, AB18, AB19, AB26, AB31, AB4, AB9, AC16, AC17, AC18, AC19, AD27, AE27, AE31, AE4, AE8, AF12, AF16, AF19, AF23, AG31, AH31, AH4, AJ14, AJ21, AK27, AK8, AL10, AL16, AL19, AL2, AL25, AL33, AP1, AP10, AP13, AP22, AP25, AP34, D10, D16, D19, D2, D25, D33, E27, E8, F14, F21, G31, G4, J12, J16, J19, J23, K27, K31, K4, K8, M16, M17, M18, M19, N16, N17, N18, N19, N26, N31, N4, N9, R16, R17, R18, R19, T12, T13, T15, T16, T17, T18, T19, T20, T22, T23, T26, T31, T4, T9, U12, U13, U15, U16, U17, U18, U19, U20, U22, U23, V12, V13, V15, V16, V17, V18, V19, V20, V22, V23, W12, W13, W15, W16, W17, W18, W19, W20, W22, W23, W26, W31, W4, W9, Y16, Y17, Y18, Y19
NC ²	LFE2M70: H2, H1, G5, G6, M9, M10, H3, H4, P3, P4, P9, M7, P1, P2, N7, P7, AC7, AC5, AC6, AD5, AD4, AD3, AD10, AD8, AD2, AD1, AD9, AC11, AD6, AD7, AE1, AE2, AJ12, AH12, AL13, AK13, AE14, AG13, AH22, AH21, AG22, AG21, AF33, AF34, AC27, AC28, AD29, AD30, AE33, AE34, AD32, AD31, AB25, AC25, AB28, AA26, AD33, AD34, P30, P29, P31, P32, R25, T24, N34, N33, F24, G23, J22, G22, H21, K21, L19, L20, L18, K19, J14, L15, H14, K14, F12, D11, F11, E11, A11, A12, A23, A24, AA11, AB11, AC26, AC30, AD11, AD12, AD13, AD14, AD15, AD19, AD21, AD22, AD23, AE10, AE11, AE12, AE13, AE19, AE21, AE22, AE23, AF11, AF21, AF22, AF24, AF8, AF9, AG10, AG11, AG24, AG25, AG26, AG3, AG7, AG8, AG9, AH10, AH11, AH13, AH24, AH25, AH26, AH27, AH5, AH6, AH7, AH8, AH9, AJ10, AJ11, AJ13, AJ24, AJ25, AJ26, AJ27, AJ3, AJ4, AJ5, AJ6, AJ7, AJ8, AJ9, AK10, AK11, AK12, AK24, AK25, AK26, AK4, AK9, AL11, AL12, AL34, AM10, AM11, AM13, AM25, AN10, AN11, AN12, AN13, AN24, AN25, AP11, AP12, AP24, B10, B11, B12, B13, B22, B23, B24, B25, C10, C11, C13, C22, C24, C25, D1, D15, D24, D34, E10, E24, E25, E26, E3, E31, E32, E33, E34, E4, E9, F10, F25, F26, F27, F28, F29, F30, F31, F32, F33, F34, F5, F6, F7, F8, F9, G10, G11, G24, G25, G26, G27, G28, G29, G30, G33, G34, G7, G8, G9, H10, H11, H24, H25, H26, H27, H28, H29, H8, H9, J10, J11, J24, J25, J26, J9, K10, K11, K12, K13, K23, K24, K25, K26, L11, L12, L13, L14, L21, L22, L23, L24, L25, L26, M11, M24, M25, M6, M8, N10, N11, P10, P25, P26, R9, T11, U11, W11, Y10, Y11 LFE2M100: A11, A12, A23, A24, AA11, AB11, AC26, AC30, AD11, AD12, AD13, AD14, AD15, AD19, AD21, AD22, AD23, AE10, AE11, AE12, AE13, AE19, AE21, AE22, AE23, AF11, AF21, AF22, AF24, AF8, AF9, AG10, AG11, AG24, AG25, AG26, AG3, AG7, AG8, AG9, AH10, AH11, AH13, AH24, AH25, AH26, AH27, AH5, AH6, AH7, AH8, AH9, AJ10, AJ11, AJ13, AJ24, AJ25, AJ26, AJ27, AJ3, AJ4, AJ5, AJ6, AJ7, AJ8, AJ9, AK10, AK11, AK12, AK24, AK25, AK26, AK4, AK9, AL11, AL12, AL34, AM10, AM11, AM13, AM25, AN10, AN11, AN12, AN13, AN24, AN25, AP11, AP12, AP24, B10, B11, B12, B13, B22, B23, B24, B25, C10, C11, C13, C22, C24, C25, D1, D15, D24, D34, E10, E24, E25, E26, E3, E31, E32, E33, E34, E4, E9, F10, F25, F26, F27, F28, F29, F30, F31, F32, F33, F34, F5, F6, F7, F8, F9, G10, G11, G24, G25, G26, G27, G28, G29, G30, G33, G34, G7, G8, G9, H10, H11, H24, H25, H26, H27, H28, H29, H8, H9, J10, J11, J24, J25, J26, J9, K10, K11, K12, K13, K23, K24, K25, K26, L11, L12, L13, L14, L21, L22, L23, L24, L25, L26, M11, M24, M25, M6, M8, N10, N11, P10, P25, P26, R9, T11, U11, W11, Y10, Y11

1. All grounds must be electrically connected at the board level. For fpBGA packages, the total number of GND balls is less than the actual number of GND logic connections from the die to the common package GND plane.
2. NC pins should not be connected to any active signals, VCC or GND.
3. For package migration across device densities, the designer must comprehend the package pin requirements for the SERDES blocks. Specifically, the SERDES power pins of the largest density device must be accounted to accommodate migration to other smaller devices using the same package. Please refer to TN1160, [LatticeECP2/M Density Migration](#) for more details.

LFE2-20E/SE Logic Signal Connections: 256 fpBGA (Cont.)

LFE2-20E/SE					
Ball Number	Ball Number	Ball/Pad Function	Bank	Dual Function	Differential
J13	J13	PR28B	3	RLM0_GDLLC_FB_A/RDQ25	C
J12	J12	PR28A	3	RLM0_GDLLT_FB_A/RDQ25	T
H12	H12	PR27B	3	RLM0_GDLLC_IN_A**/RDQ25	C (LVDS)*
GND	GND	GNDIO3	-		
H13	H13	PR27A	3	RLM0_GDLLT_IN_A**/RDQ25	T (LVDS)*
H15	H15	PR22B	3	VREF2_3/RDQ25	C
VCCIO	VCCIO	VCCIO3	3		
H16	H16	PR22A	3	VREF1_3/RDQ25	T
H11	H11	PR21B	3	PCLKC3_0/RDQ25	C (LVDS)*
J11	J11	PR21A	3	PCLKT3_0/RDQ25	T (LVDS)*
G16	G16	PR19B	2	PCLKC2_0/RDQ16	C
GND	GND	GNDIO2	-		
G15	G15	PR19A	2	PCLKT2_0/RDQ16	T
F15	F15	PR17B	2	RDQ16	C
G11	G11	PR18B	2	RDQ16	C (LVDS)*
F14	F14	PR17A	2	RDQ16	T
VCCIO	VCCIO	VCCIO2	2		
F12	F12	PR18A	2	RDQ16	T (LVDS)*
G14	G14	PR16B	2	RDQ16	C (LVDS)*
G13	G13	PR16A	2	RDQS16	T (LVDS)*
GND	GND	GNDIO2	-		
F16	F16	PR14B	2	RDQ16	C (LVDS)*
F9	F9	PR15B	2	RDQ16	C
E16	E16	PR14A	2	RDQ16	T (LVDS)*
F10	F10	PR15A	2	RDQ16	T
VCCIO	VCCIO	VCCIO2	2		
D16	D16	PR13B	2	RDQ16	C
D15	D15	PR13A	2	RDQ16	T
C15	C15	PR6B	2	RDQ8	C (LVDS)*
C16	C16	PR7B	2	RDQ8	C
GND	GND	GNDIO2	-		
D14	D14	PR6A	2	RDQ8	T (LVDS)*
B16	B16	PR7A	2	RDQ8	T
F13	F13	PR2B	2	VREF2_2	C (LVDS)*
VCCIO	VCCIO	VCCIO2	2		
E13	E13	PR2A	2	VREF1_2	T (LVDS)*
F11	F11	PT64B	1	VREF2_1	C
E11	E11	PT64A	1	VREF1_1	T
GND	GND	GNDIO1	-		
A15	A15	PT63B	1		C
E12	E12	PT62B	1		C
B15	B15	PT63A	1		T

LFE2-12E/SE and LFE2-20E/SE Logic Signal Connections: 484 fpBGA

LFE2-12E/12SE					LFE2-20E/20SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential	
E4	PL2A	7	VREF2_7	T (LVDS)*	PL2A	7	VREF2_7	T (LVDS)*	
E5	PL2B	7	VREF1_7	C (LVDS)*	PL2B	7	VREF1_7	C (LVDS)*	
-	-	-			GNDIO7	-			
E3	NC	-			PL4A	7	LDQ8	T (LVDS)*	
F4	PL3A	7		T	PL5A	7	LDQ8	T	
F3	NC	-			PL4B	7	LDQ8	C (LVDS)*	
F5	PL3B	7		C	PL5B	7	LDQ8	C	
VCCIO	VCCIO7	7			VCCIO7	7			
E2	PL4A	7		T (LVDS)*	PL6A	7	LDQ8	T (LVDS)*	
G6	PL5A	7		T	PL7A	7	LDQ8	T	
E1	PL4B	7		C (LVDS)*	PL6B	7	LDQ8	C (LVDS)*	
G7	PL5B	7		C	PL7B	7	LDQ8	C	
GNDIO	GNDIO7	-			GNDIO7	-			
F1	NC	-			PL9A	7	LDQ8	T	
H4	NC	-			PL8A	7	LDQS8	T (LVDS)*	
F2	NC	-			PL9B	7	LDQ8	C	
-	-	-			VCCIO7	7			
H5	NC	-			PL8B	7	LDQ8	C (LVDS)*	
G1	NC	-			PL11A	7	LDQ8	T	
G3	NC	-			PL10A	7	LDQ8	T (LVDS)*	
G2	NC	-			PL11B	7	LDQ8	C	
-	-	-			GNDIO	-			
G4	NC	-			PL10B	7	LDQ8	C (LVDS)*	
J4	PL7A	7	LDQ10	T	PL13A	7	LDQ16	T	
H1	PL6A	7	LDQ10		PL12A	7	LDQ16	T (LVDS)*	
J5	PL7B	7	LDQ10	C	PL13B	7	LDQ16	C	
L6	PL9A	7	LDQ10	T	PL15A	7	LDQ16	T	
VCCIO	VCCIO7	7			VCCIO7	7			
J2	PL8A	7	LDQ10	T (LVDS)*	PL14A	7	LDQ16	T (LVDS)*	
L5	PL9B	7	LDQ10	C	PL15B	7	LDQ16	C	
J1	PL8B	7	LDQ10	C (LVDS)*	PL14B	7	LDQ16	C (LVDS)*	
K3	PL10A	7	LDQS10	T (LVDS)*	PL16A	7	LDQS16	T (LVDS)*	
GNDIO	GNDIO7	-			GNDIO	-			
K4	PL10B	7	LDQ10	C (LVDS)*	PL16B	7	LDQ16	C (LVDS)*	
K2	PL11A	7	LDQ10	T	PL17A	7	LDQ16	T	
VCCIO	VCCIO7	7			VCCIO7	7			
K1	PL11B	7	LDQ10	C	PL17B	7	LDQ16	C	
L4	PL12A	7	LDQ10	T (LVDS)*	PL18A	7	LDQ16	T (LVDS)*	
GNDIO	GNDIO7	-			GNDIO	-			
L3	PL12B	7	LDQ10	C (LVDS)*	PL18B	7	LDQ16	C (LVDS)*	
L2	PL13A	7	PCLKT7_0/LDQ10	T	PL19A	7	PCLKT7_0/LDQ16	T	
L1	PL13B	7	PCLKC7_0/LDQ10	C	PL19B	7	PCLKC7_0/LDQ16	C	
M5	PL15A	6	PCLKT6_0	T (LVDS)*	PL21A	6	PCLKT6_0/LDQ25	T (LVDS)*	
VCCIO	VCCIO6	6			-	-			

LFE2-35E/SE and LFE2-50E/SE Logic Signal Connections: 484 fpBGA

LFE2-35E/SE					LFE2-50E/SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
E4	PL2A	7	VREF2_7/LDQ6	T (LVDS)*	PL2A	7	VREF2_7	T (LVDS)*
E5	PL2B	7	VREF1_7/LDQ6	C (LVDS)*	PL2B	7	VREF1_7	C (LVDS)*
VCCIO	VCCIO7	-			GNDIO7	-		
GNDIO	GNDIO7	-			VCCIO	7		
E3	PL10A	7	LDQ14	T (LVDS)*	PL12A	7	LDQ16	T (LVDS)*
F3	PL10B	7	LDQ14	C (LVDS)*	PL12B	7	LDQ16	C (LVDS)*
F4	PL11A	7	LDQ14	T	PL13A	7	LDQ16	T
F5	PL11B	7	LDQ14	C	PL13B	7	LDQ16	C
E2	PL12A	7	LDQ14	T (LVDS)*	PL14A	7	LDQ16	T (LVDS)*
VCCIO	VCCIO7	7			VCCIO	7		
E1	PL12B	7	LDQ14	C (LVDS)*	PL14B	7	LDQ16	C (LVDS)*
G6	PL13A	7	LDQ14	T	PL15A	7	LDQ16	T
G7	PL13B	7	LDQ14	C	PL15B	7	LDQ16	C
H4	PL14A	7	LDQS14	T (LVDS)*	PL16A	7	LDQS16	T (LVDS)*
GNDIO	GNDIO7	-			GNDIO7	-		
H5	PL14B	7	LDQ14	C (LVDS)*	PL16B	7	LDQ16	C (LVDS)*
F1	PL15A	7	LDQ14	T	PL17A	7	LDQ16	T
F2	PL15B	7	LDQ14	C	PL17B	7	LDQ16	C
VCCIO	VCCIO7	7			VCCIO	7		
G3	PL16A	7	LDQ14	T (LVDS)*	PL18A	7	LDQ16	T (LVDS)*
G4	PL16B	7	LDQ14	C (LVDS)*	PL18B	7	LDQ16	C (LVDS)*
G1	PL17A	7	LDQ14	T	PL19A	7	LDQ16	T
G2	PL17B	7	LDQ14	C	PL19B	7	LDQ16	C
GNDIO	GNDIO7	-			GNDIO7	-		
-	-	-			VCCIO	7		
H6	NC	-			PL25A	7	LUM0_SPLLT_IN_A/LDQ24	T
-	-	-			VCCIO	7		
J6	NC	-			PL25B	7	LUM0_SPLLC_IN_A/LDQ24	C
H3	NC	-			PL26A	7	LUM0_SPLLT_FB_A/LDQ24	T
H2	NC	-			PL26B	7	LUM0_SPLLC_FB_A/LDQ24	C
-	-	-			GNDIO7	-		
-	-	-			VCCIO	7		
H1	PL18A	7	LDQ22		PL37A	7	LDQ41	
J4	PL19A	7	LDQ22	T	PL38A	7	LDQ41	T
J5	PL19B	7	LDQ22	C	PL38B	7	LDQ41	C
VCCIO	VCCIO7	7			VCCIO	7		
J2	PL20A	7	LDQ22	T (LVDS)*	PL39A	7	LDQ41	T (LVDS)*
J1	PL20B	7	LDQ22	C (LVDS)*	PL39B	7	LDQ41	C (LVDS)*
L6	PL21A	7	LDQ22	T	PL40A	7	LDQ41	T
L5	PL21B	7	LDQ22	C	PL40B	7	LDQ41	C
GNDIO	GNDIO7	-			GNDIO7	-		
K3	PL22A	7	LDQS22	T (LVDS)*	PL41A	7	LDQS41	T (LVDS)*
K4	PL22B	7	LDQ22	C (LVDS)*	PL41B	7	LDQ41	C (LVDS)*
K2	PL23A	7	LDQ22	T	PL42A	7	LDQ41	T
VCCIO	VCCIO7	7			VCCIO	7		

LFE2-50E/SE and LFE2-70E/SE Logic Signal Connections: 672 fpBGA (Cont.)

LFE2-50E/SE					LFE2-70E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential	
U1	PL53A	6	LDQ50	T	PL66A	6	LDQ63	T	
V1	PL53B	6	LDQ50	C	PL66B	6	LDQ63	C	
GND	GNDIO6	-			GNDIO6	-			
P3	PL54A	6	LDQ58	T (LVDS)*	PL67A	6	LDQ71	T (LVDS)*	
R3	PL54B	6	LDQ58	C (LVDS)*	PL67B	6	LDQ71	C (LVDS)*	
R4	PL55A	6	LDQ58	T	PL68A	6	LDQ71	T	
U2	PL55B	6	LDQ58	C	PL68B	6	LDQ71	C	
VCCIO	VCCIO6	6			VCCIO6	6			
V2	PL56A	6	LDQ58	T (LVDS)*	PL69A	6	LDQ71	T (LVDS)*	
W2	PL56B	6	LDQ58	C (LVDS)*	PL69B	6	LDQ71	C (LVDS)*	
T6	PL57A	6	LDQ58	T	PL70A	6	LDQ71	T	
R5	PL57B	6	LDQ58	C	PL70B	6	LDQ71	C	
GND	GNDIO6	-			GNDIO6	-			
R6	PL58A	6	LDQS58	T (LVDS)*	PL71A	6	LDQS71	T (LVDS)*	
R7	PL58B	6	LDQ58	C (LVDS)*	PL71B	6	LDQ71	C (LVDS)*	
W1	PL59A	6	LDQ58	T	PL72A	6	LDQ71	T	
VCCIO	VCCIO6	6			VCCIO6	6			
Y2	PL59B	6	LDQ58	C	PL72B	6	LDQ71	C	
Y1	PL60A	6	LLM0_GDLLT_IN_A**/LDQ58	T (LVDS)*	PL73A	6	LLM0_GDLLT_IN_A**/LDQ71	T (LVDS)*	
AA2	PL60B	6	LLM0_GDLLC_IN_A**/LDQ58	C (LVDS)*	PL73B	6	LLM0_GDLLC_IN_A**/LDQ71	C (LVDS)*	
T5	PL61A	6	LLM0_GDLLT_FB_A/LDQ58	T	PL74A	6	LLM0_GDLLT_FB_A/LDQ71	T	
GND	GNDIO6	-			GNDIO6	-			
T7	PL61B	6	LLM0_GDLLC_FB_D/LDQ58	C	PL74B	6	LLM0_GDLLC_FB_D/LDQ71	C	
R8	VCCPLL	6			VCCPLL	-			
T8	LLM0_PLLCAP	6			LLM0_PLLCAP	6			
U3	PL63A	6	LLM0_GPLLT_IN_A**/LDQ67	T (LVDS)*	PL76A	6	LLM0_GPLLT_IN_A**/LDQ80	T (LVDS)*	
U4	PL63B	6	LLM0_GPLLC_IN_A**/LDQ67	C (LVDS)*	PL76B	6	LLM0_GPLLC_IN_A**/LDQ80	C (LVDS)*	
V3	PL64A	6	LLM0_GPLLT_FB_A/LDQ67	T	PL77A	6	LLM0_GPLLT_FB_A/LDQ80	T	
U5	PL64B	6	LLM0_GPLLC_FB_A/LDQ67	C	PL77B	6	LLM0_GPLLC_FB_A/LDQ80	C	
V4	PL65A	6	LDQ67	T (LVDS)*	PL78A	6	LDQ80	T (LVDS)*	
VCCIO	VCCIO6	6			VCCIO6	6			
V5	PL65B	6	LDQ67	C (LVDS)*	PL78B	6	LDQ80	C (LVDS)*	
Y3	PL66A	6	LDQ67	T	PL79A	6	LDQ80	T	
Y4	PL66B	6	LDQ67	C	PL79B	6	LDQ80	C	
W3	PL67A	6	LDQS67	T (LVDS)*	PL80A	6	LDQS80	T (LVDS)*	
GND	GNDIO6	-			GNDIO6	-			
W4	PL67B	6	LDQ67	C (LVDS)*	PL80B	6	LDQ80	C (LVDS)*	
AA1	PL68A	6	LDQ67	T	PL81A	6	LDQ80	T	
AB1	PL68B	6	LDQ67	C	PL81B	6	LDQ80	C	
VCCIO	VCCIO6	6			VCCIO6	6			
U8	PL69A	6	LDQ67	T (LVDS)*	PL82A	6	LDQ80	T (LVDS)*	
U7	PL69B	6	LDQ67	C (LVDS)*	PL82B	6	LDQ80	C (LVDS)*	
V8	PL70A	6	LDQ67	T	PL83A	6	LDQ80	T	
U6	PL70B	6	LDQ67	C	PL83B	6	LDQ80	C	
GND	GNDIO6	-			GNDIO6	-			
W6	PL71A	6	LDQ75	T (LVDS)*	PL84A	6	LDQ88	T (LVDS)*	

LFE2-50E/SE and LFE2-70E/SE Logic Signal Connections: 672 fpBGA (Cont.)

LFE2-50E/SE					LFE2-70E/SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
GND	GNDIO5	-			GNDIO5	-		
W10	PB20A	5	BDQ24	T	PB29A	5	BDQ33	T
Y10	PB20B	5	BDQ24	C	PB29B	5	BDQ33	C
W11	PB21A	5	BDQ24	T	PB30A	5	BDQ33	T
AA10	PB21B	5	BDQ24	C	PB30B	5	BDQ33	C
AC8	PB22A	5	BDQ24	T	PB31A	5	BDQ33	T
AD8	PB22B	5	BDQ24	C	PB31B	5	BDQ33	C
VCCIO	VCCIO5	5			VCCIO5	5		
AB8	PB23A	5	BDQ24	T	PB32A	5	BDQ33	T
AB10	PB23B	5	BDQ24	C	PB32B	5	BDQ33	C
GND	GNDIO5	-			GNDIO5	-		
AE6	PB24A	5	BDQS24	T	PB33A	5	BDQS33	T
AF6	PB24B	5	BDQ24	C	PB33B	5	BDQ33	C
AA11	PB25A	5	BDQ24	T	PB34A	5	BDQ33	T
AC9	PB25B	5	BDQ24	C	PB34B	5	BDQ33	C
AB9	PB26A	5	BDQ24	T	PB35A	5	BDQ33	T
AD9	PB26B	5	BDQ24	C	PB35B	5	BDQ33	C
VCCIO	VCCIO5	5			VCCIO5	5		
Y11	PB27A	5	BDQ24	T	PB36A	5	BDQ33	T
AB11	PB27B	5	BDQ24	C	PB36B	5	BDQ33	C
AE7	PB28A	5	BDQ24	T	PB37A	5	BDQ33	T
AF7	PB28B	5	BDQ24	C	PB37B	5	BDQ33	C
GND	GNDIO5	-			GNDIO5	-		
AC10	PB29A	5	BDQ33	T	PB38A	5	BDQ42	T
AD10	PB29B	5	BDQ33	C	PB38B	5	BDQ42	C
AA12	PB30A	5	BDQ33	T	PB39A	5	BDQ42	T
W12	PB30B	5	BDQ33	C	PB39B	5	BDQ42	C
AB12	PB31A	5	BDQ33	T	PB40A	5	BDQ42	T
VCCIO	VCCIO5	5			VCCIO5	5		
Y12	PB31B	5	BDQ33	C	PB40B	5	BDQ42	C
AD12	PB32A	5	BDQ33	T	PB41A	5	BDQ42	T
AC12	PB32B	5	BDQ33	C	PB41B	5	BDQ42	C
AC13	PB33A	5	BDQS33	T	PB42A	5	BDQS42	T
GND	GNDIO5	-			GNDIO5	-		
AA13	PB33B	5	BDQ33	C	PB42B	5	BDQ42	C
AD13	PB34A	5	BDQ33	T	PB43A	5	BDQ42	T
AC14	PB34B	5	BDQ33	C	PB43B	5	BDQ42	C
AE8	PB35A	5	BDQ33	T	PB44A	5	BDQ42	T
VCCIO	VCCIO5	5			VCCIO5	5		
AF8	PB35B	5	BDQ33	C	PB44B	5	BDQ42	C
AB15	PB36A	5	BDQ33	T	PB45A	5	BDQ42	T
Y13	PB36B	5	BDQ33	C	PB45B	5	BDQ42	C
AE9	PB37A	5	BDQ33	T	PB46A	5	BDQ42	T
GND	GNDIO5	-			GNDIO5	-		
AF9	PB37B	5	BDQ33	C	PB46B	5	BDQ42	C
W13	PB38A	5	BDQ42	T	PB47A	5	BDQ51	T

LFE2-50E/SE and LFE2-70E/SE Logic Signal Connections: 672 fpBGA (Cont.)

LFE2-50E/SE					LFE2-70E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential	
G24	PR14B	2	RDQ16	C (LVDS)*	PR27B	2	RDQ29	C (LVDS)*	
G23	PR14A	2	RDQ16	T (LVDS)*	PR27A	2	RDQ29	T (LVDS)*	
VCCIO	VCCIO2	2			VCCIO2	2			
K19	PR13B	2	RDQ16	C	PR26B	2	RDQ29	C	
J19	PR13A	2	RDQ16	T	PR26A	2	RDQ29	T	
D26	PR12B	2	RDQ16	C (LVDS)*	PR25B	2	RDQ29	C (LVDS)*	
C26	PR12A	2	RDQ16	T (LVDS)*	PR25A	2	RDQ29	T (LVDS)*	
F22	PR11B	2	RDQ8	C	PR24B	2	RDQ21	C	
E24	PR11A	2	RDQ8	T	PR24A	2	RDQ21	T	
GND	GNDIO2	-			GNDIO2	-			
D25	PR10B	2	RDQ8	C (LVDS)*	PR23B	2	RDQ21	C (LVDS)*	
C25	PR10A	2	RDQ8	T (LVDS)*	PR23A	2	RDQ21	T (LVDS)*	
D24	PR9B	2	RDQ8	C	PR22B	2	RDQ21	C	
B25	PR9A	2	RDQ8	T	PR22A	2	RDQ21	T	
VCCIO	VCCIO2	2			VCCIO2	2			
H21	PR8B	2	RDQ8	C (LVDS)*	PR21B	2	RDQ21	C (LVDS)*	
G22	PR8A	2	RDQS8	T (LVDS)*	PR21A	2	RDQS21	T (LVDS)*	
B24	PR7B	2	RDQ8	C	PR20B	2	RDQ21	C	
GND	GNDIO2	-			GNDIO2	-			
C24	PR7A	2	RDQ8	T	PR20A	2	RDQ21	T	
D23	PR6B	2	RDQ8	C (LVDS)*	PR19B	2	RDQ21	C (LVDS)*	
C23	PR6A	2	RDQ8	T (LVDS)*	PR19A	2	RDQ21	T (LVDS)*	
G21	PR5B	2	RDQ8	C	PR18B	2	RDQ21	C	
VCCIO	VCCIO2	2			VCCIO2	2			
H20	PR5A	2	RDQ8	T	PR18A	2	RDQ21	T	
GND	GNDIO2	-			GNDIO2	-			
E22	PR2B	2	VREF2_2	C (LVDS)*	PR2B	2	VREF2_2	C (LVDS)*	
F21	PR2A	2	VREF1_2	T (LVDS)*	PR2A	2	VREF1_2	T (LVDS)*	
E23	PT82B	1	VREF2_1	C	PT100B	1	VREF2_1	C	
GND	GNDIO1	-			GNDIO1	-			
D22	PT82A	1	VREF1_1	T	PT100A	1	VREF1_1	T	
G20	PT81B	1		C	PT99B	1		C	
J18	PT81A	1		T	PT99A	1		T	
F20	PT80B	1		C	PT98B	1		C	
VCCIO	VCCIO1	1			VCCIO1	1			
H19	PT80A	1		T	PT98A	1		T	
A24	PT79B	1		C	PT97B	1		C	
A23	PT79A	1		T	PT97A	1		T	
E21	PT78B	1		C	PT96B	1		C	
F19	PT78A	1		T	PT96A	1		T	
C22	PT77B	1		C	PT95B	1		C	
GND	GNDIO1	-			GNDIO1	-			
E20	PT77A	1		T	PT95A	1		T	
B22	PT76B	1		C	PT94B	1		C	
VCCIO	VCCIO1	1			VCCIO1	1			
B23	PT76A	1		T	PT94A	1		T	

LFE2M20E/SE and LFE2M35E/SE Logic Signal Connections: 484 fpBGA (Cont.)

LFE2M20E/SE					LFE2M35E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential	
E13	PT28B	1		C	PT46B	1		C	
D12	PT28A	1		T	PT46A	1		T	
GNDIO	GNDIO1	-			GNDIO1	-			
A9	PT27B	1		C	PT45B	1		C	
A8	PT27A	1		T	PT45A	1		T	
A7	PT26B	1		C	PT44B	1		C	
A6	PT26A	1		T	PT44A	1		T	
VCCIO	VCCIO1	1			VCCIO1	1			
E12	PT25B	1		C	PT43B	1		C	
F12	PT25A	1		T	PT43A	1		T	
A5	PT24B	1		C	PT42B	1		C	
A4	PT24A	1		T	PT42A	1		T	
GNDIO	GNDIO1	-			GNDIO1	-			
B7	PT23B	1		C	PT41B	1		C	
B8	PT23A	1		T	PT41A	1		T	
G11	PT22B	1		C	PT40B	1		C	
E11	PT22A	1		T	PT40A	1		T	
VCCIO	VCCIO1	1			VCCIO1	1			
D11	PT21B	1	VREF2_1	C	PT39B	1	VREF2_1	C	
D10	PT21A	1	VREF1_1	T	PT39A	1	VREF1_1	T	
F11	PT20A	1	PCLKT1_0	T	PT38A	1	PCLKT1_0	T	
G10	PT20B	1	PCLKC1_0	C	PT38B	1	PCLKC1_0	C	
G9	PT19B	0	PCLKC0_0	C	PT37B	0	PCLKC0_0	C	
GNDIO	GNDIO0	-			GNDIO0	-			
F9	PT19A	0	PCLKT0_0	T	PT37A	0	PCLKT0_0	T	
C9	PT18B	0	VREF2_0	C	PT36B	0	VREF2_0	C	
D9	PT18A	0	VREF1_0	T	PT36A	0	VREF1_0	T	
A2	PT17B	0		C	PT35B	0		C	
VCCIO	VCCIO0	0			VCCIO0	0			
A3	PT17A	0		T	PT35A	0		T	
B3	PT16B	0		C	PT34B	0		C	
C4	PT16A	0		T	PT34A	0		T	
E10	PT15B	0		C	PT33B	0		C	
F10	PT15A	0		T	PT33A	0		T	
C7	PT14B	0		C	PT32B	0		C	
GNDIO	GNDIO0	-			GNDIO0	-			
B6	PT14A	0		T	PT32A	0		T	
C6	PT13B	0		C	PT31B	0		C	
VCCIO	VCCIO0	0			VCCIO0	0			
C5	PT13A	0		T	PT31A	0		T	
C8	PT12B	0		C	PT30B	0		C	
D8	PT12A	0		T	PT30A	0		T	
E8	PT11B	0		C	PT29B	0		C	
E9	PT11A	0		T	PT29A	0		T	
-	-	-			GNDIO0	-			
-	-	-			VCCIO0	0			
F8	PT10B	0		C	PT10B	0		C	
G8	PT10A	0		T	PT10A	0		T	

LFE2M20E/SE and LFE2M35E/SE Logic Signal Connections: 484 fpBGA (Cont.)

LFE2M20E/SE					LFE2M35E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential	
G18	VCCIO2	2			VCCIO2	2			
J15	VCCIO2	2			VCCIO2	2			
K19	VCCIO2	2			VCCIO2	2			
N19	VCCIO3	3			VCCIO3	3			
P15	VCCIO3	3			VCCIO3	3			
T18	VCCIO3	3			VCCIO3	3			
V21	VCCIO3	3			VCCIO3	3			
AA18	VCCIO4	4			VCCIO4	4			
R14	VCCIO4	4			VCCIO4	4			
V16	VCCIO4	4			VCCIO4	4			
W13	VCCIO4	4			VCCIO4	4			
AA5	VCCIO5	5			VCCIO5	5			
R9	VCCIO5	5			VCCIO5	5			
V7	VCCIO5	5			VCCIO5	5			
W10	VCCIO5	5			VCCIO5	5			
N4	VCCIO6	6			VCCIO6	6			
P8	VCCIO6	6			VCCIO6	6			
T5	VCCIO6	6			VCCIO6	6			
V2	VCCIO6	6			VCCIO6	6			
E2	VCCIO7	7			VCCIO7	7			
G5	VCCIO7	7			VCCIO7	7			
J8	VCCIO7	7			VCCIO7	7			
K4	VCCIO7	7			VCCIO7	7			
AA22	VCCIO8	8			VCCIO8	8			
U19	VCCIO8	8			VCCIO8	8			
H11	VCCAUX	-			VCCAUX	-			
H12	VCCAUX	-			VCCAUX	-			
L15	VCCAUX	-			VCCAUX	-			
L8	VCCAUX	-			VCCAUX	-			
M15	VCCAUX	-			VCCAUX	-			
M8	VCCAUX	-			VCCAUX	-			
R11	VCCAUX	-			VCCAUX	-			
R12	VCCAUX	-			VCCAUX	-			
A1	GND	-			GND	-			
A10	GND	-			GND	-			
A16	GND	-			GND	-			
A22	GND	-			GND	-			
AA19	GND	-			GND	-			
AA4	GND	-			GND	-			
AB1	GND	-			GND	-			
AB22	GND	-			GND	-			
B13	GND	-			GND	-			
B19	GND	-			GND	-			
B4	GND	-			GND	-			
D16	GND	-			GND	-			
D2	GND	-			GND	-			
D21	GND	-			GND	-			
D7	GND	-			GND	-			

LFE2M50E/SE Logic Signal Connections: 484 fpBGA (Cont.)

LFE2M50E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential
C12	URC_SQ_VCCIB2	12		
B12	URC_SQ_HDINN2	12		C
C11	URC_SQ_VCCR2	12		
A15	URC_SQ_HDOUTP2	12		T
C15	URC_SQ_VCCOB2	12		
B15	URC_SQ_HDOUTN2	12		C
C14	URC_SQ_VCCTX2	12		
B14	URC_SQ_HDOUTN3	12		C
A13	URC_SQ_VCCOB3	12		
A14	URC_SQ_HDOUTP3	12		T
C13	URC_SQ_VCCTX3	12		
B11	URC_SQ_HDINN3	12		C
B10	URC_SQ_VCCIB3	12		
A11	URC_SQ_HDINP3	12		T
C10	URC_SQ_VCCR3	12		
GNDIO	GNDIO1	-		
VCCIO	VCCIO1	1		
E13	PT55B	1		C
D12	PT55A	1		T
GNDIO	GNDIO1	-		
A9	PT54B	1		C
A8	PT54A	1		T
A7	PT53B	1		C
A6	PT53A	1		T
VCCIO	VCCIO1	1		
E12	PT52B	1		C
F12	PT52A	1		T
A5	PT51B	1		C
A4	PT51A	1		T
GNDIO	GNDIO1	-		
B7	PT50B	1		C
B8	PT50A	1		T
G11	PT49B	1		C
E11	PT49A	1		T
VCCIO	VCCIO1	1		
D11	PT48B	1	VREF2_1	C
D10	PT48A	1	VREF1_1	T
G10	PT47B	1	PCLKC1_0	C
F11	PT47A	1	PCLKT1_0	T
G9	PT46B	0	PCLKC0_0	C
GNDIO	GNDIO0	-		
F9	PT46A	0	PCLKT0_0	T
C9	PT45B	0	VREF2_0	C

LFE2M50E/SE Logic Signal Connections: 484 fpBGA (Cont.)

LFE2M50E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential
L11	GND	-		
L12	GND	-		
L13	GND	-		
M10	GND	-		
M11	GND	-		
M12	GND	-		
M13	GND	-		
N10	GND	-		
N11	GND	-		
N12	GND	-		
N13	GND	-		
N15	GND	-		
N20	GND	-		
N3	GND	-		
N8	GND	-		
P14	GND	-		
P9	GND	-		
R10	GND	-		
R13	GND	-		
T19	GND	-		
T4	GND	-		
W16	GND	-		
W2	GND	-		
W21	GND	-		
W7	GND	-		
Y10	GND	-		
Y13	GND	-		
Y15	NC	-		
W15	NC	-		
AB20	NC	-		
AB21	NC	-		
AA21	NC	-		
AA20	NC	-		
AB19	NC	-		
AB18	NC	-		
Y22	NC	-		
Y21	NC	-		
Y17	NC	-		
Y18	NC	-		
Y16	NC	-		
W17	NC	-		
Y19	NC	-		
Y20	NC	-		

LFE2M100E/SE Logic Signal Connections: 900 fpBGA (Cont.)

LFE2M100E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential
A9	ULC_SQ_HDOUTP0	11		T
A10	ULC_SQ_VCCOB0	11		
B9	ULC_SQ_HDOUTN0	11		C
C9	ULC_SQ_VCCTX1	11		
B8	ULC_SQ_HDOUTN1	11		C
C8	ULC_SQ_VCCOB1	11		
A8	ULC_SQ_HDOUTP1	11		T
C12	ULC_SQ_VCCRX1	11		
B11	ULC_SQ_HDINN1	11		C
C11	ULC_SQ_VCCIB1	11		
A11	ULC_SQ_HDINP1	11		T
B7	ULC_SQ_VCCAUX33	11		
E7	ULC_SQ_REFCLKN	11		C
D7	ULC_SQ_REFCLKP	11		T
C7	ULC_SQ_VCCP	11		
A3	ULC_SQ_HDINP2	11		T
C3	ULC_SQ_VCCIB2	11		
B3	ULC_SQ_HDINN2	11		C
C2	ULC_SQ_VCCRX2	11		
A6	ULC_SQ_HDOUTP2	11		T
C6	ULC_SQ_VCCOB2	11		
B6	ULC_SQ_HDOUTN2	11		C
C5	ULC_SQ_VCCTX2	11		
B5	ULC_SQ_HDOUTN3	11		C
A4	ULC_SQ_VCCOB3	11		
A5	ULC_SQ_HDOUTP3	11		T
C4	ULC_SQ_VCCTX3	11		
B2	ULC_SQ_HDINN3	11		C
B1	ULC_SQ_VCCIB3	11		
A2	ULC_SQ_HDINP3	11		T
C1	ULC_SQ_VCCRX3	11		
L12	VCC	-		
L13	VCC	-		
L18	VCC	-		
L19	VCC	-		
M11	VCC	-		
M12	VCC	-		
M13	VCC	-		
M14	VCC	-		
M15	VCC	-		
M16	VCC	-		
M17	VCC	-		
M18	VCC	-		

Industrial

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2M20SE-5F484I	304	1.2V	-5	fpBGA	484	Ind	20
LFE2M20SE-6F484I	304	1.2V	-6	fpBGA	484	Ind	20
LFE2M20SE-5F256I	140	1.2V	-5	fpBGA	256	Ind	20
LFE2M20SE-6F256I	140	1.2V	-6	fpBGA	256	Ind	20

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2M35SE-5F672I	410	1.2V	-5	fpBGA	672	Ind	35
LFE2M35SE-6F672I	410	1.2V	-6	fpBGA	672	Ind	35
LFE2M35SE-5F484I	303	1.2V	-5	fpBGA	484	Ind	35
LFE2M35SE-6F484I	303	1.2V	-6	fpBGA	484	Ind	35
LFE2M35SE-5F256I	140	1.2V	-5	fpBGA	256	Ind	35
LFE2M35SE-6F256I	140	1.2V	-6	fpBGA	256	Ind	35

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2M50SE-5F900I	410	1.2V	-5	fpBGA	900	Ind	50
LFE2M50SE-6F900I	410	1.2V	-6	fpBGA	900	Ind	50
LFE2M50SE-5F672I	372	1.2V	-5	fpBGA	672	Ind	50
LFE2M50SE-6F672I	372	1.2V	-6	fpBGA	672	Ind	50
LFE2M50SE-5F484I	270	1.2V	-5	fpBGA	484	Ind	50
LFE2M50SE-6F484I	270	1.2V	-6	fpBGA	484	Ind	50

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2M70SE-5F1152I	436	1.2V	-5	fpBGA	1152	Ind	70
LFE2M70SE-6F1152I	436	1.2V	-6	fpBGA	1152	Ind	70
LFE2M70SE-5F900I	416	1.2V	-5	fpBGA	900	Ind	70
LFE2M70SE-6F900I	416	1.2V	-6	fpBGA	900	Ind	70

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2M100SE-5F1152I	520	1.2V	-5	fpBGA	1152	Ind	100
LFE2M100SE-6F1152I	520	1.2V	-6	fpBGA	1152	Ind	100
LFE2M100SE-5F900I	416	1.2V	-5	fpBGA	900	Ind	100
LFE2M100SE-6F900I	416	1.2V	-6	fpBGA	900	Ind	100