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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details

Product Status	Active
Number of LABs/CLBs	2375
Number of Logic Elements/Cells	19000
Total RAM Bits	1246208
Number of I/O	140
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (Tj)
Package / Case	256-BGA
Supplier Device Package	256-FPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfe2m20se-6fn256c

Architecture Overview

Each LatticeECP2/M device contains an array of logic blocks surrounded by Programmable I/O Cells (PIC). Interspersed between the rows of logic blocks are rows of sysMEM™ Embedded Block RAM (EBR) and rows of sys-DSP™ Digital Signal Processing blocks, as shown in Figure 2-1. In addition, the LatticeECP2M family contains SERDES Quads in one or more of the corners. Figure 2-2 shows the block diagram of ECP2M20 with one quad.

There are two kinds of logic blocks, the Programmable Functional Unit (PFU) and Programmable Functional Unit without RAM (PFF). The PFU contains the building blocks for logic, arithmetic, RAM and ROM functions. The PFF block contains building blocks for logic, arithmetic and ROM functions. Both PFU and PFF blocks are optimized for flexibility, allowing complex designs to be implemented quickly and efficiently. Logic Blocks are arranged in a two-dimensional array. Only one type of block is used per row.

The LatticeECP2/M devices contain one or more rows of sysMEM EBR blocks. sysMEM EBRs are large dedicated 18K fast memory blocks. Each sysMEM block can be configured in a variety of depths and widths of RAM or ROM. In addition, LatticeECP2/M devices contain up to two rows of DSP Blocks. Each DSP block has multipliers and adder/accumulators, which are the building blocks for complex signal processing capabilities.

The LatticeECP2M devices feature up to 16 embedded 3.125Gbps SERDES (Serializer / Deserializer) channels. Each SERDES channel contains independent 8b/10b encoding / decoding, polarity adjust and elastic buffer logic. Each group of four SERDES channels along with its Physical Coding Sub-layer (PCS) block, creates a quad. The functionality of the SERDES/PCS Quads can be controlled by memory cells set during device configuration or by registers that are addressable during device operation. The registers in every quad can be programmed by a soft IP interface, referred to as the SERDES Client Interface (SCI). These quads (up to four) are located at the corners of the devices.

Each PIC block encompasses two PIOs (PIO pairs) with their respective sysI/O buffers. The sysI/O buffers of the LatticeECP2/M devices are arranged in eight banks, allowing the implementation of a wide variety of I/O standards. In addition, a separate I/O bank is provided for the programming interfaces. PIO pairs on the left and right edges of the device can be configured as LVDS transmit/receive pairs. The PIC logic also includes pre-engineered support to aid in the implementation of high speed source synchronous standards such as SPI4.2, along with memory interfaces including DDR2.

The LatticeECP2/M registers in PFU and sysI/O can be configured to be SET or RESET. After power up and the device is configured, it enters into user mode with these registers SET/RESET according to the configuration setting, allowing the device entering to a known state for predictable system function.

Other blocks provided include PLLs, DLLs and configuration functions. The LatticeECP2/M architecture provides two General PLLs (GPLL) and up to six Standard PLLs (SPLL) per device. In addition, each LatticeECP2/M family member provides two DLLs per device. The GPLLs and DLLs blocks are located in pairs at the end of the bottom-most EBR row; the DLL block is located towards the edge of the device. The SPLL blocks are located at the end of the other EBR/DSP rows.

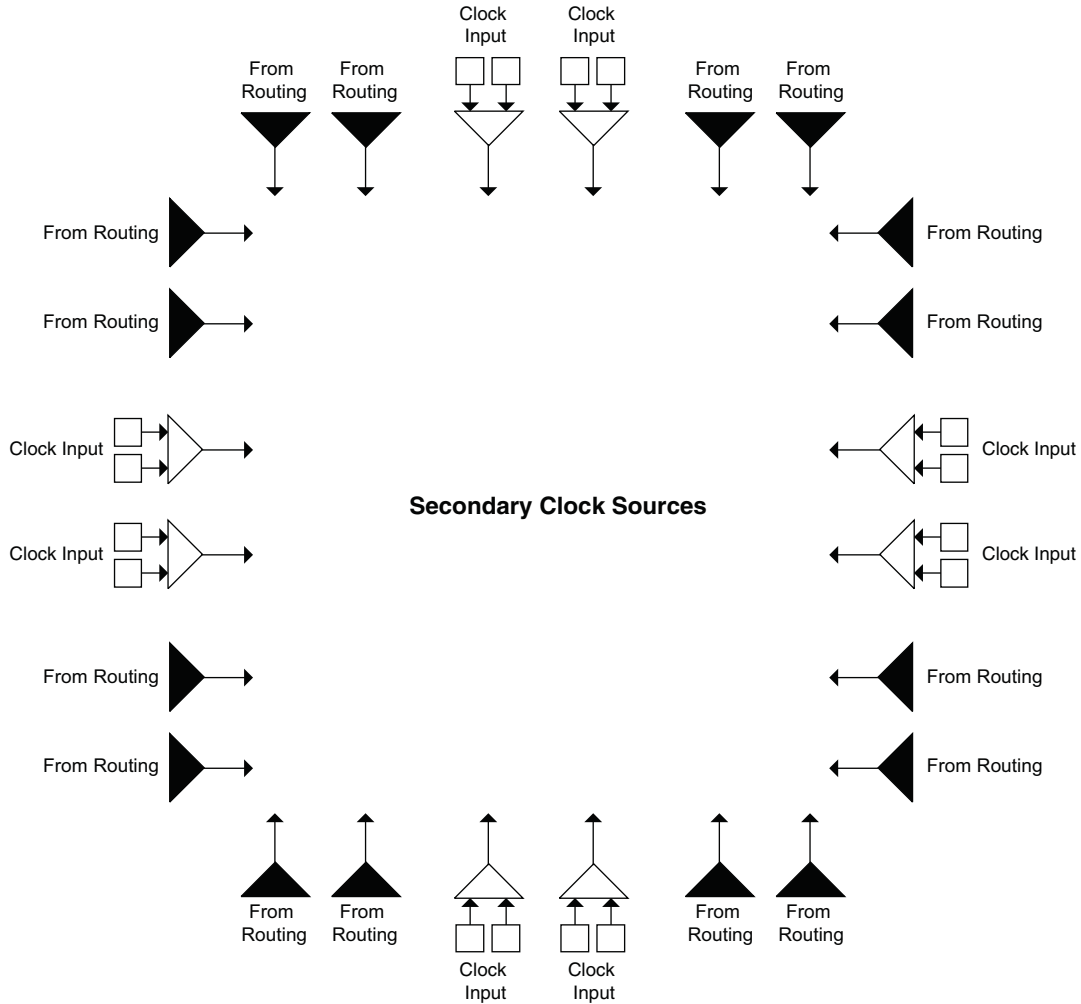
The configuration block that supports features such as configuration bit-stream decryption, transparent updates and dual boot support is located toward the center of this EBR row. The Ball Grid Array (BGA) package devices in the LatticeECP2/M family supports a sysCONFIG™ port located in the corner between banks four and five, which allows for serial or parallel device configuration.

In addition, every device in the family has a JTAG port. This family also provides an on-chip oscillator. The LatticeECP2/M devices use 1.2V as their core voltage.

Secondary Clock/Control Sources

LatticeECP2/M devices derive secondary clocks (SC0 through SC7) from eight dedicated clock input pads and the rest from routing. Figure 2-11 shows the secondary clock sources.

Figure 2-11. Secondary Clock Sources



this special vertical routing channel and the eight secondary clock regions for the ECP2-50. LatticeECP2 devices have four secondary clocks (SC0 to SC3) which are distributed to every region.

The secondary clock muxes are located in the center of the device. Figure 2-16 shows the mux structure of the secondary clock routing. Secondary clocks SC0 to SC3 are used for clock and control and SC4 to SC7 are used for high fan-out signals.

Figure 2-15. Secondary Clock Regions ECP2-50

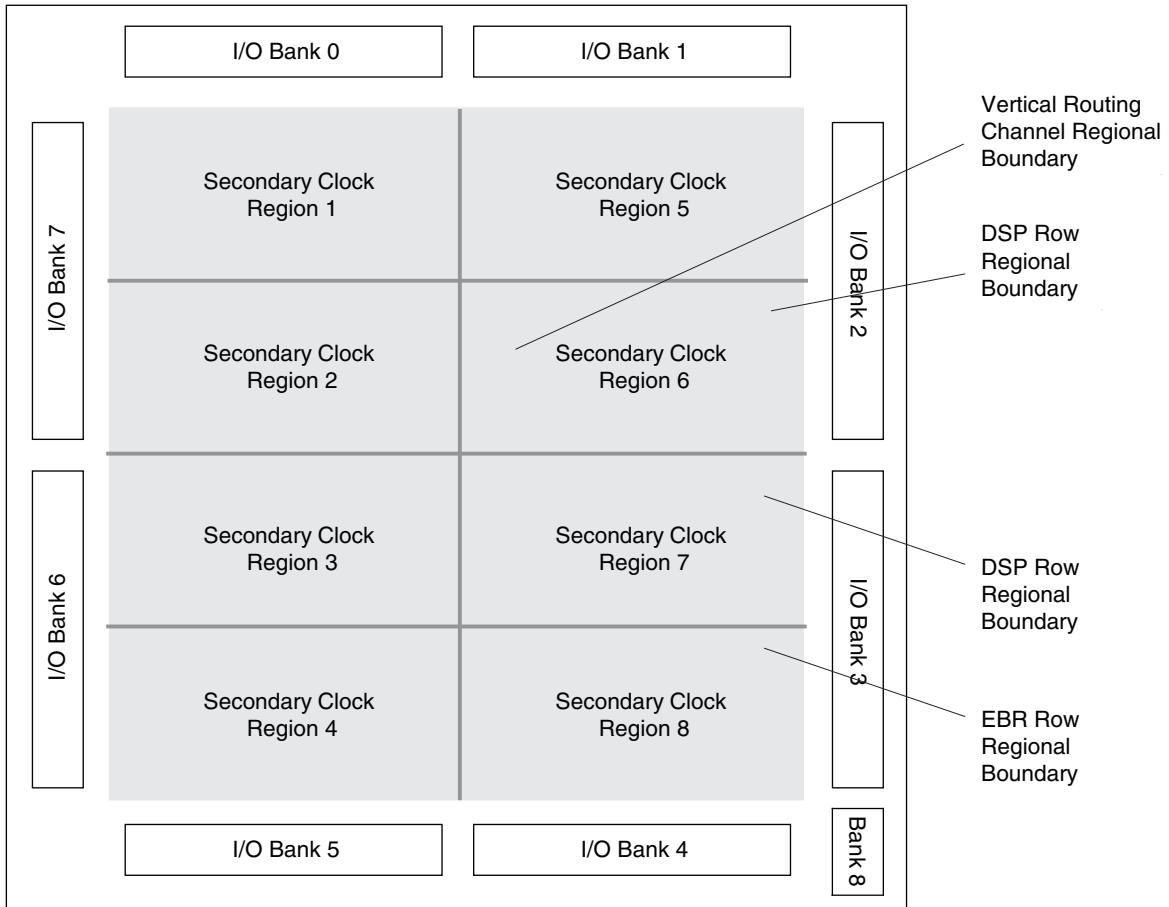
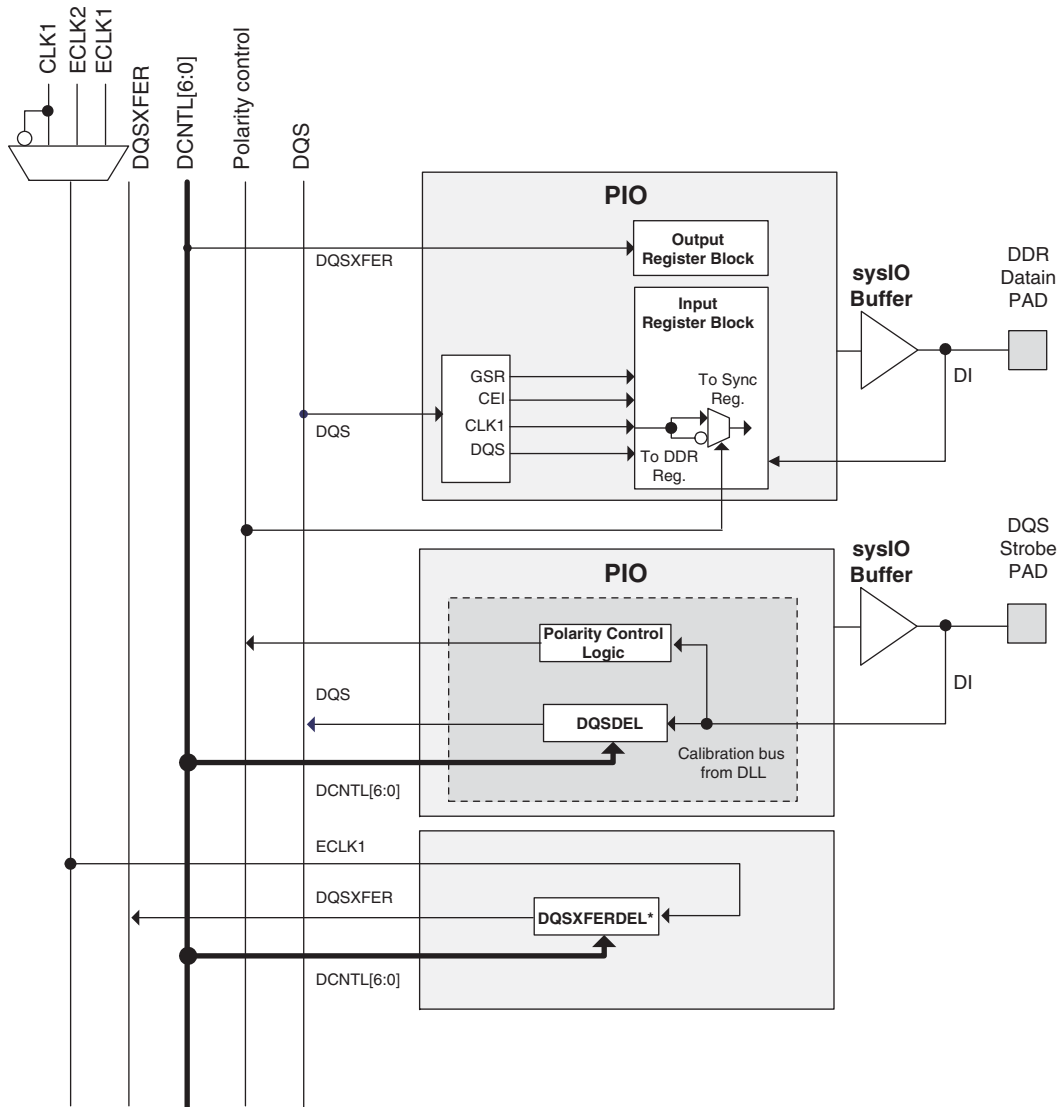


Figure 2-36. DQS Local Bus



*DQSXFERDEL shifts ECLK1 by 90% and is not associated with a particular PIO.

Polarity Control Logic

In a typical DDR Memory interface design, the phase relationship between the incoming delayed DQS strobe and the internal system clock (during the READ cycle) is unknown.

The LatticeECP2/M family contains dedicated circuits to transfer data between these domains. To prevent set-up and hold violations, at the domain transfer between DQS (delayed) and the system clock, a clock polarity selector is used. This changes the edge on which the data is registered in the synchronizing registers in the input register block. This requires evaluation at the start of each READ cycle for the correct clock polarity.

Prior to the READ operation in DDR memories, DQS is in tristate (pulled by termination). The DDR memory device drives DQS low at the start of the preamble state. A dedicated circuit detects the first DQS rising edge after the preamble state. This signal is used to control the polarity of the clock to the synchronizing registers.

LatticeECP2/M External Switching Characteristics⁹

Over Recommended Operating Conditions

Parameter	Description	Device	-7		-6		-5		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
General I/O Pin Parameters (using Primary Clock without PLL)¹									
t _{CO}	Clock to Output - PIO Output Register	LFE2-6	—	3.50	—	3.90	—	4.20	ns
		LFE2-12	—	3.50	—	3.90	—	4.20	ns
		LFE2-20	—	3.50	—	3.90	—	4.20	ns
		LFE2-35	—	3.50	—	3.90	—	4.20	ns
		LFE2-50	—	3.50	—	3.90	—	4.20	ns
		LFE2-70	—	3.70	—	4.10	—	4.40	ns
		LFE2M20	—	3.90	—	4.30	—	4.70	ns
		LFE2M35	—	3.90	—	4.30	—	4.70	ns
		LFE2M50	—	4.50	—	5.00	—	5.40	ns
		LFE2M70	—	4.50	—	5.00	—	5.40	ns
		LFE2M100	—	4.50	—	5.00	—	5.40	ns
t _{SU}	Clock to Data Setup - PIO Input Register	LFE2-6	0.00	—	0.00	—	0.00	—	ns
		LFE2-12	0.00	—	0.00	—	0.00	—	ns
		LFE2-20	0.00	—	0.00	—	0.00	—	ns
		LFE2-35	0.00	—	0.00	—	0.00	—	ns
		LFE2-50	0.00	—	0.00	—	0.00	—	ns
		LFE2-70	0.00	—	0.00	—	0.00	—	ns
		LFE2M20	0.00	—	0.00	—	0.00	—	ns
		LFE2M35	0.00	—	0.00	—	0.00	—	ns
		LFE2M50	0.00	—	0.00	—	0.00	—	ns
		LFE2M70	0.00	—	0.00	—	0.00	—	ns
		LFE2M100	0.00	—	0.00	—	0.00	—	ns
t _H	Clock to Data Hold - PIO Input Register	LFE2-6	1.40	—	1.70	—	1.90	—	ns
		LFE2-12	1.40	—	1.70	—	1.90	—	ns
		LFE2-20	1.40	—	1.70	—	1.90	—	ns
		LFE2-35	1.40	—	1.70	—	1.90	—	ns
		LFE2-50	1.40	—	1.70	—	1.90	—	ns
		LFE2-70	1.40	—	1.70	—	1.90	—	ns
		LFE2M20	1.40	—	1.70	—	1.90	—	ns
		LFE2M35	1.40	—	1.70	—	1.90	—	ns
		LFE2M50	1.80	—	2.10	—	2.30	—	ns
		LFE2M70	1.80	—	2.10	—	2.30	—	ns
		LFE2M100	1.80	—	2.10	—	2.30	—	ns

LatticeECP2 Pin Information Summary, LFE2-6 and LFE2-12 (Cont.)

Pin Type		LFE2-6		LFE2-12			
		144 TQFP	256 fpBGA	144 TQFP	208 PQFP	256 fpBGA	484 fpBGA
Available DDR-Interfaces per I/O Bank ¹	Bank0	0	0	0	0	0	0
	Bank1	0	0	0	0	0	0
	Bank2	0	1	0	0	1	1
	Bank3	0	0	0	0	0	0
	Bank4	0	2	0	0	2	3
	Bank5	0	1	0	0	1	3
	Bank6	0	1	0	0	1	1
	Bank7	0	1	0	0	1	1
	Bank8	0	0	0	0	0	0
PCI Capable I/Os per Bank	Bank0	0	0	0	0	0	0
	Bank1	0	0	0	0	0	0
	Bank2	0	0	0	0	0	0
	Bank3	0	0	0	0	0	0
	Bank4	18	32	18	19	32	46
	Bank5	8	14	10	18	17	46
	Bank6	0	0	0	0	0	0
	Bank7	0	0	0	0	0	0
	Bank8	0	0	0	0	0	0

1. Minimum requirement to implement a fully functional 8-bit wide DDR bus. Available DDR interface consists of at least 12 I/Os (1 DQS + 1 DQSB + 8 DQs + 1 DM + Bank VREF1).

LFE2-6E/SE and LFE2-12E/SE Logic Signal Connections: 256 fpBGA

LFE2-6E/SE					LFE2-12E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential	
C3	PL2A	7	VREF2_7	T (LVDS)*	PL2A	7	VREF2_7	T (LVDS)*	
C2	PL2B	7	VREF1_7	C (LVDS)*	PL2B	7	VREF1_7	C (LVDS)*	
VCCIO	VCCIO7	7			VCCIO7	7			
-	-	-			-	-			
D3	PL5A	7		T	PL5A	7		T	
D4	PL4A	7		T (LVDS)*	PL4A	7		T (LVDS)*	
D2	PL5B	7		C	PL5B	7		C	
GND	GNDIO7	-			GNDIO7	-			
E4	PL4B	7		C (LVDS)*	PL4B	7		C (LVDS)*	
B1	PL7A	7	LDQ10	T	PL7A	7	LDQ10	T	
C1	PL7B	7	LDQ10	C	PL7B	7	LDQ10	C	
F5	PL9A	7	LDQ10	T	PL9A	7	LDQ10	T	
VCCIO	VCCIO7	7			VCCIO7	7			
F4	PL8A	7	LDQ10	T (LVDS)*	PL8A	7	LDQ10	T (LVDS)*	
G6	PL9B	7	LDQ10	C	PL9B	7	LDQ10	C	
G4	PL8B	7	LDQ10	C (LVDS)*	PL8B	7	LDQ10	C (LVDS)*	
D1	PL10A	7	LDQS10	T (LVDS)*	PL10A	7	LDQS10	T (LVDS)*	
GND	GNDIO7	-			GNDIO7	-			
E1	PL10B	7	LDQ10	C (LVDS)*	PL10B	7	LDQ10	C (LVDS)*	
F3	PL11A	7	LDQ10	T	PL11A	7	LDQ10	T	
G3	PL11B	7	LDQ10	C	PL11B	7	LDQ10	C	
VCCIO	VCCIO7	7			VCCIO7	7			
F2	PL12A	7	LDQ10	T (LVDS)*	PL12A	7	LDQ10	T (LVDS)*	
F1	PL12B	7	LDQ10	C (LVDS)*	PL12B	7	LDQ10	C (LVDS)*	
GND	GNDIO7	-			GNDIO7	-			
G2	PL13A	7	PCLKT7_0/LDQ10	T	PL13A	7	PCLKT7_0/LDQ10	T	
G1	PL13B	7	PCLKC7_0/LDQ10	C	PL13B	7	PCLKC7_0/LDQ10	C	
H6	PL15A	6	PCLKT6_0	T (LVDS)*	PL15A	6	PCLKT6_0	T (LVDS)*	
VCCIO	VCCIO6	6			VCCIO6	6			
H5	PL15B	6	PCLKC6_0	C (LVDS)*	PL15B	6	PCLKC6_0	C (LVDS)*	
H4	PL16A	6	VREF2_6	T	PL16A	6	VREF2_6	T	
GND	GNDIO6	-			GNDIO6	-			
H3	PL16B	6	VREF1_6	C	PL16B	6	VREF1_6	C	
H2	PL17A	6	LLM0_GDLLT_IN_A**	T (LVDS)*	PL17A	6	LLM0_GDLLT_IN_A**	T (LVDS)*	
H1	PL17B	6	LLM0_GDLLC_IN_A**	C (LVDS)*	PL17B	6	LLM0_GDLLC_IN_A**	C (LVDS)*	
G10	VCC	-			VCC	-			
J4	PL18A	6	LLM0_GDLLT_FB_A	T	PL18A	6	LLM0_GDLLT_FB_A	T	
J5	PL18B	6	LLM0_GDLLC_FB_A	C	PL18B	6	LLM0_GDLLC_FB_A	C	
J6	LLM0_PLLCAP	6			LLM0_PLLCAP	6			
K4	PL20A	6	LLM0_GPLLT_IN_A**	T (LVDS)*	PL20A	6	LLM0_GPLLT_IN_A**	T (LVDS)*	
GND	GNDIO6	-			GNDIO6	-			
J1	PL21A	6	LLM0_GPLLT_FB_A	T	PL21A	6	LLM0_GPLLT_FB_A	T	
K3	PL20B	6	LLM0_GPLLC_IN_A**	C (LVDS)*	PL20B	6	LLM0_GPLLC_IN_A**	C (LVDS)*	
VCCIO	VCCIO6	6			VCCIO6	6			
J2	PL21B	6	LLM0_GPLLC_FB_A	C	PL21B	6	LLM0_GPLLC_FB_A	C	

LFE2-20E/SE and LFE2-35E/SE Logic Signal Connections: 672 fpBGA
(Cont.)

LFE2-20E/20SE					LFE2-35E/35SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
G24	PR6B	2	RDQ8	C (LVDS)*	PR12B	2	RDQ14	C (LVDS)*
G23	PR6A	2	RDQ8	T (LVDS)*	PR12A	2	RDQ14	T (LVDS)*
VCCIO	VCCIO2	2			VCCIO2	2		
K19	PR5B	2	RDQ8	C	PR11B	2	RDQ14	C
J19	PR5A	2	RDQ8	T	PR11A	2	RDQ14	T
D26	PR4B	2	RDQ8	C (LVDS)*	PR10B	2	RDQ14	C (LVDS)*
C26	PR4A	2	RDQ8	T (LVDS)*	PR10A	2	RDQ14	T (LVDS)*
F22	NC	-			PR9B	2	RDQ6	C
E24	NC	-			PR9A	2	RDQ6	T
GND	GNDIO2	-			GNDIO2	-		
D25	NC	-			PR8B	2	RDQ6	C (LVDS)*
C25	NC	-			PR8A	2	RDQ6	T (LVDS)*
D24	NC	-			PR7B	2	RDQ6	C
B25	NC	-			PR7A	2	RDQ6	T
VCCIO	VCCIO2	2			VCCIO2	2		
H21	NC	-			PR6B	2	RDQ6	C (LVDS)*
G22	NC	-			PR6A	2	RDQS6	T (LVDS)*
B24	NC	-			PR5B	2	RDQ6	C
GND	GNDIO2	-			GNDIO2	-		
C24	NC	-			PR5A	2	RDQ6	T
D23	NC	-			PR4B	2	RDQ6	C (LVDS)*
C23	NC	-			PR4A	2	RDQ6	T (LVDS)*
G21	PR3B	2		C	PR3B	2	RDQ6	C
VCCIO	VCCIO2	2			VCCIO2	2		
H20	PR3A	2		T	PR3A	2	RDQ6	T
GND	GNDIO2	-			GNDIO2	-		
E22	PR2B	2	VREF2_2	C (LVDS)*	PR2B	2	VREF2_2/RDQ6	C (LVDS)*
F21	PR2A	2	VREF1_2	T (LVDS)*	PR2A	2	VREF1_2/RDQ6	T (LVDS)*
E23	PT64B	1	VREF2_1	C	PT73B	1	VREF2_1	C
GND	GNDIO1	-			GNDIO1	-		
D22	PT64A	1	VREF1_1	T	PT73A	1	VREF1_1	T
G20	PT63B	1		C	PT72B	1		C
J18	PT63A	1		T	PT72A	1		T
F20	PT62B	1		C	PT71B	1		C
VCCIO	VCCIO1	1			VCCIO1	1		
H19	PT62A	1		T	PT71A	1		T
A24	PT61B	1		C	PT70B	1		C
A23	PT61A	1		T	PT70A	1		T
E21	PT60B	1		C	PT69B	1		C
F19	PT60A	1		T	PT69A	1		T
C22	PT59B	1		C	PT68B	1		C
GND	GNDIO1	-			GNDIO1	-		
E20	PT59A	1		T	PT68A	1		T
B22	PT58B	1		C	PT67B	1		C
VCCIO	VCCIO1	1			VCCIO1	1		
B23	PT58A	1		T	PT67A	1		T

**LFE2-50E/SE and LFE2-70E/SE Logic Signal Connections: 672 fpBGA
 (Cont.)**

LFE2-50E/SE					LFE2-70E/SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
AA14	PB38B	5	BDQ42	C	PB47B	5	BDQ51	C
AE10	PB39A	5	BDQ42	T	PB48A	5	BDQ51	T
AF10	PB39B	5	BDQ42	C	PB48B	5	BDQ51	C
W14	PB40A	5	BDQ42	T	PB49A	5	BDQ51	T
AB13	PB40B	5	BDQ42	C	PB49B	5	BDQ51	C
VCCIO	VCCIO5	5			VCCIO5	5		
Y14	PB41A	5	BDQ42	T	PB50A	5	BDQ51	T
AB14	PB41B	5	BDQ42	C	PB50B	5	BDQ51	C
GND	GNDIO5	-			GNDIO5	-		
AE11	PB42A	5	BDQS42	T	PB51A	5	BDQS51	T
AF11	PB42B	5	BDQ42	C	PB51B	5	BDQ51	C
AD14	PB43A	5	BDQ42	T	PB52A	5	BDQ51	T
AA15	PB43B	5	BDQ42	C	PB52B	5	BDQ51	C
AE12	PB44A	5	PCLKT5_0/BDQ42	T	PB53A	5	PCLKT5_0/BDQ51	T
AF12	PB44B	5	PCLKC5_0/BDQ42	C	PB53B	5	PCLKC5_0/BDQ51	C
VCCIO	VCCIO5	5			VCCIO5	5		
GND	GNDIO5	-			GNDIO5	-		
AD15	PB49A	4	PCLKT4_0/BDQ51	T	PB58A	4	PCLKT4_0/BDQ60	T
VCCIO	VCCIO4	4			VCCIO4	4		
AC15	PB49B	4	PCLKC4_0/BDQ51	C	PB58B	4	PCLKC4_0/BDQ60	C
AE13	PB50A	4	BDQ51	T	PB59A	4	BDQ60	T
AF13	PB50B	4	BDQ51	C	PB59B	4	BDQ60	C
AB17	PB51A	4	BDQS51	T	PB60A	4	BDQS60	T
GND	GNDIO4	-			GNDIO4	-		
Y15	PB51B	4	BDQ51	C	PB60B	4	BDQ60	C
AE14	PB52A	4	BDQ51	T	PB61A	4	BDQ60	T
AF14	PB52B	4	BDQ51	C	PB61B	4	BDQ60	C
AA16	PB53A	4	BDQ51	T	PB62A	4	BDQ60	T
VCCIO	VCCIO4	4			VCCIO4	4		
W15	PB53B	4	BDQ51	C	PB62B	4	BDQ60	C
AC17	PB54A	4	BDQ51	T	PB63A	4	BDQ60	T
AB16	PB54B	4	BDQ51	C	PB63B	4	BDQ60	C
AE15	PB55A	4	BDQ51	T	PB64A	4	BDQ60	T
GND	GNDIO4	-			GNDIO4	-		
AF15	PB55B	4	BDQ51	C	PB64B	4	BDQ60	C
AE16	PB56A	4	BDQ60	T	PB65A	4	BDQ69	T
AF16	PB56B	4	BDQ60	C	PB65B	4	BDQ69	C
Y16	PB57A	4	BDQ60	T	PB66A	4	BDQ69	T
AB18	PB57B	4	BDQ60	C	PB66B	4	BDQ69	C
AD17	PB58A	4	BDQ60	T	PB67A	4	BDQ69	T
AD18	PB58B	4	BDQ60	C	PB67B	4	BDQ69	C
VCCIO	VCCIO4	4			VCCIO4	4		
AC18	PB59A	4	BDQ60	T	PB68A	4	BDQ69	T
AD19	PB59B	4	BDQ60	C	PB68B	4	BDQ69	C
GND	GNDIO4	-			GNDIO4	-		
AC19	PB60A	4	BDQS60	T	PB69A	4	BDQS69	T

LFE2-50E/SE and LFE2-70E/SE Logic Signal Connections: 672 fpBGA
(Cont.)

LFE2-50E/SE					LFE2-70E/SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
U24	PR63B	3	RLM0_GPLL_C_IN_A**/RDQ67	C (LVDS)*	PR76B	3	RLM0_GPLL_C_IN_A**/RDQ80	C (LVDS)*
U25	PR63A	3	RLM0_GPLL_T_IN_A**/RDQ67	T (LVDS)*	PR76A	3	RLM0_GPLL_T_IN_A**/RDQ80	T (LVDS)*
R20	RLM0_PLLCAP	3			RLM0_PLLCAP	3		
P18	VCCPLL	3			VCCPLL	-		
T19	PR61B	3	RLM0_GDLLC_FB_A/RDQ58	C	PR74B	3	RLM0_GDLLC_FB_A/RDQ71	C
U20	PR61A	3	RLM0_GDLLT_FB_A/RDQ58	T	PR74A	3	RLM0_GDLLT_FB_A/RDQ71	T
GND	GNDIO3	-			GNDIO3	-		
T25	PR60B	3	RLM0_GDLLC_IN_A**/RDQ58	C (LVDS)*	PR73B	3	RLM0_GDLLC_IN_A**/RDQ71	C (LVDS)*
T26	PR60A	3	RLM0_GDLLT_IN_A**/RDQ58	T (LVDS)*	PR73A	3	RLM0_GDLLT_IN_A**/RDQ71	T (LVDS)*
T20	PR59B	3	RDQ58	C	PR72B	3	RDQ71	C
T22	PR59A	3	RDQ58	T	PR72A	3	RDQ71	T
VCCIO	VCCIO3	3			VCCIO3	3		
R26	PR58B	3	RDQ58	C (LVDS)*	PR71B	3	RDQ71	C (LVDS)*
R25	PR58A	3	RDQS58	T (LVDS)*	PR71A	3	RDQS71	T (LVDS)*
R22	PR57B	3	RDQ58	C	PR70B	3	RDQ71	C
GND	GNDIO3	-			GNDIO3	-		
T21	PR57A	3	RDQ58	T	PR70A	3	RDQ71	T
P26	PR56B	3	RDQ58	C (LVDS)*	PR69B	3	RDQ71	C (LVDS)*
P25	PR56A	3	RDQ58	T (LVDS)*	PR69A	3	RDQ71	T (LVDS)*
R24	PR55B	3	RDQ58	C	PR68B	3	RDQ71	C
VCCIO	VCCIO3	3			VCCIO3	3		
R23	PR55A	3	RDQ58	T	PR68A	3	RDQ71	T
P20	PR54B	3	RDQ58	C (LVDS)*	PR67B	3	RDQ71	C (LVDS)*
R19	PR54A	3	RDQ58	T (LVDS)*	PR67A	3	RDQ71	T (LVDS)*
P21	PR53B	3	RDQ50	C	PR66B	3	RDQ63	C
GND	GNDIO3	-			GNDIO3	-		
P19	PR53A	3	RDQ50	T	PR66A	3	RDQ63	T
P23	PR52B	3	RDQ50	C (LVDS)*	PR65B	3	RDQ63	C (LVDS)*
P22	PR52A	3	RDQ50	T (LVDS)*	PR65A	3	RDQ63	T (LVDS)*
N22	PR51B	3	RDQ50	C	PR64B	3	RDQ63	C
VCCIO	VCCIO3	3			VCCIO3	3		
R21	PR51A	3	RDQ50	T	PR64A	3	RDQ63	T
N26	PR50B	3	RDQ50	C (LVDS)*	PR63B	3	RDQ63	C (LVDS)*
N25	PR50A	3	RDQS50	T (LVDS)*	PR63A	3	RDQS63	T (LVDS)*
GND	GNDIO3	-			GNDIO3	-		
N19	PR49B	3	RDQ50	C	PR62B	3	RDQ63	C
N20	PR49A	3	RDQ50	T	PR62A	3	RDQ63	T
M26	PR48B	3	RDQ50	C (LVDS)*	PR61B	3	RDQ63	C (LVDS)*
M25	PR48A	3	RDQ50	T (LVDS)*	PR61A	3	RDQ63	T (LVDS)*
VCCIO	VCCIO3	3			VCCIO3	3		
N18	PR47B	3	VREF2_3/RDQ50	C	PR60B	3	VREF2_3/RDQ63	C
N21	PR47A	3	VREF1_3/RDQ50	T	PR60A	3	VREF1_3/RDQ63	T
L26	PR46B	3	PCLKC3_0/RDQ50	C (LVDS)*	PR59B	3	PCLKC3_0/RDQ63	C (LVDS)*
L25	PR46A	3	PCLKT3_0/RDQ50	T (LVDS)*	PR59A	3	PCLKT3_0/RDQ63	T (LVDS)*
N24	PR44B	2	PCLKC2_0/RDQ41	C	PR57B	2	PCLKC2_0/RDQ54	C
M23	PR44A	2	PCLKT2_0/RDQ41	T	PR57A	2	PCLKT2_0/RDQ54	T

LFE2M20E/SE and LFE2M35E/SE Logic Signal Connections: 484 fpBGA

LFE2M20E/SE					LFE2M35E/SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
D1	PL2A	7	LDQ6	T (LVDS)*	PL2A	7	LDQ6	T (LVDS)*
E1	PL2B	7	LDQ6	C (LVDS)*	PL2B	7	LDQ6	C (LVDS)*
F1	PL3A	7	LDQ6	T	PL3A	7	LDQ6	T
F2	PL3B	7	LDQ6	C	PL3B	7	LDQ6	C
F5	PL4A	7	LDQ6	T (LVDS)*	PL4A	7	LDQ6	T (LVDS)*
VCCIO	VCCIO7	7			VCCIO7	7		
G6	PL4B	7	LDQ6	C (LVDS)*	PL4B	7	LDQ6	C (LVDS)*
F4	PL5A	7	LDQ6	T	PL5A	7	LDQ6	T
F3	PL5B	7	LDQ6	C	PL5B	7	LDQ6	C
G1	PL6A	7	LDQS6	T (LVDS)*	PL6A	7	LDQS6	T (LVDS)*
GNDIO	GNDIO7	-			GNDIO7	-		
G2	PL6B	7	LDQ6	C (LVDS)*	PL6B	7	LDQ6	C (LVDS)*
H1	PL7A	7	LDQ6	T	PL7A	7	LDQ6	T
H2	PL7B	7	LDQ6	C	PL7B	7	LDQ6	C
VCCIO	VCCIO7	7			VCCIO7	7		
H7	PL8A	7	LDQ6	T (LVDS)*	PL8A	7	LDQ6	T (LVDS)*
H6	PL8B	7	LDQ6	C (LVDS)*	PL8B	7	LDQ6	C (LVDS)*
G3	PL9A	7	VREF2_7/LDQ6	T	PL9A	7	VREF2_7/LDQ6	T
H3	PL9B	7	VREF1_7/LDQ6	C	PL9B	7	VREF1_7/LDQ6	C
GNDIO	GNDIO7	-			GNDIO7	-		
H5	PL11A	7	LUM0_SPLLT_IN_A	T (LVDS)*	PL11A	7	LUM0_SPLLT_IN_A/LDQ15	T (LVDS)*
H4	PL11B	7	LUM0_SPLLC_IN_A	C (LVDS)*	PL11B	7	LUM0_SPLLC_IN_A/LDQ15	C (LVDS)*
J1	PL12A	7	LUM0_SPLLT_FB_A	T	PL12A	7	LUM0_SPLLT_FB_A/LDQ15	T
J2	PL12B	7	LUM0_SPLLC_FB_A	C	PL12B	7	LUM0_SPLLC_FB_A/LDQ15	C
J3	PL13A	7		T (LVDS)*	PL13A	7	LDQ15	T (LVDS)*
VCCIO	VCCIO7	7			VCCIO7	7		
J4	PL13B	7		C (LVDS)*	PL13B	7	LDQ15	C (LVDS)*
J7	PL14A	7		T	PL14A	7	LDQ15	T
J6	PL14B	7		C	PL14B	7	LDQ15	C
GNDIO	GNDIO7	-			GNDIO7	-		
VCCIO	VCCIO7	7			VCCIO7	7		
K1	PL18A	7	LUM1_SPLLT_IN_A/LDQ22	T (LVDS)*	PL28A	7	LUM1_SPLLT_IN_A/LDQ32	T (LVDS)*
K2	PL18B	7	LUM1_SPLLC_IN_A/LDQ22	C (LVDS)*	PL28B	7	LUM1_SPLLC_IN_A/LDQ32	C (LVDS)*
J5	PL19A	7	LUM1_SPLLT_FB_A/LDQ22	T	PL29A	7	LUM1_SPLLT_FB_A/LDQ32	T
K5	PL19B	7	LUM1_SPLLC_FB_A/LDQ22	C	PL29B	7	LUM1_SPLLC_FB_A/LDQ32	C
VCCIO	VCCIO7	7			VCCIO7	7		
K7	PL20A	7	LDQ22	T (LVDS)*	PL30A	7	LDQ32	T (LVDS)*
K6	PL20B	7	LDQ22	C (LVDS)*	PL30B	7	LDQ32	C (LVDS)*
L6	PL21A	7	LDQ22	T	PL31A	7	LDQ32	T
L7	PL21B	7	LDQ22	C	PL31B	7	LDQ32	C
GNDIO	GNDIO7	-			GNDIO7	-		
L1	PL22A	7	LDQS22	T (LVDS)*	PL32A	7	LDQS32	T (LVDS)*
L2	PL22B	7	LDQ22	C (LVDS)*	PL32B	7	LDQ32	C (LVDS)*
M7	PL23A	7	LDQ22	T	PL33A	7	LDQ32	T
VCCIO	VCCIO7	7			VCCIO7	7		
L5	PL23B	7	LDQ22	C	PL33B	7	LDQ32	C
L3	PL24A	7	LDQ22	T (LVDS)*	PL34A	7	LDQ32	T (LVDS)*

LFE2M50E/SE Logic Signal Connections: 484 fpBGA (Cont.)

LFE2M50E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential
G5	VCCIO7	7		
J8	VCCIO7	7		
K4	VCCIO7	7		
AA22	VCCIO8	8		
U19	VCCIO8	8		
H11	VCCAUX	-		
H12	VCCAUX	-		
L15	VCCAUX	-		
L8	VCCAUX	-		
M15	VCCAUX	-		
M8	VCCAUX	-		
R11	VCCAUX	-		
R12	VCCAUX	-		
A1	GND	-		
A10	GND	-		
A16	GND	-		
A22	GND	-		
AA19	GND	-		
AA4	GND	-		
AB1	GND	-		
AB22	GND	-		
B13	GND	-		
B19	GND	-		
B4	GND	-		
D16	GND	-		
D2	GND	-		
D21	GND	-		
D7	GND	-		
G19	GND	-		
G4	GND	-		
H10	GND	-		
H13	GND	-		
J14	GND	-		
J9	GND	-		
K10	GND	-		
K11	GND	-		
K12	GND	-		
K13	GND	-		
K15	GND	-		
K20	GND	-		
K3	GND	-		
K8	GND	-		
L10	GND	-		

LFE2M35E/SE and LFE2M50E/SE Logic Signal Connections: 672 fpBGA
(Cont.)

LFE2M35E/SE					LFE2M50E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential	
N23	PR37A	3	PCLKT3_0	T (LVDS)*	PR41A	3	PCLKT3_0	T*	
N24	PR35B	2	PCLKC2_0/RDQ32	C	PR39B	2	PCLKC2_0/RDQ36	C	
N25	PR35A	2	PCLKT2_0/RDQ32	T	PR39A	2	PCLKT2_0/RDQ36	T	
GNDIO	GNDIO2	-			GNDIO2	-			
M22	PR34B	2	RDQ32	C (LVDS)*	PR38B	2	RDQ36	C*	
M24	PR34A	2	RDQ32	T (LVDS)*	PR38A	2	RDQ36	T*	
M23	PR33B	2	RDQ32	C	PR37B	2	RDQ36	C	
N26	PR33A	2	RDQ32	T	PR37A	2	RDQ36	T	
VCCIO	VCCIO2	2			VCCIO2	2			
L22	PR32B	2	RDQ32	C (LVDS)*	PR36B	2	RDQ36	C*	
L24	PR32A	2	RDQS32	T (LVDS)*	PR36A	2	RDQS36	T*	
L23	PR31B	2	RDQ32	C	PR35B	2	RDQ36	C	
GNDIO	GNDIO2	-			GNDIO2	-			
M20	PR31A	2	RDQ32	T	PR35A	2	RDQ36	T	
M26	PR30B	2	RDQ32	C (LVDS)*	PR34B	2	RDQ36	C*	
L26	PR30A	2	RDQ32	T (LVDS)*	PR34A	2	RDQ36	T*	
K22	PR29B	2	RUM1_SPLLC_FB_A/RDQ32	C	PR33B	2	RUM3_SPLLC_FB_A/RDQ36	C	
VCCIO	VCCIO2	2			VCCIO2	2			
M19	PR29A	2	RUM1_SPLLT_FB_A/RDQ32	T	PR33A	2	RUM3_SPLLT_FB_A/RDQ36	T	
K25	PR28B	2	RUM1_SPLLC_IN_A/RDQ32	C (LVDS)*	PR32B	2	RUM3_SPLLC_IN_A/RDQ36	C*	
K26	PR28A	2	RUM1_SPLLT_IN_A/RDQ32	T (LVDS)*	PR32A	2	RUM3_SPLLT_IN_A/RDQ36	T*	
K24	PR26B	2	RDQ23	C	PR30B	2	RDQ27	C	
K23	PR26A	2	RDQ23	T	PR30A	2	RDQ27	T	
GNDIO	GNDIO2	-			GNDIO2	-			
L19	PR25B	2	RDQ23	C (LVDS)*	PR29B	2	RDQ27	C*	
K21	PR25A	2	RDQ23	T (LVDS)*	PR29A	2	RDQ27	T*	
J23	PR24B	2	RDQ23	C	PR28B	2	RDQ27	C	
J24	PR24A	2	RDQ23	T	PR28A	2	RDQ27	T	
VCCIO	VCCIO2	2			VCCIO2	2			
K20	PR23B	2	RDQ23	C (LVDS)*	PR27B	2	RDQ27	C*	
J21	PR23A	2	RDQS23	T (LVDS)*	PR27A	2	RDQS27	T*	
H21	PR22B	2	RDQ23	C	PR26B	2	RDQ27	C	
GNDIO	GNDIO2	-			GNDIO2	-			
K18	PR22A	2	RDQ23	T	PR26A	2	RDQ27	T	
H22	PR21B	2	RDQ23	C (LVDS)*	PR25B	2	RDQ27	C*	
J20	PR21A	2	RDQ23	T (LVDS)*	PR25A	2	RDQ27	T*	
J25	PR20B	2	RDQ23	C	PR24B	2	RDQ27	C	
VCCIO	VCCIO2	2			VCCIO2	2			
J26	PR20A	2	RDQ23	T	PR24A	2	RDQ27	T	
G21	PR19B	2	RDQ23	C (LVDS)*	PR23B	2	RDQ27	C*	
J19	PR19A	2	RDQ23	T (LVDS)*	PR23A	2	RDQ27	T*	
GNDIO	GNDIO2	-			GNDIO2	-			
H23	PR18B	2	RDQ15	C	PR21B	2		C	
H24	PR18A	2	RDQ15	T	PR21A	2		T	
H25	PR17B	2	RDQ15	C (LVDS)*	PR20B	2		C*	
H26	PR17A	2	RDQ15	T (LVDS)*	PR20A	2		T*	
VCCIO	VCCIO2	2			VCCIO2	2			
G22	PR16B	2	RDQ15	C	PR19B	2		C	

**LFE2M35E/SE and LFE2M50E/SE Logic Signal Connections: 672 fpBGA
 (Cont.)**

LFE2M35E/SE					LFE2M50E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential	
A12	PT35B	0		C	PT44B	0		C	
VCCIO	VCCIO0	0			VCCIO0	0			
A11	PT35A	0		T	PT44A	0		T	
D12	PT34B	0		C	PT43B	0		C	
H16	PT34A	0		T	PT43A	0		T	
H18	PT33B	0		C	PT42B	0		C	
H15	PT33A	0		T	PT42A	0		T	
A10	PT32B	0		C	PT41B	0		C	
GNDIO	GNDIO0	-			GNDIO0	-			
B10	PT32A	0		T	PT41A	0		T	
D11	PT31B	0		C	PT40B	0		C	
VCCIO	VCCIO0	0			VCCIO0	0			
G14	PT31A	0		T	PT40A	0		T	
E11	PT30B	0		C	PT39B	0		C	
F13	PT30A	0		T	PT39A	0		T	
D10	PT29B	0		C	PT38B	0		C	
H14	PT29A	0		T	PT38A	0		T	
GNDIO	GNDIO0	-			GNDIO0	-			
VCCIO	VCCIO0	0			VCCIO0	0			
A9	PT24B	0		C	PT24B	0		C	
C10	PT23B	0		C	PT23B	0		C	
GNDIO	GNDIO0	-			GNDIO0	-			
E8	PT23A	0		T	PT23A	0		T	
B9	PT22B	0		C	PT22B	0		C	
A8	PT22A	0		T	PT22A	0		T	
VCCIO	VCCIO0	0			VCCIO0	0			
F12	PT21B	0		C	PT21B	0		C	
E10	PT21A	0		T	PT21A	0		T	
G13	PT20B	0		C	PT20B	0		C	
C9	PT20A	0		T	PT20A	0		T	
B8	PT19B	0		C	PT19B	0		C	
GNDIO	GNDIO0	-			GNDIO0	-			
A7	PT19A	0		T	PT19A	0		T	
D9	PT18B	0		C	PT18B	0		C	
H13	PT18A	0		T	PT18A	0		T	
D6	PT17B	0		C	PT17B	0		C	
C7	PT17A	0		T	PT17A	0		T	
VCCIO	VCCIO0	0			VCCIO0	0			
C8	PT16B	0		C	PT16B	0		C	
G12	PT16A	0		T	PT16A	0		T	
D8	PT15B	0		C	PT15B	0		C	
H12	PT15A	0		T	PT15A	0		T	
GNDIO	GNDIO0	-			GNDIO0	-			
A6	PT14B	0		C	PT14B	0		C	
A5	PT14A	0		T	PT14A	0		T	
A4	PT13B	0		C	PT13B	0		C	
A3	PT13A	0		T	PT13A	0		T	
VCCIO	VCCIO0	0			VCCIO0	0			

LFE2M100E/SE Logic Signal Connections: 900 fpBGA (Cont.)

LFE2M100E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential
AJ30	LRC_SQ_VCCIB0	13		
AK29	LRC_SQ_HDINP0	13		T
AH30	LRC_SQ_VCCRX0	13		
AG27	CFG2	8		
AD25	CFG1	8		
AG28	CFG0	8		
AG30	PROGRAMN	8		
AG29	CCLK	8		
AC24	INITN	8		
AF27	DONE	8		
GNDIO	GNDIO8	-		
AF28	WRITEN***	8		
AE26	CS1N***	8		
AB23	CSN***	8		
AF29	D0/SPIFASTN***	8		
VCCIO	VCCIO8	8		
AF30	D1***	8		
AD26	D2***	8		
AE29	D3***	8		
GNDIO	GNDIO8	-		
AE30	D4***	8		
AD29	D5***	8		
AC25	D6***	8		
AD30	D7/SPID0***	8		
VCCIO	VCCIO8	8		
AA22	DI/CSSPI0N***	8		
AC26	DOUT/CSON/CSSPI1N***	8		
AA23	BUSY/SISPI***	8		
AB22	RLM0_PLLCAP	3		
AC27	PR102B	3	RLM0_GDLLC_FB_A/RDQ99	C
GNDIO	GNDIO3	-		
AC28	PR102A	3	RLM0_GDLLT_FB_A/RDQ99	T
AC29	PR101B	3	RLM0_GDLLC_IN_A**/RDQ99	C (LVDS)*
AC30	PR101A	3	RLM0_GDLLT_IN_A**/RDQ99	T (LVDS)*
AB30	PR100B	3	RLM0_GPLLC_IN_A**/RDQ99	C
VCCIO	VCCIO3	3		
AA30	PR100A	3	RLM0_GPLLT_IN_A**/RDQ99	T
AB29	PR99B	3	RLM0_GPLLC_FB_A/RDQ99	C (LVDS)*
AB28	PR99A	3	RLM0_GPLLT_FB_A/RDQS99	T (LVDS)*
GNDIO	GNDIO3	-		
Y22	PR98B	3	RDQ99	C
Y23	PR98A	3	RDQ99	T
AB26	PR97B	3	RDQ99	C (LVDS)*

LFE2M70E/SE and LFE2M100E/SE Logic Signal Connections: 1152 fpBGA (Cont.)

LFE2M70E/SE				LFE2M100E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
GNDIO	GNDIO1	-			GNDIO1	-		
F19	PT59B	1		C	PT68B	1		C
D18	PT59A	1		T	PT68A	1		T
L18	NC	-			PT67B	1		C
K19	NC	-			PT67A	1		T
VCCIO	VCCIO1	1			VCCIO1	1		
A18	PT57B	1	VREF2_1	C	PT66B	1	VREF2_1	C
B18	PT57A	1	VREF1_1	T	PT66A	1	VREF1_1	T
G18	PT56B	1	PCLKC1_0	C	PT65B	1	PCLKC1_0	C
E18	PT56A	1	PCLKT1_0	T	PT65A	1	PCLKT1_0	T
F18	PT55B	0	PCLKC0_0	C	PT64B	0	PCLKC0_0	C
GNDIO	GNDIO0	-			GNDIO0	-		
G19	PT55A	0	PCLKT0_0	T	PT64A	0	PCLKT0_0	T
H18	PT54B	0	VREF2_0	C	PT63B	0	VREF2_0	C
K18	PT54A	0	VREF1_0	T	PT63A	0	VREF1_0	T
VCCIO	VCCIO0	0			VCCIO0	0		
J18	PT53B	0		C	PT60B	0		C
L17	PT53A	0		T	PT60A	0		T
G17	PT52B	0		C	PT59B	0		C
-	-	-			GNDIO0	-		
J17	PT52A	0		T	PT59A	0		T
H17	PT51B	0		C	PT58B	0		C
-	-	-			VCCIO0	0		
K17	PT51A	0		T	PT58A	0		T
B17	PT50B	0		C	PT57B	0		C
GNDIO	GNDIO0	-			-	-		
A17	PT50A	0		T	PT57A	0		T
D17	PT49B	0		C	PT56B	0		C
VCCIO	VCCIO0	0			-	-		
F17	PT49A	0		T	PT56A	0		T
B16	PT48B	0		C	PT55B	0		C
A16	PT48A	0		T	PT55A	0		T
-	-	-			GNDIO0	-		
-	-	-			VCCIO0	0		
E17	PT47B	0		C	PT52B	0		C
C17	PT47A	0		T	PT52A	0		T
K16	PT46B	0		C	PT51B	0		C
J15	PT46A	0		T	PT51A	0		T
GNDIO	GNDIO0	-			GNDIO0	-		
G16	PT45B	0		C	PT50B	0		C
H15	PT45A	0		T	PT50A	0		T
A15	PT44B	0		C	PT49B	0		C
B15	PT44A	0		T	PT49A	0		T
VCCIO	VCCIO0	0			VCCIO0	0		
L16	PT43B	0		C	PT48B	0		C
K15	PT43A	0		T	PT48A	0		T
F16	PT42B	0		C	PT47B	0		C
E16	PT42A	0		T	PT47A	0		T
E15	PT41B	0		C	PT46B	0		C

LatticeECP2 S-Series Devices, Conventional Packaging
Commercial

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2-6SE-5T144C	90	1.2V	-5	TQFP	144	Com	6
LFE2-6SE-6T144C	90	1.2V	-6	TQFP	144	Com	6
LFE2-6SE-7T144C	90	1.2V	-7	TQFP	144	Com	6
LFE2-6SE-5F256C	190	1.2V	-5	fpBGA	256	Com	6
LFE2-6SE-6F256C	190	1.2V	-6	fpBGA	256	Com	6
LFE2-6SE-7F256C	190	1.2V	-7	fpBGA	256	Com	6

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2-12SE-5T144C	93	1.2V	-5	TQFP	144	Com	12
LFE2-12SE-6T144C	93	1.2V	-6	TQFP	144	Com	12
LFE2-12SE-7T144C	93	1.2V	-7	TQFP	144	Com	12
LFE2-12SE-5Q208C	131	1.2V	-5	PQFP	208	Com	12
LFE2-12SE-6Q208C	131	1.2V	-6	PQFP	208	Com	12
LFE2-12SE-7Q208C	131	1.2V	-7	PQFP	208	Com	12
LFE2-12SE-5F256C	193	1.2V	-5	fpBGA	256	Com	12
LFE2-12SE-6F256C	193	1.2V	-6	fpBGA	256	Com	12
LFE2-12SE-7F256C	193	1.2V	-7	fpBGA	256	Com	12
LFE2-12SE-5F484C	297	1.2V	-5	fpBGA	484	Com	12
LFE2-12SE-6F484C	297	1.2V	-6	fpBGA	484	Com	12
LFE2-12SE-7F484C	297	1.2V	-7	fpBGA	484	Com	12

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2-20SE-5Q208C	131	1.2V	-5	PQFP	208	Com	20
LFE2-20SE-6Q208C	131	1.2V	-6	PQFP	208	Com	20
LFE2-20SE-7Q208C	131	1.2V	-7	PQFP	208	Com	20
LFE2-20SE-5F256C	193	1.2V	-5	fpBGA	256	Com	20
LFE2-20SE-6F256C	193	1.2V	-6	fpBGA	256	Com	20
LFE2-20SE-7F256C	193	1.2V	-7	fpBGA	256	Com	20
LFE2-20SE-5F484C	331	1.2V	-5	fpBGA	484	Com	20
LFE2-20SE-6F484C	331	1.2V	-6	fpBGA	484	Com	20
LFE2-20SE-7F484C	331	1.2V	-7	fpBGA	484	Com	20
LFE2-20SE-5F672C	402	1.2V	-5	fpBGA	672	Com	20
LFE2-20SE-6F672C	402	1.2V	-6	fpBGA	672	Com	20
LFE2-20SE-7F672C	402	1.2V	-7	fpBGA	672	Com	20

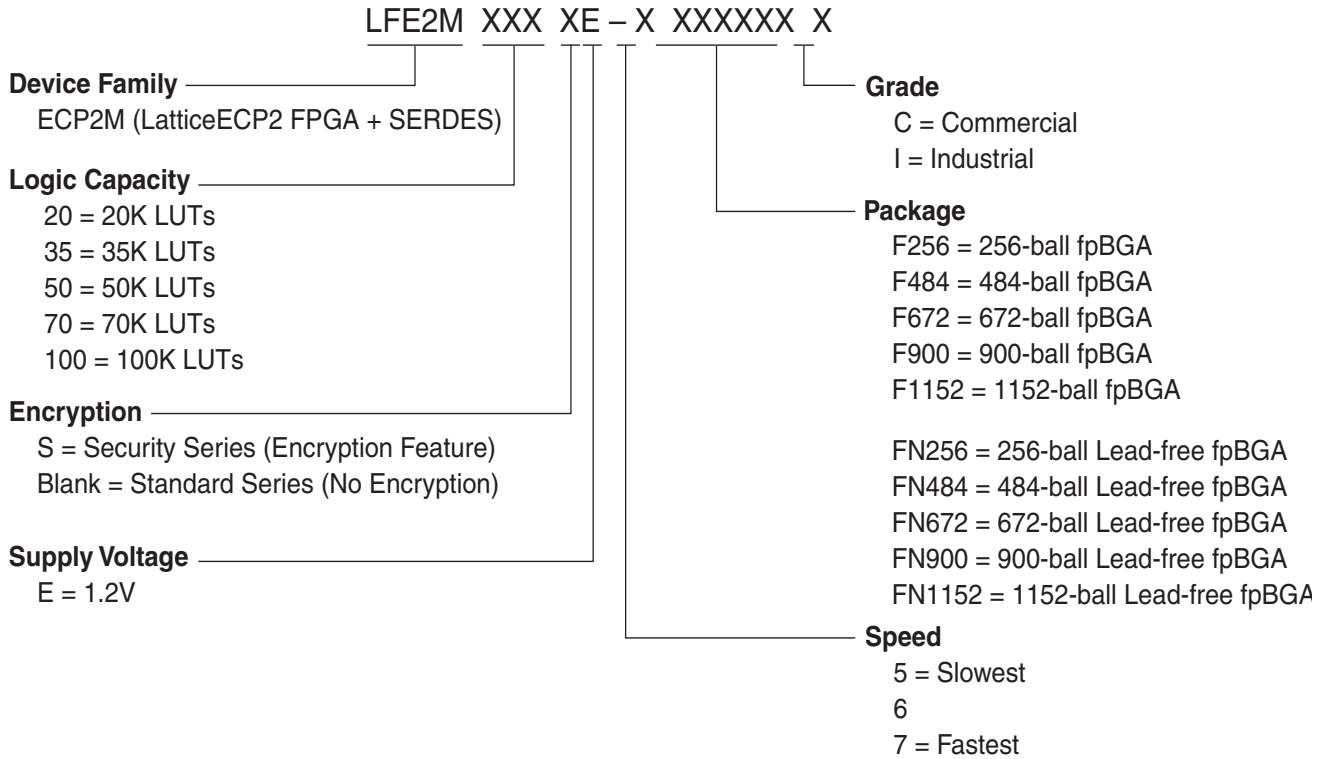
LatticeECP2 S-Series Devices, Lead-Free Packaging
Commercial

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2-6SE-5TN144C	90	1.2V	-5	Lead-Free TQFP	144	Com	6
LFE2-6SE-6TN144C	90	1.2V	-6	Lead-Free TQFP	144	Com	6
LFE2-6SE-7TN144C	90	1.2V	-7	Lead-Free TQFP	144	Com	6
LFE2-6SE-5FN256C	190	1.2V	-5	Lead-Free fpBGA	256	Com	6
LFE2-6SE-6FN256C	190	1.2V	-6	Lead-Free fpBGA	256	Com	6
LFE2-6SE-7FN256C	190	1.2V	-7	Lead-Free fpBGA	256	Com	6

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2-12SE-5TN144C	93	1.2V	-5	Lead-Free TQFP	144	Com	12
LFE2-12SE-6TN144C	93	1.2V	-6	Lead-Free TQFP	144	Com	12
LFE2-12SE-7TN144C	93	1.2V	-7	Lead-Free TQFP	144	Com	12
LFE2-12SE-5QN208C	131	1.2V	-5	Lead-Free PQFP	208	Com	12
LFE2-12SE-6QN208C	131	1.2V	-6	Lead-Free PQFP	208	Com	12
LFE2-12SE-7QN208C	131	1.2V	-7	Lead-Free PQFP	208	Com	12
LFE2-12SE-5FN256C	193	1.2V	-5	Lead-Free fpBGA	256	Com	12
LFE2-12SE-6FN256C	193	1.2V	-6	Lead-Free fpBGA	256	Com	12
LFE2-12SE-7FN256C	193	1.2V	-7	Lead-Free fpBGA	256	Com	12
LFE2-12SE-5FN484C	297	1.2V	-5	Lead-Free fpBGA	484	Com	12
LFE2-12SE-6FN484C	297	1.2V	-6	Lead-Free fpBGA	484	Com	12
LFE2-12SE-7FN484C	297	1.2V	-7	Lead-Free fpBGA	484	Com	12

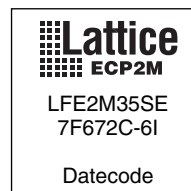
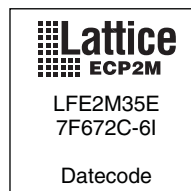
Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2-20SE-5QN208C	131	1.2V	-5	Lead-Free PQFP	208	Com	20
LFE2-20SE-6QN208C	131	1.2V	-6	Lead-Free PQFP	208	Com	20
LFE2-20SE-7QN208C	131	1.2V	-7	Lead-Free PQFP	208	Com	20
LFE2-20SE-5FN256C	193	1.2V	-5	Lead-Free fpBGA	256	Com	20
LFE2-20SE-6FN256C	193	1.2V	-6	Lead-Free fpBGA	256	Com	20
LFE2-20SE-7FN256C	193	1.2V	-7	Lead-Free fpBGA	256	Com	20
LFE2-20SE-5FN484C	331	1.2V	-5	Lead-Free fpBGA	484	Com	20
LFE2-20SE-6FN484C	331	1.2V	-6	Lead-Free fpBGA	484	Com	20
LFE2-20SE-7FN484C	331	1.2V	-7	Lead-Free fpBGA	484	Com	20
LFE2-20SE-5FN672C	402	1.2V	-5	Lead-Free fpBGA	672	Com	20
LFE2-20SE-6FN672C	402	1.2V	-6	Lead-Free fpBGA	672	Com	20
LFE2-20SE-7FN672C	402	1.2V	-7	Lead-Free fpBGA	672	Com	20

LatticeECP2M Part Number Description



Ordering Information

Note: LatticeECP2M devices are dual marked. For example, the commercial speed grade LFE2M50E-7F672C is also marked with industrial grade -6I (LFE2M50E-6F672I). The commercial grade is one speed grade faster than the associated dual mark industrial grade. The slowest commercial grade does not have industrial markings. The markings appear as follows:



Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2M100E-5FN1152I	520	1.2V	-5	Lead-Free fpBGA	1152	Ind	100
LFE2M100E-6FN1152I	520	1.2V	-6	Lead-Free fpBGA	1152	Ind	100
LFE2M100E-5FN900I	416	1.2V	-5	Lead-Free fpBGA	900	Ind	100
LFE2M100E-6FN900I	416	1.2V	-6	Lead-Free fpBGA	900	Ind	100

LatticeECP2M S-Series Devices, Conventional Packaging
Commercial

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2M20SE-5F484C	304	1.2V	-5	fpBGA	484	Com	20
LFE2M20SE-6F484C	304	1.2V	-6	fpBGA	484	Com	20
LFE2M20SE-7F484C	304	1.2V	-7	fpBGA	484	Com	20
LFE2M20SE-5F256C	140	1.2V	-5	fpBGA	256	Com	20
LFE2M20SE-6F256C	140	1.2V	-6	fpBGA	256	Com	20
LFE2M20SE-7F256C	140	1.2V	-7	fpBGA	256	Com	20

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2M35SE-5F672C	410	1.2V	-5	fpBGA	672	Com	35
LFE2M35SE-6F672C	410	1.2V	-6	fpBGA	672	Com	35
LFE2M35SE-7F672C	410	1.2V	-7	fpBGA	672	Com	35
LFE2M35SE-5F484C	303	1.2V	-5	fpBGA	484	Com	35
LFE2M35SE-6F484C	303	1.2V	-6	fpBGA	484	Com	35
LFE2M35SE-7F484C	303	1.2V	-7	fpBGA	484	Com	35
LFE2M35SE-5F256C	140	1.2V	-5	fpBGA	256	Com	35
LFE2M35SE-6F256C	140	1.2V	-6	fpBGA	256	Com	35
LFE2M35SE-7F256C	140	1.2V	-7	fpBGA	256	Com	35

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2M50SE-5F900C	410	1.2V	-5	fpBGA	900	Com	50
LFE2M50SE-6F900C	410	1.2V	-6	fpBGA	900	Com	50
LFE2M50SE-7F900C	410	1.2V	-7	fpBGA	900	Com	50
LFE2M50SE-5F672C	372	1.2V	-5	fpBGA	672	Com	50
LFE2M50SE-6F672C	372	1.2V	-6	fpBGA	672	Com	50
LFE2M50SE-7F672C	372	1.2V	-7	fpBGA	672	Com	50
LFE2M50SE-5F484C	270	1.2V	-5	fpBGA	484	Com	50
LFE2M50SE-6F484C	270	1.2V	-6	fpBGA	484	Com	50
LFE2M50SE-7F484C	270	1.2V	-7	fpBGA	484	Com	50