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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	4250
Number of Logic Elements/Cells	34000
Total RAM Bits	2151424
Number of I/O	303
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	484-BBGA
Supplier Device Package	484-FPBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfe2m35e-5fn484c

LFE2-35E/SE and LFE2-50E/SE Logic Signal Connections: 484 fpBGA (Cont.)

LFE2-35E/SE					LFE2-50E/SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
U8	PB23A	5	BDQ24	T	PB32A	5	BDQ33	T
U9	PB23B	5	BDQ24	C	PB32B	5	BDQ33	C
W9	PB24A	5	BDQS24	T	PB33A	5	BDQS33	T
GNDIO	GNDIO5	-			GNDIO5	-		
V9	PB24B	5	BDQ24	C	PB33B	5	BDQ33	C
Y8	PB25A	5	BDQ24	T	PB34A	5	BDQ33	T
AA8	PB25B	5	BDQ24	C	PB34B	5	BDQ33	C
W10	PB26A	5	BDQ24	T	PB35A	5	BDQ33	T
VCCIO	VCCIO5	5			VCCIO	5		
V10	PB26B	5	BDQ24	C	PB35B	5	BDQ33	C
AB8	PB27A	5	BDQ24	T	PB36A	5	BDQ33	T
AA9	PB27B	5	BDQ24	C	PB36B	5	BDQ33	C
GNDIO	GNDIO5	-			GNDIO5	-		
AB9	PB29A	5	BDQ33	T	PB38A	5	BDQ42	T
AB10	PB29B	5	BDQ33	C	PB38B	5	BDQ42	C
Y10	PB30A	5	BDQ33	T	PB39A	5	BDQ42	T
AA10	PB30B	5	BDQ33	C	PB39B	5	BDQ42	C
U10	PB31A	5	BDQ33	T	PB40A	5	BDQ42	T
U11	PB31B	5	BDQ33	C	PB40B	5	BDQ42	C
VCCIO	VCCIO5	5			VCCIO	5		
AB11	PB32A	5	BDQ33	T	PB41A	5	BDQ42	T
AA11	PB32B	5	BDQ33	C	PB41B	5	BDQ42	C
GNDIO	GNDIO5	-			GNDIO5	-		
Y11	PB33A	5	BDQS33	T	PB42A	5	BDQS42	T
W11	PB33B	5	BDQ33	C	PB42B	5	BDQ42	C
AB12	PB34A	5	BDQ33	T	PB43A	5	BDQ42	T
AA12	PB34B	5	BDQ33	C	PB43B	5	BDQ42	C
AB13	PB35A	5	PCLKT5_0/BDQ33	T	PB44A	5	PCLKT5_0/BDQ42	T
AB14	PB35B	5	PCLKC5_0/BDQ33	C	PB44B	5	PCLKC5_0/BDQ42	C
VCCIO	VCCIO5	5			VCCIO	5		
GNDIO	GNDIO5	-			GNDIO5	-		
U12	PB40A	4	PCLKT4_0/BDQ42	T	PB49A	4	PCLKT4_0/BDQ51	T
VCCIO	VCCIO4	4			VCCIO	4		
V12	PB40B	4	PCLKC4_0/BDQ42	C	PB49B	4	PCLKC4_0/BDQ51	C
Y12	PB41A	4	BDQ42	T	PB50A	4	BDQ51	T
W12	PB41B	4	BDQ42	C	PB50B	4	BDQ51	C
AA13	PB42A	4	BDQS42	T	PB51A	4	BDQS51	T
GNDIO	GNDIO4	-			GNDIO4	-		
Y13	PB42B	4	BDQ42	C	PB51B	4	BDQ51	C
U13	PB43A	4	BDQ42	T	PB52A	4	BDQ51	T
U14	PB43B	4	BDQ42	C	PB52B	4	BDQ51	C
AB15	PB44A	4	BDQ42	T	PB53A	4	BDQ51	T
VCCIO	VCCIO4	4			VCCIO	4		
AA14	PB44B	4	BDQ42	C	PB53B	4	BDQ51	C
AB16	PB45A	4	BDQ42	T	PB54A	4	BDQ51	T
AB17	PB45B	4	BDQ42	C	PB54B	4	BDQ51	C

LFE2-35E/SE and LFE2-50E/SE Logic Signal Connections: 484 fpBGA (Cont.)

LFE2-35E/SE					LFE2-50E/SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
J22	PR29B	3	RDQ31	C (LVDS)*	PR48B	3	RDQ50	C (LVDS)*
H22	PR29A	3	RDQ31	T (LVDS)*	PR48A	3	RDQ50	T (LVDS)*
VCCIO	VCCIO3	3			VCCIO	3		
M20	PR28B	3	VREF2_3/RDQ31	C	PR47B	3	VREF2_3/RDQ50	C
L21	PR28A	3	VREF1_3/RDQ31	T	PR47A	3	VREF1_3/RDQ50	T
K21	PR27B	3	PCLKC3_0/RDQ31	C (LVDS)*	PR46B	3	PCLKC3_0/RDQ50	C (LVDS)*
J21	PR27A	3	PCLKT3_0/RDQ31	T (LVDS)*	PR46A	3	PCLKT3_0/RDQ50	T (LVDS)*
M18	PR25B	2	PCLKC2_0/RDQ22	C	PR44B	2	PCLKC2_0/RDQ41	C
L17	PR25A	2	PCLKT2_0/RDQ22	T	PR44A	2	PCLKT2_0/RDQ41	T
GNDIO	GNDIO2	-			GNDIO2	-		
L19	PR24B	2	RDQ22	C (LVDS)*	PR43B	2	RDQ41	C (LVDS)*
L20	PR24A	2	RDQ22	T (LVDS)*	PR43A	2	RDQ41	T (LVDS)*
L18	PR23B	2	RDQ22	C	PR42B	2	RDQ41	C
K17	PR23A	2	RDQ22	T	PR42A	2	RDQ41	T
VCCIO	VCCIO2	2			VCCIO	2		
K18	PR22B	2	RDQ22	C (LVDS)*	PR41B	2	RDQ41	C (LVDS)*
K19	PR22A	2	RDQS22	T (LVDS)*	PR41A	2	RDQS41	T (LVDS)*
G22	PR21B	2	RDQ22	C	PR40B	2	RDQ41	C
GNDIO	GNDIO2	-			GNDIO2	-		
F22	PR21A	2	RDQ22	T	PR40A	2	RDQ41	T
J17	PR20B	2	RDQ22	C (LVDS)*	PR39B	2	RDQ41	C (LVDS)*
J18	PR20A	2	RDQ22	T (LVDS)*	PR39A	2	RDQ41	T (LVDS)*
K20	PR19B	2	RDQ22	C	PR38B	2	RDQ41	C
VCCIO	VCCIO2	2			VCCIO	2		
J19	PR19A	2	RDQ22	T	PR38A	2	RDQ41	T
H21	PR18B	2	RDQ22	C (LVDS)*	PR37B	2	RDQ41	C (LVDS)*
G21	PR18A	2	RDQ22	T (LVDS)*	PR37A	2	RDQ41	T (LVDS)*
-	-	-			GNDIO2	-		
-	-	-			VCCIO	2		
H17	NC	-			PR26B	2	RUM0_SPLLC_FB_A/RDQ24	C
H16	NC	-			PR26A	2	RUM0_SPLLT_FB_A/RDQ24	T
H20	NC	-			PR25B	2	RUM0_SPLLC_IN_A/RDQ24	C
H18	NC	-			PR25A	2	RUM0_SPLLT_IN_A/RDQ24	T
-	-	-			GNDIO2	-		
-	-	-			VCCIO	2		
F21	PR17B	2	RDQ14	C	PR19B	2	RDQ16	C
GNDIO	GNDIO2	-			GNDIO2	-		
E22	PR17A	2	RDQ14	T	PR19A	2	RDQ16	T
D22	PR16B	2	RDQ14	C (LVDS)*	PR18B	2	RDQ16	C (LVDS)*
E21	PR16A	2	RDQ14	T (LVDS)*	PR18A	2	RDQ16	T (LVDS)*
G20	PR15B	2	RDQ14	C	PR17B	2	RDQ16	C
VCCIO	VCCIO2	2			VCCIO	2		
F20	PR15A	2	RDQ14	T	PR17A	2	RDQ16	T
H19	PR14B	2	RDQ14	C (LVDS)*	PR16B	2	RDQ16	C (LVDS)*
G19	PR14A	2	RDQS14	T (LVDS)*	PR16A	2	RDQS16	T (LVDS)*
GNDIO	GNDIO2	-			GNDIO2	-		

LFE2-20E/SE and LFE2-35E/SE Logic Signal Connections: 672 fpBGA (Cont.)

LFE2-20E/20SE					LFE2-35E/35SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential	
G24	PR6B	2	RDQ8	C (LVDS)*	PR12B	2	RDQ14	C (LVDS)*	
G23	PR6A	2	RDQ8	T (LVDS)*	PR12A	2	RDQ14	T (LVDS)*	
VCCIO	VCCIO2	2			VCCIO2	2			
K19	PR5B	2	RDQ8	C	PR11B	2	RDQ14	C	
J19	PR5A	2	RDQ8	T	PR11A	2	RDQ14	T	
D26	PR4B	2	RDQ8	C (LVDS)*	PR10B	2	RDQ14	C (LVDS)*	
C26	PR4A	2	RDQ8	T (LVDS)*	PR10A	2	RDQ14	T (LVDS)*	
F22	NC	-			PR9B	2	RDQ6	C	
E24	NC	-			PR9A	2	RDQ6	T	
GND	GNDIO2	-			GNDIO2	-			
D25	NC	-			PR8B	2	RDQ6	C (LVDS)*	
C25	NC	-			PR8A	2	RDQ6	T (LVDS)*	
D24	NC	-			PR7B	2	RDQ6	C	
B25	NC	-			PR7A	2	RDQ6	T	
VCCIO	VCCIO2	2			VCCIO2	2			
H21	NC	-			PR6B	2	RDQ6	C (LVDS)*	
G22	NC	-			PR6A	2	RDQS6	T (LVDS)*	
B24	NC	-			PR5B	2	RDQ6	C	
GND	GNDIO2	-			GNDIO2	-			
C24	NC	-			PR5A	2	RDQ6	T	
D23	NC	-			PR4B	2	RDQ6	C (LVDS)*	
C23	NC	-			PR4A	2	RDQ6	T (LVDS)*	
G21	PR3B	2		C	PR3B	2	RDQ6	C	
VCCIO	VCCIO2	2			VCCIO2	2			
H20	PR3A	2		T	PR3A	2	RDQ6	T	
GND	GNDIO2	-			GNDIO2	-			
E22	PR2B	2	VREF2_2	C (LVDS)*	PR2B	2	VREF2_2/RDQ6	C (LVDS)*	
F21	PR2A	2	VREF1_2	T (LVDS)*	PR2A	2	VREF1_2/RDQ6	T (LVDS)*	
E23	PT64B	1	VREF2_1	C	PT73B	1	VREF2_1	C	
GND	GNDIO1	-			GNDIO1	-			
D22	PT64A	1	VREF1_1	T	PT73A	1	VREF1_1	T	
G20	PT63B	1		C	PT72B	1		C	
J18	PT63A	1		T	PT72A	1		T	
F20	PT62B	1		C	PT71B	1		C	
VCCIO	VCCIO1	1			VCCIO1	1			
H19	PT62A	1		T	PT71A	1		T	
A24	PT61B	1		C	PT70B	1		C	
A23	PT61A	1		T	PT70A	1		T	
E21	PT60B	1		C	PT69B	1		C	
F19	PT60A	1		T	PT69A	1		T	
C22	PT59B	1		C	PT68B	1		C	
GND	GNDIO1	-			GNDIO1	-			
E20	PT59A	1		T	PT68A	1		T	
B22	PT58B	1		C	PT67B	1		C	
VCCIO	VCCIO1	1			VCCIO1	1			
B23	PT58A	1		T	PT67A	1		T	

LFE2-50E/SE and LFE2-70E/SE Logic Signal Connections: 672 fpBGA (Cont.)

LFE2-50E/SE					LFE2-70E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential	
W5	PL71B	6	LDQ75	C (LVDS)*	PL84B	6	LDQ88	C (LVDS)*	
AC1	PL72A	6	LDQ75	T	PL85A	6	LDQ88	T	
AD1	PL72B	6	LDQ75	C	PL85B	6	LDQ88	C	
VCCIO	VCCIO6	6			VCCIO6	6			
Y6	PL73A	6	LDQ75	T (LVDS)*	PL86A	6	LDQ88	T (LVDS)*	
Y5	PL73B	6	LDQ75	C (LVDS)*	PL86B	6	LDQ88	C (LVDS)*	
AE2	PL74A	6	LDQ75	T	PL87A	6	LDQ88	T	
AD2	PL74B	6	LDQ75	C	PL87B	6	LDQ88	C	
GND	GNDIO6	-			GNDIO6	-			
AB3	PL75A	6	LDQS75	T (LVDS)*	PL88A	6	LDQS88	T (LVDS)*	
AB2	PL75B	6	LDQ75	C (LVDS)*	PL88B	6	LDQ88	C (LVDS)*	
W7	PL76A	6	LDQ75	T	PL89A	6	LDQ88	T	
VCCIO	VCCIO6	6			VCCIO6	6			
W8	PL76B	6	LDQ75	C	PL89B	6	LDQ88	C	
Y7	PL77A	6	LDQ75	T (LVDS)*	PL90A	6	LDQ88	T (LVDS)*	
Y8	PL77B	6	LDQ75	C (LVDS)*	PL90B	6	LDQ88	C (LVDS)*	
AC2	PL78A	6	LDQ75	T	PL91A	6	LDQ88	T	
GND	GNDIO6	-			GNDIO6	-			
AD3	PL78B	6	LDQ75	C	PL91B	6	LDQ88	C	
AC3	TCK	-			TCK	-			
AA8	TDI	-			TDI	-			
AB4	TMS	-			TMS	-			
AA5	TDO	-			TDO	-			
AB5	VCCJ	-			VCCJ	-			
AE3	PB2A	5	VREF2_5/BDQ6	T	PB2A	5	VREF2_5/BDQ6	T	
AF3	PB2B	5	VREF1_5/BDQ6	C	PB2B	5	VREF1_5/BDQ6	C	
AC4	PB3A	5	BDQ6	T	PB3A	5	BDQ6	T	
AD4	PB3B	5	BDQ6	C	PB3B	5	BDQ6	C	
AE4	PB4A	5	BDQ6	T	PB4A	5	BDQ6	T	
AF4	PB4B	5	BDQ6	C	PB4B	5	BDQ6	C	
VCCIO	VCCIO5	5			VCCIO5	5			
V9	PB5A	5	BDQ6	T	PB5A	5	BDQ6	T	
W9	PB5B	5	BDQ6	C	PB5B	5	BDQ6	C	
GND	GNDIO5	-			GNDIO5	-			
AA6	PB6A	5	BDQS6	T	PB6A	5	BDQS6	T	
AB6	PB6B	5	BDQ6	C	PB6B	5	BDQ6	C	
AC5	PB7A	5	BDQ6	T	PB7A	5	BDQ6	T	
AD5	PB7B	5	BDQ6	C	PB7B	5	BDQ6	C	
AA7	PB8A	5	BDQ6	T	PB8A	5	BDQ6	T	
AB7	PB8B	5	BDQ6	C	PB8B	5	BDQ6	C	
VCCIO	VCCIO5	5			VCCIO5	5			
AE5	PB9A	5	BDQ6	T	PB9A	5	BDQ6	T	
AF5	PB9B	5	BDQ6	C	PB9B	5	BDQ6	C	
AC7	PB10A	5	BDQ6	T	PB10A	5	BDQ6	T	
AD7	PB10B	5	BDQ6	C	PB10B	5	BDQ6	C	
VCCIO	VCCIO5	5			VCCIO5	5			

LFE2-50E/SE and LFE2-70E/SE Logic Signal Connections: 672 fpBGA (Cont.)

LFE2-50E/SE					LFE2-70E/SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
A7	PT35B	0		C	PT44B	0		C
B7	PT35A	0		T	PT44A	0		T
VCCIO	VCCIO0	0			VCCIO0	0		
F12	PT34B	0		C	PT43B	0		C
D10	PT34A	0		T	PT43A	0		T
H11	PT33B	0		C	PT42B	0		C
G11	PT33A	0		T	PT42A	0		T
GND	GNDIO0	-			GNDIO0	-		
A6	PT32B	0		C	PT41B	0		C
B6	PT32A	0		T	PT41A	0		T
D8	PT31B	0		C	PT40B	0		C
C8	PT31A	0		T	PT40A	0		T
VCCIO	VCCIO0	0			VCCIO0	0		
F11	PT30B	0		C	PT39B	0		C
E10	PT30A	0		T	PT39A	0		T
E9	PT29B	0		C	PT38B	0		C
D9	PT29A	0		T	PT38A	0		T
G10	PT28B	0		C	PT37B	0		C
GND	GNDIO0	-			GNDIO0	-		
H10	PT28A	0		T	PT37A	0		T
A5	PT27B	0		C	PT36B	0		C
B5	PT27A	0		T	PT36A	0		T
C7	PT26B	0		C	PT35B	0		C
VCCIO	VCCIO0	0			VCCIO0	0		
D7	PT26A	0		T	PT35A	0		T
E8	PT25B	0		C	PT34B	0		C
F10	PT25A	0		T	PT34A	0		T
F8	PT24B	0		C	PT33B	0		C
H9	PT24A	0		T	PT33A	0		T
C5	PT23B	0		C	PT32B	0		C
GND	GNDIO0	-			GNDIO0	-		
D5	PT23A	0		T	PT32A	0		T
B4	PT22B	0			PT31B	0		
VCCIO	VCCIO0	0			VCCIO0	0		
GND	GNDIO0	-			GNDIO0	-		
VCCIO	VCCIO0	0			VCCIO0	0		
GND	GNDIO0	-			GNDIO0	-		
VCCIO	VCCIO0	0			VCCIO0	0		
C4	PT10B	0		C	PT10B	0		C
GND	GNDIO0	-			GNDIO0	-		
C3	PT10A	0		T	PT10A	0		T
A4	PT9B	0		C	PT9B	0		C
A3	PT9A	0		T	PT9A	0		T
B3	PT8B	0		C	PT8B	0		C
VCCIO	VCCIO0	0			VCCIO0	0		
B2	PT8A	0		T	PT8A	0		T

LFE2M35E/SE and LFE2M50E/SE Logic Signal Connections: 672 fpBGA (Cont.)

LFE2M35E/SE					LFE2M50E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential	
F11	VCCIO0	0			VCCIO0	0			
J13	VCCIO0	0			VCCIO0	0			
K12	VCCIO0	0			VCCIO0	1			
D18	VCCIO1	1			VCCIO1	1			
F16	VCCIO1	1			VCCIO1	1			
J14	VCCIO1	1			VCCIO1	1			
K15	VCCIO1	1			VCCIO1	1			
G25	VCCIO2	2			VCCIO2	2			
L21	VCCIO2	2			VCCIO2	2			
M17	VCCIO2	2			VCCIO2	2			
M25	VCCIO2	2			VCCIO2	2			
N18	VCCIO2	2			VCCIO2	2			
P18	VCCIO3	3			VCCIO3	3			
R17	VCCIO3	3			VCCIO3	3			
R25	VCCIO3	3			VCCIO3	3			
T21	VCCIO3	3			VCCIO3	3			
Y25	VCCIO3	3			VCCIO3	3			
AA16	VCCIO4	4			VCCIO4	4			
AC18	VCCIO4	4			VCCIO4	4			
U15	VCCIO4	4			VCCIO4	4			
V14	VCCIO4	4			VCCIO4	4			
AA11	VCCIO5	5			VCCIO5	5			
V13	VCCIO5	5			VCCIO5	5			
AE12	VCCIO5	5			VCCIO5	5			
AE7	VCCIO5	5			VCCIO5	5			
U12	VCCIO5	5			VCCIO5	5			
P9	VCCIO6	6			VCCIO6	6			
R10	VCCIO6	6			VCCIO6	6			
R2	VCCIO6	6			VCCIO6	6			
T6	VCCIO6	6			VCCIO6	6			
Y2	VCCIO6	6			VCCIO6	6			
G2	VCCIO7	7			VCCIO7	7			
L6	VCCIO7	7			VCCIO7	7			
M10	VCCIO7	7			VCCIO7	7			
M2	VCCIO7	7			VCCIO7	7			
N9	VCCIO7	7			VCCIO7	7			
AC24	VCCIO8	8			VCCIO8	8			
U17	VCCIO8	8			VCCIO8	8			
J11	VCCAUX	-			VCCAUX	-			
J12	VCCAUX	-			VCCAUX	-			
J15	VCCAUX	-			VCCAUX	-			
J16	VCCAUX	-			VCCAUX	-			
L18	VCCAUX	-			VCCAUX	-			
L9	VCCAUX	-			VCCAUX	-			
M18	VCCAUX	-			VCCAUX	-			
M9	VCCAUX	-			VCCAUX	-			
R18	VCCAUX	-			VCCAUX	-			
R9	VCCAUX	-			VCCAUX	-			

LFE2M50E/SE and LFE2M70E/SE Logic Signal Connections: 900 fpBGA

LFE2M50E/SE					LFE2M70E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential	
D2	PL9A	7	VREF2_7/LDQ6	T	PL9A	7	VREF2_7	T	
D3	PL9B	7	VREF1_7/LDQ6	C	PL9B	7	VREF1_7	C	
GNDIO	GNDIO7	-			GNDIO7	-			
J8	PL11A	7	LUM0_SPLLT_IN_A	T (LVDS)*	PL11A	7	LUM0_SPLLT_IN_A/LDQ15	T (LVDS)*	
H7	PL11B	7	LUM0_SPLLC_IN_A	C (LVDS)*	PL11B	7	LUM0_SPLLC_IN_A/LDQ15	C (LVDS)*	
E3	PL12A	7	LUM0_SPLLT_FB_A	T	PL12A	7	LUM0_SPLLT_FB_A/LDQ15	T	
E4	PL12B	7	LUM0_SPLLC_FB_A	C	PL12B	7	LUM0_SPLLC_FB_A/LDQ15	C	
GNDIO	GNDIO7	-			-	-			
G6	PL13A	7		T (LVDS)*	PL13A	7	LDQ15	T (LVDS)*	
F5	PL13B	7		C (LVDS)*	PL13B	7	LDQ15	C (LVDS)*	
E2	PL14A	7		T	PL14A	7	LDQ15	T	
D1	PL14B	7		C	PL14B	7	LDQ15	C	
-	-	-			GNDIO7	-			
G5	NC	-			PL15A	7	LDQS15	T (LVDS)*	
G4	NC	-			PL15B	7	LDQ15	C (LVDS)*	
K7	NC	-			PL16A	7	LDQ15	T	
K8	NC	-			PL16B	7	LDQ15	C	
E1	NC	-			PL17A	7	LDQ15	T (LVDS)*	
F2	NC	-			PL17B	7	LDQ15	C (LVDS)*	
F1	NC	-			PL18A	7	LDQ15	T	
-	-	-			GNDIO7	-			
G3	NC	-			PL18B	7	LDQ15	C	
H5	PL15A	7		T (LVDS)*	PL21A	7		T (LVDS)*	
H4	PL15B	7		C (LVDS)*	PL21B	7		C (LVDS)*	
J5	PL16A	7		T	PL22A	7		T	
J4	PL16B	7		C	PL22B	7		C	
GNDIO	GNDIO7	-			GNDIO7	-			
G2	NC	-			PL24A	7	LDQ28	T (LVDS)*	
G1	NC	-			PL24B	7	LDQ28	C (LVDS)*	
L9	NC	-			PL25A	7	LDQ28	T	
L7	NC	-			PL25B	7	LDQ28	C	
K6	NC	-			PL26A	7	LDQ28	T (LVDS)*	
K5	NC	-			PL26B	7	LDQ28	C (LVDS)*	
L8	NC	-			PL27A	7	LDQ28	T	
L6	NC	-			PL27B	7	LDQ28	C	
-	-	-			GNDIO7	-			
H3	PL18A	7		T (LVDS)*	PL28A	7	LDQS28	T (LVDS)*	
H2	PL18B	7		C (LVDS)*	PL28B	7	LDQ28	C (LVDS)*	
N8	PL19A	7		T	PL29A	7	LDQ28	T	
M9	PL19B	7		C	PL29B	7	LDQ28	C	
J3	PL20A	7		T (LVDS)*	PL30A	7	LDQ28	T (LVDS)*	
VCCIO	VCCIO7	7			-	-			
J2	PL20B	7		C (LVDS)*	PL30B	7	LDQ28	C (LVDS)*	
H1	PL21A	7		T	PL31A	7	LDQ28	T	
GNDIO	GNDIO7	-			GNDIO7	-			
J1	PL21B	7		C	PL31B	7	LDQ28	C	
-	-	-			-	-			
-	-	-			-	-			

LFE2M50E/SE and LFE2M70E/SE Logic Signal Connections: 900 fpBGA (Cont.)

LFE2M50E/SE					LFE2M70E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential	
AA6	NC	-			PL79B	6	LDQ82	C	
AB4	NC	-			PL80A	6	LDQ82	T (LVDS)*	
-	-	-			VCCIO6	6			
AB5	NC	-			PL80B	6	LDQ82	C (LVDS)*	
AA8	NC	-			PL81A	6	LDQ82	T	
AA9	NC	-			PL81B	6	LDQ82	C	
AC1	PL62A	6	LLM0_GPLLT_IN_A**	T (LVDS)*	PL82A	6	LLM0_GPLLT_IN_A**/LDQS82	T (LVDS)*	
GNDIO	GNDIO6	-			GNDIO6	-			
AC2	PL62B	6	LLM0_GPLLC_IN_A**	C (LVDS)*	PL82B	6	LLM0_GPLLC_IN_A**/LDQ82	C (LVDS)*	
AC4	PL63A	6	LLM0_GPLLT_FB_A	T	PL83A	6	LLM0_GPLLT_FB_A/LDQ82	T	
AC3	PL63B	6	LLM0_GPLLC_FB_A	C	PL83B	6	LLM0_GPLLC_FB_A/LDQ82	C	
VCCIO	VCCIO6	6			VCCIO6	6			
AC7	PL64A	6	LLM0_GDLLT_IN_A**	T (LVDS)*	PL84A	6	LLM0_GDLLT_IN_A**/LDQ82	T (LVDS)*	
AC6	PL64B	6	LLM0_GDLLC_IN_A**	C (LVDS)*	PL84B	6	LLM0_GDLLC_IN_A**/LDQ82	C (LVDS)*	
AC5	PL65A	6	LLM0_GDLLT_FB_A	T	PL85A	6	LLM0_GDLLT_FB_A/LDQ82	T	
AD3	PL65B	6	LLM0_GDLLC_FB_A	C	PL85B	6	LLM0_GDLLC_FB_A/LDQ82	C	
GNDIO	GNDIO6	-			GNDIO6	-			
AB8	LLM0_PLLCAP	6			LLM0_PLLCAP	6			
AD2	PL67A	6	LDQ71	T (LVDS)*	PL87A	6		T	
AD1	PL67B	6	LDQ71	C (LVDS)*	PL87B	6		C	
AE2	TCK	-			TCK	-			
AE1	TDI	-			TDI	-			
AF2	TMS	-			TMS	-			
AF1	TDO	-			TDO	-			
AG1	VCCJ	-			VCCJ	-			
AH1	VCC	-			LLC_SQ_VCCR3	14			
AK2	PB11A	5	BDQ15	T	LLC_SQ_HDINP3	14		T	
AJ1	NC	-			LLC_SQ_VCCIB3	14			
AJ2	PB11B	5	BDQ15	C	LLC_SQ_HDINN3	14		C	
AH4	VCC	-			LLC_SQ_VCCTX3	14			
AK5	PB13A	5	BDQ15	T	LLC_SQ_HDOUTP3	14		T	
AK4	NC	-			LLC_SQ_VCCOB3	14			
AJ5	PB13B	5	BDQ15	C	LLC_SQ_HDOUTN3	14		C	
AH5	VCC	-			LLC_SQ_VCCTX2	14			
AJ6	PB14B	5	BDQ15	C	LLC_SQ_HDOUTN2	14		C	
AH6	NC	-			LLC_SQ_VCCOB2	14			
AK6	PB14A	5	BDQ15	T	LLC_SQ_HDOUTP2	14		T	
AH2	VCC	-			LLC_SQ_VCCR2	14			
AJ3	PB12B	5	BDQ15	C	LLC_SQ_HDINN2	14		C	
AH3	NC	-			LLC_SQ_VCCIB2	14			
AK3	PB12A	5	BDQ15	T	LLC_SQ_HDINP2	14		T	
AH7	VCC	-			LLC_SQ_VCCP	14			
AG7	PB15A	5	BDQS15	T	LLC_SQ_REFCLKP	14		T	
AF7	PB15B	5	BDQ15	C	LLC_SQ_REFCLKN	14		C	
AJ7	VCCAUX	-			LLC_SQ_VCCAUX33	14			
AK11	PB18A	5	BDQ15	T	LLC_SQ_HDINP1	14		T	
AH11	NC	-			LLC_SQ_VCCIB1	14			
AJ11	PB18B	5	BDQ15	C	LLC_SQ_HDINN1	14		C	

LFE2M50E/SE and LFE2M70E/SE Logic Signal Connections: 900 fpBGA (Cont.)

LFE2M50E/SE					LFE2M70E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential	
L13	VCC	-			VCC	-			
L18	VCC	-			VCC	-			
L19	VCC	-			VCC	-			
M11	VCC	-			VCC	-			
M12	VCC	-			VCC	-			
M13	VCC	-			VCC	-			
M14	VCC	-			VCC	-			
M15	VCC	-			VCC	-			
M16	VCC	-			VCC	-			
M17	VCC	-			VCC	-			
M18	VCC	-			VCC	-			
M19	VCC	-			VCC	-			
M20	VCC	-			VCC	-			
N11	VCC	-			VCC	-			
N12	VCC	-			VCC	-			
N19	VCC	-			VCC	-			
N20	VCC	-			VCC	-			
P12	VCC	-			VCC	-			
P19	VCC	-			VCC	-			
R12	VCC	-			VCC	-			
R19	VCC	-			VCC	-			
T12	VCC	-			VCC	-			
T19	VCC	-			VCC	-			
U12	VCC	-			VCC	-			
U19	VCC	-			VCC	-			
V11	VCC	-			VCC	-			
V12	VCC	-			VCC	-			
V19	VCC	-			VCC	-			
V20	VCC	-			VCC	-			
W11	VCC	-			VCC	-			
W12	VCC	-			VCC	-			
W13	VCC	-			VCC	-			
W14	VCC	-			VCC	-			
W15	VCC	-			VCC	-			
W16	VCC	-			VCC	-			
W17	VCC	-			VCC	-			
W18	VCC	-			VCC	-			
W19	VCC	-			VCC	-			
W20	VCC	-			VCC	-			
Y12	VCC	-			VCC	-			
Y13	VCC	-			VCC	-			
Y18	VCC	-			VCC	-			
Y19	VCC	-			VCC	-			
D14	VCCIO0	0			VCCIO0	0			
E6	VCCIO0	0			VCCIO0	0			
E9	VCCIO0	0			VCCIO0	0			
F12	VCCIO0	0			VCCIO0	0			
K12	VCCIO0	0			VCCIO0	0			

LFE2M50E/SE and LFE2M70E/SE Logic Signal Connections: 900 fpBGA (Cont.)

LFE2M50E/SE					LFE2M70E/SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
Y15	GND	-			GND	-		
Y16	GND	-			GND	-		
Y17	GND	-			GND	-		
AA26	NC	-			NC	-		
AB10	PL73B	6	LDQ71	C (LVDS)*	NC	-		
AB11	NC	-			NC	-		
AB12	NC	-			NC	-		
AB13	NC	-			NC	-		
AB14	NC	-			NC	-		
AB15	NC	-			NC	-		
AB16	NC	-			NC	-		
AB17	NC	-			NC	-		
AB19	NC	-			NC	-		
AB20	NC	-			NC	-		
AB21	NC	-			NC	-		
AB9	PL73A	6	LDQ71	T (LVDS)*	NC	-		
AC10	PL74B	6	LDQ71	C	NC	-		
AC11	NC	-			NC	-		
AC21	NC	-			NC	-		
AC22	NC	-			NC	-		
AC8	PL70B	6	LDQ71	C	NC	-		
AC9	PL74A	6	LDQ71	T	NC	-		
AD21	NC	-			NC	-		
AD22	NC	-			NC	-		
AD4	PL68A	6	LDQ71	T	NC	-		
AD5	PL68B	6	LDQ71	C	NC	-		
AD6	PL71A	6	LDQS71	T (LVDS)*	NC	-		
AD7	PL72A	6	LDQ71	T	NC	-		
AD8	PL72B	6	LDQ71	C	NC	-		
AE23	NC	-			NC	-		
AE5	PL69A	6	LDQ71	T (LVDS)*	NC	-		
AE6	PL70A	6	LDQ71	T	NC	-		
AE7	PL71B	6	LDQ71	C (LVDS)*	NC	-		
AF20	NC	-			NC	-		
AF23	NC	-			NC	-		
AF5	PL69B	6	LDQ71	C (LVDS)*	NC	-		
AG23	NC	-			NC	-		
AG26	NC	-			NC	-		
D10	PT10A	0		T	NC	-		
E10	PT9B	0		C	NC	-		
E11	PT10B	0		C	NC	-		
F10	PT9A	0		T	NC	-		
F20	NC	-			NC	-		
F23	NC	-			NC	-		
F8	PL6B	7	LDQ6	C (LVDS)*	NC	-		
G10	NC	-			NC	-		
G20	NC	-			NC	-		
G21	NC	-			NC	-		

LFE2M100E/SE Logic Signal Connections: 900 fpBGA (Cont.)

LFE2M100E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential
C29	URC_SQ_VCCR1	12		
B28	URC_SQ_HDINN1	12		C
C28	URC_SQ_VCCIB1	12		
A28	URC_SQ_HDINP1	12		T
B24	URC_SQ_VCCAUX33	12		
E24	URC_SQ_REFCLKN	12		C
D24	URC_SQ_REFCLKP	12		T
C24	URC_SQ_VCCP	12		
A20	URC_SQ_HDINP2	12		T
C20	URC_SQ_VCCIB2	12		
B20	URC_SQ_HDINN2	12		C
C19	URC_SQ_VCCR2	12		
A23	URC_SQ_HDOUTP2	12		T
C23	URC_SQ_VCCOB2	12		
B23	URC_SQ_HDOUTN2	12		C
C22	URC_SQ_VCCTX2	12		
B22	URC_SQ_HDOUTN3	12		C
A21	URC_SQ_VCCOB3	12		
A22	URC_SQ_HDOUTP3	12		T
C21	URC_SQ_VCCTX3	12		
B19	URC_SQ_HDINN3	12		C
B18	URC_SQ_VCCIB3	12		
A19	URC_SQ_HDINP3	12		T
C18	URC_SQ_VCCR3	12		
D23	PT100B	1		C
GNDIO	GNDIO1	-		
E21	PT100A	1		T
D26	PT99B	1		C
E26	PT99A	1		T
E23	PT98B	1		C
VCCIO	VCCIO1	1		
G22	PT98A	1		T
-	-	-		
D22	PT97B	1		C
F21	PT97A	1		T
G18	PT96B	1		C
H18	PT96A	1		T
D20	PT95B	1		C
GNDIO	GNDIO1	-		
D21	PT95A	1		T
E20	PT94B	1		C
VCCIO	VCCIO1	1		
E19	PT94A	1		T

LFE2M100E/SE Logic Signal Connections: 900 fpBGA (Cont.)

LFE2M100E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential
K19	VCCIO1	1		
F28	VCCIO2	2		
J25	VCCIO2	2		
K28	VCCIO2	2		
M21	VCCIO2	2		
M24	VCCIO2	2		
N21	VCCIO2	2		
N28	VCCIO2	2		
P21	VCCIO2	2		
R25	VCCIO2	2		
AA28	VCCIO3	3		
AB25	VCCIO3	3		
AE28	VCCIO3	3		
T25	VCCIO3	3		
U21	VCCIO3	3		
V21	VCCIO3	3		
V28	VCCIO3	3		
W21	VCCIO3	3		
W24	VCCIO3	3		
AA18	VCCIO4	4		
AA19	VCCIO4	4		
AE19	VCCIO4	4		
AF22	VCCIO4	4		
AG17	VCCIO4	4		
AG25	VCCIO4	4		
AA12	VCCIO5	5		
AA13	VCCIO5	5		
AE12	VCCIO5	5		
AF9	VCCIO5	5		
AG14	VCCIO5	5		
AG6	VCCIO5	5		
AA3	VCCIO6	6		
AB6	VCCIO6	6		
AE3	VCCIO6	6		
T6	VCCIO6	6		
U10	VCCIO6	6		
V10	VCCIO6	6		
V3	VCCIO6	6		
W10	VCCIO6	6		
W7	VCCIO6	6		
F3	VCCIO7	7		
J6	VCCIO7	7		
K3	VCCIO7	7		

LFE2M100E/SE Logic Signal Connections: 900 fpBGA (Cont.)

LFE2M100E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential
AE23	NC	-		
AE5	NC	-		
AE6	NC	-		
AE7	NC	-		
AF20	NC	-		
AF23	NC	-		
AF5	NC	-		
AG23	NC	-		
AG26	NC	-		
D10	NC	-		
E10	NC	-		
E11	NC	-		
F10	NC	-		
F20	NC	-		
F23	NC	-		
F8	NC	-		
G10	NC	-		
G20	NC	-		
G21	NC	-		
G7	NC	-		
G8	NC	-		
G9	NC	-		
H19	NC	-		
H20	NC	-		
H21	NC	-		
H22	NC	-		
H6	NC	-		
H8	NC	-		
H9	NC	-		
J10	NC	-		
J20	NC	-		
J21	NC	-		
J9	NC	-		
K9	NC	-		
R9	NC	-		
U22	NC	-		
W9	NC	-		
N13	VCCPLL	-		
N18	VCCPLL	-		
V13	VCCPLL	-		

LFE2M70E/SE and LFE2M100E/SE Logic Signal Connections: 1152 fpBGA (Cont.)

LFE2M70E/SE				LFE2M100E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
AL8	LLC_SQ_VCCIB1	14			LLC_SQ_VCCIB1	14		
AM7	LLC_SQ_HDINN1	14		C	LLC_SQ_HDINN1	14		C
AN6	LLC_SQ_VCCRX1	14			LLC_SQ_VCCRX1	14		
AP6	LLC_SQ_HDOUTP1	14		T	LLC_SQ_HDOUTP1	14		T
AK7	LLC_SQ_VCCOB1	14			LLC_SQ_VCCOB1	14		
AP7	LLC_SQ_HDOUTN1	14		C	LLC_SQ_HDOUTN1	14		C
AN7	LLC_SQ_VCCTX1	14			LLC_SQ_VCCTX1	14		
AP8	LLC_SQ_HDOUTN0	14		C	LLC_SQ_HDOUTN0	14		C
AL9	LLC_SQ_VCCOB0	14			LLC_SQ_VCCOB0	14		
AP9	LLC_SQ_HDOUTP0	14		T	LLC_SQ_HDOUTP0	14		T
AN8	LLC_SQ_VCCTX0	14			LLC_SQ_VCCTX0	14		
AM8	LLC_SQ_HDINN0	14		C	LLC_SQ_HDINN0	14		C
AN9	LLC_SQ_VCCIB0	14			LLC_SQ_VCCIB0	14		
AM9	LLC_SQ_HDINP0	14		T	LLC_SQ_HDINP0	14		T
AL7	LLC_SQ_VCCRX0	14			LLC_SQ_VCCRX0	14		
-	-	-			VCCIO5	5		
AJ12	NC	-			PB32A	5	BDQ33	T
AH12	NC	-			PB32B	5	BDQ33	C
-	-	-			GNDIO5	-		
-	-	-			VCCIO5	5		
AL13	NC	-			PB36A	5	BDQ33	T
AK13	NC	-			PB36B	5	BDQ33	C
-	-	-			GNDIO5	-		
AE14	NC	-			PB38A	5	BDQ42	T
AG13	NC	-			PB38B	5	BDQ42	C
AN14	PB30A	5	BDQ33	T	PB39A	5	BDQ42	T
AP14	PB30B	5	BDQ33	C	PB39B	5	BDQ42	C
AH14	PB31A	5	BDQ33	T	PB40A	5	BDQ42	T
AJ15	PB31B	5	BDQ33	C	PB40B	5	BDQ42	C
VCCIO	VCCIO5	5			VCCIO5	5		
GNDIO	GNDIO5	-			GNDIO5	-		
AL14	PB33A	5	BDQS33	T	PB42A	5	BDQS42	T
AM14	PB33B	5	BDQ33	C	PB42B	5	BDQ42	C
AF14	PB35A	5	BDQ33	T	PB44A	5	BDQ42	T
AF13	PB35B	5	BDQ33	C	PB44B	5	BDQ42	C
VCCIO	VCCIO5	5			VCCIO5	5		
AE15	PB36A	5	BDQ33	T	PB45A	5	BDQ42	T
AG14	PB36B	5	BDQ33	C	PB45B	5	BDQ42	C
AH15	PB37A	5	BDQ33	T	PB46A	5	BDQ42	T
AK15	PB37B	5	BDQ33	C	PB46B	5	BDQ42	C
GNDIO	GNDIO5	-			GNDIO5	-		
AL15	PB38A	5	BDQ42	T	PB47A	5	BDQ51	T
AM15	PB38B	5	BDQ42	C	PB47B	5	BDQ51	C
AK16	PB39A	5	BDQ42	T	PB48A	5	BDQ51	T
AJ16	PB39B	5	BDQ42	C	PB48B	5	BDQ51	C
AN15	PB40A	5	BDQ42	T	PB49A	5	BDQ51	T
VCCIO	VCCIO5	5			VCCIO5	5		
AP15	PB40B	5	BDQ42	C	PB49B	5	BDQ51	C
AG15	PB42A	5	BDQS42	T	PB51A	5	BDQS51	T

LFE2M70E/SE and LFE2M100E/SE Logic Signal Connections: 1152 fpBGA (Cont.)

LFE2M70E/SE				LFE2M100E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
AA25	PR74B	3	RDQ73	C	PR82B	3	RDQ81	C
VCCIO	VCCIO3	3			VCCIO3	3		
AC24	PR74A	3	RDQ73	T	PR82A	3	RDQ81	T
AC33	PR73B	3	RDQ73	C (LVDS)*	PR81B	3	RDQ81	C (LVDS)*
AC34	PR73A	3	RDQS73	T (LVDS)*	PR81A	3	RDQS81	T (LVDS)*
GNDIO	GNDIO3	-			GNDIO3	-		
AB24	PR72B	3	RDQ73	C	PR80B	3	RDQ81	C
Y26	PR72A	3	RDQ73	T	PR80A	3	RDQ81	T
AB33	PR71B	3	RDQ73	C (LVDS)*	PR79B	3	RDQ81	C (LVDS)*
AB34	PR71A	3	RDQ73	T (LVDS)*	PR79A	3	RDQ81	T (LVDS)*
VCCIO	VCCIO3	3			VCCIO3	3		
Y27	PR70B	3	RDQ73	C	PR78B	3	RDQ81	C
AB29	PR70A	3	RDQ73	T	PR78A	3	RDQ81	T
AA34	PR69B	3	RDQ73	C (LVDS)*	PR77B	3	RDQ81	C (LVDS)*
AA33	PR69A	3	RDQ73	T (LVDS)*	PR77A	3	RDQ81	T (LVDS)*
AA31	PR67B	3	RDQ64	C	PR75B	3	RDQ72	C
AA32	PR67A	3	RDQ64	T	PR75A	3	RDQ72	T
GNDIO	GNDIO3	-			GNDIO3	-		
AA28	PR66B	3	RDQ64	C (LVDS)*	PR74B	3	RDQ72	C (LVDS)*
AA29	PR66A	3	RDQ64	T (LVDS)*	PR74A	3	RDQ72	T (LVDS)*
AA30	PR65B	3	RDQ64	C	PR73B	3	RDQ72	C
AB30	PR65A	3	RDQ64	T	PR73A	3	RDQ72	T
VCCIO	VCCIO3	3			VCCIO3	3		
Y28	PR64B	3	RDQ64	C (LVDS)*	PR72B	3	RDQ72	C (LVDS)*
Y29	PR64A	3	RDQS64	T (LVDS)*	PR72A	3	RDQS72	T (LVDS)*
AA24	PR63B	3	RDQ64	C	PR71B	3	RDQ72	C
GNDIO	GNDIO3	-			GNDIO3	-		
Y25	PR63A	3	RDQ64	T	PR71A	3	RDQ72	T
Y31	PR62B	3	RDQ64	C (LVDS)*	PR70B	3	RDQ72	C (LVDS)*
Y30	PR62A	3	RDQ64	T (LVDS)*	PR70A	3	RDQ72	T (LVDS)*
Y24	PR61B	3	RDQ64	C	PR69B	3	RDQ72	C
VCCIO	VCCIO3	3			VCCIO3	3		
W25	PR61A	3	RDQ64	T	PR69A	3	RDQ72	T
Y33	PR60B	3	RDQ64	C (LVDS)*	PR68B	3	RDQ72	C (LVDS)*
Y34	PR60A	3	RDQ64	T (LVDS)*	PR68A	3	RDQ72	T (LVDS)*
W28	PR58B	3	RLM3_SPLLC_FB_A/RDQ55	C	PR66B	3	RLM4_SPLLC_FB_A/RDQ63	C
GNDIO	GNDIO3	-			GNDIO3	-		
V26	PR58A	3	RLM3_SPLLT_FB_A/RDQ55	T	PR66A	3	RLM4_SPLLT_FB_A/RDQ63	T
V28	PR57B	3	RLM3_SPLLC_IN_A/RDQ55	C (LVDS)*	PR65B	3	RLM4_SPLLC_IN_A/RDQ63	C (LVDS)*
V27	PR57A	3	RLM3_SPLLT_IN_A/RDQ55	T (LVDS)*	PR65A	3	RLM4_SPLLT_IN_A/RDQ63	T (LVDS)*
V25	PR56B	3	RDQ55	C	PR64B	3	RDQ63	C
VCCIO	VCCIO3	3			VCCIO3	3		
W24	PR56A	3	RDQ55	T	PR64A	3	RDQ63	T
W33	PR55B	3	RDQ55	C (LVDS)*	PR63B	3	RDQ63	C (LVDS)*
W34	PR55A	3	RDQS55	T (LVDS)*	PR63A	3	RDQS63	T (LVDS)*
GNDIO	GNDIO3	-			GNDIO3	-		
V24	PR54B	3	RDQ55	C	PR62B	3	RDQ63	C
U26	PR54A	3	RDQ55	T	PR62A	3	RDQ63	T
W29	PR53B	3	RDQ55	C (LVDS)*	PR61B	3	RDQ63	C (LVDS)*

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2-20E-5QN208I	131	1.2V	-5	Lead-Free PQFP	208	IND	20
LFE2-20E-6QN208I	131	1.2V	-6	Lead-Free PQFP	208	IND	20
LFE2-20E-5FN256I	193	1.2V	-5	Lead-Free fpBGA	256	IND	20
LFE2-20E-6FN256I	193	1.2V	-6	Lead-Free fpBGA	256	IND	20
LFE2-20E-5FN484I	331	1.2V	-5	Lead-Free fpBGA	484	IND	20
LFE2-20E-6FN484I	331	1.2V	-6	Lead-Free fpBGA	484	IND	20
LFE2-20E-5FN672I	402	1.2V	-5	Lead-Free fpBGA	672	IND	20
LFE2-20E-6FN672I	402	1.2V	-6	Lead-Free fpBGA	672	IND	20

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2-35E-5FN484I	331	1.2V	-5	Lead-Free fpBGA	484	IND	35
LFE2-35E-6FN484I	331	1.2V	-6	Lead-Free fpBGA	484	IND	35
LFE2-35E-5FN672I	450	1.2V	-5	Lead-Free fpBGA	672	IND	35
LFE2-35E-6FN672I	450	1.2V	-6	Lead-Free fpBGA	672	IND	35

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2-50E-5FN484I	339	1.2V	-5	Lead-Free fpBGA	484	IND	50
LFE2-50E-6FN484I	339	1.2V	-6	Lead-Free fpBGA	484	IND	50
LFE2-50E-5FN672I	500	1.2V	-5	Lead-Free fpBGA	672	IND	50
LFE2-50E-6FN672I	500	1.2V	-6	Lead-Free fpBGA	672	IND	50

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2-70E-5FN672I	500	1.2V	-5	Lead-Free fpBGA	672	IND	70
LFE2-70E-6FN672I	500	1.2V	-6	Lead-Free fpBGA	672	IND	70
LFE2-70E-5FN900I	583	1.2V	-5	Lead-Free fpBGA	900	IND	70
LFE2-70E-6FN900I	583	1.2V	-6	Lead-Free fpBGA	900	IND	70

Industrial

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2M20E-5F484I	304	1.2V	-5	fpBGA	484	IND	20
LFE2M20E-6F484I	304	1.2V	-6	fpBGA	484	IND	20
LFE2M20E-5F256I	140	1.2V	-5	fpBGA	256	IND	20
LFE2M20E-6F256I	140	1.2V	-6	fpBGA	256	IND	20

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2M35E-5F672I	410	1.2V	-5	fpBGA	672	IND	35
LFE2M35E-6F672I	410	1.2V	-6	fpBGA	672	IND	35
LFE2M35E-5F484I	303	1.2V	-5	fpBGA	484	IND	35
LFE2M35E-6F484I	303	1.2V	-6	fpBGA	484	IND	35
LFE2M35E-5F256I	140	1.2V	-5	fpBGA	256	IND	35
LFE2M35E-6F256I	140	1.2V	-6	fpBGA	256	IND	35

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2M50E-5F900I	410	1.2V	-5	fpBGA	900	IND	50
LFE2M50E-6F900I	410	1.2V	-6	fpBGA	900	IND	50
LFE2M50E-5F672I	372	1.2V	-5	fpBGA	672	IND	50
LFE2M50E-6F672I	372	1.2V	-6	fpBGA	672	IND	50
LFE2M50E-5F484I	270	1.2V	-5	fpBGA	484	IND	50
LFE2M50E-6F484I	270	1.2V	-6	fpBGA	484	IND	50

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2M70E-5F1152I	436	1.2V	-5	fpBGA	1152	IND	70
LFE2M70E-6F1152I	436	1.2V	-6	fpBGA	1152	IND	70
LFE2M70E-5F900I	416	1.2V	-5	fpBGA	900	IND	70
LFE2M70E-6F900I	416	1.2V	-6	fpBGA	900	IND	70

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2M100E-5F1152I	520	1.2V	-5	fpBGA	1152	IND	100
LFE2M100E-6F1152I	520	1.2V	-6	fpBGA	1152	IND	100
LFE2M100E-5F900I	416	1.2V	-5	fpBGA	900	IND	100
LFE2M100E-6F900I	416	1.2V	-6	fpBGA	900	IND	100



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For Further Information

A variety of technical notes for the LatticeECP2/M family are available on the Lattice web site at www.latticesemi.com.

- TN1102, [LatticeECP2/M sysIO Usage Guide](#)
- TN1103, [LatticeECP2/M sysCLOCK PLL Design and Usage Guide](#)
- TN1104, [LatticeECP2/M Memory Usage Guide](#)
- TN1105, [LatticeECP2/M High-Speed I/O Interface](#)
- TN1106, [Power Estimation and Management for LatticeECP2/M Devices](#)
- TN1107, [LatticeECP2/M sysDSP Usage Guide](#)
- TN1108, [LatticeECP2/M sysCONFIG Usage Guide](#)
- TN1109, [LatticeECP2/M Configuration Encryption Usage Guide](#)
- TN1113, [LatticeECP2/M Soft Error Detection \(SED\) Usage Guide](#)
- TN1124, [LatticeECP2M SERDES/PCS Usage Guide](#)
- TN1162, [LatticeECP2/M Hardware Checklist](#)

For further information about interface standards refer to the following web sites:

- JEDEC Standards (LVTTTL, LVCMOS, SSTL, HSTL): www.jedec.org
- PCI: www.pcisig.com



LatticeECP2/M Family Data Sheet

Revision History

September 2013

Data Sheet DS1006

Date	Version	Section	Change Summary
February 2006	01.0	—	Initial release.
August 2006	01.1	Introduction	
			Updated Table 1-1 "LatticeECP2 Family Selection Guide".
		Architecture	Updated Figure 2-2 "PFU Diagram".
			Updated Figure 2-13 "Secondary Clock Regions ECP2-50".
			Updated Figure 2-25 "PIC Diagram".
			Updated Figure 2-26 "Input Register Block for Left, Right and Bottom Edges".
			Updated Figure 2-28 "Output Register Block for Left, Right and Bottom Edges".
			Updated Figure 2-30 "DQS Input Routing for Left and Right Edges".
			Updated Figure 2-32 "Edge Clock, DLL Calibration and DQS Local Bus Distribution".
			Table 2-15 Selectable Master Clock (CCLK) Frequencies - Removed frequencies 15, 20, 21, 22, 23, 30, 34, 41, 45, 51, 55, 60.
			Replaced "CLKINDEL" with "CLKO".
			Updated SED section.
			Qualified device migration capability when using DQS banks for DDR interfaces.
		DC and Switching Characteristics	Added VCCPLL to the Recommended Operating Conditions table.
			Removed note 5 from "Hot Specifications" section.
			Added notes 7 and 8 to "Initialization Supply" Current table.
			Change note 6 - "...down to 95MHz" to "...down to 95MHz for DDR and 133MHz for DDR2" .
			New "Typical Building Block Function Performance" numbers.
			New External Switching Characteristics numbers.
			New Internal Switching Characteristics numbers.
			New Family Timing Adders numbers.
			Updated Timings for GPLLs, SPLLs and DLLs.
			Added sysCONFIG waveforms.
			Remove HSTL15D_II from sysIO Recommended Operating Conditions table.
			Updated Supply and Initialization Currents for ECP2-50.
		Pinout Information	Added VCCPLL to the Signal Descriptions table.
			Updated Logic Signal Connections tables to include 484-fpBGA for the ECP2-50.
			Added Logic Signal Connections tables for ECP2-12 devices.
			Updated Pin Information Summary table to include ECP2-12.
			Updated Power Supply and NC Connections table to include ECP2-12.
			Added note 2 to DDR Strobe (DQS) Pin table.
			Added Information on: PCI, DDR & SPI4.2 Capabilities of the device-Package combination.

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Date	Version	Section	Change Summary
November 2009 (cont.)	03.5 (cont.)	Pinout Information (cont.)	LatticeECP2M Pin Information Summary, LFE2M50, LFE2M70 and LFE2M100 table - corrected values for LFE2M50, 672 fpBGA in Available DDR-Interfaces per I/O Bank.
			Minor corrections in LFE2M20E/SE and LFE2M35E/SE Logic Signal Connections: 484 fpBGA table.
			Minor corrections in LFE2M50E/SE and LFE2M70E/SE Logic Signal Connections: 900 fpBGA table.
			Minor corrections in LFE2M100E/SE Logic Signal Connections: 900 fpBGA table.
			Updated LFE2-6E/SE and LFE2-12E/SE Logical Signal Connections (changed D1/SPIDS to D1).
		Ordering Information	Updated LatticeECP2M Part Number Description diagram.
March 2010	03.6	DC and Switching Characteristics	Footnote for SED operating frequency added to the sysCONFIG Port Timing Specifications table.
		Pinout Information	Changed Dual Function pin E7 to be D7/SPDI0 in Logic Signal Connections tables. Changed footnote (***) in Logic Signal Connections table.
July 2010	03.7	Architecture	Updated the Typical sysIO Behavior During Power-up text section.
		Pinout Information	Added reference to powerup information.
			Corrected reference to footnote for pins 131 and 132 for the LFE-20E/SE, 208 PQFP.
			Referenced footnote (***) for all D7/SPID0.
			Changed D7*** to D7/SPID0.
			Corrected *** footnote.
		All Sections	Included references to Lattice Diamond design software wherever ispLEVER and ispLeverCORE is specified.
April 2011	03.8	DC and Switching Characteristics	DC Electrical Characteristics table: - Added footnote 3 to I_{IH} - Added footnote 2 to I_{IL} , I_{IH} - Updated C1 and C2 typ. and max. data.
			DLL Timing table – Removed line for t_R and t_F
			LatticeECP2/M sysCONFIG Port Timing Specifications table – added footnote to t_{DINIT} .
			Figure 3-18 – Corrected label to be PRGM (not PRGMRJ).
		Pinout Information	LFE2-12E/SE and LFE-20/SE Logical Signal Connections for 208 PQFP – Corrected Dual Function information for pins 112, 114, 117, 119.
January 2012	03.9	Multiple	Removed references to ispLEVER design software.
		Architecture	Corrected information regarding SED support.
		DC and Switching Characteristics	Added reference to ESD information.
June 2013	04.0	All	Updated document with new corporate logo.
		Architecture	Architecture Overview – Added information on the state of the register on power up and after configuration.