Lattice Semiconductor Corporation - LFE2M35E-7F672C Datasheet

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

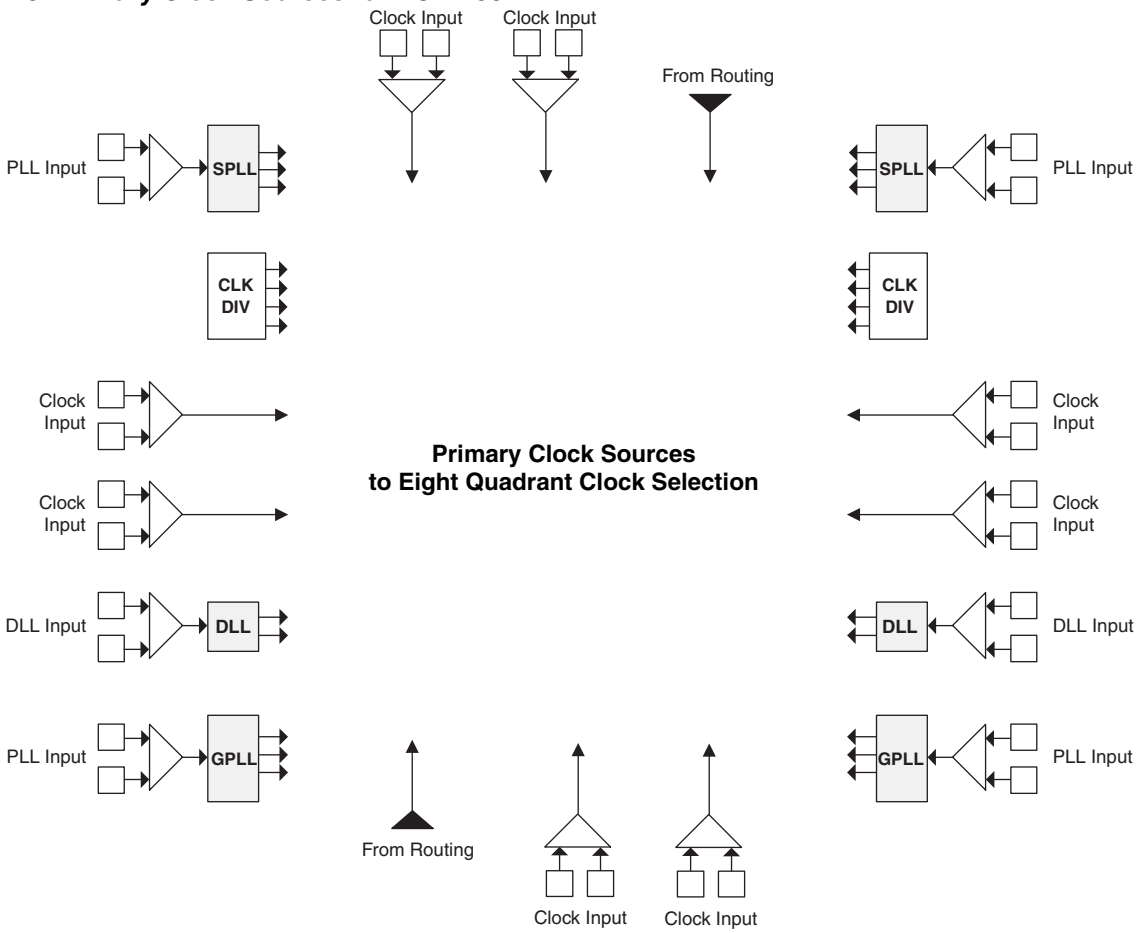
Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	4250
Number of Logic Elements/Cells	34000
Total RAM Bits	2151424
Number of I/O	410
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	672-BBGA
Supplier Device Package	672-FPBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfe2m35e-7f672c

Figure 2-10. Primary Clock Sources for ECP2-50



Note: This diagram shows sources for the ECP2-50 device. Smaller LatticeECP2 devices have fewer SPLLs. All LatticeECP2M devices have six SPLLs.

Register-to-Register Performance (Continued)

Function	-7 Timing	Units
36x36 Multiplier (All Registers)	372	MHz
18x18 Multiplier/Accumulate (Input and Output Registers)	295	MHz
18x18 Multiplier-Add/Sub-Sum (All Registers)	420	MHz
DSP IP Functions		
16-Tap Fully-Parallel FIR Filter	304	MHz
1024-pt, Radix 4, Decimation in Frequency FFT	227	MHz
8x8 Matrix Multiplier	223	MHz

Derating Timing Tables

Logic timing provided in the following sections of this data sheet and the Diamond design tool are worst case numbers in the operating range. Actual delays at nominal temperature and voltage for best case process, can be much better than the values given in the tables. The Diamond design tool can provide logic timing numbers at a particular temperature and voltage.

Figure 3-7. DDR and DDR2 Parameters

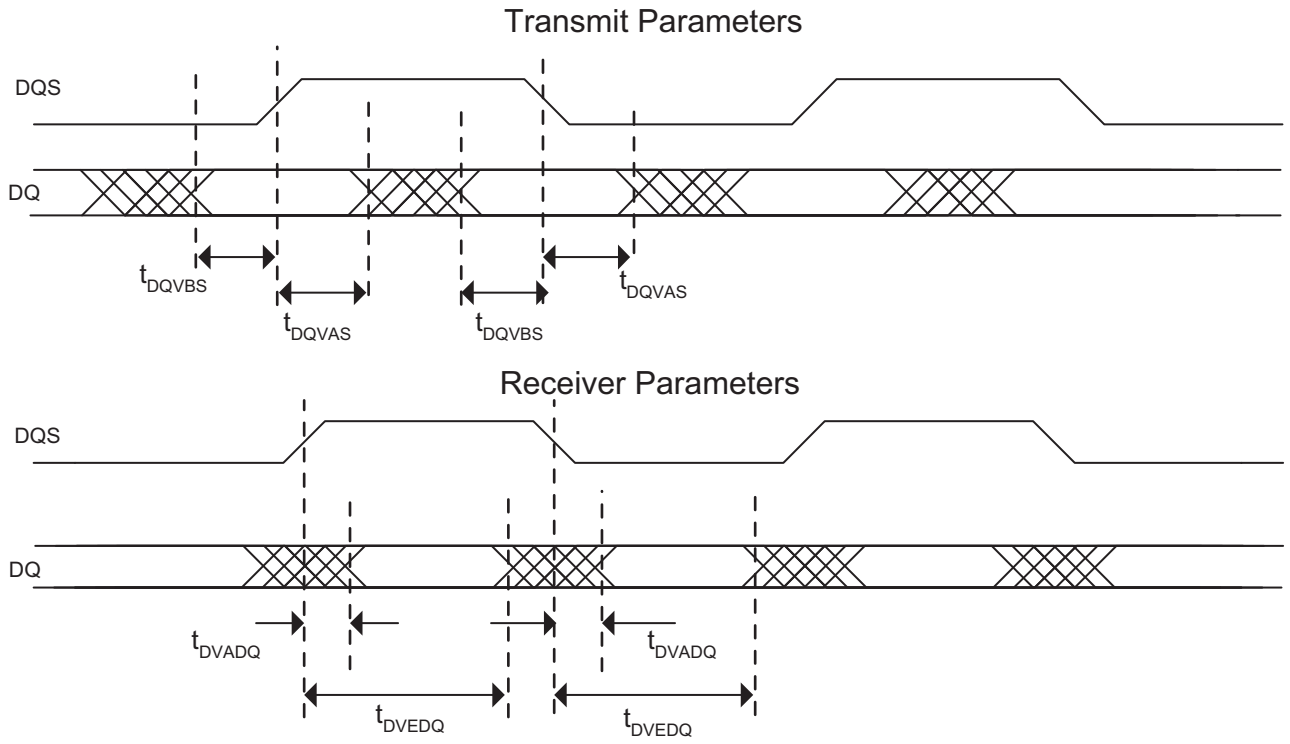
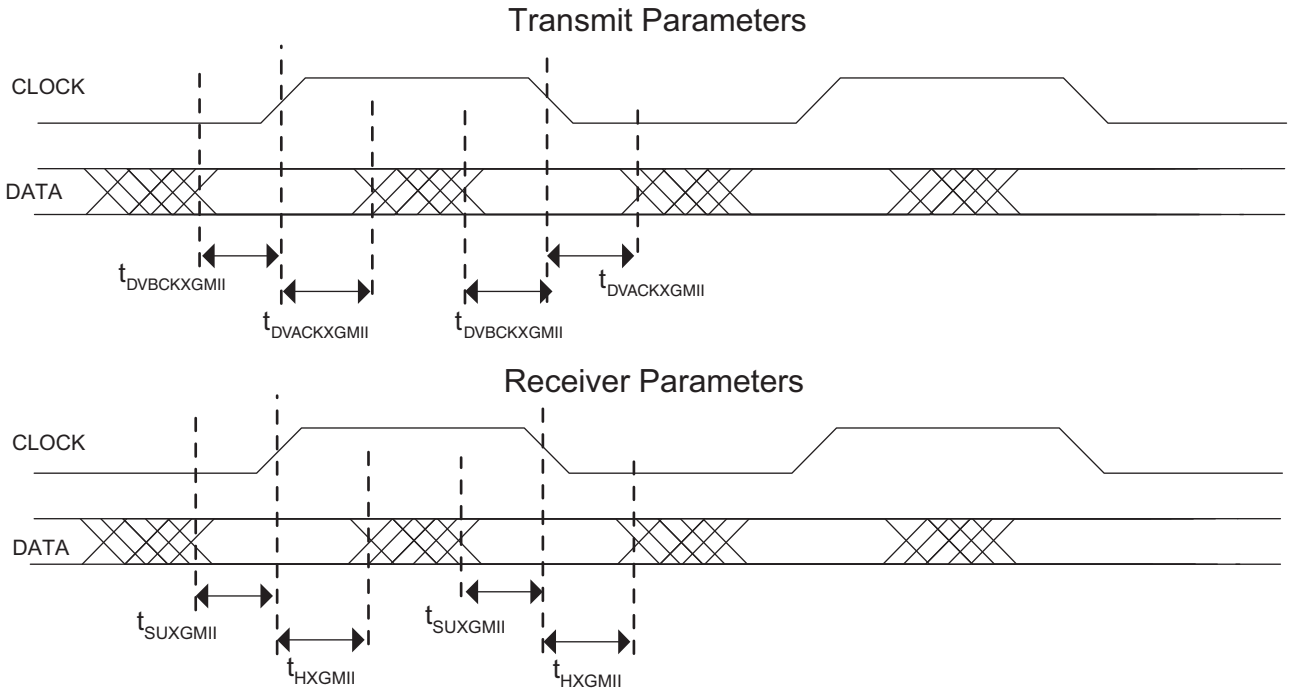


Figure 3-8. XGMII Parameters



LatticeECP2/M sysCONFIG Port Timing Specifications

Over Recommended Operating Conditions

Parameter	Description	Min.	Max.	Units
sysCONFIG Byte Data Flow				
t_{SUCBDI}	Byte D[0:7] Setup Time to CCLK	7	—	ns
t_{HCBDI}	Byte D[0:7] Hold Time to CCLK	1	—	ns
t_{CODO}	CCLK to DOUT in Flowthrough Mode	—	12	ns
t_{SUCS}	CSN[0:1] Setup Time to CCLK	7	—	ns
t_{HCS}	CSN[0:1] Hold Time to CCLK	1	—	ns
t_{SUWD}	Write Signal Setup Time to CCLK	7	—	ns
t_{HWD}	Write Signal Hold Time to CCLK	1	—	ns
t_{DCB}	CCLK to BUSY Delay Time	—	12	ns
t_{CORD}	CCLK to Out for Read Data	—	12	ns
sysCONFIG Byte Slave Clocking				
t_{BSCH}	Byte Slave CCLK Minimum High Pulse	6	—	ns
t_{BSCL}	Byte Slave CCLK Minimum Low Pulse	9	—	ns
t_{BSCYC}	Byte Slave CCLK Cycle Time	15	—	ns
sysCONFIG Serial (Bit) Data Flow				
t_{SUSCDI}	DI Setup Time to CCLK Slave Mode	7	—	ns
t_{HSCDI}	DI Hold Time to CCLK Slave Mode	1	—	ns
t_{CODO}	CCLK to DOUT in Flowthrough Mode	—	12	ns
sysCONFIG Serial Slave Clocking				
t_{SSCH}	Serial Slave CCLK Minimum High Pulse	6	—	ns
t_{SSCL}	Serial Slave CCLK Minimum Low Pulse	6	—	ns
sysCONFIG POR, Initialization and Wake-up				
t_{ICFG}	Minimum Vcc to INITN High	—	28	ms
t_{VMC}	Time from t_{ICFG} to Valid Master CCLK	—	2	us
t_{PRGMRJ}	PROGRAMN Pin Pulse Rejection	—	8	ns
t_{PRGM}	PROGRAMN Low Time to Start Configuration	25	—	ns
t_{DINIT}	PROGRAMN High to INITN High Delay[1]	—	1.5	ms
$t_{DPPINIT}$	Delay Time from PROGRAMN Low to INITN Low	—	37	ns
$t_{DPPDONE}$	Delay Time from PROGRAMN Low to DONE Low	—	37	ns
t_{IODISS}	User I/O Disable from PROGRAMN Low	—	35	ns
t_{IOENSS}	User I/O Enabled Time from CCLK Edge During Wake-up Sequence	—	25	ns
t_{MWC}	Additional Wake Master Clock Signals after DONE Pin High	120	—	cycles
sysCONFIG SPI Port[2]				
t_{CFGX}	INITN High to CCLK Low	—	1	µs
t_{CSSPI}	INITN High to CSSPIN Low	—	2	us
t_{CSCCLK}	CCLK Low before CSSPIN Low	0	—	ns
t_{SOCDO}	CCLK Low to Output Valid	—	15	ns
t_{SOE}	CSSPIN[0:1] Active Setup Time	300	—	ns
t_{CSPID}	CSSPIN[0:1] Low to First CCLK Edge Setup Time	300+3cyc	600+6cyc	ns

Signal Descriptions (Cont.)

Signal Name	I/O	Description
[LOC]_SQ_VCCIBm	—	Input buffer power supply, channel m (1.2V/1.5V). This pin should be left floating if the channel is unused.
[LOC]_SQ_VCCOBm	—	Output buffer power supply, channel m (1.2V/1.5V). This pin should be left floating if the channel is unused.
[LOC]_SQ_HDOUTNm	O	High-speed output, negative channel m
[LOC]_SQ_HDOUTPm	O	High-speed output, positive channel m
[LOC]_SQ_HDINNm	I	High-speed input, negative channel m
[LOC]_SQ_HDINPm	I	High-speed input, positive channel m
[LOC]_SQ_VCCTXm[4]	—	Transmitter power supply, channel m (1.2V). This pin must be tied to 1.2V even if the channel is unused.
[LOC]_SQ_VCCRXm[4]	—	Receiver power supply, channel m (1.2V). This pin must be tied to 1.2V even if the channel is unused.

1. These signals are relevant for LatticeECP2M family.
2. m defines the associated channel in the Quad.
3. These signals are defined in Quads [LOC] indicates the corner SERDES Quad is located: ULC (upper left), URC (upper right), LLC (lower left), LRC (lower right).
4. When placing switching I/Os around these critical pins that are designed to supply the device with the proper reference or supply voltage, care must be given. For more information, refer to TN1159, LatticeECP2/M Pin Assignment Recommendations.
5. There may be SPLLs that do not have dedicated I/Os.

LatticeECP2M Power Supply and NC (Cont.)

Signal	672 fpBGA	900 fpBGA
GND[1]	A13, A19, A2, A25, AA2, AA25, AB18, AB22, AB5, AB9, AE1, AE11, AE16, AE22, AE26, AE6, AF13, AF19, AF2, AF25, B1, B11, B16, B22, B26, B6, E18, E22, E5, E9, F2, F25, G11, G16, J22, J5, K11, K13, K14, K16, L10, L11, L16, L17, L2, L20, L25, L7, M13, M14, N10, N12, N13, N14, N15, N17, P10, P12, P13, P14, P15, P17, R13, R14, T10, T11, T16, T17, T2, T20, T25, T7, U11, U13, U14, U16, V22, V5, Y11, Y16	**LFE2M50:** A1, A13, A18, A24, A30, A7, AA14, AA15, AA16, AA17, AA24, AA27, AA4, AB24, AB7, AD12, AD19, AD27, AE22, AE27, AE4, AE9, AF14, AF17, AF25, AF6, AJ10, AJ21, AJ27, AJ4, AK1, AK13, AK18, AK24, AK30, AK7, B10, B21, B27, B4, D25, D6, E14, E17, F22, F27, F4, F9, G12, G19, J24, J7, K14, K15, K16, K17, K27, K4, L14, L15, L16, L17, M23, M8, N14, N15, N16, N17, N27, N4, P11, P13, P14, P15, P16, P17, P18, P20, R10, R11, R13, R14, R15, R16, R17, R18, R20, R21, R24, R7, T10, T11, T13, T14, T15, T16, T17, T18, T20, T21, T24, T7, U11, U13, U14, U15, U16, U17, U18, U20, V14, V15, V16, V17, V27, V4, W23, W8, Y14, Y15, Y16, Y17 **LFE2M70/LFE2M100:** A1, A13, A18, A24, A30, A7, AA14, AA15, AA16, AA17, AA24, AA27, AA4, AB24, AB7, AD12, AD19, AD27, AE22, AE27, AE4, AE9, AF14, AF17, AF25, AF6, AJ10, AJ21, AJ27, AJ4, AK1, AK13, AK18, AK24, AK30, AK7, B10, B21, B27, B4, D25, D6, E14, E17, F22, F27, F4, F9, G12, G19, J24, J7, K14, K15, K16, K17, K27, K4, L14, L15, L16, L17, M23, M8, N14, N15, N16, N17, N27, N4, P11, P13, P14, P15, P16, P17, P18, P20, R10, R11, R13, R14, R15, R16, R17, R18, R20, R21, R24, R7, T10, T11, T13, T14, T15, T16, T17, T18, T20, T21, T24, T7, U11, U13, U14, U15, U16, U17, U18, U20, V14, V15, V16, V17, V27, V4, W23, W8, Y14, Y15, Y16, Y17
NC[2]	**LFE2M35:** AB3, AB4, AC1, AC2, AD15, AD18, AD20, AD23, AE13, AE25, AF16, AF22, B4, B5, C26, D20, D21, D22, D23, D24, D25, D26, E20, E21, E25, E26, F20, G20, K10, K17, R4, U10, U23, V10, W7, N7, V7 **LFE2M50:** AB3, AB4, AC1, AC2, B4, B5, C26, D20, D21, D22, D23, D24, D25, D26, E20, E21, E25, E26, F20, G20, K10, K17, R4, U10, U23, V10, W7, AB21, AC20, AC21, AC22, AC23, AC25, AD26, W20	**LFE2M50:** G5, G4, K7, K8, E1, F2, F1, G3, G2, G1, L9, L7, K6, K5, L8, L6, AA1, AA2, Y3, AB1, Y9, Y8, Y7, AA7, AB2, AB3, AA5, AA6, AB4, AB5, AA8, AA9, AJ1, AK4, AH6, AH3, AH11, AH8, AK10, AJ13, AB26, AB27, Y24, Y25, AA29, Y28, Y30, Y29, W22, V22, Y27, Y26, W30, W29, W25, W26, L24, L23, D30, D29, K24, K25, J27, K26, J26, H26, H27, G26, H23, H24, D28, E28, J18, J19, H17, J17, F18, F17, B13, A10, C8, C11, C3, C6, A4, B1, AA26, AB11, AB12, AB13, AB14, AB15, AB16, AB17, AB19, AB20, AB21, AC11, AC21, AC22, AD21, AD22, AE23, AF20, AF23, AG23, AG26, F20, F23, G10, G20, G21, H19, H20, H21, H22, J20, J21, R9, U22, W9 **LFE2M70/LFE2M100:** AA26, AB10, AB11, AB12, AB13, AB14, AB15, AB16, AB17, AB19, AB20, AB21, AB9, AC10, AC11, AC21, AC22, AC8, AC9, AD21, AD22, AD4, AD5, AD6, AD7, AD8, AE23, AE5, AE6, AE7, AF20, AF23, AF5, AG23, AG26, D10, E10, E11, F10, F20, F23, F8, G10, G20, G21, G7, G8, G9, H19, H20, H21, H22, H6, H8, H9, J10, J20, J21, J9, K9, R9, U22, W9

1. All grounds must be electrically connected at the board level. For fpBGA packages, the total number of GND balls is less than the actual number of GND logic connections from the die to the common package GND plane.
2. NC pins should not be connected to any active signals, VCC or GND.
3. For package migration across device densities, the designer must comprehend the package pin requirements for the SERDES blocks. Specifically, the SERDES power pins of the largest density device must be accounted to accommodate migration to other smaller devices using the same package. Please refer to TN1160, LatticeECP2/M Density Migration for more details.

LFE2-6E/SE and LFE2-12E/SE Logic Signal Connections: 256 fpBGA

LFE2-6E/SE					LFE2-12E/SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
C3	PL2A	7	VREF2_7	T (LVDS)*	PL2A	7	VREF2_7	T (LVDS)*
C2	PL2B	7	VREF1_7	C (LVDS)*	PL2B	7	VREF1_7	C (LVDS)*
VCCIO	VCCIO7	7			VCCIO7	7		
-	-	-			-	-		
D3	PL5A	7		T	PL5A	7		T
D4	PL4A	7		T (LVDS)*	PL4A	7		T (LVDS)*
D2	PL5B	7		C	PL5B	7		C
GND	GNDIO7	-			GNDIO7	-		
E4	PL4B	7		C (LVDS)*	PL4B	7		C (LVDS)*
B1	PL7A	7	LDQ10	T	PL7A	7	LDQ10	T
C1	PL7B	7	LDQ10	C	PL7B	7	LDQ10	C
F5	PL9A	7	LDQ10	T	PL9A	7	LDQ10	T
VCCIO	VCCIO7	7			VCCIO7	7		
F4	PL8A	7	LDQ10	T (LVDS)*	PL8A	7	LDQ10	T (LVDS)*
G6	PL9B	7	LDQ10	C	PL9B	7	LDQ10	C
G4	PL8B	7	LDQ10	C (LVDS)*	PL8B	7	LDQ10	C (LVDS)*
D1	PL10A	7	LDQS10	T (LVDS)*	PL10A	7	LDQS10	T (LVDS)*
GND	GNDIO7	-			GNDIO7	-		
E1	PL10B	7	LDQ10	C (LVDS)*	PL10B	7	LDQ10	C (LVDS)*
F3	PL11A	7	LDQ10	T	PL11A	7	LDQ10	T
G3	PL11B	7	LDQ10	C	PL11B	7	LDQ10	C
VCCIO	VCCIO7	7			VCCIO7	7		
F2	PL12A	7	LDQ10	T (LVDS)*	PL12A	7	LDQ10	T (LVDS)*
F1	PL12B	7	LDQ10	C (LVDS)*	PL12B	7	LDQ10	C (LVDS)*
GND	GNDIO7	-			GNDIO7	-		
G2	PL13A	7	PCLKT7_0/LDQ10	T	PL13A	7	PCLKT7_0/LDQ10	T
G1	PL13B	7	PCLKC7_0/LDQ10	C	PL13B	7	PCLKC7_0/LDQ10	C
H6	PL15A	6	PCLKT6_0	T (LVDS)*	PL15A	6	PCLKT6_0	T (LVDS)*
VCCIO	VCCIO6	6			VCCIO6	6		
H5	PL15B	6	PCLKC6_0	C (LVDS)*	PL15B	6	PCLKC6_0	C (LVDS)*
H4	PL16A	6	VREF2_6	T	PL16A	6	VREF2_6	T
GND	GNDIO6	-			GNDIO6	-		
H3	PL16B	6	VREF1_6	C	PL16B	6	VREF1_6	C
H2	PL17A	6	LLM0_GDLLT_IN_A**	T (LVDS)*	PL17A	6	LLM0_GDLLT_IN_A**	T (LVDS)*
H1	PL17B	6	LLM0_GDLLC_IN_A**	C (LVDS)*	PL17B	6	LLM0_GDLLC_IN_A**	C (LVDS)*
G10	VCC	-			VCC	-		
J4	PL18A	6	LLM0_GDLLT_FB_A	T	PL18A	6	LLM0_GDLLT_FB_A	T
J5	PL18B	6	LLM0_GDLLC_FB_A	C	PL18B	6	LLM0_GDLLC_FB_A	C
J6	LLM0_PLLCAP	6			LLM0_PLLCAP	6		
K4	PL20A	6	LLM0_GPLLT_IN_A**	T (LVDS)*	PL20A	6	LLM0_GPLLT_IN_A**	T (LVDS)*
GND	GNDIO6	-			GNDIO6	-		
J1	PL21A	6	LLM0_GPLLT_FB_A	T	PL21A	6	LLM0_GPLLT_FB_A	T
K3	PL20B	6	LLM0_GPLLC_IN_A**	C (LVDS)*	PL20B	6	LLM0_GPLLC_IN_A**	C (LVDS)*
VCCIO	VCCIO6	6			VCCIO6	6		
J2	PL21B	6	LLM0_GPLLC_FB_A	C	PL21B	6	LLM0_GPLLC_FB_A	C

LFE2-12E/SE and LFE2-20E/SE Logic Signal Connections: 484 fpBGA (Cont.)

LFE2-12E/12SE					LFE2-20E/20SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
R8	VCCIO6	6			VCCIO6	6		
J8	VCCIO7	7			VCCIO7	7		
K7	VCCIO7	7			VCCIO7	7		
L7	VCCIO7	7			VCCIO7	7		
M7	VCCIO7	7			VCCIO7	7		
P15	VCCIO8	8			VCCIO8	8		
R15	VCCIO8	8			VCCIO8	8		
C5	VCCAUX	-			VCCAUX	-		
D11	VCCAUX	-			VCCAUX	-		
E17	VCCAUX	-			VCCAUX	-		
E6	VCCAUX	-			VCCAUX	-		
F13	VCCAUX	-			VCCAUX	-		
G18	VCCAUX	-			VCCAUX	-		
G5	VCCAUX	-			VCCAUX	-		
K5	VCCAUX	-			VCCAUX	-		
M17	VCCAUX	-			VCCAUX	-		
P17	VCCAUX	-			VCCAUX	-		
R5	VCCAUX	-			VCCAUX	-		
V11	VCCAUX	-			VCCAUX	-		
V13	VCCAUX	-			VCCAUX	-		
V15	VCCAUX	-			VCCAUX	-		
V7	VCCAUX	-			VCCAUX	-		
V8	VCCAUX	-			VCCAUX	-		
A1	GND	-			GND	-		
A22	GND	-			GND	-		
AA19	GND	-			GND	-		
AA4	GND	-			GND	-		
AB1	GND	-			GND	-		
AB22	GND	-			GND	-		
B19	GND	-			GND	-		
B4	GND	-			GND	-		
C14	GND	-			GND	-		
C9	GND	-			GND	-		
D2	GND	-			GND	-		
D21	GND	-			GND	-		
F17	GND	-			GND	-		
F6	GND	-			GND	-		
H10	GND	-			GND	-		
H11	GND	-			GND	-		
H12	GND	-			GND	-		
H13	GND	-			GND	-		
J14	GND	-			GND	-		
J20	GND	-			GND	-		
J3	GND	-			GND	-		

LFE2-35E/SE and LFE2-50E/SE Logic Signal Connections: 484 fpBGA (Cont.)

LFE2-35E/SE					LFE2-50E/SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
W20	CFG0	8			CFG0	8		
V20	PROGRAMN	8			PROGRAMN	8		
W22	CCLK	8			CCLK	8		
V22	INITN	8			INITN	8		
V21	DONE	8			DONE	8		
GNDIO	GNDIO8	-			GNDIO8	-		
R16	PR58B	8	WRITEN	C	PR77B	8	WRITEN	C
R17	PR58A	8	CS1N	T	PR77A	8	CS1N	T
U19	PR57B	8	CSN	C	PR76B	8	CSN	C
U20	PR57A	8	D0/SPIFASTN	T	PR76A	8	D0/SPIFASTN	T
VCCIO	VCCIO8	8			VCCIO	8		
U22	PR56B	8	D1	C	PR75B	8	D1	C
U21	PR56A	8	D2	T	PR75A	8	D2	T
T20	PR55B	8	D3	C	PR74B	8	D3	C
GNDIO	GNDIO8	-			GNDIO8	-		
T19	PR55A	8	D4	T	PR74A	8	D4	T
T17	PR54B	8	D5	C	PR73B	8	D5	C
T18	PR54A	8	D6	T	PR73A	8	D6	T
T21	PR53B	8	D7/SPID0	C	PR72B	8	D7/SPID0	C
VCCIO	VCCIO8	8			VCCIO	8		
T22	PR53A	8	DI/CSSPI0N	T	PR72A	8	DI/CSSPI0N	T
R18	PR52B	8	DOUT/CSON	C	PR71B	8	DOUT/CSON	C
R19	PR52A	8	BUSY/SISPI	T	PR71A	8	BUSY/SISPI	T
GNDIO	GNDIO3	-			GNDIO3	-		
VCCIO	VCCIO3	3			VCCIO	3		
R22	PR47B	3	RDQ48	C	PR66B	3	RDQ67	C
R21	PR47A	3	RDQ48	T	PR66A	3	RDQ67	T
P18	PR46B	3	RDQ48	C (LVDS)*	PR65B	3	RDQ67	C (LVDS)*
P19	PR46A	3	RDQ48	T (LVDS)*	PR65A	3	RDQ67	T (LVDS)*
VCCIO	VCCIO3	3			VCCIO	3		
R20	PR45B	3	RLM0_GPLLC_FB_A/RDQ48	C	PR64B	3	RLM0_GPLLC_FB_A/RDQ67	C
P22	PR45A	3	RLM0_GPLLT_FB_A/RDQ48	T	PR64A	3	RLM0_GPLLT_FB_A/RDQ67	T
P21	PR44B	3	RLM0_GPLLC_IN_A**/RDQ48	C (LVDS)*	PR63B	3	RLM0_GPLLC_IN_A**/RDQ67	C (LVDS)*
N21	PR44A	3	RLM0_GPLLT_IN_A**/RDQ48	T (LVDS)*	PR63A	3	RLM0_GPLLT_IN_A**/RDQ67	T (LVDS)*
N17	RLM0_PLLCAP	3			RLM0_PLLCAP	3		
N22	PR42B	3	RLM0_GDLLC_FB_A/RDQ39	C	PR61B	3	RLM0_GDLLC_FB_A/RDQ58	C
N20	PR42A	3	RLM0_GDLLT_FB_A/RDQ39	T	PR61A	3	RLM0_GDLLT_FB_A/RDQ58	T
GNDIO	GNDIO3	-			GNDIO3	-		
M22	PR41B	3	RLM0_GDLLC_IN_A**/RDQ39	C (LVDS)*	PR60B	3	RLM0_GDLLC_IN_A**/RDQ58	C (LVDS)*
M21	PR41A	3	RLM0_GDLLT_IN_A**/RDQ39	T (LVDS)*	PR60A	3	RLM0_GDLLT_IN_A**/RDQ58	T (LVDS)*
N19	PR40B	3	RDQ39	C	PR59B	3	RDQ58	C
M19	PR40A	3	RDQ39	T	PR59A	3	RDQ58	T
VCCIO	VCCIO3	3			VCCIO	3		
GNDIO	GNDIO3	-			GNDIO3	-		
L22	PR30B	3	RDQ31	C	PR49B	3	RDQ50	C
K22	PR30A	3	RDQ31	T	PR49A	3	RDQ50	T

LFE2-20E/SE and LFE2-35E/SE Logic Signal Connections: 672 fpBGA (Cont.)

LFE2-20E/20SE					LFE2-35E/35SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
W5	PL38B	6	LDQ42	C (LVDS)*	PL52B	6	LDQ56	C (LVDS)*
AC1	PL39A	6	LDQ42	T	PL53A	6	LDQ56	T
AD1	PL39B	6	LDQ42	C	PL53B	6	LDQ56	C
VCCIO	VCCIO6	6			VCCIO6	6		
Y6	PL40A	6	LDQ42	T (LVDS)*	PL54A	6	LDQ56	T (LVDS)*
Y5	PL40B	6	LDQ42	C (LVDS)*	PL54B	6	LDQ56	C (LVDS)*
AE2	PL41A	6	LDQ42	T	PL55A	6	LDQ56	T
AD2	PL41B	6	LDQ42	C	PL55B	6	LDQ56	C
GND	GNDIO6	-			GNDIO6	-		
AB3	PL42A	6	LDQS42	T (LVDS)*	PL56A	6	LDQS56	T (LVDS)*
AB2	PL42B	6	LDQ42	C (LVDS)*	PL56B	6	LDQ56	C (LVDS)*
W7	PL43A	6	LDQ42	T	PL57A	6	LDQ56	T
VCCIO	VCCIO6	6			VCCIO6	6		
W8	PL43B	6	LDQ42	C	PL57B	6	LDQ56	C
Y7	PL44A	6	LDQ42	T (LVDS)*	PL58A	6	LDQ56	T (LVDS)*
Y8	PL44B	6	LDQ42	C (LVDS)*	PL58B	6	LDQ56	C (LVDS)*
AC2	PL45A	6	LDQ42	T	PL59A	6	LDQ56	T
GND	GNDIO6	-			GNDIO6	-		
AD3	PL45B	6	LDQ42	C	PL59B	6	LDQ56	C
AC3	TCK	-			TCK	-		
AA8	TDI	-			TDI	-		
AB4	TMS	-			TMS	-		
AA5	TDO	-			TDO	-		
AB5	VCCJ	-			VCCJ	-		
AE3	PB2A	5	VREF2_5/BDQ6	T	PB2A	5	VREF2_5/BDQ6	T
AF3	PB2B	5	VREF1_5/BDQ6	C	PB2B	5	VREF1_5/BDQ6	C
AC4	PB3A	5	BDQ6	T	PB3A	5	BDQ6	T
AD4	PB3B	5	BDQ6	C	PB3B	5	BDQ6	C
AE4	PB4A	5	BDQ6	T	PB4A	5	BDQ6	T
AF4	PB4B	5	BDQ6	C	PB4B	5	BDQ6	C
VCCIO	VCCIO5	5			VCCIO5	5		
V9	PB5A	5	BDQ6	T	PB5A	5	BDQ6	T
W9	PB5B	5	BDQ6	C	PB5B	5	BDQ6	C
GND	GNDIO5	-			GNDIO5	-		
AA6	PB6A	5	BDQS6	T	PB6A	5	BDQS6	T
AB6	PB6B	5	BDQ6	C	PB6B	5	BDQ6	C
AC5	PB7A	5	BDQ6	T	PB7A	5	BDQ6	T
AD5	PB7B	5	BDQ6	C	PB7B	5	BDQ6	C
AA7	PB8A	5	BDQ6	T	PB8A	5	BDQ6	T
AB7	PB8B	5	BDQ6	C	PB8B	5	BDQ6	C
VCCIO	VCCIO5	5			VCCIO5	5		
AE5	PB9A	5	BDQ6	T	PB9A	5	BDQ6	T
AF5	PB9B	5	BDQ6	C	PB9B	5	BDQ6	C
AC7	PB10A	5	BDQ6	T	PB10A	5	BDQ6	T
AD7	PB10B	5	BDQ6	C	PB10B	5	BDQ6	C
VCCIO	VCCIO5	5			VCCIO5	5		

LFE2-20E/SE and LFE2-35E/SE Logic Signal Connections: 672 fpBGA (Cont.)

LFE2-20E/20SE					LFE2-35E/35SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
Y21	PB64A	4	VREF2_4/BDQ60	T	PB73A	4	VREF2_4/BDQ69	T
AB23	PB64B	4	VREF1_4/BDQ60	C	PB73B	4	VREF1_4/BDQ69	C
GND	GNDIO4	-			GNDIO4	-		
AD24	CFG2	8			CFG2	8		
W20	CFG1	8			CFG1	8		
AC24	CFG0	8			CFG0	8		
V19	PROGRAMN	8			PROGRAMN	8		
AA22	CCLK	8			CCLK	8		
AB24	INITN	8			INITN	8		
AD25	DONE	8			DONE	8		
GND	GNDIO8	-			GNDIO8	-		
W21	PR44B	8	WRITEN	C	PR58B	8	WRITEN	C
Y22	PR44A	8	CS1N	T	PR58A	8	CS1N	T
AC25	PR43B	8	CSN	C	PR57B	8	CSN	C
AB25	PR43A	8	D0/SPIFASTN	T	PR57A	8	D0/SPIFASTN	T
VCCIO	VCCIO8	8			VCCIO8	8		
AD26	PR42B	8	D1	C	PR56B	8	D1	C
AC26	PR42A	8	D2	T	PR56A	8	D2	T
Y23	PR41B	8	D3	C	PR55B	8	D3	C
GND	GNDIO8	-			GNDIO8	-		
W22	PR41A	8	D4	T	PR55A	8	D4	T
AA25	PR40B	8	D5	C	PR54B	8	D5	C
AB26	PR40A	8	D6	T	PR54A	8	D6	T
W23	PR39B	8	D7/SPID0	C	PR53B	8	D7/SPID0	C
VCCIO	VCCIO8	8			VCCIO8	8		
V22	PR39A	8	DI/CSSPI0N	T	PR53A	8	DI/CSSPI0N	T
Y24	PR38B	8	DOUT/CSON	C	PR52B	8	DOUT/CSON	C
Y25	PR38A	8	BUSY/SISPI	T	PR52A	8	BUSY/SISPI	T
W24	PR37B	3	RDQ34	C	PR51B	3	RDQ48	C
GND	GNDIO3	-			GNDIO3	-		
V23	PR37A	3	RDQ34	T	PR51A	3	RDQ48	T
AA26	PR36B	3	RDQ34	C (LVDS)*	PR50B	3	RDQ48	C (LVDS)*
Y26	PR36A	3	RDQ34	T (LVDS)*	PR50A	3	RDQ48	T (LVDS)*
U21	PR35B	3	RDQ34	C	PR49B	3	RDQ48	C
VCCIO	VCCIO3	3			VCCIO3	3		
U19	PR35A	3	RDQ34	T	PR49A	3	RDQ48	T
W25	PR34B	3	RDQ34	C (LVDS)*	PR48B	3	RDQ48	C (LVDS)*
W26	PR34A	3	RDQS34	T (LVDS)*	PR48A	3	RDQS48	T (LVDS)*
GND	GNDIO3	-			GNDIO3	-		
V24	PR33B	3	RDQ34	C	PR47B	3	RDQ48	C
V25	PR33A	3	RDQ34	T	PR47A	3	RDQ48	T
V26	PR32B	3	RDQ34	C (LVDS)*	PR46B	3	RDQ48	C (LVDS)*
U26	PR32A	3	RDQ34	T (LVDS)*	PR46A	3	RDQ48	T (LVDS)*
VCCIO	VCCIO3	3			VCCIO3	3		
U22	PR31B	3	RLM0_GPLLC_FB_A/RDQ34	C	PR45B	3	RLM0_GPLLC_FB_A/RDQ48	C
U23	PR31A	3	RLM0_GPLLT_FB_A/RDQ34	T	PR45A	3	RLM0_GPLLT_FB_A/RDQ48	T

LFE2-50E/SE and LFE2-70E/SE Logic Signal Connections: 672 fpBGA (Cont.)

LFE2-50E/SE					LFE2-70E/SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
GND	GNDIO5	-			GNDIO5	-		
W10	PB20A	5	BDQ24	T	PB29A	5	BDQ33	T
Y10	PB20B	5	BDQ24	C	PB29B	5	BDQ33	C
W11	PB21A	5	BDQ24	T	PB30A	5	BDQ33	T
AA10	PB21B	5	BDQ24	C	PB30B	5	BDQ33	C
AC8	PB22A	5	BDQ24	T	PB31A	5	BDQ33	T
AD8	PB22B	5	BDQ24	C	PB31B	5	BDQ33	C
VCCIO	VCCIO5	5			VCCIO5	5		
AB8	PB23A	5	BDQ24	T	PB32A	5	BDQ33	T
AB10	PB23B	5	BDQ24	C	PB32B	5	BDQ33	C
GND	GNDIO5	-			GNDIO5	-		
AE6	PB24A	5	BDQS24	T	PB33A	5	BDQS33	T
AF6	PB24B	5	BDQ24	C	PB33B	5	BDQ33	C
AA11	PB25A	5	BDQ24	T	PB34A	5	BDQ33	T
AC9	PB25B	5	BDQ24	C	PB34B	5	BDQ33	C
AB9	PB26A	5	BDQ24	T	PB35A	5	BDQ33	T
AD9	PB26B	5	BDQ24	C	PB35B	5	BDQ33	C
VCCIO	VCCIO5	5			VCCIO5	5		
Y11	PB27A	5	BDQ24	T	PB36A	5	BDQ33	T
AB11	PB27B	5	BDQ24	C	PB36B	5	BDQ33	C
AE7	PB28A	5	BDQ24	T	PB37A	5	BDQ33	T
AF7	PB28B	5	BDQ24	C	PB37B	5	BDQ33	C
GND	GNDIO5	-			GNDIO5	-		
AC10	PB29A	5	BDQ33	T	PB38A	5	BDQ42	T
AD10	PB29B	5	BDQ33	C	PB38B	5	BDQ42	C
AA12	PB30A	5	BDQ33	T	PB39A	5	BDQ42	T
W12	PB30B	5	BDQ33	C	PB39B	5	BDQ42	C
AB12	PB31A	5	BDQ33	T	PB40A	5	BDQ42	T
VCCIO	VCCIO5	5			VCCIO5	5		
Y12	PB31B	5	BDQ33	C	PB40B	5	BDQ42	C
AD12	PB32A	5	BDQ33	T	PB41A	5	BDQ42	T
AC12	PB32B	5	BDQ33	C	PB41B	5	BDQ42	C
AC13	PB33A	5	BDQS33	T	PB42A	5	BDQS42	T
GND	GNDIO5	-			GNDIO5	-		
AA13	PB33B	5	BDQ33	C	PB42B	5	BDQ42	C
AD13	PB34A	5	BDQ33	T	PB43A	5	BDQ42	T
AC14	PB34B	5	BDQ33	C	PB43B	5	BDQ42	C
AE8	PB35A	5	BDQ33	T	PB44A	5	BDQ42	T
VCCIO	VCCIO5	5			VCCIO5	5		
AF8	PB35B	5	BDQ33	C	PB44B	5	BDQ42	C
AB15	PB36A	5	BDQ33	T	PB45A	5	BDQ42	T
Y13	PB36B	5	BDQ33	C	PB45B	5	BDQ42	C
AE9	PB37A	5	BDQ33	T	PB46A	5	BDQ42	T
GND	GNDIO5	-			GNDIO5	-		
AF9	PB37B	5	BDQ33	C	PB46B	5	BDQ42	C
W13	PB38A	5	BDQ42	T	PB47A	5	BDQ51	T

LFE2-50E/SE and LFE2-70E/SE Logic Signal Connections: 672 fpBGA (Cont.)

LFE2-50E/SE					LFE2-70E/SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
U24	PR63B	3	RLM0_GPLLC_IN_A**/RDQ67	C (LVDS)*	PR76B	3	RLM0_GPLLC_IN_A**/RDQ80	C (LVDS)*
U25	PR63A	3	RLM0_GPLLT_IN_A**/RDQ67	T (LVDS)*	PR76A	3	RLM0_GPLLT_IN_A**/RDQ80	T (LVDS)*
R20	RLM0_PLLCAP	3			RLM0_PLLCAP	3		
P18	VCCPLL	3			VCCPLL	-		
T19	PR61B	3	RLM0_GDLLC_FB_A/RDQ58	C	PR74B	3	RLM0_GDLLC_FB_A/RDQ71	C
U20	PR61A	3	RLM0_GDLLT_FB_A/RDQ58	T	PR74A	3	RLM0_GDLLT_FB_A/RDQ71	T
GND	GNDIO3	-			GNDIO3	-		
T25	PR60B	3	RLM0_GDLLC_IN_A**/RDQ58	C (LVDS)*	PR73B	3	RLM0_GDLLC_IN_A**/RDQ71	C (LVDS)*
T26	PR60A	3	RLM0_GDLLT_IN_A**/RDQ58	T (LVDS)*	PR73A	3	RLM0_GDLLT_IN_A**/RDQ71	T (LVDS)*
T20	PR59B	3	RDQ58	C	PR72B	3	RDQ71	C
T22	PR59A	3	RDQ58	T	PR72A	3	RDQ71	T
VCCIO	VCCIO3	3			VCCIO3	3		
R26	PR58B	3	RDQ58	C (LVDS)*	PR71B	3	RDQ71	C (LVDS)*
R25	PR58A	3	RDQS58	T (LVDS)*	PR71A	3	RDQS71	T (LVDS)*
R22	PR57B	3	RDQ58	C	PR70B	3	RDQ71	C
GND	GNDIO3	-			GNDIO3	-		
T21	PR57A	3	RDQ58	T	PR70A	3	RDQ71	T
P26	PR56B	3	RDQ58	C (LVDS)*	PR69B	3	RDQ71	C (LVDS)*
P25	PR56A	3	RDQ58	T (LVDS)*	PR69A	3	RDQ71	T (LVDS)*
R24	PR55B	3	RDQ58	C	PR68B	3	RDQ71	C
VCCIO	VCCIO3	3			VCCIO3	3		
R23	PR55A	3	RDQ58	T	PR68A	3	RDQ71	T
P20	PR54B	3	RDQ58	C (LVDS)*	PR67B	3	RDQ71	C (LVDS)*
R19	PR54A	3	RDQ58	T (LVDS)*	PR67A	3	RDQ71	T (LVDS)*
P21	PR53B	3	RDQ50	C	PR66B	3	RDQ63	C
GND	GNDIO3	-			GNDIO3	-		
P19	PR53A	3	RDQ50	T	PR66A	3	RDQ63	T
P23	PR52B	3	RDQ50	C (LVDS)*	PR65B	3	RDQ63	C (LVDS)*
P22	PR52A	3	RDQ50	T (LVDS)*	PR65A	3	RDQ63	T (LVDS)*
N22	PR51B	3	RDQ50	C	PR64B	3	RDQ63	C
VCCIO	VCCIO3	3			VCCIO3	3		
R21	PR51A	3	RDQ50	T	PR64A	3	RDQ63	T
N26	PR50B	3	RDQ50	C (LVDS)*	PR63B	3	RDQ63	C (LVDS)*
N25	PR50A	3	RDQS50	T (LVDS)*	PR63A	3	RDQS63	T (LVDS)*
GND	GNDIO3	-			GNDIO3	-		
N19	PR49B	3	RDQ50	C	PR62B	3	RDQ63	C
N20	PR49A	3	RDQ50	T	PR62A	3	RDQ63	T
M26	PR48B	3	RDQ50	C (LVDS)*	PR61B	3	RDQ63	C (LVDS)*
M25	PR48A	3	RDQ50	T (LVDS)*	PR61A	3	RDQ63	T (LVDS)*
VCCIO	VCCIO3	3			VCCIO3	3		
N18	PR47B	3	VREF2_3/RDQ50	C	PR60B	3	VREF2_3/RDQ63	C
N21	PR47A	3	VREF1_3/RDQ50	T	PR60A	3	VREF1_3/RDQ63	T
L26	PR46B	3	PCLKC3_0/RDQ50	C (LVDS)*	PR59B	3	PCLKC3_0/RDQ63	C (LVDS)*
L25	PR46A	3	PCLKT3_0/RDQ50	T (LVDS)*	PR59A	3	PCLKT3_0/RDQ63	T (LVDS)*
N24	PR44B	2	PCLKC2_0/RDQ41	C	PR57B	2	PCLKC2_0/RDQ54	C
M23	PR44A	2	PCLKT2_0/RDQ41	T	PR57A	2	PCLKT2_0/RDQ54	T

LFE2M35E/SE and LFE2M50E/SE Logic Signal Connections: 672 fpBGA (Cont.)

LFE2M35E/SE					LFE2M50E/SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
D23	NC	-			NC	-		
D24	NC	-			NC	-		
D25	NC	-			NC	-		
D26	NC	-			NC	-		
E20	NC	-			NC	-		
E21	NC	-			NC	-		
E25	NC	-			NC	-		
E26	NC	-			NC	-		
F20	NC	-			NC	-		
G20	NC	-			NC	-		
K10	NC	-			NC	-		
K17	NC	-			NC	-		
R4	NC	-			NC	-		
U10	NC	-			NC	-		
U23	NC	-			NC	-		
V10	NC	-			NC	-		
W7	NC	-			NC	-		
AB21	PB69B	4	BDQ69	C	NC	-		
AC20	PB58A	4	BDQ60	T	NC	-		
AC21	PB63A	4	BDQ60	T	NC	-		
AC22	PB69A	4	BDQS69****	T	NC	-		
AC23	PB71A	4	BDQ69	T	NC	-		
AC25	PB71B	4	BDQ69	C	NC	-		
AD26	PB70B	4	BDQ69	C	NC	-		
W20	PB72B	4	BDQ69	C	NC	-		
H7	L_VCCPLL	-			L_VCCPLL	-		
K6	L_VCCPLL	-			L_VCCPLL	-		
P7	L_VCCPLL	-			L_VCCPLL	-		
R8	L_VCCPLL	-			L_VCCPLL	-		
V18	R_VCCPLL	-			R_VCCPLL	-		
P20	R_VCCPLL	-			R_VCCPLL	-		
J17	R_VCCPLL	-			R_VCCPLL	-		
G19	R_VCCPLL	-			R_VCCPLL	-		

* Supports true LVDS. Other differential signals must be emulated with external resistors.
** These dedicated input pins can be used for GPLLs or GDLLs within the respective quadrant.
*** For density migration, board design must take into account that these sysCONFIG pins are dual function for the lower density devices (ECP2M20 and ECP2M35). They can be either sysCONFIG pins or general purpose I/Os. These pins are dedicated pins for the higher density devices (ECP2M50, ECP2M70 and ECP2M100).
****Due to packaging bond out option, this DQS does not have all the necessary DQ pins bonded out for a full 8-bit data width.

Note: VCCIO and GND pads are used to determine the average DC current drawn by I/Os between GND/VCCIO connections, or between the last GND/VCCIO in an I/O bank and the end of an I/O bank. The substrate pads listed in the Pin Table do not necessarily have a one to one connection with a package ball or pin.

LFE2M50E/SE and LFE2M70E/SE Logic Signal Connections: 900 fpBGA (Cont.)

LFE2M50E/SE					LFE2M70E/SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
K3	VCCIO7	7			VCCIO7	7		
M10	VCCIO7	7			VCCIO7	7		
M7	VCCIO7	7			VCCIO7	7		
N10	VCCIO7	7			VCCIO7	7		
N3	VCCIO7	7			VCCIO7	7		
P10	VCCIO7	7			VCCIO7	7		
R6	VCCIO7	7			VCCIO7	7		
AA25	VCCIO8	8			VCCIO8	8		
AD28	VCCIO8	8			VCCIO8	8		
AA10	VCCAUX	-			VCCAUX	-		
AA11	VCCAUX	-			VCCAUX	-		
AA20	VCCAUX	-			VCCAUX	-		
AA21	VCCAUX	-			VCCAUX	-		
K10	VCCAUX	-			VCCAUX	-		
K11	VCCAUX	-			VCCAUX	-		
K20	VCCAUX	-			VCCAUX	-		
K21	VCCAUX	-			VCCAUX	-		
L10	VCCAUX	-			VCCAUX	-		
L11	VCCAUX	-			VCCAUX	-		
L20	VCCAUX	-			VCCAUX	-		
L21	VCCAUX	-			VCCAUX	-		
Y10	VCCAUX	-			VCCAUX	-		
Y11	VCCAUX	-			VCCAUX	-		
Y20	VCCAUX	-			VCCAUX	-		
Y21	VCCAUX	-			VCCAUX	-		
A1	GND	-			GND	-		
A13	GND	-			GND	-		
A18	GND	-			GND	-		
A24	GND	-			GND	-		
A30	GND	-			GND	-		
A7	GND	-			GND	-		
AA14	GND	-			GND	-		
AA15	GND	-			GND	-		
AA16	GND	-			GND	-		
AA17	GND	-			GND	-		
AA24	GND	-			GND	-		
AA27	GND	-			GND	-		
AA4	GND	-			GND	-		
AB24	GND	-			GND	-		
AB7	GND	-			GND	-		
AD12	GND	-			GND	-		
AD19	GND	-			GND	-		
AD27	GND	-			GND	-		
AE22	GND	-			GND	-		
AE27	GND	-			GND	-		
AE4	GND	-			GND	-		
AE9	GND	-			GND	-		
AF14	GND	-			GND	-		

LFE2M100E/SE Logic Signal Connections: 900 fpBGA (Cont.)

LFE2M100E/SE				
Ball Number	**Ball/Pad Function**	**Bank**	**Dual Function**	**Differential**
C29	URC_SQ_VCCRX1	12		
B28	URC_SQ_HDINN1	12		C
C28	URC_SQ_VCCIB1	12		
A28	URC_SQ_HDINP1	12		T
B24	URC_SQ_VCCAUX33	12		
E24	URC_SQ_REFCLKN	12		C
D24	URC_SQ_REFCLKP	12		T
C24	URC_SQ_VCCP	12		
A20	URC_SQ_HDINP2	12		T
C20	URC_SQ_VCCIB2	12		
B20	URC_SQ_HDINN2	12		C
C19	URC_SQ_VCCRX2	12		
A23	URC_SQ_HDOUTP2	12		T
C23	URC_SQ_VCCOB2	12		
B23	URC_SQ_HDOUTN2	12		C
C22	URC_SQ_VCCTX2	12		
B22	URC_SQ_HDOUTN3	12		C
A21	URC_SQ_VCCOB3	12		
A22	URC_SQ_HDOUTP3	12		T
C21	URC_SQ_VCCTX3	12		
B19	URC_SQ_HDINN3	12		C
B18	URC_SQ_VCCIB3	12		
A19	URC_SQ_HDINP3	12		T
C18	URC_SQ_VCCRX3	12		
D23	PT100B	1		C
GNDIO	GNDIO1	-		
E21	PT100A	1		T
D26	PT99B	1		C
E26	PT99A	1		T
E23	PT98B	1		C
VCCIO	VCCIO1	1		
G22	PT98A	1		T
-	-	-		
D22	PT97B	1		C
F21	PT97A	1		T
G18	PT96B	1		C
H18	PT96A	1		T
D20	PT95B	1		C
GNDIO	GNDIO1	-		
D21	PT95A	1		T
E20	PT94B	1		C
VCCIO	VCCIO1	1		
E19	PT94A	1		T

LFE2M70E/SE and LFE2M100E/SE Logic Signal Connections: 1152 fpBGA (Cont.)

LFE2M70E/SE				LFE2M100E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
GNDIO	GNDIO1	-			GNDIO1	-		
F19	PT59B	1		C	PT68B	1		C
D18	PT59A	1		T	PT68A	1		T
L18	NC	-			PT67B	1		C
K19	NC	-			PT67A	1		T
VCCIO	VCCIO1	1			VCCIO1	1		
A18	PT57B	1	VREF2_1	C	PT66B	1	VREF2_1	C
B18	PT57A	1	VREF1_1	T	PT66A	1	VREF1_1	T
G18	PT56B	1	PCLKC1_0	C	PT65B	1	PCLKC1_0	C
E18	PT56A	1	PCLKT1_0	T	PT65A	1	PCLKT1_0	T
F18	PT55B	0	PCLKC0_0	C	PT64B	0	PCLKC0_0	C
GNDIO	GNDIO0	-			GNDIO0	-		
G19	PT55A	0	PCLKT0_0	T	PT64A	0	PCLKT0_0	T
H18	PT54B	0	VREF2_0	C	PT63B	0	VREF2_0	C
K18	PT54A	0	VREF1_0	T	PT63A	0	VREF1_0	T
VCCIO	VCCIO0	0			VCCIO0	0		
J18	PT53B	0		C	PT60B	0		C
L17	PT53A	0		T	PT60A	0		T
G17	PT52B	0		C	PT59B	0		C
-	-	-			GNDIO0	-		
J17	PT52A	0		T	PT59A	0		T
H17	PT51B	0		C	PT58B	0		C
-	-	-			VCCIO0	0		
K17	PT51A	0		T	PT58A	0		T
B17	PT50B	0		C	PT57B	0		C
GNDIO	GNDIO0	-			-	-		
A17	PT50A	0		T	PT57A	0		T
D17	PT49B	0		C	PT56B	0		C
VCCIO	VCCIO0	0			-	-		
F17	PT49A	0		T	PT56A	0		T
B16	PT48B	0		C	PT55B	0		C
A16	PT48A	0		T	PT55A	0		T
-	-	-			GNDIO0	-		
-	-	-			VCCIO0	0		
E17	PT47B	0		C	PT52B	0		C
C17	PT47A	0		T	PT52A	0		T
K16	PT46B	0		C	PT51B	0		C
J15	PT46A	0		T	PT51A	0		T
GNDIO	GNDIO0	-			GNDIO0	-		
G16	PT45B	0		C	PT50B	0		C
H15	PT45A	0		T	PT50A	0		T
A15	PT44B	0		C	PT49B	0		C
B15	PT44A	0		T	PT49A	0		T
VCCIO	VCCIO0	0			VCCIO0	0		
L16	PT43B	0		C	PT48B	0		C
K15	PT43A	0		T	PT48A	0		T
F16	PT42B	0		C	PT47B	0		C
E16	PT42A	0		T	PT47A	0		T
E15	PT41B	0		C	PT46B	0		C

LatticeECP2 S-Series Devices, Lead-Free Packaging

Commercial

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2-6SE-5TN144C	90	1.2V	-5	Lead-Free TQFP	144	Com	6
LFE2-6SE-6TN144C	90	1.2V	-6	Lead-Free TQFP	144	Com	6
LFE2-6SE-7TN144C	90	1.2V	-7	Lead-Free TQFP	144	Com	6
LFE2-6SE-5FN256C	190	1.2V	-5	Lead-Free fpBGA	256	Com	6
LFE2-6SE-6FN256C	190	1.2V	-6	Lead-Free fpBGA	256	Com	6
LFE2-6SE-7FN256C	190	1.2V	-7	Lead-Free fpBGA	256	Com	6

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2-12SE-5TN144C	93	1.2V	-5	Lead-Free TQFP	144	Com	12
LFE2-12SE-6TN144C	93	1.2V	-6	Lead-Free TQFP	144	Com	12
LFE2-12SE-7TN144C	93	1.2V	-7	Lead-Free TQFP	144	Com	12
LFE2-12SE-5QN208C	131	1.2V	-5	Lead-Free PQFP	208	Com	12
LFE2-12SE-6QN208C	131	1.2V	-6	Lead-Free PQFP	208	Com	12
LFE2-12SE-7QN208C	131	1.2V	-7	Lead-Free PQFP	208	Com	12
LFE2-12SE-5FN256C	193	1.2V	-5	Lead-Free fpBGA	256	Com	12
LFE2-12SE-6FN256C	193	1.2V	-6	Lead-Free fpBGA	256	Com	12
LFE2-12SE-7FN256C	193	1.2V	-7	Lead-Free fpBGA	256	Com	12
LFE2-12SE-5FN484C	297	1.2V	-5	Lead-Free fpBGA	484	Com	12
LFE2-12SE-6FN484C	297	1.2V	-6	Lead-Free fpBGA	484	Com	12
LFE2-12SE-7FN484C	297	1.2V	-7	Lead-Free fpBGA	484	Com	12

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2-20SE-5QN208C	131	1.2V	-5	Lead-Free PQFP	208	Com	20
LFE2-20SE-6QN208C	131	1.2V	-6	Lead-Free PQFP	208	Com	20
LFE2-20SE-7QN208C	131	1.2V	-7	Lead-Free PQFP	208	Com	20
LFE2-20SE-5FN256C	193	1.2V	-5	Lead-Free fpBGA	256	Com	20
LFE2-20SE-6FN256C	193	1.2V	-6	Lead-Free fpBGA	256	Com	20
LFE2-20SE-7FN256C	193	1.2V	-7	Lead-Free fpBGA	256	Com	20
LFE2-20SE-5FN484C	331	1.2V	-5	Lead-Free fpBGA	484	Com	20
LFE2-20SE-6FN484C	331	1.2V	-6	Lead-Free fpBGA	484	Com	20
LFE2-20SE-7FN484C	331	1.2V	-7	Lead-Free fpBGA	484	Com	20
LFE2-20SE-5FN672C	402	1.2V	-5	Lead-Free fpBGA	672	Com	20
LFE2-20SE-6FN672C	402	1.2V	-6	Lead-Free fpBGA	672	Com	20
LFE2-20SE-7FN672C	402	1.2V	-7	Lead-Free fpBGA	672	Com	20

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2M100SE-5FN1152C	520	1.2V	-5	Lead-Free fpBGA	1152	Com	100
LFE2M100SE-6FN1152C	520	1.2V	-6	Lead-Free fpBGA	1152	Com	100
LFE2M100SE-7FN1152C	520	1.2V	-7	Lead-Free fpBGA	1152	Com	100
LFE2M100SE-5FN900C	416	1.2V	-5	Lead-Free fpBGA	900	Com	100
LFE2M100SE-6FN900C	416	1.2V	-6	Lead-Free fpBGA	900	Com	100
LFE2M100SE-7FN900C	416	1.2V	-7	Lead-Free fpBGA	900	Com	100

LatticeECP2/M Family Data Sheet Revision History

September 2013 **Data Sheet DS1006**

Date	Version	Section	Change Summary
February 2006	01.0	—	Initial release.
August 2006	01.1	Introduction	
			Updated Table 1-1 “LatticeECP2 Family Selection Guide”.
		Architecture	Updated Figure 2-2 “PFU Diagram”.
			Updated Figure 2-13 “Secondary Clock Regions ECP2-50”.
			Updated Figure 2-25 “PIC Diagram”.
			Updated Figure 2-26 “Input Register Block for Left, Right and Bottom Edges”.
			Updated Figure 2-28 “Output Register Block for Left, Right and Bottom Edges”.
			Updated Figure 2-30 “DQS Input Routing for Left and Right Edges”.
			Updated Figure 2-32 “Edge Clock, DLL Calibration and DQS Local Bus Distribution”.
			Table 2-15 Selectable Master Clock (CCLK) Frequencies - Removed frequencies 15, 20, 21, 22, 23, 30, 34, 41, 45, 51, 55, 60.
			Replaced “CLKINDEL” with “CLKO”.
			Updated SED section.
			Qualified device migration capability when using DQS banks for DDR interfaces.
		DC and Switching Characteristics	Added VCCPLL to the Recommended Operating Conditions table.
			Removed note 5 from “Hot Specifications” section.
			Added notes 7 and 8 to “Initialization Supply” Current table.
			Change note 6 - “...down to 95MHz” to “...down to 95MHz for DDR and 133MHz for DDR2” .
			New “Typical Building Block Function Performance” numbers.
			New External Switching Characteristics numbers.
			New Internal Switching Characteristics numbers.
			New Family Timing Adders numbers.
			Updated Timings for GPLLs, SPLLs and DLLs.
			Added sysCONFIG waveforms.
			Remove HSTL15D_II from sysIO Recommended Operating Conditions table.
			Updated Supply and Initialization Currents for ECP2-50.
		Pinout Information	Added VCCPLL to the Signal Descriptions table.
			Updated Logic Signal Connections tables to include 484-fpBGA for the ECP2-50.
			Added Logic Signal Connections tables for ECP2-12 devices.
			Updated Pin Information Summary table to include ECP2-12.
			Updated Power Supply and NC Connections table to include ECP2-12.
			Added note 2 to DDR Strobe (DQS) Pin table.
			Added Information on: PCI, DDR & SPI4.2 Capabilities of the device-Package combination.