



Welcome to [E-XFL.COM](https://www.e-xfl.com)

Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	4250
Number of Logic Elements/Cells	34000
Total RAM Bits	2151424
Number of I/O	410
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	672-BBGA
Supplier Device Package	672-FPBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfe2m35e-7fn672c

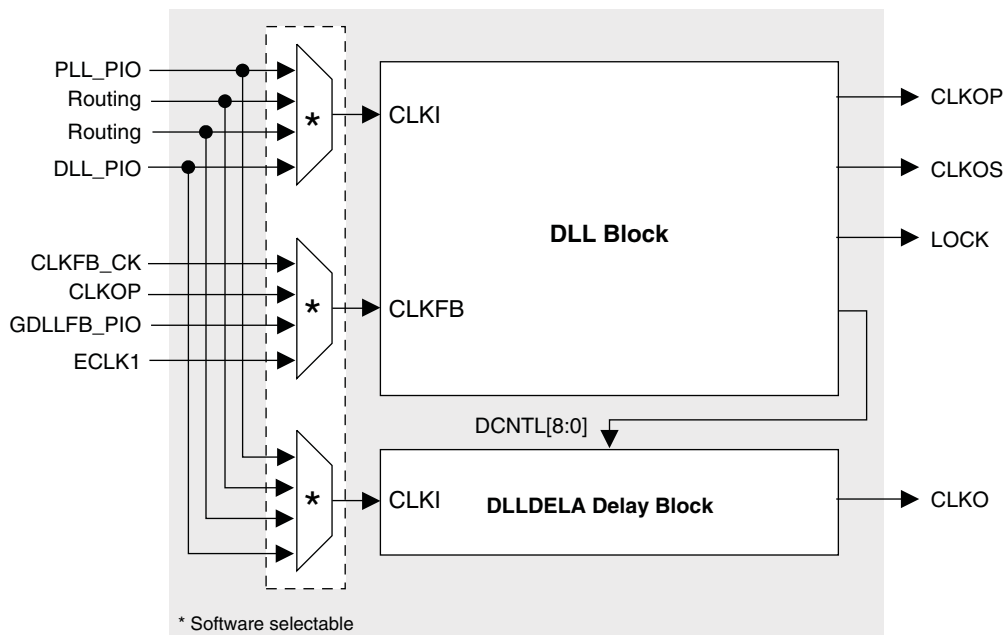
Table 2-5. DLL Signals

Signal	I/O	Description
CLKI	I	Clock input from external pin or routing
CLKFB	I	DLL feed input from DLL output, clock net, routing or external pin
RSTN	I	Active low synchronous reset
ALUHOLD	I	Active high freezes the ALU
UDDCNTL	I	Synchronous enable signal (hold high for two cycles) from routing
DCNTL[8:0]	O	Encoded digital control signals for PIC INDEL and slave delay calibration
CLKOP	O	The primary clock output
CLKOS	O	The secondary clock output with fine phase shift and/or division by 2 or by 4
LOCK	O	Active high phase lock indicator

DLLDELA Delay Block

Closely associated with each DLL is a DLLDELA block. This is a delay block consisting of a delay line with taps and a selection scheme that selects one of the taps. The DCNTL[8:0] bus controls the delay of the CLKO signal. Typically this is the delay setting that the DLL uses to achieve phase alignment. This results in the delay providing a calibrated 90° phase shift that is useful in centering a clock in the middle of a data cycle for source synchronous data. The CLKO signal feeds the edge clock network. Figure 2-7 shows the connections between the DLL block and the DLLDELA delay block. For more information, please see the list of additional technical documentation at the end of this data sheet.

Figure 2-7. DLLDELA Delay Block



PLL/DLL Cascading

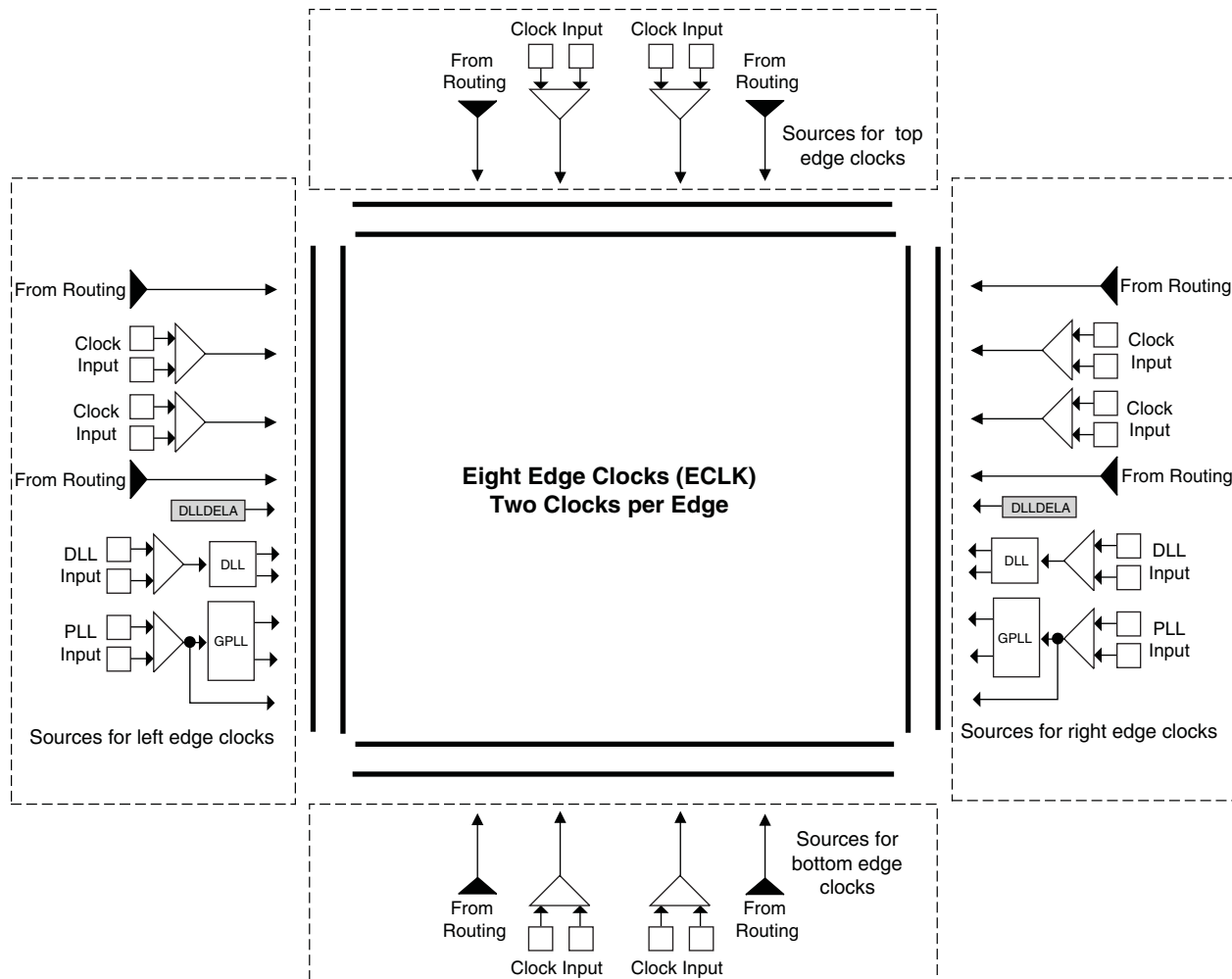
LatticeECP2/M devices have been designed to allow certain combinations of PLL (GPLL and SPLL) and DLL cascading. The allowable combinations are:

- PLL to PLL supported
- PLL to DLL supported

Edge Clock Sources

Edge clock resources can be driven from a variety of sources at the same edge. Edge clock resources can be driven from adjacent edge clock PIOs, primary clock PIOs, PLLs/DLLs and clock dividers as shown in Figure 2-12.

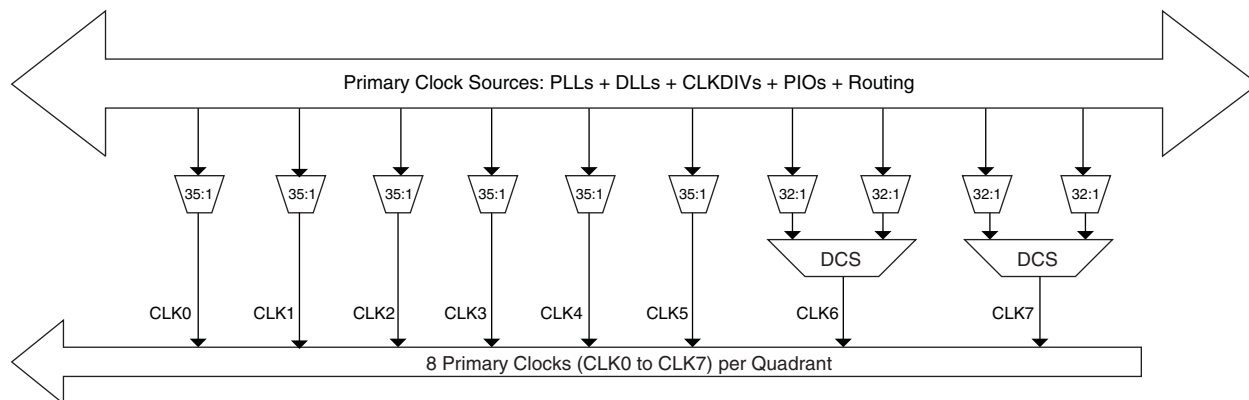
Figure 2-12. Edge Clock Sources



Primary Clock Routing

The clock routing structure in LatticeECP2/M devices consists of a network of eight primary clock lines (CLK0 through CLK7) per quadrant. The primary clocks of each quadrant are generated from muxes located in the center of the device. All the clock sources are connected to these muxes. Figure 2-13 shows the clock routing for one quadrant. Each quadrant mux is identical. If desired, any clock can be routed globally

Figure 2-13. Per Quadrant Primary Clock Selection

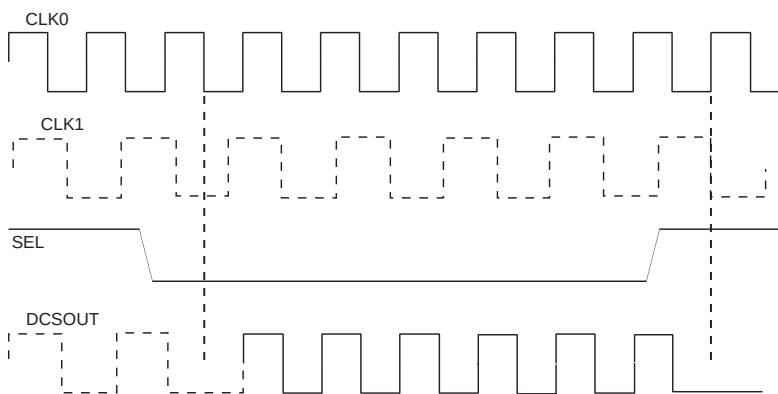


Dynamic Clock Select (DCS)

The DCS is a smart multiplexer function available in the primary clock routing. It switches between two independent input clock sources without any glitches or runt pulses. This is achieved regardless of when the select signal is toggled. There are two DCS blocks per quadrant; in total, there are eight DCS blocks per device. The inputs to the DCS block come from the center muxes. The output of the DCS is connected to primary clocks CLK6 and CLK7 (see Figure 2-13).

Figure 2-14 shows the timing waveforms of the default DCS operating mode. The DCS block can be programmed to other modes. For more information about the DCS, please see the list of additional technical documentation at the end of this data sheet.

Figure 2-14. DCS Waveforms



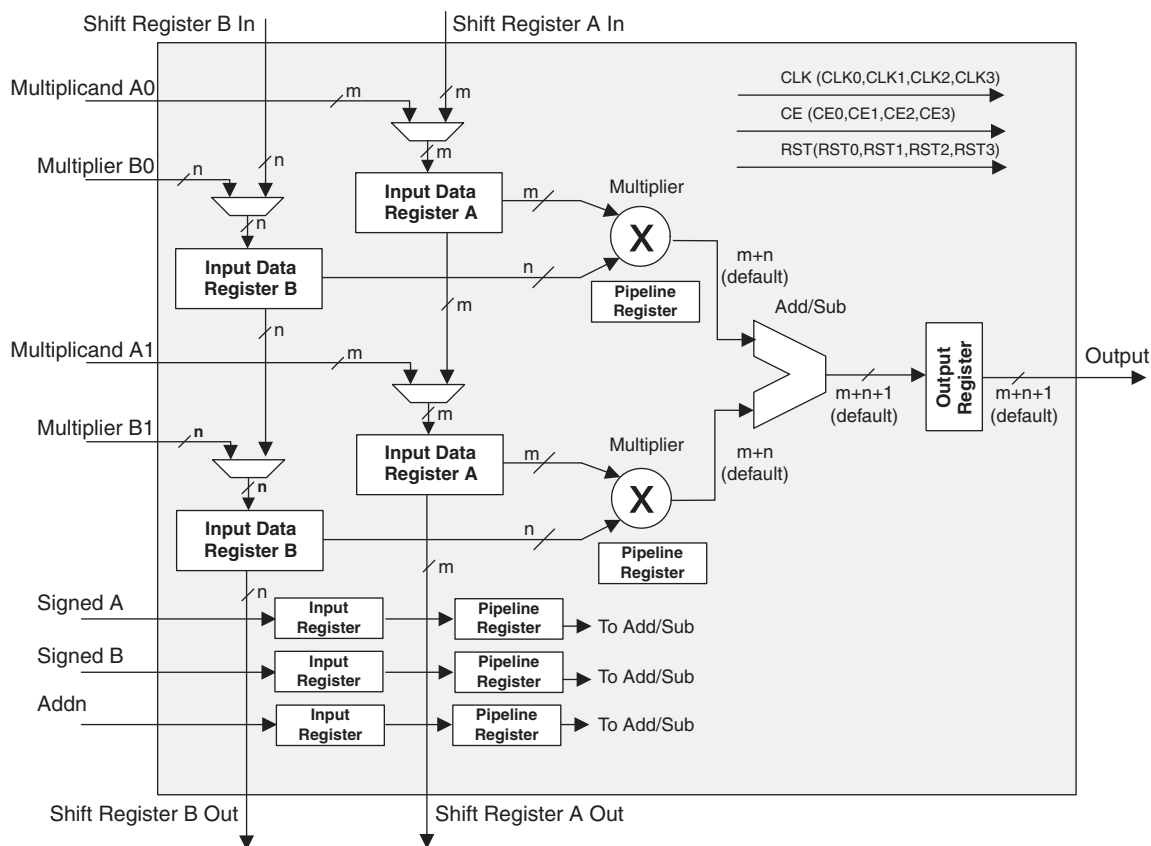
Secondary Clock/Control Routing

Secondary clocks in the LatticeECP2 devices are region-based resources. The benefit of region-based resources is the relatively low injection delay and skew within the region, as compared to primary clocks. EBR/DSP rows and a special vertical routing channel bound the secondary clock regions. This special vertical routing channel aligns with either the left edge of the center DSP block in the DSP row or the center of the DSP row. Figure 2-15 shows

MULTADDSUB sysDSP Element

In this case, the operands A0 and B0 are multiplied and the result is added/subtracted with the result of the multiplier operation of operands A1 and A2. The user can enable the input, output and pipeline registers. Figure 2-25 shows the MULTADDSUB sysDSP element.

Figure 2-25. MULTADDSUB



LVDS25E

The top and bottom sides of LatticeECP2/M devices support LVDS outputs via emulated complementary LVCMOS outputs in conjunction with a parallel resistor across the driver outputs. The scheme shown in Figure 3-1 is one possible solution for point-to-point signals.

Figure 3-1. LVDS25E Output Termination Example

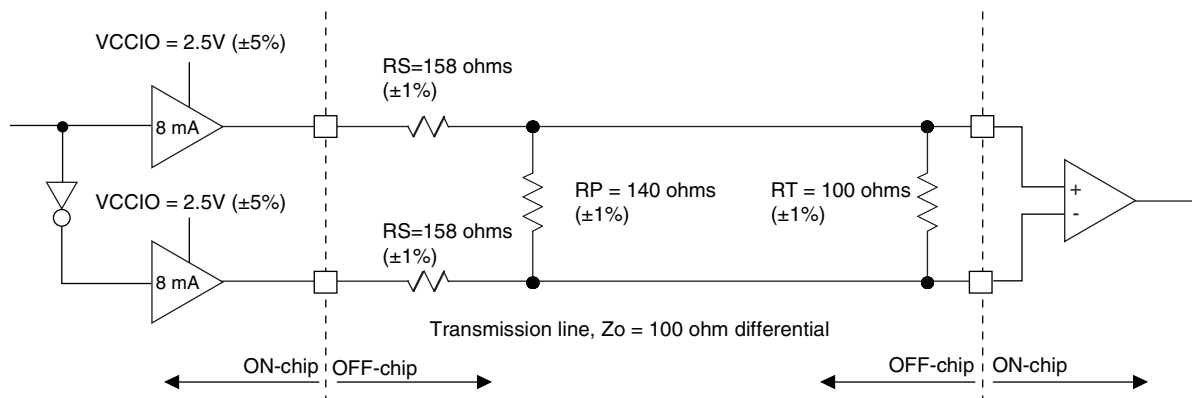


Table 3-2. LVDS25E DC Conditions

Parameter	Description	Typical	Units
V _{CCIO}	Output Driver Supply (+/-5%)	2.50	V
Z _{OUT}	Driver Impedance	20	Ω
R _S	Driver Series Resistor (+/-1%)	158	Ω
R _P	Driver Parallel Resistor (+/-1%)	140	Ω
R _T	Receiver Termination (+/-1%)	100	Ω
V _{OH}	Output High Voltage	1.43	V
V _{OL}	Output Low Voltage	1.07	V
V _{OD}	Output Differential Voltage	0.35	V
V _{CM}	Output Common Mode Voltage	1.25	V
Z _{BACK}	Back Impedance	100.5	Ω
I _{DC}	DC Output Current	6.03	mA

LVCMOS33D

All I/O banks support emulated differential I/O using the LVCMOS33D I/O type. This option, along with the external resistor network, provides the system designer the flexibility to place differential outputs on an I/O bank with 3.3V VCCIO. The default drive current for LVCMOS33D output is 12mA with the option to change the device strength to 4mA, 8mA, 16mA or 20mA. Follow the LVCMOS33 specifications for the DC characteristics of the LVCMOS33D.

RSDS

The LatticeECP2/M devices support differential RSDS standard. This standard is emulated using complementary LVCMOS outputs in conjunction with a parallel resistor across the driver outputs. The RSDS input standard is supported by the LVDS differential input buffer. The scheme shown in Figure 3-4 is one possible solution for RSDS standard implementation. Resistor values in Figure 3-4 are industry standard values for 1% resistors.

Figure 3-4. RSDS (Reduced Swing Differential Signaling)

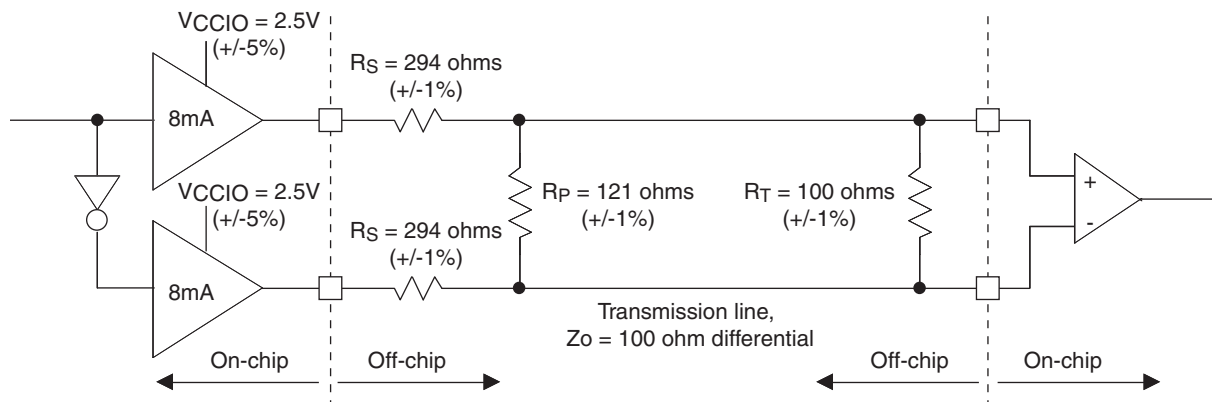


Table 3-5. RSDS DC Conditions¹

Over Recommended Operating Conditions

Parameter	Description	Typical	Units
V_{CCIO}	Output Driver Supply (+/-5%)	2.50	V
Z_{OUT}	Driver Impedance	20	Ω
R_S	Driver Series Resistor (+/-1%)	294	Ω
R_P	Driver Parallel Resistor (+/-1%)	121	Ω
R_T	Receiver Termination (+/-1%)	100	Ω
V_{OH}	Output High Voltage	1.35	V
V_{OL}	Output Low Voltage	1.15	V
V_{OD}	Output Differential Voltage	0.20	V
V_{CM}	Output Common Mode Voltage	1.25	V
Z_{BACK}	Back Impedance	101.5	Ω
I_{DC}	DC Output Current	3.66	mA

1. For input buffer, see LVDS table.

LatticeECP2/M External Switching Characteristics⁹

Over Recommended Operating Conditions

Parameter	Description	Device	-7		-6		-5		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
General I/O Pin Parameters (using Primary Clock without PLL) ¹									
t _{CO}	Clock to Output - PIO Output Register	LFE2-6	—	3.50	—	3.90	—	4.20	ns
		LFE2-12	—	3.50	—	3.90	—	4.20	ns
		LFE2-20	—	3.50	—	3.90	—	4.20	ns
		LFE2-35	—	3.50	—	3.90	—	4.20	ns
		LFE2-50	—	3.50	—	3.90	—	4.20	ns
		LFE2-70	—	3.70	—	4.10	—	4.40	ns
		LFE2M20	—	3.90	—	4.30	—	4.70	ns
		LFE2M35	—	3.90	—	4.30	—	4.70	ns
		LFE2M50	—	4.50	—	5.00	—	5.40	ns
		LFE2M70	—	4.50	—	5.00	—	5.40	ns
		LFE2M100	—	4.50	—	5.00	—	5.40	ns
t _{SU}	Clock to Data Setup - PIO Input Register	LFE2-6	0.00	—	0.00	—	0.00	—	ns
		LFE2-12	0.00	—	0.00	—	0.00	—	ns
		LFE2-20	0.00	—	0.00	—	0.00	—	ns
		LFE2-35	0.00	—	0.00	—	0.00	—	ns
		LFE2-50	0.00	—	0.00	—	0.00	—	ns
		LFE2-70	0.00	—	0.00	—	0.00	—	ns
		LFE2M20	0.00	—	0.00	—	0.00	—	ns
		LFE2M35	0.00	—	0.00	—	0.00	—	ns
		LFE2M50	0.00	—	0.00	—	0.00	—	ns
		LFE2M70	0.00	—	0.00	—	0.00	—	ns
		LFE2M100	0.00	—	0.00	—	0.00	—	ns
t _H	Clock to Data Hold - PIO Input Register	LFE2-6	1.40	—	1.70	—	1.90	—	ns
		LFE2-12	1.40	—	1.70	—	1.90	—	ns
		LFE2-20	1.40	—	1.70	—	1.90	—	ns
		LFE2-35	1.40	—	1.70	—	1.90	—	ns
		LFE2-50	1.40	—	1.70	—	1.90	—	ns
		LFE2-70	1.40	—	1.70	—	1.90	—	ns
		LFE2M20	1.40	—	1.70	—	1.90	—	ns
		LFE2M35	1.40	—	1.70	—	1.90	—	ns
		LFE2M50	1.80	—	2.10	—	2.30	—	ns
		LFE2M70	1.80	—	2.10	—	2.30	—	ns
		LFE2M100	1.80	—	2.10	—	2.30	—	ns

LatticeECP2/M Family Timing Adders^{1, 2, 3} (Continued)
Over Recommended Operating Conditions

Buffer Type	Description	-7	-6	-5	Units
HSTL15_I	HSTL_15 class I 4mA drive	-0.22	-0.25	-0.27	ns
HSTL15D_I	Differential HSTL 15 class I 4mA drive	-0.22	-0.25	-0.27	ns
SSTL33_I	SSTL_3 class I	-0.12	-0.15	-0.18	ns
SSTL33_II	SSTL_3 class II	-0.20	-0.23	-0.27	ns
SSTL33D_I	Differential SSTL_3 class I	-0.12	-0.15	-0.18	ns
SSTL33D_II	Differential SSTL_3 class II	-0.20	-0.23	-0.27	ns
SSTL25_I	SSTL_2 class I 8mA drive	-0.16	-0.19	-0.22	ns
SSTL25_II	SSTL_2 class II 16mA drive	-0.19	-0.22	-0.25	ns
SSTL25D_I	Differential SSTL_2 class I 8mA drive	-0.16	-0.19	-0.22	ns
SSTL25D_II	Differential SSTL_2 class II 16mA drive	-0.19	-0.22	-0.25	ns
SSTL18_I	SSTL_1.8 class I	-0.14	-0.17	-0.20	ns
SSTL18_II	SSTL_1.8 class II 8mA drive	-0.20	-0.23	-0.25	ns
SSTL18D_I	Differential SSTL_1.8 class I	-0.14	-0.17	-0.20	ns
SSTL18D_II	Differential SSTL_1.8 class II 8mA drive	-0.20	-0.23	-0.25	ns
LVTTTL33_4mA	LVTTTL 4mA drive	0.52	0.60	0.68	ns
LVTTTL33_8mA	LVTTTL 8mA drive	0.06	0.08	0.09	ns
LVTTTL33_12mA	LVTTTL 12mA drive	0.04	0.04	0.05	ns
LVTTTL33_16mA	LVTTTL 16mA drive	0.03	0.02	0.02	ns
LVTTTL33_20mA	LVTTTL 20mA drive	-0.09	-0.09	-0.10	ns
LVC MOS33_4mA	LVC MOS 3.3 4mA drive, fast slew rate	0.52	0.60	0.68	ns
LVC MOS33_8mA	LVC MOS 3.3 8mA drive, fast slew rate	0.06	0.08	0.09	ns
LVC MOS33_12mA	LVC MOS 3.3 12mA drive, fast slew rate	0.04	0.04	0.05	ns
LVC MOS33_16mA	LVC MOS 3.3 16mA drive, fast slew rate	0.03	0.02	0.02	ns
LVC MOS33_20mA	LVC MOS 3.3 20mA drive, fast slew rate	-0.09	-0.09	-0.10	ns
LVC MOS25_4mA	LVC MOS 2.5 4mA drive, fast slew rate	0.41	0.47	0.53	ns
LVC MOS25_8mA	LVC MOS 2.5 8mA drive, fast slew rate	0.01	0.01	0.00	ns
LVC MOS25_12mA	LVC MOS 2.5 12mA drive, fast slew rate	0.00	0.00	0.00	ns
LVC MOS25_16mA	LVC MOS 2.5 16mA drive, fast slew rate	0.04	0.04	0.04	ns
LVC MOS25_20mA	LVC MOS 2.5 20mA drive, fast slew rate	-0.09	-0.10	-0.11	ns
LVC MOS18_4mA	LVC MOS 1.8 4mA drive, fast slew rate	0.37	0.40	0.43	ns
LVC MOS18_8mA	LVC MOS 1.8 8mA drive, fast slew rate	0.10	0.12	0.13	ns
LVC MOS18_12mA	LVC MOS 1.8 12mA drive, fast slew rate	-0.02	-0.02	-0.02	ns
LVC MOS18_16mA	LVC MOS 1.8 16mA drive, fast slew rate	-0.02	-0.03	-0.03	ns
LVC MOS15_4mA	LVC MOS 1.5 4mA drive, fast slew rate	0.29	0.31	0.32	ns
LVC MOS15_8mA	LVC MOS 1.5 8mA drive, fast slew rate	0.05	0.05	0.06	ns
LVC MOS12_2mA	LVC MOS 1.2 2mA drive, fast slew rate	0.58	0.69	0.79	ns
LVC MOS12_6mA	LVC MOS 1.2 6mA drive, fast slew rate	0.13	0.19	0.26	ns
LVC MOS33_4mA	LVC MOS 3.3 4mA drive, slow slew rate	2.17	2.44	2.71	ns
LVC MOS33_8mA	LVC MOS 3.3 8mA drive, slow slew rate	2.50	2.67	2.83	ns
LVC MOS33_12mA	LVC MOS 3.3 12mA drive, slow slew rate	1.72	1.88	2.05	ns
LVC MOS33_16mA	LVC MOS 3.3 16mA drive, slow slew rate	1.64	1.63	1.62	ns
LVC MOS33_20mA	LVC MOS 3.3 20mA drive, slow slew rate	1.33	1.36	1.39	ns

LatticeECP2/M Family Timing Adders^{1, 2, 3} (Continued)
Over Recommended Operating Conditions

Buffer Type	Description	-7	-6	-5	Units
LVC MOS25_4mA	LVC MOS 2.5 4mA drive, slow slew rate	2.18	2.26	2.33	ns
LVC MOS25_8mA	LVC MOS 2.5 8mA drive, slow slew rate	2.19	2.35	2.51	ns
LVC MOS25_12mA	LVC MOS 2.5 12mA drive, slow slew rate	1.50	1.66	1.82	ns
LVC MOS25_16mA	LVC MOS 2.5 16mA drive, slow slew rate	1.60	1.59	1.58	ns
LVC MOS25_20mA	LVC MOS 2.5 20mA drive, slow slew rate	1.43	1.39	1.34	ns
LVC MOS18_4mA	LVC MOS 1.8 4mA drive, slow slew rate	2.22	2.27	2.32	ns
LVC MOS18_8mA	LVC MOS 1.8 8mA drive, slow slew rate	1.93	2.08	2.23	ns
LVC MOS18_12mA	LVC MOS 1.8 12mA drive, slow slew rate	1.43	1.51	1.58	ns
LVC MOS18_16mA	LVC MOS 1.8 16mA drive, slow slew rate	1.47	1.46	1.45	ns
LVC MOS15_4mA	LVC MOS 1.5 4mA drive, slow slew rate	2.32	2.38	2.43	ns
LVC MOS15_8mA	LVC MOS 1.5 8mA drive, slow slew rate	1.84	1.98	2.12	ns
LVC MOS12_2mA	LVC MOS 1.2 2mA drive, slow slew rate	2.52	2.63	2.74	ns
LVC MOS12_6mA	LVC MOS 1.2 6mA drive, slow slew rate	1.69	1.83	1.96	ns
PCI33	PCI33	0.04	0.04	0.04	ns

1. Timing Adders are characterized but not tested on every device.
 2. LVC MOS timing measured with the load specified in Switching Test Condition table.
 3. All other standards tested according to the appropriate specifications.
 4. These timing adders are measured with the recommended resistor values.
- Timing v.A 0.11

LFE2-20E/SE Logic Signal Connections: 256 fpBGA (Cont.)

LFE2-20E/SE					
Ball Number	Ball Number	Ball/Pad Function	Bank	Dual Function	Differential
GND	GND	GNDIO5	-		
R4	R4	PB33A	5	BDQS33	T
L6	L6	PB34A	5	BDQ33	T
T4	T4	PB33B	5	BDQ33	C
L7	L7	PB34B	5	BDQ33	C
N7	N7	PB35A	5	PCLKT5_0/BDQ33	T
VCCIO	VCCIO	VCCIO5	5		
M8	M8	PB35B	5	PCLKC5_0/BDQ33	C
GND	GND	GNDIO5	-		
P7	P7	PB40A	4	PCLKT4_0/BDQ42	T
R8	R8	PB40B	4	PCLKC4_0/BDQ42	C
VCCIO	VCCIO	VCCIO4	4		
T5	T5	PB41A	4	BDQ42	T
T6	T6	PB41B	4	BDQ42	C
T8	T8	PB42A	4	BDQS42	T
GND	GND	GNDIO4	-		
R7	R7	PB43A	4	BDQ42	T
T9	T9	PB42B	4	BDQ42	C
T7	T7	PB43B	4	BDQ42	C
L8	L8	PB44A	4	BDQ42	T
VCCIO	VCCIO	VCCIO4	4		
P8	P8	PB45A	4	BDQ42	T
L9	L9	PB44B	4	BDQ42	C
N8	N8	PB45B	4	BDQ42	C
R9	R9	PB46A	4	BDQ42	T
GND	GND	GNDIO4	-		
R10	R10	PB46B	4	BDQ42	C
-	VCC	VCCIO	4		
-	GND	GNDIO4	4		
N9	N9	PB56A	4	BDQ60	T
T10	T10	PB57A	4	BDQ60	T
M9	M9	PB56B	4	BDQ60	C
R11	R11	PB57B	4	BDQ60	C
P10	P10	PB58A	4	BDQ60	T
N11	N11	PB59A	4	BDQ60	T
VCCIO	VCCIO	VCCIO4	4		
N10	N10	PB58B	4	BDQ60	C
P11	P11	PB59B	4	BDQ60	C
T11	T11	PB60A	4	BDQS60	T
GND	GND	GNDIO4	-		
M11	M11	PB61A	4	BDQ60	T
T12	T12	PB60B	4	BDQ60	C

LFE2-20E/SE Logic Signal Connections: 256 fpBGA (Cont.)

LFE2-20E/SE					
Ball Number	Ball Number	Ball/Pad Function	Bank	Dual Function	Differential
P5	P5	VCCIO5	5		
K5	K5	VCCIO6	6		
M3	M3	VCCIO6	6		
E3	E3	VCCIO7	7		
G5	G5	VCCIO7	7		
T15	T15	VCCIO8	8		
A1	A1	GND	-		
A16	A16	GND	-		
B12	B12	GND	-		
B5	B5	GND	-		
C8	C8	GND	-		
E15	E15	GND	-		
E2	E2	GND	-		
H14	H14	GND	-		
H8	H8	GND	-		
H9	H9	GND	-		
J3	J3	GND	-		
J8	J8	GND	-		
J9	J9	GND	-		
M15	M15	GND	-		
M2	M2	GND	-		
P9	P9	GND	-		
R12	R12	GND	-		
R5	R5	GND	-		
T1	T1	GND	-		
T16	T16	GND	-		

* Supports true LVDS. Other differential signals must be emulated with external resistors.

** These dedicated input pins can be used for GPLLs or GDLLs within the respective quadrant.

Note: VCCIO and GND pads are used to determine the average DC current drawn by I/Os between GND/VCCIO connections, or between the last GND/VCCIO in an I/O bank and the end of an I/O bank. The substrate pads listed in the Pin Table do not necessarily have a one to one connection with a package ball or pin.

LFE2-35E/SE and LFE2-50E/SE Logic Signal Connections: 484 fpBGA (Cont.)

LFE2-35E/SE					LFE2-50E/SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
W13	PB46A	4	BDQ42	T	PB55A	4	BDQ51	T
GNDIO	GNDIO4	-			GNDIO4	-		
W14	PB46B	4	BDQ42	C	PB55B	4	BDQ51	C
AB18	PB48A	4	BDQ51	T	PB57A	4	BDQ60	T
AB19	PB48B	4	BDQ51	C	PB57B	4	BDQ60	C
V14	PB49A	4	BDQ51	T	PB58A	4	BDQ60	T
W15	PB49B	4	BDQ51	C	PB58B	4	BDQ60	C
VCCIO	VCCIO4	4			VCCIO	4		
Y15	PB50A	4	BDQ51	T	PB59A	4	BDQ60	T
AA15	PB50B	4	BDQ51	C	PB59B	4	BDQ60	C
GNDIO	GNDIO4	-			GNDIO4	-		
AA16	PB51A	4	BDQS51	T	PB60A	4	BDQS60	T
AA17	PB51B	4	BDQ51	C	PB60B	4	BDQ60	C
AB20	PB52A	4	BDQ51	T	PB61A	4	BDQ60	T
AB21	PB52B	4	BDQ51	C	PB61B	4	BDQ60	C
U15	PB53A	4	BDQ51	T	PB62A	4	BDQ60	T
U16	PB53B	4	BDQ51	C	PB62B	4	BDQ60	C
VCCIO	VCCIO4	4			VCCIO	4		
Y16	PB54A	4	BDQ51	T	PB63A	4	BDQ60	T
W16	PB54B	4	BDQ51	C	PB63B	4	BDQ60	C
AA18	PB55A	4	BDQ51	T	PB64A	4	BDQ60	T
AA20	PB55B	4	BDQ51	C	PB64B	4	BDQ60	C
GNDIO	GNDIO4	-			GNDIO4	-		
VCCIO	VCCIO4	4			VCCIO	4		
AA21	PB66A	4	BDQ69	T	PB75A	4	BDQ78	T
AA22	PB66B	4	BDQ69	C	PB75B	4	BDQ78	C
V16	PB67A	4	BDQ69	T	PB76A	4	BDQ78	T
V17	PB67B	4	BDQ69	C	PB76B	4	BDQ78	C
VCCIO	VCCIO4	4			VCCIO	4		
Y18	PB68A	4	BDQ69	T	PB77A	4	BDQ78	T
Y17	PB68B	4	BDQ69	C	PB77B	4	BDQ78	C
GNDIO	GNDIO4	-			GNDIO4	-		
Y19	PB69A	4	BDQS69	T	PB78A	4	BDQS78	T
Y20	PB69B	4	BDQ69	C	PB78B	4	BDQ78	C
W17	PB70A	4	BDQ69	T	PB79A	4	BDQ78	T
W18	PB70B	4	BDQ69	C	PB79B	4	BDQ78	C
Y21	PB71A	4	BDQ69	T	PB80A	4	BDQ78	T
Y22	PB71B	4	BDQ69	C	PB80B	4	BDQ78	C
VCCIO	VCCIO4	4			VCCIO	4		
U18	PB72A	4	BDQ69	T	PB81A	4	BDQ78	T
V18	PB72B	4	BDQ69	C	PB81B	4	BDQ78	C
T15	PB73A	4	VREF2_4/BDQ69	T	PB82A	4	VREF2_4/BDQ78	T
T16	PB73B	4	VREF1_4/BDQ69	C	PB82B	4	VREF1_4/BDQ78	C
GNDIO	GNDIO4	-			GNDIO4	-		
W19	CFG2	8			CFG2	8		
V19	CFG1	8			CFG1	8		

LFE2-70E/SE Logic Signal Connections: 900 fpBGA (Cont.)

LFE2-70E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential
C5	PT11B	0		C
D5	PT11A	0		T
E9	PT10B	0		C
G9	PT10A	0		T
GND	GNDIO0	-		
B10	PT9B	0		C
A10	PT9A	0		T
D9	PT8B	0		C
C9	PT8A	0		T
VCCIO	VCCIO0	0		
F9	PT7B	0		C
H9	PT7A	0		T
B9	PT6B	0		C
A9	PT6A	0		T
GND	GNDIO0	-		
E8	PT5B	0		C
G8	PT5A	0		T
A8	PT4B	0		C
B8	PT4A	0		T
VCCIO	VCCIO0	0		
F8	PT3B	0		C
F7	PT3A	0		T
J10	PT2B	0	VREF2_0	C
J9	PT2A	0	VREF1_0	T
AA11	VCC	-		
AA20	VCC	-		
K11	VCC	-		
K21	VCC	-		
K22	VCC	-		
L11	VCC	-		
L12	VCC	-		
L13	VCC	-		
L18	VCC	-		
L19	VCC	-		
L20	VCC	-		
M11	VCC	-		
M20	VCC	-		
N11	VCC	-		
N20	VCC	-		
V11	VCC	-		
V20	VCC	-		
W11	VCC	-		
W20	VCC	-		

LFE2M-20E/SE and LFE2M-35E/SE Logic Signal Connections: 256 fpBGA (Cont.)

LFE2M20E/SE					LFE2M35E/SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
N11	CCLK	8			CCLK	8		
M11	INITN	8			INITN	8		
N13	DONE	8			DONE	8		
GNDIO	GNDIO8	-			GNDIO8	-		
M12	PR53B	8	WRITEN	C	PR68B	8	WRITEN	C
M13	PR53A	8	CS1N	T	PR68A	8	CS1N	T
N14	PR52B	8	CSN	C	PR67B	8	CSN	C
N15	PR52A	8	D0/SPIFASTN	T	PR67A	8	D0/SPIFASTN	T
VCCIO	VCCIO8	8			VCCIO8	8		
N16	PR51B	8	D1	C	PR66B	8	D1	C
M16	PR51A	8	D2	T	PR66A	8	D2	T
L12	PR50B	8	D3	C	PR65B	8	D3	C
GNDIO	GNDIO8	-			GNDIO8	-		
L13	PR50A	8	D4	T	PR65A	8	D4	T
L16	PR49B	8	D5	C	PR64B	8	D5	C
K16	PR49A	8	D6	T	PR64A	8	D6	T
L14	PR48B	8	D7/SPID0***	C	PR63B	8	D7/SPID0***	C
VCCIO	VCCIO8	8			VCCIO8	8		
L15	PR48A	8	DI/CSSPI0N	T	PR63A	8	DI/CSSPI0N	T
K13	PR47B	8	DOUT/CSN/CSSPI1N	C	PR62B	8	DOUT/CSN/CSSPI1N	C
K14	PR47A	8	BUSY/SISPI	T	PR62A	8	BUSY/SISPI	T
K11	RLM0_PLLCAP	3			RLM0_PLLCAP	3		
K15	PR45B	3	RLM0_GDLLC_FB_A	C	PR60B	3	RLM0_GDLLC_FB_A/RDQ57	C
GNDIO	GNDIO3	-			GNDIO3	-		
J16	PR45A	3	RLM0_GDLLT_FB_A	T	PR60A	3	RLM0_GDLLT_FB_A/RDQ57	T
H16	PR44B	3	RLM0_GDLLC_IN_A	C (LVDS)*	PR59B	3	RLM0_GDLLC_IN_A**/RDQ57	C (LVDS)*
J15	PR44A	3	RLM0_GDLLT_IN_A	T (LVDS)*	PR59A	3	RLM0_GDLLT_IN_A**/RDQ57	T (LVDS)*
J14	PR43B	3	RLM0_GPLLC_IN_A	C	PR58B	3	RLM0_GPLLC_IN_A**/RDQ57	C
VCCIO	VCCIO3	3			VCCIO3	3		
J13	PR43A	3	RLM0_GPLLT_IN_A	T	PR58A	3	RLM0_GPLLT_IN_A**/RDQ57	T
H13	PR42B	3	RLM0_GPLLC_FB_A	C (LVDS)*	PR57B	3	RLM0_GPLLC_FB_A/RDQ57	C (LVDS)*
H12	PR42A	3	RLM0_GPLLT_FB_A	T (LVDS)*	PR57A	3	RLM0_GPLLT_FB_A/RDQS57***	T (LVDS)*
GNDIO	GNDIO3	-			GNDIO3	-		
VCCIO	VCCIO3	3			VCCIO3	3		
G16	PR32B	3	RLM1_SPLLC_FB_A	C	PR42B	3	RLM2_SPLLC_FB_A	C
VCCIO	VCCIO3	3			VCCIO3	3		
H15	PR32A	3	RLM1_SPLLT_FB_A	T	PR42A	3	RLM2_SPLLT_FB_A	T
E16	PR31B	3	RLM1_SPLLC_IN_A	C (LVDS)*	PR41B	3	RLM2_SPLLC_IN_A	C (LVDS)*
F15	PR31A	3	RLM1_SPLLT_IN_A	T (LVDS)*	PR41A	3	RLM2_SPLLT_IN_A	T (LVDS)*
GNDIO	GNDIO3	-			GNDIO3	-		
VCCIO	VCCIO3	3			VCCIO3	3		
F16	PR28B	3	VREF2_3	C	PR38B	3	VREF2_3	C
G15	PR28A	3	VREF1_3	T	PR38A	3	VREF1_3	T
J11	PR27B	3	PCLKC3_0	C (LVDS)*	PR37B	3	PCLKC3_0	C (LVDS)*
J12	PR27A	3	PCLKT3_0	T (LVDS)*	PR37A	3	PCLKT3_0	T (LVDS)*
G14	PR25B	2	PCLKC2_0/RDQ22	C	PR35B	2	PCLKC2_0/RDQ32	C
G13	PR25A	2	PCLKT2_0/RDQ22	T	PR35A	2	PCLKT2_0/RDQ32	T
GNDIO	GNDIO2	-			GNDIO2	-		

LFE2M20E/SE and LFE2M35E/SE Logic Signal Connections: 484 fpBGA (Cont.)

LFE2M20E/SE					LFE2M35E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential	
G18	VCCIO2	2			VCCIO2	2			
J15	VCCIO2	2			VCCIO2	2			
K19	VCCIO2	2			VCCIO2	2			
N19	VCCIO3	3			VCCIO3	3			
P15	VCCIO3	3			VCCIO3	3			
T18	VCCIO3	3			VCCIO3	3			
V21	VCCIO3	3			VCCIO3	3			
AA18	VCCIO4	4			VCCIO4	4			
R14	VCCIO4	4			VCCIO4	4			
V16	VCCIO4	4			VCCIO4	4			
W13	VCCIO4	4			VCCIO4	4			
AA5	VCCIO5	5			VCCIO5	5			
R9	VCCIO5	5			VCCIO5	5			
V7	VCCIO5	5			VCCIO5	5			
W10	VCCIO5	5			VCCIO5	5			
N4	VCCIO6	6			VCCIO6	6			
P8	VCCIO6	6			VCCIO6	6			
T5	VCCIO6	6			VCCIO6	6			
V2	VCCIO6	6			VCCIO6	6			
E2	VCCIO7	7			VCCIO7	7			
G5	VCCIO7	7			VCCIO7	7			
J8	VCCIO7	7			VCCIO7	7			
K4	VCCIO7	7			VCCIO7	7			
AA22	VCCIO8	8			VCCIO8	8			
U19	VCCIO8	8			VCCIO8	8			
H11	VCCAUX	-			VCCAUX	-			
H12	VCCAUX	-			VCCAUX	-			
L15	VCCAUX	-			VCCAUX	-			
L8	VCCAUX	-			VCCAUX	-			
M15	VCCAUX	-			VCCAUX	-			
M8	VCCAUX	-			VCCAUX	-			
R11	VCCAUX	-			VCCAUX	-			
R12	VCCAUX	-			VCCAUX	-			
A1	GND	-			GND	-			
A10	GND	-			GND	-			
A16	GND	-			GND	-			
A22	GND	-			GND	-			
AA19	GND	-			GND	-			
AA4	GND	-			GND	-			
AB1	GND	-			GND	-			
AB22	GND	-			GND	-			
B13	GND	-			GND	-			
B19	GND	-			GND	-			
B4	GND	-			GND	-			
D16	GND	-			GND	-			
D2	GND	-			GND	-			
D21	GND	-			GND	-			
D7	GND	-			GND	-			

LFE2M35E/SE and LFE2M50E/SE Logic Signal Connections: 672 fpBGA (Cont.)

LFE2M35E/SE					LFE2M50E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential	
AF4	PB17B	5	BDQ15	C	PB17B	5	BDQ15	C	
VCCIO	VCCIO5	5			VCCIO5	5			
AF5	PB18A	5	BDQ15	T	PB18A	5	BDQ15	T	
AF6	PB18B	5	BDQ15	C	PB18B	5	BDQ15	C	
Y12	PB19A	5	BDQ15	T	PB19A	5	BDQ15	T	
GNDIO	GNDIO5	-			GNDIO5	-			
AB11	PB19B	5	BDQ15	C	PB19B	5	BDQ15	C	
-	-	-			VCCIO5	5			
-	-	-			GNDIO5	-			
AD7	PB20A	5	BDQ24	T	PB29A	5	BDQ33	T	
AF7	PB20B	5	BDQ24	C	PB29B	5	BDQ33	C	
AD8	PB21A	5	BDQ24	T	PB30A	5	BDQ33	T	
AA12	PB21B	5	BDQ24	C	PB30B	5	BDQ33	C	
AE8	PB22A	5	BDQ24	T	PB31A	5	BDQ33	T	
VCCIO	VCCIO5	5			VCCIO5	5			
AF8	PB22B	5	BDQ24	C	PB31B	5	BDQ33	C	
AD9	PB23A	5	BDQ24	T	PB32A	5	BDQ33	T	
AC10	PB23B	5	BDQ24	C	PB32B	5	BDQ33	C	
AC11	PB24A	5	BDQS24	T	PB33A	5	BDQS33	T	
GNDIO	GNDIO5	-			GNDIO5	-			
AB12	PB24B	5	BDQ24	C	PB33B	5	BDQ33	C	
AD10	PB25A	5	BDQ24	T	PB34A	5	BDQ33	T	
Y13	PB25B	5	BDQ24	C	PB34B	5	BDQ33	C	
AF9	PB26A	5	BDQ24	T	PB35A	5	BDQ33	T	
VCCIO	VCCIO5	5			VCCIO5	5			
AE9	PB26B	5	BDQ24	C	PB35B	5	BDQ33	C	
AF10	PB27A	5	BDQ24	T	PB36A	5	BDQ33	T	
AE10	PB27B	5	BDQ24	C	PB36B	5	BDQ33	C	
AD11	PB28A	5	BDQ24	T	PB37A	5	BDQ33	T	
GNDIO	GNDIO5	-			GNDIO5	-			
AF11	PB28B	5	BDQ24	C	PB37B	5	BDQ33	C	
VCCIO	VCCIO5	5			VCCIO5	5			
GNDIO	GNDIO5	-			GNDIO5	-			
AA13	PB33A	5	BDQS33****	T	PB42A	5	BDQS42****	T	
AB13	PB33B	5	BDQ33	C	PB42B	5	BDQ42	C	
W14	PB34A	5	VREF2_5/BDQ33	T	PB43A	5	VREF2_5/BDQ42	T	
AC12	PB34B	5	VREF1_5/BDQ33	C	PB43B	5	VREF1_5/BDQ42	C	
AF12	PB35A	5	PCLKT5_0/BDQ33	T	PB44A	5	PCLKT5_0/BDQ42	T	
AD12	PB35B	5	PCLKC5_0/BDQ33	C	PB44B	5	PCLKC5_0/BDQ42	C	
VCCIO	VCCIO5	5			VCCIO5	5			
GNDIO	GNDIO5	-			GNDIO5	-			
AC13	PB40A	4	PCLKT4_0/BDQ42	T	PB49A	4	PCLKT4_0/BDQ51	T	
VCCIO	VCCIO4	4			VCCIO4	4			
Y14	PB40B	4	PCLKC4_0/BDQ42	C	PB49B	4	PCLKC4_0/BDQ51	C	
AB20	PB57A	4	BDQ60	T	PB50A	4	VREF2_4/BDQ51	T	
AC14	PB41B	4	VREF1_4/BDQ42	C	PB50B	4	VREF1_4/BDQ51	C	
AB14	PB42A	4	BDQS42****	T	PB51A	4	BDQS51****	T	
GNDIO	GNDIO4	-			GNDIO4	-			

LFE2M70E/SE and LFE2M100E/SE Logic Signal Connections: 1152 fpBGA

LFE2M70E/SE				LFE2M100E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
VCCIO	VCCIO7	7			VCCIO7	7		
F4	PL9A	7	VREF2_7	T	PL9A	7	VREF2_7	T
F3	PL9B	7	VREF1_7	C	PL9B	7	VREF1_7	C
GNDIO	GNDIO7	-			GNDIO7	-		
E1	PL11A	7	LUM0_SPLLT_IN_A/LDQ15	T (LVDS)*	PL11A	7	LUM0_SPLLT_IN_A/LDQ15	T (LVDS)*
E2	PL11B	7	LUM0_SPLLC_IN_A/LDQ15	C (LVDS)*	PL11B	7	LUM0_SPLLC_IN_A/LDQ15	C (LVDS)*
K9	PL12A	7	LUM0_SPLLT_FB_A/LDQ15	T	PL12A	7	LUM0_SPLLT_FB_A/LDQ15	T
H7	PL12B	7	LUM0_SPLLC_FB_A/LDQ15	C	PL12B	7	LUM0_SPLLC_FB_A/LDQ15	C
VCCIO	VCCIO7	7			VCCIO7	7		
F1	PL13A	7	LDQ15	T (LVDS)*	PL13A	7	LDQ15	T (LVDS)*
F2	PL13B	7	LDQ15	C (LVDS)*	PL13B	7	LDQ15	C (LVDS)*
J8	PL14A	7	LDQ15	T	PL14A	7	LDQ15	T
H6	PL14B	7	LDQ15	C	PL14B	7	LDQ15	C
GNDIO	GNDIO7	-			GNDIO7	-		
G2	PL15A	7	LDQS15	T (LVDS)*	PL15A	7	LDQS15	T (LVDS)*
G1	PL15B	7	LDQ15	C (LVDS)*	PL15B	7	LDQ15	C (LVDS)*
J7	PL16A	7	LDQ15	T	PL16A	7	LDQ15	T
VCCIO	VCCIO7	7			VCCIO7	7		
L8	PL16B	7	LDQ15	C	PL16B	7	LDQ15	C
L9	PL17A	7	LDQ15	T (LVDS)*	PL17A	7	LDQ15	T (LVDS)*
L10	PL17B	7	LDQ15	C (LVDS)*	PL17B	7	LDQ15	C (LVDS)*
H5	PL18A	7	LDQ15	T	PL18A	7	LDQ15	T
GNDIO	GNDIO7	-			GNDIO7	-		
J6	PL18B	7	LDQ15	C	PL18B	7	LDQ15	C
H2	NC	-			PL19A	7	LDQ23	T (LVDS)*
H1	NC	-			PL19B	7	LDQ23	C (LVDS)*
G5	NC	-			PL20A	7	LDQ23	T
G6	NC	-			PL20B	7	LDQ23	C
M9	NC	-			PL21A	7	LDQ23	T (LVDS)*
-	-	-			VCCIO7	7		
M10	NC	-			PL21B	7	LDQ23	C (LVDS)*
H3	NC	-			PL22A	7	LDQ23	T
H4	NC	-			PL22B	7	LDQ23	C
J2	PL19A	7		T (LVDS)*	PL23A	7	LDQS23	T (LVDS)*
-	-	-			GNDIO7	-		
J1	PL19B	7		C (LVDS)*	PL23B	7	LDQ23	C (LVDS)*
K2	PL20A	7		T	PL24A	7	LDQ23	T
K1	PL20B	7		C	PL24B	7	LDQ23	C
VCCIO	VCCIO7	7			VCCIO7	7		
J4	PL21A	7		T (LVDS)*	PL25A	7	LDQ23	T (LVDS)*
J3	PL21B	7		C (LVDS)*	PL25B	7	LDQ23	C (LVDS)*
J5	PL22A	7		T	PL26A	7	LDQ23	T
K5	PL22B	7		C	PL26B	7	LDQ23	C
GNDIO	GNDIO7	-			GNDIO7	-		
L2	PL24A	7	LDQ28	T (LVDS)*	PL28A	7	LDQ32	T (LVDS)*
L1	PL24B	7	LDQ28	C (LVDS)*	PL28B	7	LDQ32	C (LVDS)*
L7	PL25A	7	LDQ28	T	PL29A	7	LDQ32	T
K6	PL25B	7	LDQ28	C	PL29B	7	LDQ32	C
VCCIO	VCCIO7	7			VCCIO7	7		

LFE2M70E/SE and LFE2M100E/SE Logic Signal Connections: 1152 fpBGA (Cont.)

LFE2M70E/SE				LFE2M100E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
H33	PR14B	2	RDQ15	C	PR14B	2	RDQ15	C
GNDIO	GNDIO2	-			GNDIO2	-		
H34	PR14A	2	RDQ15	T	PR14A	2	RDQ15	T
J30	PR13B	2	RDQ15	C (LVDS)*	PR13B	2	RDQ15	C (LVDS)*
J29	PR13A	2	RDQ15	T (LVDS)*	PR13A	2	RDQ15	T (LVDS)*
VCCIO	VCCIO2	2			VCCIO2	2		
J27	PR11B	2	RUM0_SPLLC_IN_A/RDQ15	C (LVDS)*	PR11B	2	RUM0_SPLLC_IN_A/RDQ15	C (LVDS)*
J28	PR11A	2	RUM0_SPLLT_IN_A/RDQ15	T (LVDS)*	PR11A	2	RUM0_SPLLT_IN_A/RDQ15	T (LVDS)*
H31	PR9B	2	VREF2_2	C	PR9B	2	VREF2_2	C
GNDIO	GNDIO2	-			GNDIO2	-		
H32	PR9A	2	VREF1_2	T	PR9A	2	VREF1_2	T
VCCIO	VCCIO2	2			VCCIO2	2		
H30	XRES	1			XRES	1		
B33	URC_SQ_VCCRX0	12			URC_SQ_VCCRX0	12		
C33	URC_SQ_HDINP0	12		T	URC_SQ_HDINP0	12		T
B34	URC_SQ_VCCIB0	12			URC_SQ_VCCIB0	12		
C32	URC_SQ_HDINN0	12		C	URC_SQ_HDINN0	12		C
B32	URC_SQ_VCCTX0	12			URC_SQ_VCCTX0	12		
A33	URC_SQ_HDOUTP0	12		T	URC_SQ_HDOUTP0	12		T
C34	URC_SQ_VCCOB0	12			URC_SQ_VCCOB0	12		
A32	URC_SQ_HDOUTN0	12		C	URC_SQ_HDOUTN0	12		C
B31	URC_SQ_VCCTX1	12			URC_SQ_VCCTX1	12		
A31	URC_SQ_HDOUTN1	12		C	URC_SQ_HDOUTN1	12		C
D32	URC_SQ_VCCOB1	12			URC_SQ_VCCOB1	12		
A30	URC_SQ_HDOUTP1	12		T	URC_SQ_HDOUTP1	12		T
B30	URC_SQ_VCCRX1	12			URC_SQ_VCCRX1	12		
C31	URC_SQ_HDINN1	12		C	URC_SQ_HDINN1	12		C
D31	URC_SQ_VCCIB1	12			URC_SQ_VCCIB1	12		
C30	URC_SQ_HDINP1	12		T	URC_SQ_HDINP1	12		T
E29	URC_SQ_VCCAUX33	12			URC_SQ_VCCAUX33	12		
E30	URC_SQ_REFCLKN	12		C	URC_SQ_REFCLKN	12		C
D30	URC_SQ_REFCLKP	12		T	URC_SQ_REFCLKP	12		T
D29	URC_SQ_VCCP	12			URC_SQ_VCCP	12		
C29	URC_SQ_HDINP2	12		T	URC_SQ_HDINP2	12		T
D27	URC_SQ_VCCIB2	12			URC_SQ_VCCIB2	12		
C28	URC_SQ_HDINN2	12		C	URC_SQ_HDINN2	12		C
B29	URC_SQ_VCCRX2	12			URC_SQ_VCCRX2	12		
A29	URC_SQ_HDOUTP2	12		T	URC_SQ_HDOUTP2	12		T
E28	URC_SQ_VCCOB2	12			URC_SQ_VCCOB2	12		
A28	URC_SQ_HDOUTN2	12		C	URC_SQ_HDOUTN2	12		C
B28	URC_SQ_VCCTX2	12			URC_SQ_VCCTX2	12		
A27	URC_SQ_HDOUTN3	12		C	URC_SQ_HDOUTN3	12		C
D26	URC_SQ_VCCOB3	12			URC_SQ_VCCOB3	12		
A26	URC_SQ_HDOUTP3	12		T	URC_SQ_HDOUTP3	12		T
B27	URC_SQ_VCCTX3	12			URC_SQ_VCCTX3	12		
C27	URC_SQ_HDINN3	12		C	URC_SQ_HDINN3	12		C
B26	URC_SQ_VCCIB3	12			URC_SQ_VCCIB3	12		
C26	URC_SQ_HDINP3	12		T	URC_SQ_HDINP3	12		T
D28	URC_SQ_VCCRX3	12			URC_SQ_VCCRX3	12		

LFE2M70E/SE and LFE2M100E/SE Logic Signal Connections: 1152 fpBGA (Cont.)

LFE2M70E/SE				LFE2M100E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
F21	GND	-			GND	-		
G31	GND	-			GND	-		
G4	GND	-			GND	-		
J12	GND	-			GND	-		
J16	GND	-			GND	-		
J19	GND	-			GND	-		
J23	GND	-			GND	-		
K27	GND	-			GND	-		
K31	GND	-			GND	-		
K4	GND	-			GND	-		
K8	GND	-			GND	-		
M16	GND	-			GND	-		
M17	GND	-			GND	-		
M18	GND	-			GND	-		
M19	GND	-			GND	-		
N16	GND	-			GND	-		
N17	GND	-			GND	-		
N18	GND	-			GND	-		
N19	GND	-			GND	-		
N26	GND	-			GND	-		
N31	GND	-			GND	-		
N4	GND	-			GND	-		
N9	GND	-			GND	-		
R16	GND	-			GND	-		
R17	GND	-			GND	-		
R18	GND	-			GND	-		
R19	GND	-			GND	-		
T12	GND	-			GND	-		
T13	GND	-			GND	-		
T15	GND	-			GND	-		
T16	GND	-			GND	-		
T17	GND	-			GND	-		
T18	GND	-			GND	-		
T19	GND	-			GND	-		
T20	GND	-			GND	-		
T22	GND	-			GND	-		
T23	GND	-			GND	-		
T26	GND	-			GND	-		
T31	GND	-			GND	-		
T4	GND	-			GND	-		
T9	GND	-			GND	-		
U12	GND	-			GND	-		
U13	GND	-			GND	-		
U15	GND	-			GND	-		
U16	GND	-			GND	-		
U17	GND	-			GND	-		
U18	GND	-			GND	-		
U19	GND	-			GND	-		
U20	GND	-			GND	-		

LatticeECP2M S-Series Devices, Lead-Free Packaging
Commercial

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2M20SE-5FN484C	304	1.2V	-5	Lead-Free fpBGA	484	Com	20
LFE2M20SE-6FN484C	304	1.2V	-6	Lead-Free fpBGA	484	Com	20
LFE2M20SE-7FN484C	304	1.2V	-7	Lead-Free fpBGA	484	Com	20
LFE2M20SE-5FN256C	140	1.2V	-5	Lead-Free fpBGA	256	Com	20
LFE2M20SE-6FN256C	140	1.2V	-6	Lead-Free fpBGA	256	Com	20
LFE2M20SE-7FN256C	140	1.2V	-7	Lead-Free fpBGA	256	Com	20

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2M35SE-5FN672C	410	1.2V	-5	Lead-Free fpBGA	672	Com	35
LFE2M35SE-6FN672C	410	1.2V	-6	Lead-Free fpBGA	672	Com	35
LFE2M35SE-7FN672C	410	1.2V	-7	Lead-Free fpBGA	672	Com	35
LFE2M35SE-5FN484C	303	1.2V	-5	Lead-Free fpBGA	484	Com	35
LFE2M35SE-6FN484C	303	1.2V	-6	Lead-Free fpBGA	484	Com	35
LFE2M35SE-7FN484C	303	1.2V	-7	Lead-Free fpBGA	484	Com	35
LFE2M35SE-5FN256C	140	1.2V	-5	Lead-Free fpBGA	256	Com	35
LFE2M35SE-6FN256C	140	1.2V	-6	Lead-Free fpBGA	256	Com	35
LFE2M35SE-7FN256C	140	1.2V	-7	Lead-Free fpBGA	256	Com	35

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2M50SE-5FN900C	410	1.2V	-5	Lead-Free fpBGA	900	Com	50
LFE2M50SE-6FN900C	410	1.2V	-6	Lead-Free fpBGA	900	Com	50
LFE2M50SE-7FN900C	410	1.2V	-7	Lead-Free fpBGA	900	Com	50
LFE2M50SE-5FN672C	372	1.2V	-5	Lead-Free fpBGA	672	Com	50
LFE2M50SE-6FN672C	372	1.2V	-6	Lead-Free fpBGA	672	Com	50
LFE2M50SE-7FN672C	372	1.2V	-7	Lead-Free fpBGA	672	Com	50
LFE2M50SE-5FN484C	270	1.2V	-5	Lead-Free fpBGA	484	Com	50
LFE2M50SE-6FN484C	270	1.2V	-6	Lead-Free fpBGA	484	Com	50
LFE2M50SE-7FN484C	270	1.2V	-7	Lead-Free fpBGA	484	Com	50

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2M70SE-5FN1152C	436	1.2V	-5	Lead-Free fpBGA	1152	Com	70
LFE2M70SE-6FN1152C	436	1.2V	-6	Lead-Free fpBGA	1152	Com	70
LFE2M70SE-7FN1152C	436	1.2V	-7	Lead-Free fpBGA	1152	Com	70
LFE2M70SE-5FN900C	416	1.2V	-5	Lead-Free fpBGA	900	Com	70
LFE2M70SE-6FN900C	416	1.2V	-6	Lead-Free fpBGA	900	Com	70
LFE2M70SE-7FN900C	416	1.2V	-7	Lead-Free fpBGA	900	Com	70