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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

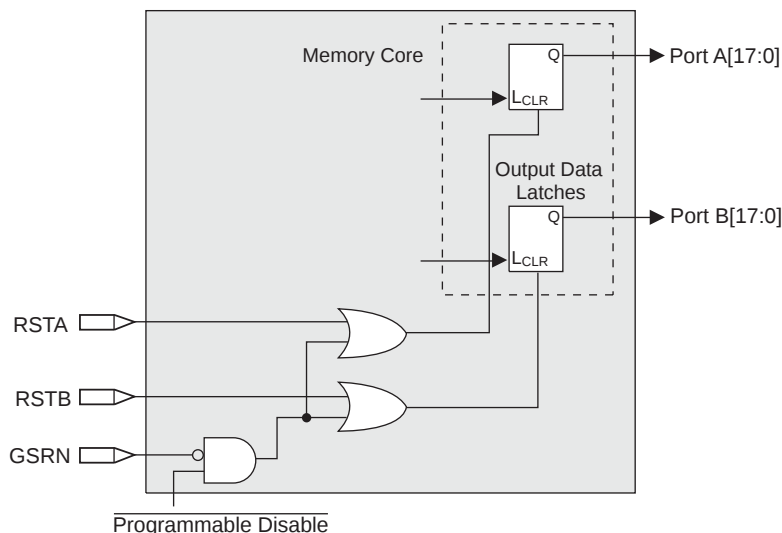
Product Status	Active
Number of LABs/CLBs	4250
Number of Logic Elements/Cells	34000
Total RAM Bits	2151424
Number of I/O	410
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	672-BBGA
Supplier Device Package	672-FPBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfe2m35se-5fn672i

2. Write Through – A copy of the input data appears at the output of the same port during a write cycle. This mode is supported for all data widths.

Memory Core Reset

The memory array in the EBR utilizes latches at the A and B output ports. These latches can be reset asynchronously or synchronously. RSTA and RSTB are local signals, which reset the output latches associated with Port A and Port B, respectively. The Global Reset (GSRN) signal resets both ports. The output data latches and associated resets for both ports are as shown in Figure 2-20.

Figure 2-20. Memory Core Reset

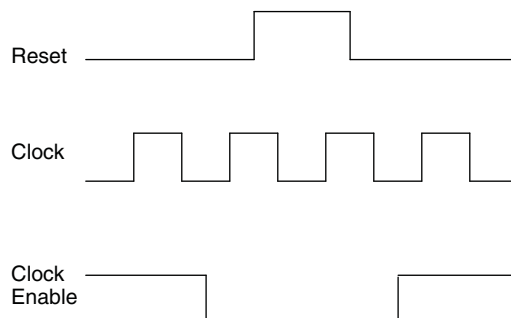


For further information about the sysMEM EBR block, please see the the list of additional technical documentation at the end of this data sheet.

EBR Asynchronous Reset

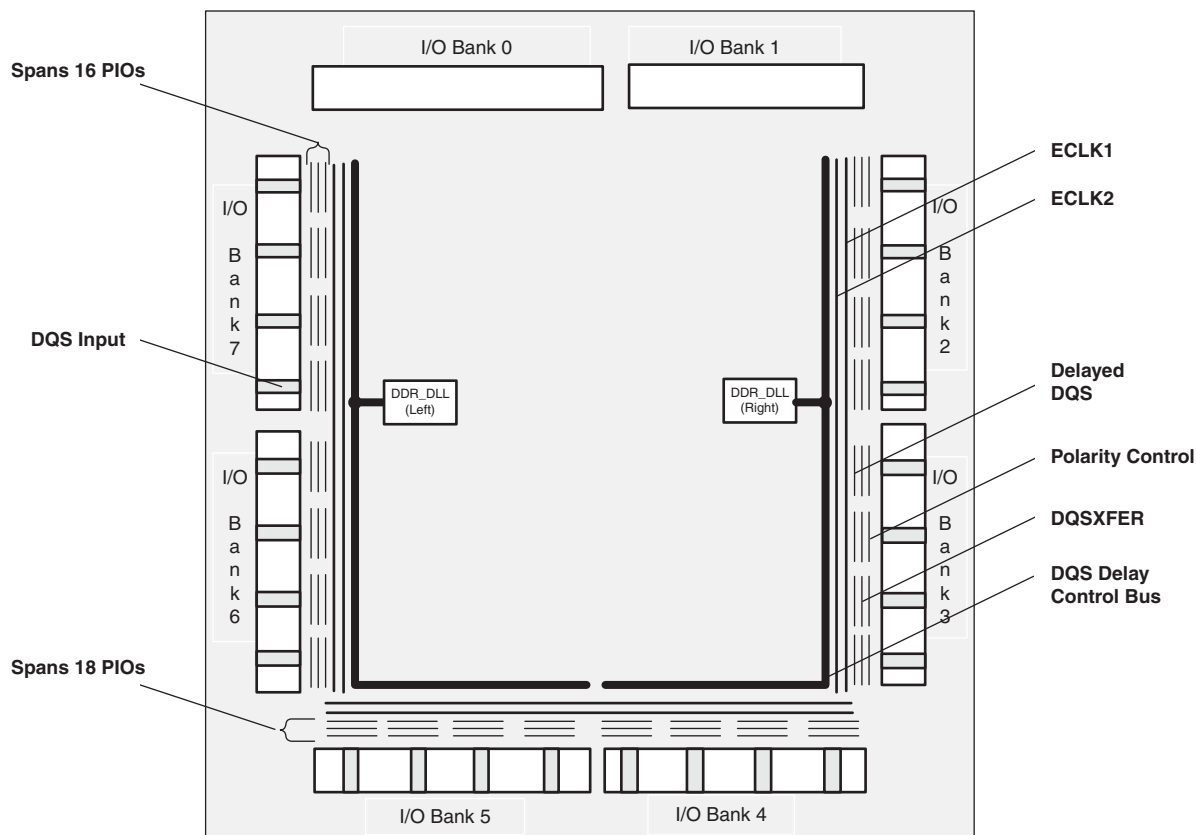
EBR asynchronous reset or GSR (if used) can only be applied if all clock enables are low for a clock cycle before the reset is applied and released a clock cycle after the reset is released, as shown in Figure 2-21. The GSR input to the EBR is always asynchronous.

Figure 2-21. EBR Asynchronous Reset (Including GSR) Timing Diagram



If all clock enables remain enabled, the EBR asynchronous reset or GSR may only be applied and released after the EBR read and write clock inputs are in a steady state condition for a minimum of $1/f_{MAX}$ (EBR clock). The reset release must adhere to the EBR synchronous reset setup time before the next active read or write clock edge.

Figure 2-35. Edge Clock, DLL Calibration and DQS Local Bus Distribution



Note: Bank 8 is not shown.

sys/I/O Recommended Operating Conditions

Standard	V _{CCIO}			V _{REF} (V)		
	Min.	Typ.	Max.	Min.	Typ.	Max.
LVC MOS 3.3 ²	3.135	3.3	3.465	—	—	—
LVC MOS 2.5 ²	2.375	2.5	2.625	—	—	—
LVC MOS 1.8	1.71	1.8	1.89	—	—	—
LVC MOS 1.5	1.425	1.5	1.575	—	—	—
LVC MOS 1.2 ²	1.14	1.2	1.26	—	—	—
LVTTL ²	3.135	3.3	3.465	—	—	—
PCI	3.135	3.3	3.465	—	—	—
SSTL18 ² Class I, II	1.71	1.8	1.89	0.833	0.9	0.969
SSTL2 ² Class I, II	2.375	2.5	2.625	1.15	1.25	1.35
SSTL3 ² Class I, II	3.135	3.3	3.465	1.3	1.5	1.7
HSTL ² 15 Class I	1.425	1.5	1.575	0.68	0.75	0.9
HSTL ² 18 Class I, II	1.71	1.8	1.89	0.816	0.9	1.08
LVDS ²	2.375	2.5	2.625	—	—	—
MLVDS25 ¹	2.375	2.5	2.625	—	—	—
LVPECL33 ^{1,2}	3.135	3.3	3.465	—	—	—
BLVDS25 ^{1,2}	2.375	2.5	2.625	—	—	—
RSDS ^{1,2}	2.375	2.5	2.625	—	—	—
SSTL18D_I ² , II ²	1.71	1.8	1.89	—	—	—
SSTL25D_I ² , II ²	2.375	2.5	2.625	—	—	—
SSTL33D_I ² , II ²	3.135	3.3	3.465	—	—	—
HSTL15D_I ²	1.425	1.5	1.575	—	—	—
HSTL18D_I ² , II ²	1.71	1.8	1.89	—	—	—

1. Inputs on chip. Outputs are implemented with the addition of external resistors.

2. Input on this standard does not depend on the value of V_{CCIO}.

LatticeECP2/M External Switching Characteristics⁹ (Continued)

Over Recommended Operating Conditions

Parameter	Description	Device	-7		-6		-5		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
t _{SU_DEL}	Clock to Data Setup - PIO Input Register with Data Input Delay	LFE2-6	1.40	—	1.70	—	1.90	—	ns
		LFE2-12	1.40	—	1.70	—	1.90	—	ns
		LFE2-20	1.40	—	1.70	—	1.90	—	ns
		LFE2-35	1.40	—	1.70	—	1.90	—	ns
		LFE2-50	1.40	—	1.70	—	1.90	—	ns
		LFE2-70	1.40	—	1.70	—	1.90	—	ns
		LFE2M20	1.40	—	1.70	—	1.90	—	ns
		LFE2M35	1.40	—	1.70	—	1.90	—	ns
		LFE2M50	1.40	—	1.70	—	1.90	—	ns
		LFE2M70	1.40	—	1.70	—	1.90	—	ns
		LFE2M100	1.40	—	1.70	—	1.90	—	ns
t _{H_DEL}	Clock to Data Hold - PIO Input Register with Input Data Delay	LFE2-6	0.00	—	0.00	—	0.00	—	ns
		LFE2-12	0.00	—	0.00	—	0.00	—	ns
		LFE2-20	0.00	—	0.00	—	0.00	—	ns
		LFE2-35	0.00	—	0.00	—	0.00	—	ns
		LFE2-50	0.00	—	0.00	—	0.00	—	ns
		LFE2-70	0.00	—	0.00	—	0.00	—	ns
		LFE2M20	0.00	—	0.00	—	0.00	—	ns
		LFE2M35	0.00	—	0.00	—	0.00	—	ns
		LFE2M50	0.00	—	0.00	—	0.00	—	ns
		LFE2M70	0.00	—	0.00	—	0.00	—	ns
		LFE2M100	0.00	—	0.00	—	0.00	—	ns
f _{MAX_IO}	Clock Frequency of I/O Register and PFU Register	ECP2/M	—	420	—	357	—	311	MHz
General I/O Pin Parameters (using Edge Clock without PLL)¹									
t _{COE}	Clock to Output - PIO Output Register	LFE2-6	—	2.60	—	2.90	—	3.20	ns
		LFE2-12	—	2.60	—	2.90	—	3.20	ns
		LFE2-20	—	2.60	—	2.90	—	3.20	ns
		LFE2-35	—	2.60	—	2.90	—	3.20	ns
		LFE2-50	—	2.60	—	2.90	—	3.20	ns
		LFE2-70	—	2.60	—	2.90	—	3.20	ns
		LFE2M20	—	2.60	—	2.90	—	3.20	ns
		LFE2M35	—	2.60	—	2.90	—	3.20	ns
		LFE2M50	—	3.10	—	3.40	—	3.70	ns
		LFE2M70	—	3.10	—	3.40	—	3.70	ns
		LFE2M100	—	3.10	—	3.40	—	3.70	ns

LatticeECP2 Power Supply and NC

Signals	144 TQFP ³	208 PQFP ³	256 fpBGA ⁴	484 fpBGA ⁴
VCC	16, 22, 29, 48, 54, 83, 94, 102, 128, 135	12, 19, 28, 40, 74, 80, 97, 116, 129, 140, 146, 171, 188, 198	LFE2-6: G7, G9, G10, H7, J10, K10, K8 LFE2-12/LFE2-20: G7, G9, G10, H7, J10, K10, K8	LFE2-12/LFE2-20: N6, N18, J10, J11, J12, J13, K14, K9, L14, L9, M14, M9, N14, N9, P10, P11, P12, P13 LFE2-35/LFE2-50: J10, J11, J12, J13, K14, K9, L14, L9, M14, M9, N14, N9, P10, P11, P12, P13
VCCIO0	139	195, 206	C5, E7	G10, G9, H8, H9
VCCIO1	117	162, 170	C12, E10	G11, G12, G13, G14
VCCIO2	106	143, 148	E14, G12	H14, H15, J15, K16
VCCIO3	89	123, 135	K12, M14	L16, M16, N16, P16
VCCIO4	64	93, 100	M10, P12	R14, T12, T13, T14
VCCIO5	42	55, 63	M7, P5	R9, T10, T11, T9
VCCIO6	31	38, 44	K5, M3	N7, P7, P8, R8
VCCIO7	9	10, 14	E3, G5	J8, K7, L7, M7
VCCIO8	85	113, 118	T15	P15, R15
VCCJ	35	51	K7	T8
VCCAUX	6, 39, 90, 142	7, 30, 70, 86, 125, 151, 174, 190	G8, H10, J7, K9	G5, K5, R5, V7, V11, V8, V13, V15, M17, P17, E17, G18, D11, F13, C5, E6
VCCPLL	None	None	None	LFE2-12/LFE2-20: None LFE2-35: N6, N18 LFE2-50: N6, N18, K6, J16
GND ¹	11, 21, 30, 47, 51, 61, 81, 95, 105, 120, 133, 138	5, 13, 17, 25, 32, 42, 60, 68, 77, 81, 89, 102, 115, 122, 139, 145, 159, 169, 175, 184, 192, 201	A1, A16, B12, B5, C8, E15, E2, H14, H8, H9, J3, J8, J9, M15, M2, P9, R12, R5, T1, T16	A22, AA19, AA4, AB1, AB22, B19, B4, C14, C9, D2, D21, F17, F6, H10, H11, H12, H13, J14, J20, J3, J9, K10, K11, K12, K13, K15, K8, L10, L11, L12, L13, L15, L8, M10, M11, M12, M13, M15, M8, N10, N11, N12, N13, N15, N8, P14, P20, P3, P9, R10, R11, R12, R13, U17, U6, W2, W21, Y14, Y9, A1
NC ²	LFE2-6: 45, 46, 124, 127 LFE2-12: 127	None	LFE2-6: K6, R3, P4 LFE2-12/LFE2-20: None	LFE2-12: E3, F3, F1, H4, F2, H5, G1, G3, G2, G4, K6, N1, M2, N2, M1, N3, N5, N4, P5, N19, M19, J22, L22, H22, K22, J16, D22, F21, E21, E22, H19, G20, G19, F20, C21, C22, H6, J6, H3, H2, H17, H16, H20, H18 LFE2-20/LFE2-35: K6, J16, H6, J6, H3, H2, H17, H16, H20, H18 LFE2-50: None

1. All grounds must be electrically connected at the board level. For fpBGA packages, the total number of GND balls is less than the actual number of GND logic connections from the die to the common package GND plane.
2. NC pins should not be connected to any active signals, VCC or GND.
3. Pin orientation follows the conventional order from the pin 1 marking of the top side view and counter-clockwise.
4. Pin orientation A1 starts from the upper left corner of the top side view with alphabetical order ascending vertically and numerical order ascending horizontally.

LFE2-12E/SE and LFE2-20E/SE Logic Signal Connections: 208 PQFP (Cont.)

LFE2-12E/SE					LFE2-20E/SE				
Pin Number	Pin/Pad Function	Bank	Dual Function	Differential	Pin/Pad Function	Bank	Dual Function	Differential	
46	PL28B	6	LDQ28	C (LVDS)*	PL42B	6	LDQ42	C (LVDS)*	
47	PL30A	6	LDQ28		PL44A	6	LDQ42		
48	TCK	-			TCK	-			
49	TDI	-			TDI	-			
50	TDO	-			TDO	-			
51	VCCJ	-			VCCJ	-			
52	TMS	-			TMS	-			
53	PB2A	5	VREF2_5/BDQ6	T	PB2A	5	VREF2_5/BDQ6	T	
54	PB2B	5	VREF1_5/BDQ6	C	PB2B	5	VREF1_5/BDQ6	C	
55	VCCIO5	5			VCCIO5	5			
56	PB6A	5	BDQS6	T	PB6A	5	BDQS6	T	
57	PB6B	5	BDQ6	C	PB6B	5	BDQ6	C	
58	PB8A	5	BDQ6	T	PB8A	5	BDQ6	T	
59	PB8B	5	BDQ6	C	PB8B	5	BDQ6	C	
60	GND	-			GND	-			
61	PB12A	5	BDQ15	T	PB12A	5	BDQ15	T	
62	PB12B	5	BDQ15	C	PB12B	5	BDQ15	C	
63	VCCIO5	5			VCCIO5	5			
64	PB16A	5	BDQ15	T	PB16A	5	BDQ15	T	
65	PB16B	5	BDQ15	C	PB16B	5	BDQ15	C	
66	PB18A	5	BDQ15	T	PB18A	5	BDQ15	T	
67	PB18B	5	BDQ15	C	PB18B	5	BDQ15	C	
68	GND	-			GND	-			
69	PB20A	5	BDQ24	T	PB30A	5	BDQ33	T	
70	VCCAUX	-			VCCAUX	-			
71	PB20B	5	BDQ24	C	PB30B	5	BDQ33	C	
72	PB22A	5	BDQ24	T	PB32A	5	BDQ33	T	
73	PB22B	5	BDQ24	C	PB32B	5	BDQ33	C	
74	VCC	-			VCC	-			
75	PB26A	5	PCLKT5_0/BDQ24	T	PB35A	5	PCLKT5_0/BDQ33	T	
76	PB26B	5	PCLKC5_0/BDQ24	C	PB35B	5	PCLKC5_0/BDQ33	C	
77	GND	-			GND	-			
78	PB31A	4	PCLKT4_0/BDQ33	T	PB40A	4	PCLKT4_0/BDQ42	T	
79	PB31B	4	PCLKC4_0/BDQ33	C	PB40B	4	PCLKC4_0/BDQ42	C	
80	VCC	-			VCC	-			
81	GND	-			GND	-			
82	PB34A	4	BDQ33	T	PB42A	4	BDQS42	T	
83	PB34B	4	BDQ33	C	PB42B	4	BDQ42	C	
84	PB36A	4	BDQ33	T	PB44A	4	BDQ42	T	
85	PB36B	4	BDQ33	C	PB44B	4	BDQ42	C	
86	VCCAUX	-			VCCAUX	-			
87	PB40A	4	BDQ42	T	PB50A	4	BDQ51	T	
88	PB40B	4	BDQ42	C	PB50B	4	BDQ51	C	
89	GND	-			GND	-			
90	PB42A	4	BDQS42	T	PB52A	4	BDQ51	T	
91	PB42B	4	BDQ42	C	PB52B	4	BDQ51	C	

LFE2-12E/SE and LFE2-20E/SE Logic Signal Connections: 208 PQFP (Cont.)

LFE2-12E/SE					LFE2-20E/SE				
Pin Number	Pin/Pad Function	Bank	Dual Function	Differential	Pin/Pad Function	Bank	Dual Function	Differential	
138	PR15A	3	PCLKT3_0	T (LVDS)*	PR21A	3	PCLKT3_0/RDQ25	T (LVDS)*	
139	GND	-			GND	-			
140	VCC	-			VCC	-			
141	PR13B	2	PCLKC2_0/RDQ10	C	PR19B	2	PCLKC2_0/RDQ16	C	
142	PR13A	2	PCLKT2_0/RDQ10	T	PR19A	2	PCLKT2_0/RDQ16	T	
143	VCCIO2	2			VCCIO2	2			
144	PR12A	2	RDQ10		PR16A	2	RDQS16		
145	GND	-			GND	-			
146	VCC	-			VCC	-			
147	PR8B	2	RDQ10	C (LVDS)*	PR14B	2	RDQ16	C (LVDS)*	
148	VCCIO2	2			VCCIO2	2			
149	PR8A	2	RDQ10	T (LVDS)*	PR14A	2	RDQ16	T (LVDS)*	
150	PR6B	2	RDQ10	C (LVDS)*	PR12B	2	RDQ16	C (LVDS)*	
151	VCCAUX	-			VCCAUX	-			
152	PR6A	2	RDQ10	T (LVDS)*	PR12A	2	RDQ16	T (LVDS)*	
153	PR4B	2		C (LVDS)*	PR6B	2	RDQ8	C (LVDS)*	
154	PR4A	2		T (LVDS)*	PR6A	2	RDQ8	T (LVDS)*	
155	PR2B	2	VREF2_2	C (LVDS)*	PR2B	2	VREF2_2	C (LVDS)*	
156	PR2A	2	VREF1_2	T (LVDS)*	PR2A	2	VREF1_2	T (LVDS)*	
157	PT55B	1	VREF2_1	C	PT64B	1	VREF2_1	C	
158	PT55A	1	VREF1_1	T	PT64A	1	VREF1_1	T	
159	GND	-			GND	-			
160	PT54B	1		C	PT62B	1		C	
161	PT54A	1		T	PT62A	1		T	
162	VCCIO1	1			VCCIO1	1			
163	PT52B	1		C	PT60B	1		C	
164	PT52A	1		T	PT60A	1		T	
165	PT50B	1		C	PT58B	1		C	
166	PT50A	1		T	PT58A	1		T	
167	PT48B	1		C	PT56B	1		C	
168	PT48A	1		T	PT56A	1		T	
169	GND	-			GND	-			
170	VCCIO1	1			VCCIO1	1			
171	VCC	-			VCC	-			
172	PT40B	1		C	PT50B	1		C	
173	PT40A	1		T	PT50A	1		T	
174	VCCAUX	-			VCCAUX	-			
175	GND	-			GND	-			
176	PT36B	1		C	PT44B	1		C	
177	PT36A	1		T	PT44A	1		T	
178	PT34B	1		C	PT42B	1		C	
179	PT34A	1		T	PT42A	1		T	
180	PT30B	1	PCLKC1_0	C	PT39B	1	PCLKC1_0	C	
181	PT30A	1	PCLKT1_0	T	PT39A	1	PCLKT1_0	T	
182	XRES	1			XRES	1			
183	PT28B	0	PCLKC0_0	C	PT37B	0	PCLKC0_0	C	

LFE2-20E/SE Logic Signal Connections: 256 fpBGA (Cont.)

LFE2-20E/SE					
Ball Number	Ball Number	Ball/Pad Function	Bank	Dual Function	Differential
L11	L11	PB61B	4	BDQ60	C
T13	T13	PB62A	4	BDQ60	T
R13	R13	PB63A	4	BDQ60	T
VCCIO	VCCIO	VCCIO4	4		
T14	T14	PB62B	4	BDQ60	C
P13	P13	PB63B	4	BDQ60	C
GND	GND	GNDIO4	-		
N12	N12	PB64A	4	VREF2_4/BDQ60	T
M12	M12	PB64B	4	VREF1_4/BDQ60	C
R15	R15	CFG2	8		
N14	N14	CFG1	8		
N13	N13	PROGRAMN	8		
N15	N15	CFG0	8		
P15	P15	PR44B	8	WRITEN	C
L12	L12	INITN	8		
N16	N16	PR43B	8	CSN	C
GND	GND	GNDIO8	-		
R14	R14	CCLK	8		
P14	P14	PR44A	8	CS1N	T
M13	M13	DONE	8		
R16	R16	PR42B	8	D1	C
VCCIO	VCCIO	VCCIO8	8		
M16	M16	PR43A	8	D0/SPIFASTN	T
P16	P16	PR42A	8	D2	T
L15	L15	PR41B	8	D3	C
GND	GND	GNDIO8	-		
L14	L14	PR40A	8	D6	T
L16	L16	PR41A	8	D4	T
L10	L10	PR39B	8	D7/SPID0	C
L13	L13	PR40B	8	D5	C
VCCIO	VCCIO	VCCIO8	8		
K11	K11	PR39A	8	DI/CSSPI0N	T
K14	K14	PR38B	8	DOU/CSON	C
K13	K13	PR38A	8	BUSY/SISPI	T
GND	GND	GNDIO8	-		
K15	K15	PR31B	3	RLM0_GPLL_C_FB_A/RDQ34	C
VCCIO	VCCIO	VCCIO3	3		
K16	K16	PR31A	3	RLM0_GPLLT_FB_A/RDQ34	T
GND	GND	GNDIO3	-		
J16	J16	PR30B	3	RLM0_GPLL_C_IN_A**/RDQ34	C (LVDS)*
J15	J15	PR30A	3	RLM0_GPLLT_IN_A**/RDQ34	T (LVDS)*
J14	J14	RLM0_PLLCAP	3		

LFE2-20E/SE and LFE2-35E/SE Logic Signal Connections: 672 fpBGA (Cont.)

LFE2-20E/20SE					LFE2-35E/35SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential	
W5	PL38B	6	LDQ42	C (LVDS)*	PL52B	6	LDQ56	C (LVDS)*	
AC1	PL39A	6	LDQ42	T	PL53A	6	LDQ56	T	
AD1	PL39B	6	LDQ42	C	PL53B	6	LDQ56	C	
VCCIO	VCCIO6	6			VCCIO6	6			
Y6	PL40A	6	LDQ42	T (LVDS)*	PL54A	6	LDQ56	T (LVDS)*	
Y5	PL40B	6	LDQ42	C (LVDS)*	PL54B	6	LDQ56	C (LVDS)*	
AE2	PL41A	6	LDQ42	T	PL55A	6	LDQ56	T	
AD2	PL41B	6	LDQ42	C	PL55B	6	LDQ56	C	
GND	GNDIO6	-			GNDIO6	-			
AB3	PL42A	6	LDQS42	T (LVDS)*	PL56A	6	LDQS56	T (LVDS)*	
AB2	PL42B	6	LDQ42	C (LVDS)*	PL56B	6	LDQ56	C (LVDS)*	
W7	PL43A	6	LDQ42	T	PL57A	6	LDQ56	T	
VCCIO	VCCIO6	6			VCCIO6	6			
W8	PL43B	6	LDQ42	C	PL57B	6	LDQ56	C	
Y7	PL44A	6	LDQ42	T (LVDS)*	PL58A	6	LDQ56	T (LVDS)*	
Y8	PL44B	6	LDQ42	C (LVDS)*	PL58B	6	LDQ56	C (LVDS)*	
AC2	PL45A	6	LDQ42	T	PL59A	6	LDQ56	T	
GND	GNDIO6	-			GNDIO6	-			
AD3	PL45B	6	LDQ42	C	PL59B	6	LDQ56	C	
AC3	TCK	-			TCK	-			
AA8	TDI	-			TDI	-			
AB4	TMS	-			TMS	-			
AA5	TDO	-			TDO	-			
AB5	VCCJ	-			VCCJ	-			
AE3	PB2A	5	VREF2_5/BDQ6	T	PB2A	5	VREF2_5/BDQ6	T	
AF3	PB2B	5	VREF1_5/BDQ6	C	PB2B	5	VREF1_5/BDQ6	C	
AC4	PB3A	5	BDQ6	T	PB3A	5	BDQ6	T	
AD4	PB3B	5	BDQ6	C	PB3B	5	BDQ6	C	
AE4	PB4A	5	BDQ6	T	PB4A	5	BDQ6	T	
AF4	PB4B	5	BDQ6	C	PB4B	5	BDQ6	C	
VCCIO	VCCIO5	5			VCCIO5	5			
V9	PB5A	5	BDQ6	T	PB5A	5	BDQ6	T	
W9	PB5B	5	BDQ6	C	PB5B	5	BDQ6	C	
GND	GNDIO5	-			GNDIO5	-			
AA6	PB6A	5	BDQS6	T	PB6A	5	BDQS6	T	
AB6	PB6B	5	BDQ6	C	PB6B	5	BDQ6	C	
AC5	PB7A	5	BDQ6	T	PB7A	5	BDQ6	T	
AD5	PB7B	5	BDQ6	C	PB7B	5	BDQ6	C	
AA7	PB8A	5	BDQ6	T	PB8A	5	BDQ6	T	
AB7	PB8B	5	BDQ6	C	PB8B	5	BDQ6	C	
VCCIO	VCCIO5	5			VCCIO5	5			
AE5	PB9A	5	BDQ6	T	PB9A	5	BDQ6	T	
AF5	PB9B	5	BDQ6	C	PB9B	5	BDQ6	C	
AC7	PB10A	5	BDQ6	T	PB10A	5	BDQ6	T	
AD7	PB10B	5	BDQ6	C	PB10B	5	BDQ6	C	
VCCIO	VCCIO5	5			VCCIO5	5			

LFE2-20E/SE and LFE2-35E/SE Logic Signal Connections: 672 fpBGA (Cont.)

LFE2-20E/20SE					LFE2-35E/35SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential	
Y21	PB64A	4	VREF2_4/BDQ60	T	PB73A	4	VREF2_4/BDQ69	T	
AB23	PB64B	4	VREF1_4/BDQ60	C	PB73B	4	VREF1_4/BDQ69	C	
GND	GNDIO4	-			GNDIO4	-			
AD24	CFG2	8			CFG2	8			
W20	CFG1	8			CFG1	8			
AC24	CFG0	8			CFG0	8			
V19	PROGRAMN	8			PROGRAMN	8			
AA22	CCLK	8			CCLK	8			
AB24	INITN	8			INITN	8			
AD25	DONE	8			DONE	8			
GND	GNDIO8	-			GNDIO8	-			
W21	PR44B	8	WRITEN	C	PR58B	8	WRITEN	C	
Y22	PR44A	8	CS1N	T	PR58A	8	CS1N	T	
AC25	PR43B	8	CSN	C	PR57B	8	CSN	C	
AB25	PR43A	8	D0/SPIFASTN	T	PR57A	8	D0/SPIFASTN	T	
VCCIO	VCCIO8	8			VCCIO8	8			
AD26	PR42B	8	D1	C	PR56B	8	D1	C	
AC26	PR42A	8	D2	T	PR56A	8	D2	T	
Y23	PR41B	8	D3	C	PR55B	8	D3	C	
GND	GNDIO8	-			GNDIO8	-			
W22	PR41A	8	D4	T	PR55A	8	D4	T	
AA25	PR40B	8	D5	C	PR54B	8	D5	C	
AB26	PR40A	8	D6	T	PR54A	8	D6	T	
W23	PR39B	8	D7/SPID0	C	PR53B	8	D7/SPID0	C	
VCCIO	VCCIO8	8			VCCIO8	8			
V22	PR39A	8	DI/CSSPI0N	T	PR53A	8	DI/CSSPI0N	T	
Y24	PR38B	8	DOU/CSON	C	PR52B	8	DOU/CSON	C	
Y25	PR38A	8	BUSY/SISPI	T	PR52A	8	BUSY/SISPI	T	
W24	PR37B	3	RDQ34	C	PR51B	3	RDQ48	C	
GND	GNDIO3	-			GNDIO3	-			
V23	PR37A	3	RDQ34	T	PR51A	3	RDQ48	T	
AA26	PR36B	3	RDQ34	C (LVDS)*	PR50B	3	RDQ48	C (LVDS)*	
Y26	PR36A	3	RDQ34	T (LVDS)*	PR50A	3	RDQ48	T (LVDS)*	
U21	PR35B	3	RDQ34	C	PR49B	3	RDQ48	C	
VCCIO	VCCIO3	3			VCCIO3	3			
U19	PR35A	3	RDQ34	T	PR49A	3	RDQ48	T	
W25	PR34B	3	RDQ34	C (LVDS)*	PR48B	3	RDQ48	C (LVDS)*	
W26	PR34A	3	RDQS34	T (LVDS)*	PR48A	3	RDQS48	T (LVDS)*	
GND	GNDIO3	-			GNDIO3	-			
V24	PR33B	3	RDQ34	C	PR47B	3	RDQ48	C	
V25	PR33A	3	RDQ34	T	PR47A	3	RDQ48	T	
V26	PR32B	3	RDQ34	C (LVDS)*	PR46B	3	RDQ48	C (LVDS)*	
U26	PR32A	3	RDQ34	T (LVDS)*	PR46A	3	RDQ48	T (LVDS)*	
VCCIO	VCCIO3	3			VCCIO3	3			
U22	PR31B	3	RLM0_GPLL_C_FB_A/RDQ34	C	PR45B	3	RLM0_GPLL_C_FB_A/RDQ48	C	
U23	PR31A	3	RLM0_GPLL_T_FB_A/RDQ34	T	PR45A	3	RLM0_GPLL_T_FB_A/RDQ48	T	

LFE2-50E/SE and LFE2-70E/SE Logic Signal Connections: 672 fpBGA (Cont.)

LFE2-50E/SE					LFE2-70E/SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
C20	PT75B	1		C	PT93B	1		C
D20	PT75A	1		T	PT93A	1		T
A22	PT74B	1		C	PT92B	1		C
A21	PT74A	1		T	PT92A	1		T
GND	GNDIO1	-			GNDIO1	-		
E19	PT71B	1		C	PT85B	1		C
C19	PT71A	1		T	PT85A	1		T
VCCIO	VCCIO1	1			VCCIO1	1		
B21	PT70B	1		C	PT79B	1		C
B20	PT70A	1		T	PT79A	1		T
D19	PT69B	1		C	PT78B	1		C
B19	PT69A	1		T	PT78A	1		T
GND	GNDIO1	-			GNDIO1	-		
G17	PT68B	1		C	PT77B	1		C
E18	PT68A	1		T	PT77A	1		T
G19	PT67B	1		C	PT76B	1		C
F17	PT67A	1		T	PT76A	1		T
VCCIO	VCCIO1	1			VCCIO1	1		
A20	PT66B	1		C	PT75B	1		C
A19	PT66A	1		T	PT75A	1		T
E17	PT65B	1		C	PT74B	1		C
D18	PT65A	1		T	PT74A	1		T
B18	PT64B	1		C	PT73B	1		C
GND	GNDIO1	-			GNDIO1	-		
A18	PT64A	1		T	PT73A	1		T
E16	PT63B	1		C	PT72B	1		C
G16	PT63A	1		T	PT72A	1		T
F16	PT62B	1		C	PT71B	1		C
VCCIO	VCCIO1	1			VCCIO1	1		
H18	PT62A	1		T	PT71A	1		T
A17	PT61B	1		C	PT70B	1		C
B17	PT61A	1		T	PT70A	1		T
C18	PT60B	1		C	PT69B	1		C
B16	PT60A	1		T	PT69A	1		T
C17	PT59B	1		C	PT68B	1		C
GND	GNDIO1	-			GNDIO1	-		
D17	PT59A	1		T	PT68A	1		T
E15	PT58B	1		C	PT67B	1		C
VCCIO	VCCIO1	1			VCCIO1	1		
G15	PT58A	1		T	PT67A	1		T
A16	PT57B	1		C	PT66B	1		C
B15	PT57A	1		T	PT66A	1		T
D15	PT56B	1		C	PT65B	1		C
F15	PT56A	1		T	PT65A	1		T
A14	PT55B	1		C	PT64B	1		C
B14	PT55A	1		T	PT64A	1		T

LFE2-50E/SE and LFE2-70E/SE Logic Signal Connections: 672 fpBGA (Cont.)

LFE2-50E/SE					LFE2-70E/SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
N15	GND	-			GND	-		
N17	GND	-			GND	-		
P10	GND	-			GND	-		
P12	GND	-			GND	-		
P13	GND	-			GND	-		
P14	GND	-			GND	-		
P15	GND	-			GND	-		
P17	GND	-			GND	-		
R13	GND	-			GND	-		
R14	GND	-			GND	-		
T10	GND	-			GND	-		
T11	GND	-			GND	-		
T16	GND	-			GND	-		
T17	GND	-			GND	-		
T24	GND	-			GND	-		
T3	GND	-			GND	-		
U10	GND	-			GND	-		
U11	GND	-			GND	-		
U13	GND	-			GND	-		
U14	GND	-			GND	-		
U16	GND	-			GND	-		
U17	GND	-			GND	-		
V13	GND	-			GND	-		
V14	GND	-			GND	-		
V21	GND	-			GND	-		
V6	GND	-			GND	-		
M3	NC	-			NC	-		
N6	NC	-			NC	-		
P24	NC	-			NC	-		

* Supports true LVDS. Other differential signals must be emulated with external resistors.

** These dedicated input pins can be used for GPLLs or GDLLs within the respective quadrant.

***Due to packaging bond out option, this DQS does not have all the necessary DQ pins bonded out for a full 8-bit data width.

Note: VCCIO and GND pads are used to determine the average DC current drawn by I/Os between GND/VCCIO connections, or between the last GND/VCCIO in an I/O bank and the end of an I/O bank. The substrate pads listed in the Pin Table do not necessarily have a one to one connection with a package ball or pin.

LFE2-70E/SE Logic Signal Connections: 900 fpBGA (Cont.)

LFE2-70E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential
G12	PT40B	0		C
E12	PT40A	0		T
VCCIO	VCCIO0	0		
B13	PT39B	0		C
A13	PT39A	0		T
H12	PT38B	0		C
F12	PT38A	0		T
C12	PT37B	0		C
GND	GNDIO0	-		
D12	PT37A	0		T
B12	PT36B	0		C
A12	PT36A	0		T
E11	PT35B	0		C
VCCIO	VCCIO0	0		
G11	PT35A	0		T
F11	PT34B	0		C
H11	PT34A	0		T
C11	PT33B	0		C
D11	PT33A	0		T
B11	PT32B	0		C
GND	GNDIO0	-		
A11	PT32A	0		T
E10	PT31B	0		C
VCCIO	VCCIO0	0		
G10	PT31A	0		T
F10	PT30B	0		C
H10	PT30A	0		T
D10	PT29B	0		C
C10	PT29A	0		T
GND	GNDIO0	-		
VCCIO	VCCIO0	0		
A7	PT16B	0		C
B7	PT16A	0		T
A6	PT15B	0		C
B6	PT15A	0		T
C7	PT14B	0		C
GND	GNDIO0	-		
D7	PT14A	0		T
D8	PT13B	0		C
VCCIO	VCCIO0	0		
E7	PT13A	0		T
C6	PT12B	0		C
D6	PT12A	0		T

LFE2M20E/SE and LFE2M35E/SE Logic Signal Connections: 484 fpBGA (Cont.)

LFE2M20E/SE					LFE2M35E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential	
GNDIO	GNDIO4	-			GNDIO4	-			
AA15	PB42B	4	BDQ42	C	PB60B	4	BDQ60	C	
V15	PB43A	4	BDQ42	T	PB61A	4	BDQ60	T	
U15	PB43B	4	BDQ42	C	PB61B	4	BDQ60	C	
AB16	PB44A	4	BDQ42	T	PB62A	4	BDQ60	T	
VCCIO	VCCIO4	4			VCCIO4	4			
AA16	PB44B	4	BDQ42	C	PB62B	4	BDQ60	C	
AB17	PB45A	4	BDQ42	T	PB63A	4	BDQ60	T	
AA17	PB45B	4	BDQ42	C	PB63B	4	BDQ60	C	
Y15	PB46A	4	BDQ42	T	PB64A	4	BDQ60	T	
GNDIO	GNDIO4	-			GNDIO4	-			
W15	PB46B	4	BDQ42	C	PB64B	4	BDQ60	C	
AB20	PB47A	4	BDQ51	T	PB65A	4	BDQ69	T	
AB21	PB47B	4	BDQ51	C	PB65B	4	BDQ69	C	
AA21	PB48A	4	BDQ51	T	PB66A	4	BDQ69	T	
AA20	PB48B	4	BDQ51	C	PB66B	4	BDQ69	C	
AB19	PB49A	4	BDQ51	T	PB67A	4	BDQ69	T	
AB18	PB49B	4	BDQ51	C	PB67B	4	BDQ69	C	
VCCIO	VCCIO4	4			VCCIO4	4			
Y22	PB50A	4	BDQ51	T	PB68A	4	BDQ69	T	
Y21	PB50B	4	BDQ51	C	PB68B	4	BDQ69	C	
GNDIO	GNDIO4	-			GNDIO4	-			
Y17	PB51A	4	BDQS51	T	PB69A	4	BDQS69	T	
Y18	PB51B	4	BDQ51	C	PB69B	4	BDQ69	C	
Y16	PB52A	4	BDQ51	T	PB70A	4	BDQ69	T	
W17	PB52B	4	BDQ51	C	PB70B	4	BDQ69	C	
Y19	PB53A	4	BDQ51	T	PB71A	4	BDQ69	T	
Y20	PB53B	4	BDQ51	C	PB71B	4	BDQ69	C	
VCCIO	VCCIO4	4			VCCIO4	4			
W19	PB54A	4	BDQ51	T	PB72A	4	BDQ69	T	
W18	PB54B	4	BDQ51	C	PB72B	4	BDQ69	C	
V17	PB55A	4	BDQ51	T	PB73A	4	BDQ69	T	
V18	PB55B	4	BDQ51	C	PB73B	4	BDQ69	C	
GNDIO	GNDIO4	-			GNDIO4	-			
W20	CFG2	8			CFG2	8			
V20	CFG1	8			CFG1	8			
V19	CFG0	8			CFG0	8			
V22	PROGRAMN	8			PROGRAMN	8			
W22	CCLK	8			CCLK	8			
U18	INITN	8			INITN	8			
U22	DONE	8			DONE	8			
GNDIO	GNDIO8	-			GNDIO8	-			
U20	PR53B	8	WRITEN***	C	PR68B	8	WRITEN***	C	
U21	PR53A	8	CS1N***	T	PR68A	8	CS1N***	T	
U17	PR52B	8	CSN***	C	PR67B	8	CSN***	C	
U16	PR52A	8	D0/SPIFASTN***	T	PR67A	8	D0/SPIFASTN***	T	
VCCIO	VCCIO8	8			VCCIO8	8			
T16	PR51B	8	D1***	C	PR66B	8	D1***	C	

LFE2M50E/SE Logic Signal Connections: 484 fpBGA

LFE2M50E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential
D1	PL2A	7	LDQ6	T (LVDS)*
E1	PL2B	7	LDQ6	C (LVDS)*
F1	PL3A	7	LDQ6	T
F2	PL3B	7	LDQ6	C
F5	PL4A	7	LDQ6	T (LVDS)*
VCCIO	VCCIO7	7		
G6	PL4B	7	LDQ6	C (LVDS)*
F4	PL5A	7	LDQ6	T
F3	PL5B	7	LDQ6	C
G1	PL6A	7	LDQS6	T (LVDS)*
GNDIO	GNDIO7	-		
G2	PL6B	7	LDQ6	C (LVDS)*
H1	PL7A	7	LDQ6	T
H2	PL7B	7	LDQ6	C
VCCIO	VCCIO7	7		
H7	PL8A	7	LDQ6	T (LVDS)*
H6	PL8B	7	LDQ6	C (LVDS)*
G3	PL9A	7	VREF2_7/LDQ6	T
H3	PL9B	7	VREF1_7/LDQ6	C
GNDIO	GNDIO7	-		
VCCIO	VCCIO7	7		
H5	PL11A	7	LUM0_SPLLT_IN_A	T (LVDS)*
H4	PL11B	7	LUM0_SPLLC_IN_A	C (LVDS)*
J1	PL12A	7	LUM0_SPLLT_FB_A	T
J2	PL12B	7	LUM0_SPLLC_FB_A	C
GNDIO	GNDIO7	-		
J3	PL13A	7		T (LVDS)*
J4	PL13B	7		C (LVDS)*
J7	PL14A	7		T
VCCIO	VCCIO7	7		
J6	PL14B	7		C
GNDIO	GNDIO7	-		
VCCIO	VCCIO7	7		
K1	PL32A	7	LUM3_SPLLT_IN_A/LDQ36	T (LVDS)*
K2	PL32B	7	LUM3_SPLLC_IN_A/LDQ36	C (LVDS)*
J5	PL33A	7	LUM3_SPLLT_FB_A/LDQ36	T
K5	PL33B	7	LUM3_SPLLC_FB_A/LDQ36	C
VCCIO	VCCIO7	7		
K7	PL34A	7	LDQ36	T (LVDS)*
K6	PL34B	7	LDQ36	C (LVDS)*
L6	PL35A	7	LDQ36	T
L7	PL35B	7	LDQ36	C

LFE2M50E/SE Logic Signal Connections: 484 fpBGA (Cont.)

LFE2M50E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential
W19	NC	-		
W18	NC	-		
V17	NC	-		
V18	NC	-		
D15	NC	-		
G14	NC	-		
G15	NC	-		
D14	NC	-		
E15	NC	-		
E14	NC	-		
F15	NC	-		
F14	NC	-		
F13	NC	-		
G12	NC	-		
G13	NC	-		
H8	VCCPLL	-		
H15	VCCPLL	-		
R8	VCCPLL	-		
R15	VCCPLL	-		

* Supports true LVDS. Other differential signals must be emulated with external resistors.

** These dedicated input pins can be used for GPLLs or GDLLs within the respective quadrant.

***For density migration, board design must take into account that these sysCONFIG pins are dual function for the lower density devices (ECP2M20 and ECP2M35). They can be either sysCONFIG pins or general purpose I/Os. These pins are dedicated pins for the higher density devices (ECP2M50, ECP2M70 and ECP2M100).

****Due to packaging bond out option, this DQS does not have all the necessary DQ pins bonded out for a full 8-bit data width.

Note: VCCIO and GND pads are used to determine the average DC current drawn by I/Os between GND/VCCIO connections, or between the last GND/VCCIO in an I/O bank and the end of an I/O bank. The substrate pads listed in the Pin Table do not necessarily have a one to one connection with a package ball or pin.

LFE2M50E/SE and LFE2M70E/SE Logic Signal Connections: 900 fpBGA (Cont.)

LFE2M50E/SE					LFE2M70E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential	
Y22	PR60B	3		C	PR81B	3	RDQ82	C	
Y23	PR60A	3		T	PR81A	3	RDQ82	T	
AB26	NC	-			PR80B	3	RDQ82	C (LVDS)*	
AB27	NC	-			PR80A	3	RDQ82	T (LVDS)*	
-	-	-			VCCIO3	3			
Y24	NC	-			PR79B	3	RDQ82	C	
Y25	NC	-			PR79A	3	RDQ82	T	
AA29	NC	-			PR78B	3	RDQ82	C (LVDS)*	
Y28	NC	-			PR78A	3	RDQ82	T (LVDS)*	
Y30	NC	-			PR76B	3	RDQ73	C	
Y29	NC	-			PR76A	3	RDQ73	T	
-	-	-			GNDIO3	-			
-	-	-			-	-			
W22	NC	-			PR75B	3	RDQ73	C (LVDS)*	
V22	NC	-			PR75A	3	RDQ73	T (LVDS)*	
Y27	NC	-			PR74B	3	RDQ73	C	
-	-	-			VCCIO3	3			
Y26	NC	-			PR74A	3	RDQ73	T	
W30	NC	-			PR73B	3	RDQ73	C (LVDS)*	
W29	NC	-			PR73A	3	RDQS73	T (LVDS)*	
-	-	-			GNDIO3	-			
W25	NC	-			PR72B	3	RDQ73	C	
W26	NC	-			PR72A	3	RDQ73	T	
U29	PR59B	3		C (LVDS)*	PR71B	3	RDQ73	C (LVDS)*	
V29	PR59A	3		T (LVDS)*	PR71A	3	RDQ73	T (LVDS)*	
VCCIO	VCCIO3	3			VCCIO3	3			
V30	PR58B	3		C	PR70B	3	RDQ73	C	
U30	PR58A	3		T	PR70A	3	RDQ73	T	
W27	PR57B	3		C (LVDS)*	PR69B	3	RDQ73	C (LVDS)*	
W28	PR57A	3		T (LVDS)*	PR69A	3	RDQ73	T (LVDS)*	
V24	PR55B	3	RDQ52	C	PR67B	3	RDQ64	C	
V25	PR55A	3	RDQ52	T	PR67A	3	RDQ64	T	
GNDIO	GNDIO3	-			GNDIO3	-			
U28	PR54B	3	RDQ52	C (LVDS)*	PR66B	3	RDQ64	C (LVDS)*	
U27	PR54A	3	RDQ52	T (LVDS)*	PR66A	3	RDQ64	T (LVDS)*	
U23	PR53B	3	RDQ52	C	PR65B	3	RDQ64	C	
V23	PR53A	3	RDQ52	T	PR65A	3	RDQ64	T	
VCCIO	VCCIO3	3			VCCIO3	3			
V26	PR52B	3	RDQ52	C (LVDS)*	PR64B	3	RDQ64	C (LVDS)*	
U26	PR52A	3	RDQS52	T (LVDS)*	PR64A	3	RDQS64	T (LVDS)*	
U25	PR51B	3	RDQ52	C	PR63B	3	RDQ64	C	
GNDIO	GNDIO3	-			GNDIO3	-			
U24	PR51A	3	RDQ52	T	PR63A	3	RDQ64	T	
T30	PR50B	3	RDQ52	C (LVDS)*	PR62B	3	RDQ64	C (LVDS)*	
R30	PR50A	3	RDQ52	T (LVDS)*	PR62A	3	RDQ64	T (LVDS)*	
T23	PR49B	3	RDQ52	C	PR61B	3	RDQ64	C	
VCCIO	VCCIO3	3			VCCIO3	3			
T22	PR49A	3	RDQ52	T	PR61A	3	RDQ64	T	

LFE2M100E/SE Logic Signal Connections: 900 fpBGA (Cont.)

LFE2M100E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential
M19	VCC	-		
M20	VCC	-		
N11	VCC	-		
N12	VCC	-		
N19	VCC	-		
N20	VCC	-		
P12	VCC	-		
P19	VCC	-		
R12	VCC	-		
R19	VCC	-		
T12	VCC	-		
T19	VCC	-		
U12	VCC	-		
U19	VCC	-		
V11	VCC	-		
V12	VCC	-		
V19	VCC	-		
V20	VCC	-		
W11	VCC	-		
W12	VCC	-		
W13	VCC	-		
W14	VCC	-		
W15	VCC	-		
W16	VCC	-		
W17	VCC	-		
W18	VCC	-		
W19	VCC	-		
W20	VCC	-		
Y12	VCC	-		
Y13	VCC	-		
Y18	VCC	-		
Y19	VCC	-		
D14	VCCIO0	0		
E6	VCCIO0	0		
E9	VCCIO0	0		
F12	VCCIO0	0		
K12	VCCIO0	0		
K13	VCCIO0	0		
D17	VCCIO1	1		
E22	VCCIO1	1		
E25	VCCIO1	1		
F19	VCCIO1	1		
K18	VCCIO1	1		

Industrial

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2M20E-5F484I	304	1.2V	-5	fpBGA	484	IND	20
LFE2M20E-6F484I	304	1.2V	-6	fpBGA	484	IND	20
LFE2M20E-5F256I	140	1.2V	-5	fpBGA	256	IND	20
LFE2M20E-6F256I	140	1.2V	-6	fpBGA	256	IND	20

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2M35E-5F672I	410	1.2V	-5	fpBGA	672	IND	35
LFE2M35E-6F672I	410	1.2V	-6	fpBGA	672	IND	35
LFE2M35E-5F484I	303	1.2V	-5	fpBGA	484	IND	35
LFE2M35E-6F484I	303	1.2V	-6	fpBGA	484	IND	35
LFE2M35E-5F256I	140	1.2V	-5	fpBGA	256	IND	35
LFE2M35E-6F256I	140	1.2V	-6	fpBGA	256	IND	35

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2M50E-5F900I	410	1.2V	-5	fpBGA	900	IND	50
LFE2M50E-6F900I	410	1.2V	-6	fpBGA	900	IND	50
LFE2M50E-5F672I	372	1.2V	-5	fpBGA	672	IND	50
LFE2M50E-6F672I	372	1.2V	-6	fpBGA	672	IND	50
LFE2M50E-5F484I	270	1.2V	-5	fpBGA	484	IND	50
LFE2M50E-6F484I	270	1.2V	-6	fpBGA	484	IND	50

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2M70E-5F1152I	436	1.2V	-5	fpBGA	1152	IND	70
LFE2M70E-6F1152I	436	1.2V	-6	fpBGA	1152	IND	70
LFE2M70E-5F900I	416	1.2V	-5	fpBGA	900	IND	70
LFE2M70E-6F900I	416	1.2V	-6	fpBGA	900	IND	70

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2M100E-5F1152I	520	1.2V	-5	fpBGA	1152	IND	100
LFE2M100E-6F1152I	520	1.2V	-6	fpBGA	1152	IND	100
LFE2M100E-5F900I	416	1.2V	-5	fpBGA	900	IND	100
LFE2M100E-6F900I	416	1.2V	-6	fpBGA	900	IND	100

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2M70SE-5F1152C	436	1.2V	-5	fpBGA	1152	Com	70
LFE2M70SE-6F1152C	436	1.2V	-6	fpBGA	1152	Com	70
LFE2M70SE-7F1152C	436	1.2V	-7	fpBGA	1152	Com	70
LFE2M70SE-5F900C	416	1.2V	-5	fpBGA	900	Com	70
LFE2M70SE-6F900C	416	1.2V	-6	fpBGA	900	Com	70
LFE2M70SE-7F900C	416	1.2V	-7	fpBGA	900	Com	70

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2M100SE-5F1152C	520	1.2V	-5	fpBGA	1152	Com	100
LFE2M100SE-6F1152C	520	1.2V	-6	fpBGA	1152	Com	100
LFE2M100SE-7F1152C	520	1.2V	-7	fpBGA	1152	Com	100
LFE2M100SE-5F900C	416	1.2V	-5	fpBGA	900	Com	100
LFE2M100SE-6F900C	416	1.2V	-6	fpBGA	900	Com	100
LFE2M100SE-7F900C	416	1.2V	-7	fpBGA	900	Com	100