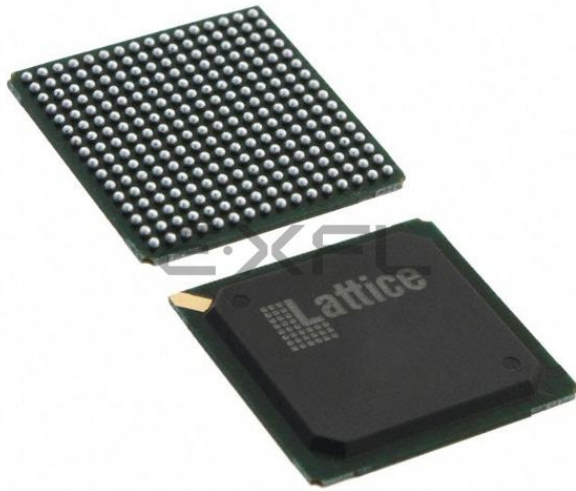




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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	4250
Number of Logic Elements/Cells	34000
Total RAM Bits	2151424
Number of I/O	140
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	256-BGA
Supplier Device Package	256-FPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfe2m35se-6f256c

Symbol	Parameter	Min.	Max.	Units
V_{CCP}^6	PLL and Reference Clock Buffer Power	1.14	1.26	V

1. If V_{CCIO} or V_{CCJ} is set to 1.2V, they must be connected to the same power supply as V_{CC} . If V_{CCIO} or V_{CCJ} is set to 3.3V, they must be connected to the same power supply as V_{CCAUX} . V_{CCPLL} must be connected to the same power supply as V_{CC} through careful filtering and decoupling.
2. See recommended voltages by I/O standard in subsequent table.
3. V_{CCAUX} ramp rate must not exceed 30mV/ μ s during power-up when transitioning between 0V and 3.3V.
4. For proper power-up configuration, users must ensure that the configuration control signals such as the CFGx, INITN, PROGRAMN and DONE pins are driven to the proper logic levels when the device powers up. The device power-up is triggered by the last of V_{CC} , V_{CCAUX} or V_{CCIO8} supplies that reaches its minimum valid levels. Alternatively, if the configuration control signals are pulled up by V_{CCIO8} , the V_{CCIO8} (configuration I/O bank) voltage must be powered up prior to or at the same time as the last of V_{CC} or V_{CCAUX} reaches its minimum levels.
5. For power-up, V_{CC} must reach its valid minimum value before powering up V_{CCAUX} (LatticeECP2/M "S" version devices only).
6. V_{CCRX} , V_{CCTX} and V_{CCP} must be tied together in each quad and all quads need to be powered up.
7. For more power supply design recommendations, refer to TN1114 [Electrical Recommendations for Lattice SERDES](#).

Hot Socketing Specifications^{1, 2, 3, 4}

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
I_{DK}	Input or I/O leakage current	$0 \leq V_{IN} \leq V_{IH} \text{ (MAX.)}$	—	—	+/-1000	μ A
I_{HDIN}^5	SERDES average input current when device is powered down and inputs are driven		—	—	4	mA

1. V_{CC} , V_{CCAUX} and V_{CCIO} should rise/fall monotonically. V_{CC} and V_{CCPLL} must be connected to the same power supply (applies to ECP2-6, ECP2-12 and ECP2-20 only).
2. $0 \leq V_{CC} \leq V_{CC} \text{ (MAX.)}$, $0 \leq V_{CCIO} \leq V_{CCIO} \text{ (MAX.)}$ or $0 \leq V_{CCAUX} \leq V_{CCAUX} \text{ (MAX.)}$.
3. I_{DK} is additive to I_{PU} , I_{PW} or I_{BH} .
4. LVCMOS and LVTTL only.
5. Assumes that the device is powered down with all supplies grounded, both P and N inputs driven by a CML driver with maximum allowed V_{CCIB} of 1.575V, 8b10b data and internal AC coupling.

ESD Performance

Please refer to [LatticeECP2/M Product Family Qualification Summary](#) for complete qualification data, including ESD performance.

LatticeECP2/M External Switching Characteristics⁹ (Continued)

Over Recommended Operating Conditions

Parameter	Description	Device	-7		-6		-5		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
t_{DQVBS}	Data Valid Before DQS (DDR Write)	ECP2/M	0.250	—	0.250	—	0.250	—	UI
t_{DQVAS}	Data Valid After DQS (DDR Write)	ECP2/M	0.250	—	0.250	—	0.250	—	UI
f_{MAX_DDR2}	DDR Clock Frequency	ECP2/M	133	266	133	200	133	166	MHz
SPI4.2 I/O Pin Parameters Static Alignment^{4, 8, 11}									
	Maximum Data Rate	ECP2-20	—	750	—	622	—	622	Mbps
		ECP2-35	—	750	—	622	—	622	Mbps
		ECP2-50	—	750	—	622	—	622	Mbps
		ECP2-70	—	750	—	622	—	622	Mbps
		ECP2M20	—	622	—	622	—	622	Mbps
		ECP2M35	—	622	—	622	—	622	Mbps
		ECP2M50	—	622	—	622	—	622	Mbps
		ECP2M70	—	622	—	622	—	622	Mbps
		ECP2M100	—	622	—	622	—	622	Mbps
$t_{DVACLKSPI}$	Data Valid After CLK (Receive)	ECP2-20	—	0.25	—	0.25	—	0.25	UI
		ECP2-35	—	0.25	—	0.25	—	0.25	UI
		ECP2-50	—	0.25	—	0.25	—	0.25	UI
		ECP2-70	—	0.25	—	0.25	—	0.25	UI
		ECP2M20	—	0.21	—	0.21	—	0.21	UI
		ECP2M35	—	0.21	—	0.21	—	0.21	UI
		ECP2M50	—	0.21	—	0.21	—	0.21	UI
		ECP2M70	—	0.21	—	0.21	—	0.21	UI
		ECP2M100	—	0.21	—	0.21	—	0.21	UI
$t_{DVECLKSPI}$	Data Hold After CLK (Receive)	ECP2-20	0.75	—	0.75	—	0.75	—	UI
		ECP2-35	0.75	—	0.75	—	0.75	—	UI
		ECP2-50	0.75	—	0.75	—	0.75	—	UI
		ECP2-70	0.75	—	0.75	—	0.75	—	UI
		ECP2M20	0.79	—	0.79	—	0.79	—	UI
		ECP2M35	0.79	—	0.79	—	0.79	—	UI
		ECP2M50	0.79	—	0.79	—	0.79	—	UI
		ECP2M70	0.79	—	0.79	—	0.79	—	UI
		ECP2M100	0.79	—	0.79	—	0.79	—	UI
t_{DIASPI}	Data Invalid After Clock (Transmit)	ECP2-20	—	280	—	280	—	280	ps
		ECP2-35	—	280	—	280	—	280	ps
		ECP2-50	—	280	—	280	—	280	ps
		ECP2-70	—	280	—	280	—	280	ps
		ECP2M20	—	230	—	230	—	230	ps
		ECP2M35	—	230	—	230	—	230	ps
		ECP2M50	—	230	—	230	—	230	ps
		ECP2M70	—	230	—	230	—	230	ps
		ECP2M100	—	230	—	230	—	230	ps

Signal Descriptions (Cont.)

Signal Name	I/O	Description
[LOC]DQS[num]	I/O	DQ input/output pads: T (top), R (right), B (bottom), L (left), DQS, num = ball function number.
[LOC]DQ[num]	I/O	DQ input/output pads: T (top), R (right), B (bottom), L (left), DQ, associated DQS number.
Test and Programming (Dedicated Pins)		
TMS	I	Test Mode Select input, used to control the 1149.1 state machine. Pull-up is enabled during configuration.
TCK	I	Test Clock input pin, used to clock the 1149.1 state machine. No pull-up enabled.
TDI	I	Test Data in pin. Used to load data into device using 1149.1 state machine. After power-up, this TAP port can be activated for configuration by sending appropriate command. (Note: once a configuration port is selected it is locked. Another configuration port cannot be selected until the power-up sequence). Pull-up is enabled during configuration.
TDO	O	Output pin. Test Data Out pin used to shift data out of a device using 1149.1.
VCCJ	—	Power supply pin for JTAG Test Access Port.
Configuration Pads (Used During sysCONFIG)		
CFG[2:0]	I	Mode pins used to specify configuration mode values latched on rising edge of INITN. During configuration, a pull-up is enabled. These are dedicated pins.
INITN	I/O	Open Drain pin. Indicates the FPGA is ready to be configured. During configuration, a pull-up is enabled. It is a dedicated pin.
PROGRAMN	I	Initiates configuration sequence when asserted low. This pin always has an active pull-up. This is a dedicated pin.
DONE	I/O	Open Drain pin. Indicates that the configuration sequence is complete, and the startup sequence is in progress. This is a dedicated pin.
CCLK	I/O	Configuration Clock for configuring an FPGA in sysCONFIG mode.
BUSY/SISPI	I/O	Read control command in SPI or SPIm mode.
CSN	I	sysCONFIG chip select (active low). During configuration, a pull-up is enabled.
CS1N	I	sysCONFIG chip select (active low). During configuration, a pull-up is enabled.
WRITEN	I	Write Data on Parallel port (active low).
D[0]/SPIFASTN	I/O	sysCONFIG Port Data I/O for Parallel mode. sysCONFIG Port Data I/O for SPI or SPIm. When using the SPI or SPIm mode, this pin should either be tied high or low, must not be left floating.
D[1:6]	I/O	sysCONFIG Port Data I/O for Parallel
D[7]/SPID0	I/O	sysCONFIG Port Data I/O for Parallel, SPI, SPIm
DOUT/CSO	O	Output for serial configuration data (rising edge of CCLK) when using sysCONFIG port.
DI/CSSPI0N	I/O	Input for serial configuration data (clocked with CCLK) when using sysCONFIG port. During configuration, a pull-up is enabled. Output when used in SPI/SPIm modes.
Dedicated SERDES Signals^{1, 2, 3}		
[LOC]_SQ_VCCAUX33	—	Termination resistor switching power (3.3V). This pin must be tied to 3.3V even if the quad is unused.
[LOC]_SQ_REFCLKN	I	Negative Reference Clock Input
[LOC]_SQ_REFCLKP	I	Positive Reference Clock Input
[LOC]_SQ_VCCP	—	PLL and Reference clock buffer power (1.2V). This pin must be tied to 1.2V even if the quad is unused.

LatticeECP2M Pin Information Summary, LFE2M20 and LFE2M35

Pin Type		LFE2M20		LFE2M35		
		256 fpBGA	484 fpBGA	256 fpBGA	484 fpBGA	672 fpBGA
Single Ended User I/O		140	304	140	303	410
Differential Pair User I/O		70	152	70	151	199
Configuration	TAP Pins	5	5	5	5	5
	Muxed Pins	14	14	14	14	14
	Dedicated Pins (Non TAP)	7	7	7	7	7
Non Configuration	Muxed Pins	64	84	60	84	89
	Dedicated Pins	3	3	3	3	3
VCC		6	16	6	16	29
VCCAUX		4	8	4	8	17
VCCPLL		1	4	1	4	8
VCCIO	Bank0	1	4	1	4	5
	Bank1	1	3	1	3	4
	Bank2	2	4	2	4	5
	Bank3	2	4	2	4	5
	Bank4	2	4	2	4	4
	Bank5	2	4	2	4	5
	Bank6	2	4	2	4	5
	Bank7	2	4	2	4	5
	Bank8	1	2	1	2	2
GND, GND0 to GND7		22	57	22	57	80
NC		17	11	17	12	37
Single Ended/ Differential I/O Pairs per Bank (including emulated with resistors)	Bank0	0/0	36/18	0/0	36/18	63/31
	Bank1	0/0	18/9	0/0	18/9	18/9
	Bank2	14/7	30/15	14/7	30/15	50/25
	Bank3	16/8	36/18	16/8	36/18	43/21
	Bank4	32/16	62/31	32/16	62/31	50/21
	Bank5	20/10	28/14	20/10	28/14	60/30
	Bank6	16/8	40/20	16/8	39/19	52/25
	Bank7	28/14	40/20	28/14	40/20	60/30
	Bank8	14/7	14/7	14/7	14/7	14/7
True LVDS I/O Pairs per Bank	Bank0 (Top Edge)	0	0	0	0	0
	Bank1 (Top Edge)	0	0	0	0	0
	Bank2 (Right Edge)	3	7	3	7	12
	Bank3 (Right Edge)	4	9	4	9	11
	Bank4 (Bottom Edge)	0	0	0	0	0
	Bank5 (Bottom Edge)	0	0	0	0	0
	Bank6 (Left Edge)	4	10	4	10	14
	Bank7 (Left Edge)	7	10	7	10	15
	Bank8 (Right Edge)	0	0	0	0	0

LFE2-6E/SE and LFE2-12E/SE Logic Signal Connections: 144 TQFP

LFE2-6E/SE					LFE2-12E/12SE				
Pin Number	Pin/Pad Function	Bank	Dual Function	Differential	Pin/Pad Function	Bank	Dual Function	Differential	
1	PL2A	7	VREF2_7	T (LVDS)*	PL2A	7	VREF2_7	T (LVDS)*	
2	PL2B	7	VREF1_7	C (LVDS)*	PL2B	7	VREF1_7	C (LVDS)*	
3	PL4A	7		T (LVDS)*	PL4A	7		T (LVDS)*	
4	PL4B	7		C (LVDS)*	PL4B	7		C (LVDS)*	
5	PL6A	7	LDQ10	T (LVDS)*	PL6A	7	LDQ10	T (LVDS)*	
6	VCCAUX	-			VCCAUX	-			
7	PL6B	7	LDQ10	C (LVDS)*	PL6B	7	LDQ10	C (LVDS)*	
8	PL8A	7	LDQ10	T (LVDS)*	PL8A	7	LDQ10	T (LVDS)*	
9	VCCIO7	7			VCCIO7	7			
10	PL8B	7	LDQ10	C (LVDS)*	PL8B	7	LDQ10	C (LVDS)*	
11	GND	-			GND	-			
12	PL12A	7	LDQ10	T (LVDS)*	PL12A	7	LDQ10	T (LVDS)*	
13	PL12B	7	LDQ10	C (LVDS)*	PL12B	7	LDQ10	C (LVDS)*	
14	PL13A	7	PCLKT7_0/LDQ10	T	PL13A	7	PCLKT7_0/LDQ10	T	
15	PL13B	7	PCLKC7_0/LDQ10	C	PL13B	7	PCLKC7_0/LDQ10	C	
16	VCC	-			VCC	-			
17	PL15A	6	PCLKT6_0	T (LVDS)*	PL15A	6	PCLKT6_0	T (LVDS)*	
18	PL15B	6	PCLKC6_0	C (LVDS)*	PL15B	6	PCLKC6_0	C (LVDS)*	
19	PL16A	6	VREF2_6	T	PL16A	6	VREF2_6	T	
20	PL16B	6	VREF1_6	C	PL16B	6	VREF1_6	C	
21	GND	-			GND	-			
22	VCC	-			VCC	-			
23	PL18A	6	LLM0_GDLLT_FB_A	T	PL18A	6	LLM0_GDLLT_FB_A	T	
24	PL18B	6	LLM0_GDLLC_FB_A	C	PL18B	6	LLM0_GDLLC_FB_A	C	
25	LLM0_PLCCAP	6			LLM0_PLCCAP	6			
26	PL20A	6	LLM0_GPLLT_IN_A**	T (LVDS)*	PL20A	6	LLM0_GPLLT_IN_A**	T (LVDS)*	
27	PL20B	6	LLM0_GPLLC_IN_A**	C (LVDS)*	PL20B	6	LLM0_GPLLC_IN_A**	C (LVDS)*	
28	PL22A	6			PL22A	6			
29	VCC	-			VCC	-			
30	GND	-			GND	-			
31	VCCIO6	6			VCCIO6	6			
32	TCK	-			TCK	-			
33	TDI	-			TDI	-			
34	TDO	-			TDO	-			
35	VCCJ	-			VCCJ	-			
36	TMS	-			TMS	-			
37	PB2A	5	VREF2_5/BDQ6	T	PB2A	5	VREF2_5/BDQ6	T	
38	PB2B	5	VREF1_5/BDQ6	C	PB2B	5	VREF1_5/BDQ6	C	
39	VCCAUX	-			VCCAUX	-			
40	PB4A	5	BDQ6	T	PB6A	5	BDQS6	T	
41	PB4B	5	BDQ6	C	PB6B	5	BDQ6	C	
42	VCCIO5	5			VCCIO5	5			
43	PB6A	5	BDQS6	T	PB12A	5	BDQ15	T	
44	PB6B	5	BDQ6	C	PB12B	5	BDQ15	C	
45	NC	5			PB16A	5	BDQ15	T	

LFE2-12E/SE and LFE2-20E/SE Logic Signal Connections: 484 fpBGA
(Cont.)

LFE2-12E/12SE					LFE2-20E/20SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
AB7	PB13B	5	BDQ15	C	PB22B	5	BDQ24	C
Y8	PB16A	5	BDQ15	T	PB25A	5	BDQ24	T
GNDIO	GNDIO5	-			GNDIO	-		
W9	PB15A	5	BDQS15	T	PB24A	5	BDQS24	T
AA8	PB16B	5	BDQ15	C	PB25B	5	BDQ24	C
V9	PB15B	5	BDQ15	C	PB24B	5	BDQ24	C
AB8	PB18A	5	BDQ15	T	PB27A	5	BDQ24	T
VCCIO	VCCIO5	5			VCCIO5	5		
W10	PB17A	5	BDQ15	T	PB26A	5	BDQ24	T
AA9	PB18B	5	BDQ15	C	PB27B	5	BDQ24	C
V10	PB17B	5	BDQ15	C	PB26B	5	BDQ24	C
GNDIO	GNDIO5	-			GNDIO	-		
Y10	PB21A	5	BDQ24	T	PB30A	5	BDQ33	T
AB9	PB20A	5	BDQ24	T	PB29A	5	BDQ33	T
AA10	PB21B	5	BDQ24	C	PB30B	5	BDQ33	C
AB10	PB20B	5	BDQ24	C	PB29B	5	BDQ33	C
AB11	PB23A	5	BDQ24	T	PB32A	5	BDQ33	T
U10	PB22A	5	BDQ24	T	PB31A	5	BDQ33	T
VCCIO	VCCIO5	5			VCCIO5	5		
AA11	PB23B	5	BDQ24	C	PB32B	5	BDQ33	C
U11	PB22B	5	BDQ24	C	PB31B	5	BDQ33	C
GNDIO	GNDIO5	-			GNDIO5	-		
AB12	PB25A	5	BDQ24	T	PB34A	5	BDQ33	T
Y11	PB24A	5	BDQS24	T	PB33A	5	BDQS33	T
AA12	PB25B	5	BDQ24	C	PB34B	5	BDQ33	C
W11	PB24B	5	BDQ24	C	PB33B	5	BDQ33	C
AB13	PB26A	5	PCLKT5_0/BDQ24	T	PB35A	5	PCLKT5_0/BDQ33	T
VCCIO	VCCIO5	5			VCCIO5	5		
AB14	PB26B	5	PCLKC5_0/BDQ24	C	PB35B	5	PCLKC5_0/BDQ33	C
GNDIO	GNDIO5	-			GNDIO5	-		
Y12	PB32A	4	BDQ33	T	PB41A	4	BDQ42	T
W12	PB32B	4	BDQ33	C	PB41B	4	BDQ42	C
VCCIO	VCCIO4	4			VCCIO4	4		
U12	PB31A	4	PCLKT4_0/BDQ33	T	PB40A	4	PCLKT4_0/BDQ42	T
V12	PB31B	4	PCLKC4_0/BDQ33	C	PB40B	4	PCLKC4_0/BDQ42	C
U13	PB34A	4	BDQ33	T	PB43A	4	BDQ42	T
GNDIO	GNDIO4	-			GNDIO4	-		
AA13	PB33A	4	BDQS33	T	PB42A	4	BDQS42	T
U14	PB34B	4	BDQ33	C	PB43B	4	BDQ42	C
Y13	PB33B	4	BDQ33	C	PB42B	4	BDQ42	C
AB16	PB36A	4	BDQ33	T	PB45A	4	BDQ42	T
VCCIO	VCCIO4	4			VCCIO4	4		
AB15	PB35A	4	BDQ33	T	PB44A	4	BDQ42	T
AB17	PB36B	4	BDQ33	C	PB45B	4	BDQ42	C

LFE2-35E/SE and LFE2-50E/SE Logic Signal Connections: 484 fpBGA (Cont.)

LFE2-35E/SE					LFE2-50E/SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
U8	PB23A	5	BDQ24	T	PB32A	5	BDQ33	T
U9	PB23B	5	BDQ24	C	PB32B	5	BDQ33	C
W9	PB24A	5	BDQS24	T	PB33A	5	BDQS33	T
GNDIO	GNDIO5	-			GNDIO5	-		
V9	PB24B	5	BDQ24	C	PB33B	5	BDQ33	C
Y8	PB25A	5	BDQ24	T	PB34A	5	BDQ33	T
AA8	PB25B	5	BDQ24	C	PB34B	5	BDQ33	C
W10	PB26A	5	BDQ24	T	PB35A	5	BDQ33	T
VCCIO	VCCIO5	5			VCCIO	5		
V10	PB26B	5	BDQ24	C	PB35B	5	BDQ33	C
AB8	PB27A	5	BDQ24	T	PB36A	5	BDQ33	T
AA9	PB27B	5	BDQ24	C	PB36B	5	BDQ33	C
GNDIO	GNDIO5	-			GNDIO5	-		
AB9	PB29A	5	BDQ33	T	PB38A	5	BDQ42	T
AB10	PB29B	5	BDQ33	C	PB38B	5	BDQ42	C
Y10	PB30A	5	BDQ33	T	PB39A	5	BDQ42	T
AA10	PB30B	5	BDQ33	C	PB39B	5	BDQ42	C
U10	PB31A	5	BDQ33	T	PB40A	5	BDQ42	T
U11	PB31B	5	BDQ33	C	PB40B	5	BDQ42	C
VCCIO	VCCIO5	5			VCCIO	5		
AB11	PB32A	5	BDQ33	T	PB41A	5	BDQ42	T
AA11	PB32B	5	BDQ33	C	PB41B	5	BDQ42	C
GNDIO	GNDIO5	-			GNDIO5	-		
Y11	PB33A	5	BDQS33	T	PB42A	5	BDQS42	T
W11	PB33B	5	BDQ33	C	PB42B	5	BDQ42	C
AB12	PB34A	5	BDQ33	T	PB43A	5	BDQ42	T
AA12	PB34B	5	BDQ33	C	PB43B	5	BDQ42	C
AB13	PB35A	5	PCLKT5_0/BDQ33	T	PB44A	5	PCLKT5_0/BDQ42	T
AB14	PB35B	5	PCLKC5_0/BDQ33	C	PB44B	5	PCLKC5_0/BDQ42	C
VCCIO	VCCIO5	5			VCCIO	5		
GNDIO	GNDIO5	-			GNDIO5	-		
U12	PB40A	4	PCLKT4_0/BDQ42	T	PB49A	4	PCLKT4_0/BDQ51	T
VCCIO	VCCIO4	4			VCCIO	4		
V12	PB40B	4	PCLKC4_0/BDQ42	C	PB49B	4	PCLKC4_0/BDQ51	C
Y12	PB41A	4	BDQ42	T	PB50A	4	BDQ51	T
W12	PB41B	4	BDQ42	C	PB50B	4	BDQ51	C
AA13	PB42A	4	BDQS42	T	PB51A	4	BDQS51	T
GNDIO	GNDIO4	-			GNDIO4	-		
Y13	PB42B	4	BDQ42	C	PB51B	4	BDQ51	C
U13	PB43A	4	BDQ42	T	PB52A	4	BDQ51	T
U14	PB43B	4	BDQ42	C	PB52B	4	BDQ51	C
AB15	PB44A	4	BDQ42	T	PB53A	4	BDQ51	T
VCCIO	VCCIO4	4			VCCIO	4		
AA14	PB44B	4	BDQ42	C	PB53B	4	BDQ51	C
AB16	PB45A	4	BDQ42	T	PB54A	4	BDQ51	T
AB17	PB45B	4	BDQ42	C	PB54B	4	BDQ51	C

LFE2-35E/SE and LFE2-50E/SE Logic Signal Connections: 484 fpBGA (Cont.)

LFE2-35E/SE					LFE2-50E/SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
J22	PR29B	3	RDQ31	C (LVDS)*	PR48B	3	RDQ50	C (LVDS)*
H22	PR29A	3	RDQ31	T (LVDS)*	PR48A	3	RDQ50	T (LVDS)*
VCCIO	VCCIO3	3			VCCIO	3		
M20	PR28B	3	VREF2_3/RDQ31	C	PR47B	3	VREF2_3/RDQ50	C
L21	PR28A	3	VREF1_3/RDQ31	T	PR47A	3	VREF1_3/RDQ50	T
K21	PR27B	3	PCLKC3_0/RDQ31	C (LVDS)*	PR46B	3	PCLKC3_0/RDQ50	C (LVDS)*
J21	PR27A	3	PCLKT3_0/RDQ31	T (LVDS)*	PR46A	3	PCLKT3_0/RDQ50	T (LVDS)*
M18	PR25B	2	PCLKC2_0/RDQ22	C	PR44B	2	PCLKC2_0/RDQ41	C
L17	PR25A	2	PCLKT2_0/RDQ22	T	PR44A	2	PCLKT2_0/RDQ41	T
GNDIO	GNDIO2	-			GNDIO2	-		
L19	PR24B	2	RDQ22	C (LVDS)*	PR43B	2	RDQ41	C (LVDS)*
L20	PR24A	2	RDQ22	T (LVDS)*	PR43A	2	RDQ41	T (LVDS)*
L18	PR23B	2	RDQ22	C	PR42B	2	RDQ41	C
K17	PR23A	2	RDQ22	T	PR42A	2	RDQ41	T
VCCIO	VCCIO2	2			VCCIO	2		
K18	PR22B	2	RDQ22	C (LVDS)*	PR41B	2	RDQ41	C (LVDS)*
K19	PR22A	2	RDQS22	T (LVDS)*	PR41A	2	RDQS41	T (LVDS)*
G22	PR21B	2	RDQ22	C	PR40B	2	RDQ41	C
GNDIO	GNDIO2	-			GNDIO2	-		
F22	PR21A	2	RDQ22	T	PR40A	2	RDQ41	T
J17	PR20B	2	RDQ22	C (LVDS)*	PR39B	2	RDQ41	C (LVDS)*
J18	PR20A	2	RDQ22	T (LVDS)*	PR39A	2	RDQ41	T (LVDS)*
K20	PR19B	2	RDQ22	C	PR38B	2	RDQ41	C
VCCIO	VCCIO2	2			VCCIO	2		
J19	PR19A	2	RDQ22	T	PR38A	2	RDQ41	T
H21	PR18B	2	RDQ22	C (LVDS)*	PR37B	2	RDQ41	C (LVDS)*
G21	PR18A	2	RDQ22	T (LVDS)*	PR37A	2	RDQ41	T (LVDS)*
-	-	-			GNDIO2	-		
-	-	-			VCCIO	2		
H17	NC	-			PR26B	2	RUM0_SPLLC_FB_A/RDQ24	C
H16	NC	-			PR26A	2	RUM0_SPLLT_FB_A/RDQ24	T
H20	NC	-			PR25B	2	RUM0_SPLLC_IN_A/RDQ24	C
H18	NC	-			PR25A	2	RUM0_SPLLT_IN_A/RDQ24	T
-	-	-			GNDIO2	-		
-	-	-			VCCIO	2		
F21	PR17B	2	RDQ14	C	PR19B	2	RDQ16	C
GNDIO	GNDIO2	-			GNDIO2	-		
E22	PR17A	2	RDQ14	T	PR19A	2	RDQ16	T
D22	PR16B	2	RDQ14	C (LVDS)*	PR18B	2	RDQ16	C (LVDS)*
E21	PR16A	2	RDQ14	T (LVDS)*	PR18A	2	RDQ16	T (LVDS)*
G20	PR15B	2	RDQ14	C	PR17B	2	RDQ16	C
VCCIO	VCCIO2	2			VCCIO	2		
F20	PR15A	2	RDQ14	T	PR17A	2	RDQ16	T
H19	PR14B	2	RDQ14	C (LVDS)*	PR16B	2	RDQ16	C (LVDS)*
G19	PR14A	2	RDQS14	T (LVDS)*	PR16A	2	RDQS16	T (LVDS)*
GNDIO	GNDIO2	-			GNDIO2	-		

LFE2-20E/SE and LFE2-35E/SE Logic Signal Connections: 672 fpBGA (Cont.)

LFE2-20E/20SE					LFE2-35E/35SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
N15	GND	-			GND	-		
N17	GND	-			GND	-		
P10	GND	-			GND	-		
P12	GND	-			GND	-		
P13	GND	-			GND	-		
P14	GND	-			GND	-		
P15	GND	-			GND	-		
P17	GND	-			GND	-		
R13	GND	-			GND	-		
R14	GND	-			GND	-		
T10	GND	-			GND	-		
T11	GND	-			GND	-		
T16	GND	-			GND	-		
T17	GND	-			GND	-		
T24	GND	-			GND	-		
T3	GND	-			GND	-		
U10	GND	-			GND	-		
U11	GND	-			GND	-		
U13	GND	-			GND	-		
U14	GND	-			GND	-		
U16	GND	-			GND	-		
U17	GND	-			GND	-		
V13	GND	-			GND	-		
V14	GND	-			GND	-		
V21	GND	-			GND	-		
V6	GND	-			GND	-		
M3	NC	-			NC	-		
N6	NC	-			NC	-		
P24	NC	-			NC	-		

* Supports true LVDS. Other differential signals must be emulated with external resistors.

** These dedicated input pins can be used for GPLLs or GDLLs within the respective quadrant.

***Due to packaging bond out option, this DQS does not have all the necessary DQ pins bonded out for a full 8-bit data width.

Note: VCCIO and GND pads are used to determine the average DC current drawn by I/Os between GND/VCCIO connections, or between the last GND/VCCIO in an I/O bank and the end of an I/O bank. The substrate pads listed in the Pin Table do not necessarily have a one to one connection with a package ball or pin.

LFE2-50E/SE and LFE2-70E/SE Logic Signal Connections: 672 fpBGA (Cont.)

LFE2-50E/SE					LFE2-70E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential	
L2	PL24B	7	LDQ24	C (LVDS)*	PL37B	7	LDQ37	C (LVDS)*	
L1	PL25A	7	LUM0_SPLLT_IN_A/LDQ24	T	PL38A	7	LUM0_SPLLT_IN_A/LDQ37	T	
VCCIO	VCCIO7	7			VCCIO7	7			
M2	PL25B	7	LUM0_SPLLC_IN_A/LDQ24	C	PL38B	7	LUM0_SPLLC_IN_A/LDQ37	C	
M1	PL26A	7	LUM0_SPLLT_FB_A/LDQ24	T	PL39A	7	LUM0_SPLLT_FB_A/LDQ37	T	
N2	PL26B	7	LUM0_SPLLC_FB_A/LDQ24	C	PL39B	7	LUM0_SPLLC_FB_A/LDQ37	C	
GND	GNDIO7	-			GNDIO7	-			
M8	VCCPLL	7			NC	-			
VCCIO	VCCIO7	7			VCCIO7	7			
GND	GNDIO7	-			GNDIO7	-			
N1	PL37A	7	LDQ41		PL50A	7	LDQ54		
L8	PL38A	7	LDQ41	T	PL51A	7	LDQ54	T	
K8	PL38B	7	LDQ41	C	PL51B	7	LDQ54	C	
VCCIO	VCCIO7	7			VCCIO7	7			
L6	PL39A	7	LDQ41	T (LVDS)*	PL52A	7	LDQ54	T (LVDS)*	
K5	PL39B	7	LDQ41	C (LVDS)*	PL52B	7	LDQ54	C (LVDS)*	
L7	PL40A	7	LDQ41	T	PL53A	7	LDQ54	T	
L5	PL40B	7	LDQ41	C	PL53B	7	LDQ54	C	
GND	GNDIO7	-			GNDIO7	-			
P1	PL41A	7	LDQS41	T (LVDS)*	PL54A	7	LDQS54	T (LVDS)*	
P2	PL41B	7	LDQ41	C (LVDS)*	PL54B	7	LDQ54	C (LVDS)*	
M6	PL42A	7	LDQ41	T	PL55A	7	LDQ54	T	
VCCIO	VCCIO7	7			VCCIO7	7			
N8	PL42B	7	LDQ41	C	PL55B	7	LDQ54	C	
R1	PL43A	7	LDQ41	T (LVDS)*	PL56A	7	LDQ54	T (LVDS)*	
R2	PL43B	7	LDQ41	C (LVDS)*	PL56B	7	LDQ54	C (LVDS)*	
M7	PL44A	7	PCLKT7_0/LDQ41	T	PL57A	7	PCLKT7_0/LDQ54	T	
GND	GNDIO7	-			GNDIO7	-			
N9	PL44B	7	PCLKC7_0/LDQ41	C	PL57B	7	PCLKC7_0/LDQ54	C	
M4	PL46A	6	PCLKT6_0/LDQ50	T (LVDS)*	PL59A	6	PCLKT6_0/LDQ63	T (LVDS)*	
M5	PL46B	6	PCLKC6_0/LDQ50	C (LVDS)*	PL59B	6	PCLKC6_0/LDQ63	C (LVDS)*	
N7	PL47A	6	VREF2_6/LDQ50	T	PL60A	6	VREF2_6/LDQ63	T	
P9	PL47B	6	VREF1_6/LDQ50	C	PL60B	6	VREF1_6/LDQ63	C	
N3	PL48A	6	LDQ50	T (LVDS)*	PL61A	6	LDQ63	T (LVDS)*	
VCCIO	VCCIO6	6			VCCIO6	6			
N4	PL48B	6	LDQ50	C (LVDS)*	PL61B	6	LDQ63	C (LVDS)*	
N5	PL49A	6	LDQ50	T	PL62A	6	LDQ63	T	
P7	PL49B	6	LDQ50	C	PL62B	6	LDQ63	C	
T1	PL50A	6	LDQS50	T (LVDS)*	PL63A	6	LDQS63	T (LVDS)*	
GND	GNDIO6	-			GNDIO6	-			
T2	PL50B	6	LDQ50	C (LVDS)*	PL63B	6	LDQ63	C (LVDS)*	
P8	PL51A	6	LDQ50	T	PL64A	6	LDQ63	T	
P6	PL51B	6	LDQ50	C	PL64B	6	LDQ63	C	
VCCIO	VCCIO6	6			VCCIO6	6			
P5	PL52A	6	LDQ50	T (LVDS)*	PL65A	6	LDQ63	T (LVDS)*	
P4	PL52B	6	LDQ50	C (LVDS)*	PL65B	6	LDQ63	C (LVDS)*	

LFE2-50E/SE and LFE2-70E/SE Logic Signal Connections: 672 fpBGA (Cont.)

LFE2-50E/SE					LFE2-70E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential	
AE17	PB60B	4	BDQ60	C	PB69B	4	BDQ69	C	
AB19	PB61A	4	BDQ60	T	PB70A	4	BDQ69	T	
AE19	PB61B	4	BDQ60	C	PB70B	4	BDQ69	C	
AF17	PB62A	4	BDQ60	T	PB71A	4	BDQ69	T	
AE18	PB62B	4	BDQ60	C	PB71B	4	BDQ69	C	
VCCIO	VCCIO4	4			VCCIO4	4			
W16	PB63A	4	BDQ60	T	PB72A	4	BDQ69	T	
AA17	PB63B	4	BDQ60	C	PB72B	4	BDQ69	C	
AF18	PB64A	4	BDQ60	T	PB73A	4	BDQ69	T	
AF19	PB64B	4	BDQ60	C	PB73B	4	BDQ69	C	
GND	GNDIO4	-			GNDIO4	-			
AA19	PB65A	4	BDQ69	T	PB74A	4	BDQ78	T	
W17	PB65B	4	BDQ69	C	PB74B	4	BDQ78	C	
Y19	PB66A	4	BDQ69	T	PB75A	4	BDQ78	T	
Y17	PB66B	4	BDQ69	C	PB75B	4	BDQ78	C	
AF20	PB67A	4	BDQ69	T	PB76A	4	BDQ78	T	
VCCIO	VCCIO4	4			VCCIO4	4			
AE20	PB67B	4	BDQ69	C	PB76B	4	BDQ78	C	
AA20	PB68A	4	BDQ69	T	PB77A	4	BDQ78	T	
W18	PB68B	4	BDQ69	C	PB77B	4	BDQ78	C	
AD20	PB69A	4	BDQS69	T	PB78A	4	BDQS78	T	
GND	GNDIO4	-			GNDIO4	-			
AE21	PB69B	4	BDQ69	C	PB78B	4	BDQ78	C	
AF21	PB70A	4	BDQ69	T	PB79A	4	BDQ78	T	
AF22	PB70B	4	BDQ69	C	PB79B	4	BDQ78	C	
VCCIO	VCCIO4	4			VCCIO4	4			
GND	GNDIO4	-			GNDIO4	-			
AE22	PB74A	4	BDQ78	T	PB92A	4	BDQ96	T	
AD22	PB74B	4	BDQ78	C	PB92B	4	BDQ96	C	
AF23	PB75A	4	BDQ78	T	PB93A	4	BDQ96	T	
AE23	PB75B	4	BDQ78	C	PB93B	4	BDQ96	C	
AD23	PB76A	4	BDQ78	T	PB94A	4	BDQ96	T	
AC23	PB76B	4	BDQ78	C	PB94B	4	BDQ96	C	
VCCIO	VCCIO4	4			VCCIO4	4			
AB20	PB77A	4	BDQ78	T	PB95A	4	BDQ96	T	
AC20	PB77B	4	BDQ78	C	PB95B	4	BDQ96	C	
GND	GNDIO4	-			GNDIO4	-			
AB21	PB78A	4	BDQS78	T	PB96A	4	BDQS96	T	
AC22	PB78B	4	BDQ78	C	PB96B	4	BDQ96	C	
W19	PB79A	4	BDQ78	T	PB97A	4	BDQ96	T	
AA21	PB79B	4	BDQ78	C	PB97B	4	BDQ96	C	
AF24	PB80A	4	BDQ78	T	PB98A	4	BDQ96	T	
AE24	PB80B	4	BDQ78	C	PB98B	4	BDQ96	C	
VCCIO	VCCIO4	4			VCCIO4	4			
Y20	PB81A	4	BDQ78	T	PB99A	4	BDQ96	T	
AB22	PB81B	4	BDQ78	C	PB99B	4	BDQ96	C	

LFE2M20E/SE and LFE2M35E/SE Logic Signal Connections: 484 fpBGA (Cont.)

LFE2M20E/SE					LFE2M35E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential	
GNDIO	GNDIO4	-			GNDIO4	-			
AA15	PB42B	4	BDQ42	C	PB60B	4	BDQ60	C	
V15	PB43A	4	BDQ42	T	PB61A	4	BDQ60	T	
U15	PB43B	4	BDQ42	C	PB61B	4	BDQ60	C	
AB16	PB44A	4	BDQ42	T	PB62A	4	BDQ60	T	
VCCIO	VCCIO4	4			VCCIO4	4			
AA16	PB44B	4	BDQ42	C	PB62B	4	BDQ60	C	
AB17	PB45A	4	BDQ42	T	PB63A	4	BDQ60	T	
AA17	PB45B	4	BDQ42	C	PB63B	4	BDQ60	C	
Y15	PB46A	4	BDQ42	T	PB64A	4	BDQ60	T	
GNDIO	GNDIO4	-			GNDIO4	-			
W15	PB46B	4	BDQ42	C	PB64B	4	BDQ60	C	
AB20	PB47A	4	BDQ51	T	PB65A	4	BDQ69	T	
AB21	PB47B	4	BDQ51	C	PB65B	4	BDQ69	C	
AA21	PB48A	4	BDQ51	T	PB66A	4	BDQ69	T	
AA20	PB48B	4	BDQ51	C	PB66B	4	BDQ69	C	
AB19	PB49A	4	BDQ51	T	PB67A	4	BDQ69	T	
AB18	PB49B	4	BDQ51	C	PB67B	4	BDQ69	C	
VCCIO	VCCIO4	4			VCCIO4	4			
Y22	PB50A	4	BDQ51	T	PB68A	4	BDQ69	T	
Y21	PB50B	4	BDQ51	C	PB68B	4	BDQ69	C	
GNDIO	GNDIO4	-			GNDIO4	-			
Y17	PB51A	4	BDQS51	T	PB69A	4	BDQS69	T	
Y18	PB51B	4	BDQ51	C	PB69B	4	BDQ69	C	
Y16	PB52A	4	BDQ51	T	PB70A	4	BDQ69	T	
W17	PB52B	4	BDQ51	C	PB70B	4	BDQ69	C	
Y19	PB53A	4	BDQ51	T	PB71A	4	BDQ69	T	
Y20	PB53B	4	BDQ51	C	PB71B	4	BDQ69	C	
VCCIO	VCCIO4	4			VCCIO4	4			
W19	PB54A	4	BDQ51	T	PB72A	4	BDQ69	T	
W18	PB54B	4	BDQ51	C	PB72B	4	BDQ69	C	
V17	PB55A	4	BDQ51	T	PB73A	4	BDQ69	T	
V18	PB55B	4	BDQ51	C	PB73B	4	BDQ69	C	
GNDIO	GNDIO4	-			GNDIO4	-			
W20	CFG2	8			CFG2	8			
V20	CFG1	8			CFG1	8			
V19	CFG0	8			CFG0	8			
V22	PROGRAMN	8			PROGRAMN	8			
W22	CCLK	8			CCLK	8			
U18	INITN	8			INITN	8			
U22	DONE	8			DONE	8			
GNDIO	GNDIO8	-			GNDIO8	-			
U20	PR53B	8	WRITEN***	C	PR68B	8	WRITEN***	C	
U21	PR53A	8	CS1N***	T	PR68A	8	CS1N***	T	
U17	PR52B	8	CSN***	C	PR67B	8	CSN***	C	
U16	PR52A	8	D0/SPIFASTN***	T	PR67A	8	D0/SPIFASTN***	T	
VCCIO	VCCIO8	8			VCCIO8	8			
T16	PR51B	8	D1***	C	PR66B	8	D1***	C	

LFE2M50E/SE Logic Signal Connections: 484 fpBGA (Cont.)

LFE2M50E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential
D9	PT45A	0	VREF1_0	T
A2	PT44B	0		C
VCCIO	VCCIO0	0		
A3	PT44A	0		T
B3	PT43B	0		C
C4	PT43A	0		T
E10	PT42B	0		C
F10	PT42A	0		T
C7	PT41B	0		C
GNDIO	GNDIO0	-		
B6	PT41A	0		T
C6	PT40B	0		C
VCCIO	VCCIO0	0		
C5	PT40A	0		T
C8	PT39B	0		C
D8	PT39A	0		T
E8	PT38B	0		C
E9	PT38A	0		T
GNDIO	GNDIO0	-		
VCCIO	VCCIO0	0		
F8	PT10B	0		C
GNDIO	GNDIO0	-		
G8	PT10A	0		T
F7	PT9B	0		C
G7	PT9A	0		T
C3	PT8B	0		C
VCCIO	VCCIO0	0		
D4	PT8A	0		T
F6	PT7B	0		C
E6	PT7A	0		T
E5	PT6B	0		C
D6	PT6A	0		T
D3	PT5B	0		C
GNDIO	GNDIO0	-		
E3	PT5A	0		T
D5	PT4B	0		C
VCCIO	VCCIO0	0		
E4	PT4A	0		T
C2	PT3B	0		C
B2	PT3A	0		T
B1	PT2B	0		C
C1	PT2A	0		T
J10	VCC	-		

LFE2M50E/SE and LFE2M70E/SE Logic Signal Connections: 900 fpBGA (Cont.)

LFE2M50E/SE					LFE2M70E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential	
L13	VCC	-			VCC	-			
L18	VCC	-			VCC	-			
L19	VCC	-			VCC	-			
M11	VCC	-			VCC	-			
M12	VCC	-			VCC	-			
M13	VCC	-			VCC	-			
M14	VCC	-			VCC	-			
M15	VCC	-			VCC	-			
M16	VCC	-			VCC	-			
M17	VCC	-			VCC	-			
M18	VCC	-			VCC	-			
M19	VCC	-			VCC	-			
M20	VCC	-			VCC	-			
N11	VCC	-			VCC	-			
N12	VCC	-			VCC	-			
N19	VCC	-			VCC	-			
N20	VCC	-			VCC	-			
P12	VCC	-			VCC	-			
P19	VCC	-			VCC	-			
R12	VCC	-			VCC	-			
R19	VCC	-			VCC	-			
T12	VCC	-			VCC	-			
T19	VCC	-			VCC	-			
U12	VCC	-			VCC	-			
U19	VCC	-			VCC	-			
V11	VCC	-			VCC	-			
V12	VCC	-			VCC	-			
V19	VCC	-			VCC	-			
V20	VCC	-			VCC	-			
W11	VCC	-			VCC	-			
W12	VCC	-			VCC	-			
W13	VCC	-			VCC	-			
W14	VCC	-			VCC	-			
W15	VCC	-			VCC	-			
W16	VCC	-			VCC	-			
W17	VCC	-			VCC	-			
W18	VCC	-			VCC	-			
W19	VCC	-			VCC	-			
W20	VCC	-			VCC	-			
Y12	VCC	-			VCC	-			
Y13	VCC	-			VCC	-			
Y18	VCC	-			VCC	-			
Y19	VCC	-			VCC	-			
D14	VCCIO0	0			VCCIO0	0			
E6	VCCIO0	0			VCCIO0	0			
E9	VCCIO0	0			VCCIO0	0			
F12	VCCIO0	0			VCCIO0	0			
K12	VCCIO0	0			VCCIO0	0			

LFE2M70E/SE and LFE2M100E/SE Logic Signal Connections: 1152 fpBGA (Cont.)

LFE2M70E/SE				LFE2M100E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
AF1	PL78B	6	LDQ82	C (LVDS)*	PL95B	6	LDQ99	C (LVDS)*
AE5	PL79A	6	LDQ82	T	PL96A	6	LDQ99	T
AE6	PL79B	6	LDQ82	C	PL96B	6	LDQ99	C
AF4	PL80A	6	LDQ82	T (LVDS)*	PL97A	6	LDQ99	T (LVDS)*
VCCIO	VCCIO6	6			VCCIO6	6		
AF3	PL80B	6	LDQ82	C (LVDS)*	PL97B	6	LDQ99	C (LVDS)*
AF5	PL81A	6	LDQ82	T	PL98A	6	LDQ99	T
AF6	PL81B	6	LDQ82	C	PL98B	6	LDQ99	C
AG1	PL82A	6	LLM0_GPLLT_IN_A**/LDQS82	T (LVDS)*	PL99A	6	LLM0_GPLLT_IN_A**/LDQS99	T (LVDS)*
GNDIO	GNDIO6	-			GNDIO6	-		
AG2	PL82B	6	LLM0_GPLLC_IN_A**/LDQ82	C (LVDS)*	PL99B	6	LLM0_GPLLC_IN_A**/LDQ99	C (LVDS)*
AE9	PL83A	6	LLM0_GPLLT_FB_A/LDQ82	T	PL100A	6	LLM0_GPLLT_FB_A/LDQ99	T
AF7	PL83B	6	LLM0_GPLLC_FB_A/LDQ82	C	PL100B	6	LLM0_GPLLC_FB_A/LDQ99	C
VCCIO	VCCIO6	6			VCCIO6	6		
AH1	PL84A	6	LLM0_GDLLT_IN_A**/LDQ82	T (LVDS)*	PL101A	6	LLM0_GDLLT_IN_A**/LDQ99	T (LVDS)*
AH2	PL84B	6	LLM0_GDLLC_IN_A**/LDQ82	C (LVDS)*	PL101B	6	LLM0_GDLLC_IN_A**/LDQ99	C (LVDS)*
AG5	PL85A	6	LLM0_GDLLT_FB_A/LDQ82	T	PL102A	6	LLM0_GDLLT_FB_A/LDQ99	T
AG4	PL85B	6	LLM0_GDLLC_FB_A/LDQ82	C	PL102B	6	LLM0_GDLLC_FB_A/LDQ99	C
GNDIO	GNDIO6	-			GNDIO6	-		
AG6	LLM0_PLLCAP	6			LLM0_PLLCAP	6		
AJ1	PL87A	6		T	PL104A	6		T
AJ2	PL87B	6		C	PL104B	6		C
AK2	TCK	-			TCK	-		
AK1	TDI	-			TDI	-		
AL1	TMS	-			TMS	-		
AF10	TDO	-			TDO	-		
AK3	VCCJ	-			VCCJ	-		
AN2	LLC_SQ_VCCRX3	14			LLC_SQ_VCCRX3	14		
AM2	LLC_SQ_HDINP3	14		T	LLC_SQ_HDINP3	14		T
AN1	LLC_SQ_VCCIB3	14			LLC_SQ_VCCIB3	14		
AM3	LLC_SQ_HDINN3	14		C	LLC_SQ_HDINN3	14		C
AN3	LLC_SQ_VCCTX3	14			LLC_SQ_VCCTX3	14		
AP2	LLC_SQ_HDOUTP3	14		T	LLC_SQ_HDOUTP3	14		T
AM1	LLC_SQ_VCCOB3	14			LLC_SQ_VCCOB3	14		
AP3	LLC_SQ_HDOUTN3	14		C	LLC_SQ_HDOUTN3	14		C
AN4	LLC_SQ_VCCTX2	14			LLC_SQ_VCCTX2	14		
AP4	LLC_SQ_HDOUTN2	14		C	LLC_SQ_HDOUTN2	14		C
AL3	LLC_SQ_VCCOB2	14			LLC_SQ_VCCOB2	14		
AP5	LLC_SQ_HDOUTP2	14		T	LLC_SQ_HDOUTP2	14		T
AN5	LLC_SQ_VCCRX2	14			LLC_SQ_VCCRX2	14		
AM4	LLC_SQ_HDINN2	14		C	LLC_SQ_HDINN2	14		C
AL4	LLC_SQ_VCCIB2	14			LLC_SQ_VCCIB2	14		
AM5	LLC_SQ_HDINP2	14		T	LLC_SQ_HDINP2	14		T
AL6	LLC_SQ_VCCP	14			LLC_SQ_VCCP	14		
AL5	LLC_SQ_REFCLKP	14		T	LLC_SQ_REFCLKP	14		T
AK5	LLC_SQ_REFCLKN	14		C	LLC_SQ_REFCLKN	14		C
AK6	LLC_SQ_VCCAUX33	14			LLC_SQ_VCCAUX33	14		
AM6	LLC_SQ_HDINP1	14		T	LLC_SQ_HDINP1	14		T

LFE2M70E/SE and LFE2M100E/SE Logic Signal Connections: 1152 fpBGA (Cont.)

LFE2M70E/SE				LFE2M100E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
W30	PR53A	3	RDQ55	T (LVDS)*	PR61A	3	RDQ63	T (LVDS)*
VCCIO	VCCIO3	3			VCCIO3	3		
U27	PR52B	3	VREF2_3/RDQ55	C	PR60B	3	VREF2_3/RDQ63	C
V29	PR52A	3	VREF1_3/RDQ55	T	PR60A	3	VREF1_3/RDQ63	T
V31	PR51B	3	PCLKC3_0/RDQ55	C (LVDS)*	PR59B	3	PCLKC3_0/RDQ63	C (LVDS)*
V32	PR51A	3	PCLKT3_0/RDQ55	T (LVDS)*	PR59A	3	PCLKT3_0/RDQ63	T (LVDS)*
V33	PR49B	2	PCLKC2_0/RDQ46	C	PR57B	2	PCLKC2_0/RDQ54	C
V34	PR49A	2	PCLKT2_0/RDQ46	T	PR57A	2	PCLKT2_0/RDQ54	T
GNDIO	GNDIO2	-			GNDIO2	-		
U24	PR48B	2	RDQ46	C (LVDS)*	PR56B	2	RDQ54	C (LVDS)*
U25	PR48A	2	RDQ46	T (LVDS)*	PR56A	2	RDQ54	T (LVDS)*
V30	PR47B	2	RDQ46	C	PR55B	2	RDQ54	C
Y32	PR47A	2	RDQ46	T	PR55A	2	RDQ54	T
VCCIO	VCCIO2	2			VCCIO2	2		
U28	PR46B	2	RDQ46	C (LVDS)*	PR54B	2	RDQ54	C (LVDS)*
U29	PR46A	2	RDQS46	T (LVDS)*	PR54A	2	RDQS54	T (LVDS)*
U33	PR45B	2	RDQ46	C	PR53B	2	RDQ54	C
GNDIO	GNDIO2	-			GNDIO2	-		
U34	PR45A	2	RDQ46	T	PR53A	2	RDQ54	T
T30	PR44B	2	RDQ46	C (LVDS)*	PR52B	2	RDQ54	C (LVDS)*
U30	PR44A	2	RDQ46	T (LVDS)*	PR52A	2	RDQ54	T (LVDS)*
T29	PR43B	2	RUM3_SPLLC_FB_A/RDQ46	C	PR51B	2	RUM3_SPLLC_FB_A/RDQ54	C
VCCIO	VCCIO2	2			VCCIO2	2		
T28	PR43A	2	RUM3_SPLLT_FB_A/RDQ46	T	PR51A	2	RUM3_SPLLT_FB_A/RDQ54	T
U31	PR42B	2	RUM3_SPLLC_IN_A/RDQ46	C (LVDS)*	PR50B	2	RUM3_SPLLC_IN_A/RDQ54	C (LVDS)*
U32	PR42A	2	RUM3_SPLLT_IN_A/RDQ46	T (LVDS)*	PR50A	2	RUM3_SPLLT_IN_A/RDQ54	T (LVDS)*
T33	PR40B	2	RDQ37	C	PR48B	2	RDQ45	C
T34	PR40A	2	RDQ37	T	PR48A	2	RDQ45	T
GNDIO	GNDIO2	-			GNDIO2	-		
R27	PR39B	2	RDQ37	C (LVDS)*	PR47B	2	RDQ45	C (LVDS)*
R28	PR39A	2	RDQ37	T (LVDS)*	PR47A	2	RDQ45	T (LVDS)*
R29	PR38B	2	RDQ37	C	PR46B	2	RDQ45	C
R30	PR38A	2	RDQ37	T	PR46A	2	RDQ45	T
VCCIO	VCCIO2	2			VCCIO2	2		
R33	PR37B	2	RDQ37	C (LVDS)*	PR45B	2	RDQ45	C (LVDS)*
R34	PR37A	2	RDQS37	T (LVDS)*	PR45A	2	RDQS45	T (LVDS)*
R32	PR36B	2	RDQ37	C	PR44B	2	RDQ45	C
GNDIO	GNDIO2	-			GNDIO2	-		
R31	PR36A	2	RDQ37	T	PR44A	2	RDQ45	T
P34	PR35B	2	RDQ37	C (LVDS)*	PR43B	2	RDQ45	C (LVDS)*
P33	PR35A	2	RDQ37	T (LVDS)*	PR43A	2	RDQ45	T (LVDS)*
R26	PR34B	2	RDQ37	C	PR42B	2	RDQ45	C
VCCIO	VCCIO2	2			VCCIO2	2		
T25	PR34A	2	RDQ37	T	PR42A	2	RDQ45	T
P28	PR33B	2	RDQ37	C (LVDS)*	PR41B	2	RDQ45	C (LVDS)*
P27	PR33A	2	RDQ37	T (LVDS)*	PR41A	2	RDQ45	T (LVDS)*
P30	NC	-			PR40B	2		C
-	-	-			GNDIO2	-		
P29	NC	-			PR40A	2		T

LFE2M70E/SE and LFE2M100E/SE Logic Signal Connections: 1152 fpBGA (Cont.)

LFE2M70E/SE				LFE2M100E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
P31	NC	-			PR39B	2		C (LVDS)*
P32	NC	-			PR39A	2		T (LVDS)*
R25	NC	-			PR38B	2		C
-	-	-			VCCIO2	2		
T24	NC	-			PR38A	2		T
N34	NC	-			PR37B	2		C (LVDS)*
N33	NC	-			PR37A	2		T (LVDS)*
GNDIO	GNDIO2	-			GNDIO2	-		
M34	PR31B	2	RDQ28	C	PR35B	2	RDQ32	C
M33	PR31A	2	RDQ28	T	PR35A	2	RDQ32	T
-	-	-			GNDIO2	-		
R24	PR30B	2	RDQ28	C (LVDS)*	PR34B	2	RDQ32	C (LVDS)*
P24	PR30A	2	RDQ28	T (LVDS)*	PR34A	2	RDQ32	T (LVDS)*
N30	PR29B	2	RDQ28	C	PR33B	2	RDQ32	C
M29	PR29A	2	RDQ28	T	PR33A	2	RDQ32	T
VCCIO	VCCIO2	2			VCCIO2	2		
N28	PR28B	2	RDQ28	C (LVDS)*	PR32B	2	RDQ32	C (LVDS)*
N29	PR28A	2	RDQS28	T (LVDS)*	PR32A	2	RDQS32	T (LVDS)*
N24	PR27B	2	RDQ28	C	PR31B	2	RDQ32	C
GNDIO	GNDIO2	-			GNDIO2	-		
N25	PR27A	2	RDQ28	T	PR31A	2	RDQ32	T
M28	PR26B	2	RDQ28	C (LVDS)*	PR30B	2	RDQ32	C (LVDS)*
M27	PR26A	2	RDQ28	T (LVDS)*	PR30A	2	RDQ32	T (LVDS)*
L27	PR25B	2	RDQ28	C	PR29B	2	RDQ32	C
VCCIO	VCCIO2	2			VCCIO2	2		
M26	PR25A	2	RDQ28	T	PR29A	2	RDQ32	T
M32	PR24B	2	RDQ28	C (LVDS)*	PR28B	2	RDQ32	C (LVDS)*
M31	PR24A	2	RDQ28	T (LVDS)*	PR28A	2	RDQ32	T (LVDS)*
GNDIO	GNDIO2	-			GNDIO2	-		
-	-	-			VCCIO2	2		
L34	PR22B	2		C	PR22B	2	RDQ23	C
L33	PR22A	2		T	PR22A	2	RDQ23	T
L32	PR21B	2		C (LVDS)*	PR21B	2	RDQ23	C (LVDS)*
L31	PR21A	2		T (LVDS)*	PR21A	2	RDQ23	T (LVDS)*
VCCIO	VCCIO2	2			VCCIO2	2		
L28	PR20B	2		C	PR20B	2	RDQ23	C
L29	PR20A	2		T	PR20A	2	RDQ23	T
M30	PR19B	2		C (LVDS)*	PR19B	2	RDQ23	C (LVDS)*
L30	PR19A	2		T (LVDS)*	PR19A	2	RDQ23	T (LVDS)*
K34	PR18B	2	RDQ15	C	PR18B	2	RDQ15	C
K33	PR18A	2	RDQ15	T	PR18A	2	RDQ15	T
GNDIO	GNDIO2	-			GNDIO2	-		
K30	PR17B	2	RDQ15	C (LVDS)*	PR17B	2	RDQ15	C (LVDS)*
K29	PR17A	2	RDQ15	T (LVDS)*	PR17A	2	RDQ15	T (LVDS)*
J34	PR16B	2	RDQ15	C	PR16B	2	RDQ15	C
J33	PR16A	2	RDQ15	T	PR16A	2	RDQ15	T
VCCIO	VCCIO2	2			VCCIO2	2		
J32	PR15B	2	RDQ15	C (LVDS)*	PR15B	2	RDQ15	C (LVDS)*
J31	PR15A	2	RDQS15	T (LVDS)*	PR15A	2	RDQS15	T (LVDS)*

Industrial

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2M20E-5F484I	304	1.2V	-5	fpBGA	484	IND	20
LFE2M20E-6F484I	304	1.2V	-6	fpBGA	484	IND	20
LFE2M20E-5F256I	140	1.2V	-5	fpBGA	256	IND	20
LFE2M20E-6F256I	140	1.2V	-6	fpBGA	256	IND	20

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2M35E-5F672I	410	1.2V	-5	fpBGA	672	IND	35
LFE2M35E-6F672I	410	1.2V	-6	fpBGA	672	IND	35
LFE2M35E-5F484I	303	1.2V	-5	fpBGA	484	IND	35
LFE2M35E-6F484I	303	1.2V	-6	fpBGA	484	IND	35
LFE2M35E-5F256I	140	1.2V	-5	fpBGA	256	IND	35
LFE2M35E-6F256I	140	1.2V	-6	fpBGA	256	IND	35

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2M50E-5F900I	410	1.2V	-5	fpBGA	900	IND	50
LFE2M50E-6F900I	410	1.2V	-6	fpBGA	900	IND	50
LFE2M50E-5F672I	372	1.2V	-5	fpBGA	672	IND	50
LFE2M50E-6F672I	372	1.2V	-6	fpBGA	672	IND	50
LFE2M50E-5F484I	270	1.2V	-5	fpBGA	484	IND	50
LFE2M50E-6F484I	270	1.2V	-6	fpBGA	484	IND	50

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2M70E-5F1152I	436	1.2V	-5	fpBGA	1152	IND	70
LFE2M70E-6F1152I	436	1.2V	-6	fpBGA	1152	IND	70
LFE2M70E-5F900I	416	1.2V	-5	fpBGA	900	IND	70
LFE2M70E-6F900I	416	1.2V	-6	fpBGA	900	IND	70

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2M100E-5F1152I	520	1.2V	-5	fpBGA	1152	IND	100
LFE2M100E-6F1152I	520	1.2V	-6	fpBGA	1152	IND	100
LFE2M100E-5F900I	416	1.2V	-5	fpBGA	900	IND	100
LFE2M100E-6F900I	416	1.2V	-6	fpBGA	900	IND	100

LatticeECP2M Standard Series Devices, Lead-Free Packaging
Commercial

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2M20E-5FN484C	304	1.2V	-5	Lead-Free fpBGA	484	COM	20
LFE2M20E-6FN484C	304	1.2V	-6	Lead-Free fpBGA	484	COM	20
LFE2M20E-7FN484C	304	1.2V	-7	Lead-Free fpBGA	484	COM	20
LFE2M20E-5FN256C	140	1.2V	-5	Lead-Free fpBGA	256	COM	20
LFE2M20E-6FN256C	140	1.2V	-6	Lead-Free fpBGA	256	COM	20
LFE2M20E-7FN256C	140	1.2V	-7	Lead-Free fpBGA	256	COM	20

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2M35E-5FN672C	410	1.2V	-5	Lead-Free fpBGA	672	COM	35
LFE2M35E-6FN672C	410	1.2V	-6	Lead-Free fpBGA	672	COM	35
LFE2M35E-7FN672C	410	1.2V	-7	Lead-Free fpBGA	672	COM	35
LFE2M35E-5FN484C	303	1.2V	-5	Lead-Free fpBGA	484	COM	35
LFE2M35E-6FN484C	303	1.2V	-6	Lead-Free fpBGA	484	COM	35
LFE2M35E-7FN484C	303	1.2V	-7	Lead-Free fpBGA	484	COM	35
LFE2M35E-5FN256C	140	1.2V	-5	Lead-Free fpBGA	256	COM	35
LFE2M35E-6FN256C	140	1.2V	-6	Lead-Free fpBGA	256	COM	35
LFE2M35E-7FN256C	140	1.2V	-7	Lead-Free fpBGA	256	COM	35

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2M50E-5FN900C	410	1.2V	-5	Lead-Free fpBGA	900	COM	50
LFE2M50E-6FN900C	410	1.2V	-6	Lead-Free fpBGA	900	COM	50
LFE2M50E-7FN900C	410	1.2V	-7	Lead-Free fpBGA	900	COM	50
LFE2M50E-5FN672C	372	1.2V	-5	Lead-Free fpBGA	672	COM	50
LFE2M50E-6FN672C	372	1.2V	-6	Lead-Free fpBGA	672	COM	50
LFE2M50E-7FN672C	372	1.2V	-7	Lead-Free fpBGA	672	COM	50
LFE2M50E-5FN484C	270	1.2V	-5	Lead-Free fpBGA	484	COM	50
LFE2M50E-6FN484C	270	1.2V	-6	Lead-Free fpBGA	484	COM	50
LFE2M50E-7FN484C	270	1.2V	-7	Lead-Free fpBGA	484	COM	50

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2M70E-5FN1152C	436	1.2V	-5	Lead-Free fpBGA	1152	COM	70
LFE2M70E-6FN1152C	436	1.2V	-6	Lead-Free fpBGA	1152	COM	70
LFE2M70E-7FN1152C	436	1.2V	-7	Lead-Free fpBGA	1152	COM	70
LFE2M70E-5FN900C	416	1.2V	-5	Lead-Free fpBGA	900	COM	70
LFE2M70E-6FN900C	416	1.2V	-6	Lead-Free fpBGA	900	COM	70
LFE2M70E-7FN900C	416	1.2V	-7	Lead-Free fpBGA	900	COM	70

Date	Version	Section	Change Summary
August 2007 (cont.)	02.8 (cont.)	DC and Switching (cont.)	sysCLOCK GPLL timing has been updated.
		Pinout Information	Added ECP2M50 (484/672/900-fpBGA), ECP2M70 (900-fpBGA) and ECP2M100 (900-fpBGA) pinout information.
		Ordering Information	1156-fpBGA package option has been removed from the LatticeECP2M family.
September 2007	02.9	Pinout Information	Added Thermal Management text section.
February 2008	03.0	Architecture	Added LVCMOS33D description.
		DC and Switching	LatticeECP2M Supply Current has been updated.
			Typical Building Block Function Performance, External Switching Characteristics, Internal Switching Characteristics, Family Timing Adders, sysCLOCK GPLL Timing, sysCLOCK SPLL Timing, DLL Timing and sysCONFIG Port Timing Specifications have been updated (timing rev. A 0.11).
			Figure 3-9. Read/Write Mode (Normal) and Figure 3-10. Read/Write Mode with Input and Output Registers have been updated.
			Table 3-8. Channel output Jitter (Max) has been updated.
		Pinout Information	Signal description has been updated.
April 2008	03.1	Pinout Information	Added 1152-fpBGA pinouts for the ECP2M70 and ECP2M100.
June 2008	03.2	Pinout Information	Available DDR Interfaces per I/O Bank for the LFE2M35 (484/672-fpBGA) have been updated.
		Introduction	Family Selection Guide table - Updated number of EBR SRAM Blocks for the ECP2-70 device.
		Architecture	Removed Read-Before-Write sysMEM EBR mode.
		Architecture	Clarification of the operation of the secondary clock regions.
August 2008	03.3	DC and Switching Characteristics	Removed Read-Before-Write sysMEM EBR mode.
		Architecture	Clarification of the operation of the secondary clock regions.
		Pinout Information	Added information for [LOC]DQ[num] to Signal Descriptions table.
January 2009	03.4	DC and Switching Characteristics	Updated typical and max. jitter numbers in Channel Output Jitter table for x10 mode.
			Added Channel Output Jitter table for x20 mode.
November 2009	03.5	DC and Switching Characteristics	Updated SPI/SPI _m Configuration Waveforms diagram.
			Updated footnotes in LatticeECP2 Initialization Supply Current table.
			Updated footnotes in LatticeECP2M Initialization Supply Current table.
			Updated footnotes in SERDES High Speed Data Receiver (LatticeECP2M Family Only) table.
			Updated max. value for t _{DINIT} parameter in LatticeECP2/M sysCONFIG Port Timing Specifications table.
			Updated Serial Output Timing and Levels table.
			Updated Figure 3-5 MLVDS
			Updated Table 3-7 Serial Output Timing and Levels
			Updated Table 3-15 Power Down/Power Up Specification
		Pinout Information	Signal Descriptions table - corrected references to ULM, URM, LRM (changed to LUM, RUM and RLM), added footnote 5.