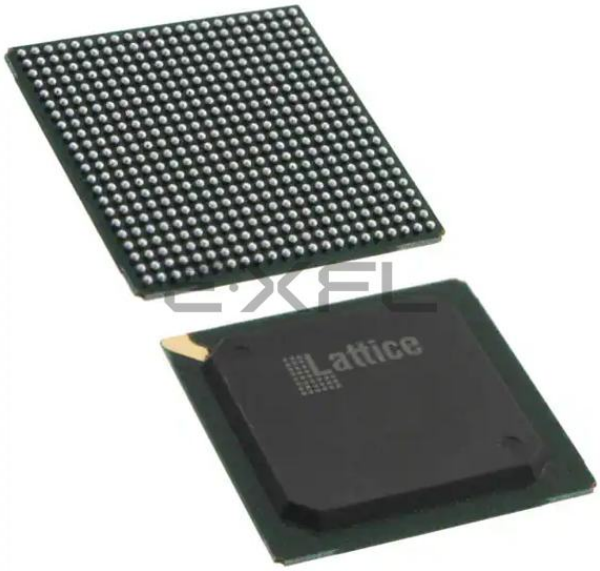
# Lattice Semiconductor Corporation - LFE2M50E-5FN484C Datasheet

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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Active |
| Number of LABs/CLBs | 6000 |
| Number of Logic Elements/Cells | 48000 |
| Total RAM Bits | 4246528 |
| Number of I/O | 270 |
| Number of Gates | - |
| Voltage - Supply | 1.14V ~ 1.26V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 85°C (TJ) |
| Package / Case | 484-BBGA |
| Supplier Device Package | 484-FPBGA (23x23) |
| Purchase URL | https://www.e-xfl.com/product-detail/lattice-semiconductor/lfe2m50e-5fn484c |

## LatticeECP2/M DSP Performance

Table 2-11 lists the maximum performance in millions of MAC operations per second (MMAC) for each member of the LatticeECP2/M family.

***Table 2-11. DSP Performance***

| Device | DSP Block | DSP Performance GMAC |
|---|---|---|
| ECP2-6 | 3 | 3.9 |
| ECP2-12 | 6 | 7.8 |
| ECP2-20 | 7 | 9.1 |
| ECP2-35 | 8 | 10.4 |
| ECP2-50 | 18 | 23.4 |
| ECP2-70 | 22 | 28.6 |
| ECP2M20 | 6 | 7.8 |
| ECP2M35 | 8 | 10.4 |
| ECP2M50 | 22 | 28.6 |
| ECP2M70 | 24 | 31.2 |
| ECP2M100 | 42 | 54.6 |

For further information about the sysDSP block, please see the list of additional technical information at the end of this data sheet.

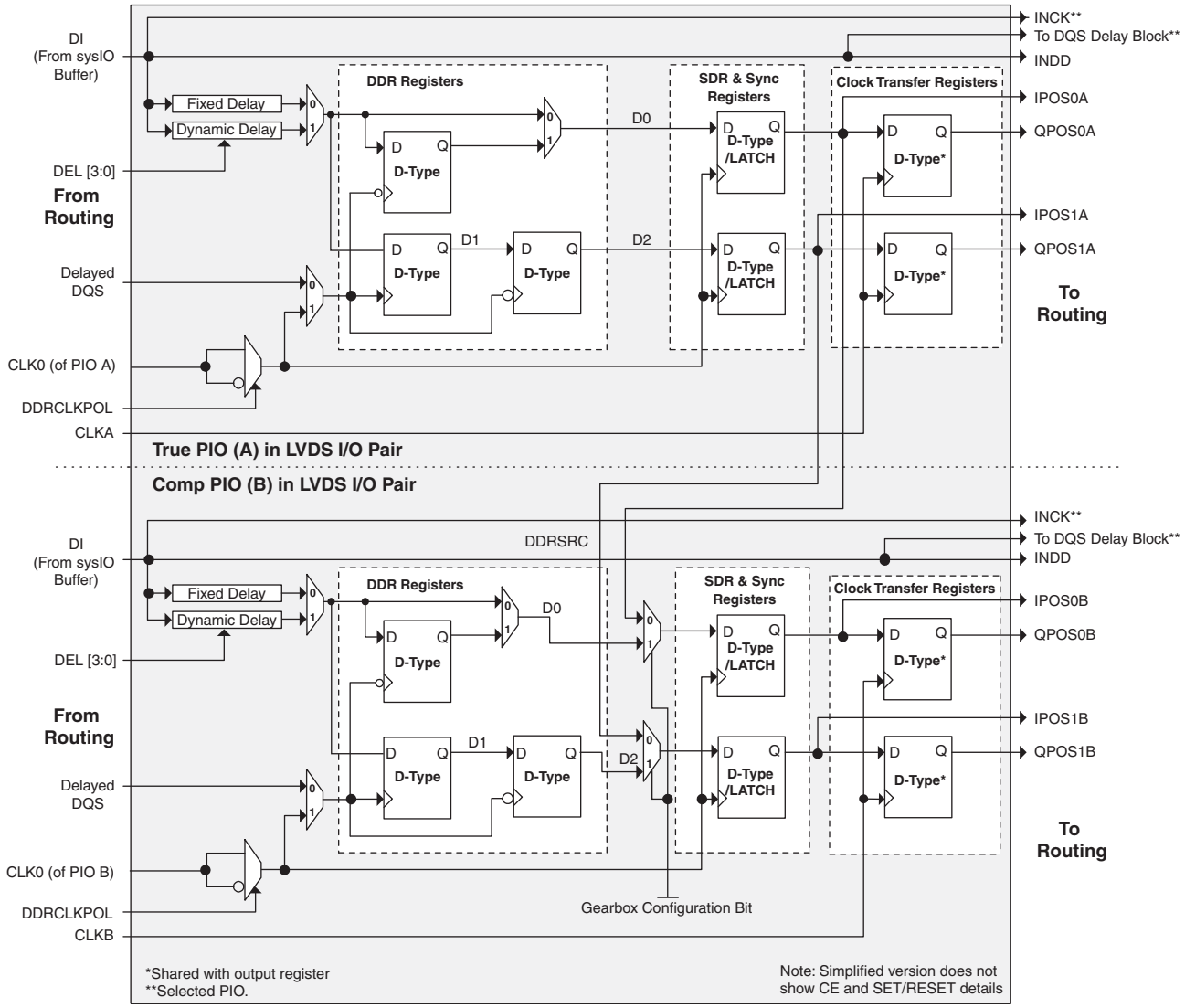
# Programmable I/O Cells (PIC)

Each PIC contains two PIOs connected to their respective sysI/O buffers as shown in Figure 2-28. The PIO Block supplies the output data (DO) and the tri-state control signal (TO) to the sysI/O buffer and receives input from the buffer. Table 2-12 provides the PIO signal list.

By combining input blocks of the complementary PIOs and sharing some registers from output blocks, a gearbox function can be implemented, which takes a double data rate signal applied to PIOA and converts it as four data streams, IPOS0A, IPOS1A, IPOS0B and IPOS1B. Figure 2-29 shows the diagram using this gearbox function. For more information about this topic, please see information regarding additional documentation at the end of this data sheet.

The signal DDRCLKPOL controls the polarity of the clock used in the synchronization registers. It ensures adequate timing when data is transferred from the DQS to the system clock domain. For further information about this topic, see the DDR Memory section of this data sheet.

***Figure 2-29. Input Register Block for Left, Right and Bottom Edges***



## SERDES Power Supply Requirements (LatticeECP2M Family Only)[1]

**Over Recommended Operating Conditions**

| Symbol | Description | Typ.[2] | Units |
|---|---|---|---|
| **Standby (Power Down)** | | | |
| $I_{CCTX-SB}$ | $V_{CCTX}$ current (per channel) | 10 | µA |
| $I_{CCRX-SB}$ | $V_{CCRX}$ current (per channel) | 75 | µA |
| $I_{CCIB-SB}$ | Input buffer current (per channel) | 0 | µA |
| $I_{CCOB-SB}$ | Output buffer current (per channel) | 0 | µA |
| $I_{CCP-SB}$ | SERDES PLL current (per quad) | 30 | µA |
| $I_{CCAX33-SB}$ | SERDES termination current (per quad) | 10 | µA |
| **Operating (Data Rate = 3.125 Gbps)** | | | |
| $I_{CCTX-OP}$ | $V_{CCTX}$ current (per channel) | 19 | mA |
| $I_{CCRX-OP}$ | $V_{CCRX}$ current (per channel) | 34 | mA |
| $I_{CCIB-OP}$ | Input buffer current (per channel) | 4 | mA |
| $I_{CCOB-OP}$ | Output buffer current (per channel) | 13 | mA |
| $I_{CCP-OP}$ | SERDES PLL current (per quad) | 26 | mA |
| $I_{CCAX33-OP}$ | SERDES termination current (per quad) | 0.01 | mA |

1. Equalization enabled, pre-emphasis disabled.
2. $T_J$ = 25°C, power supplies at nominal voltage.

## SERDES Power (LatticeECP2M Family Only)

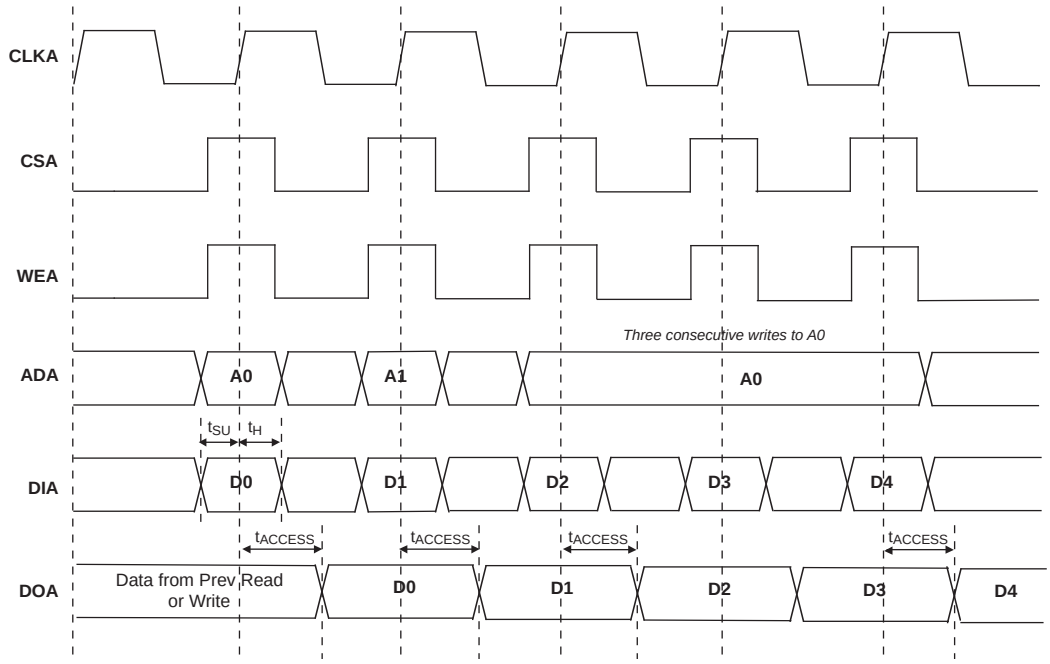
Table 3-1 presents the SERDES power for one channel.

***Table 3-1. SERDES Power[1]***

| Symbol | Description | Typ.[2] | Units |
|---|---|---|---|
| $P_{S-1CH-31}$ | SERDES power (one channel @ 3.125 Gbps) | 90 | mW |
| $P_{S-1CH-25}$ | SERDES power (one channel @ 2.5 Gbps) | 87 | mW |
| $P_{S-1CH-12}$ | SERDES power (one channel @ 1.25 Gbps) | 86 | mW |
| $P_{S-1CH-02}$ | SERDES power (one channel @ 250 Mbps) | 76 | mW |

1. One quarter of the total quad power (includes contribution from common circuits, all channels in the quad operating, pre-emphasis disabled, equalization enabled).
2. Typical values measured at 25ºC and 1.2V.

*Figure 3-11. Write Through (SP Read/Write on Port A, Input Registers Only)*




Note: Input data and address are registered at the positive edge of the clock and output data appears after the positive edge of the clock.

# SERDES High Speed Data Receiver (LatticeECP2M Family Only)

***Table 3-11. Serial Input Data Specifications***

| Symbol | Description | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| $RX\text{-}CID_S$ | Stream of nontransitions[1] (CID = Consecutive Identical Digits) @ $10^{-12}$ BER | | 7 @ 3.125 Gbps<br>20 @ 1.25 Gbps | | Bits |
| $V_{RX\text{-}DIFF\text{-}S}$ | Differential input sensitivity | 100 | — | — | mV, p-p |
| $V_{RX\text{-}IN}$ | Input levels | 0 | — | $V_{CCRX}$ + 0.8 | V |
| $V_{RX\text{-}CM\text{-}DC}$ | Input common mode range (DC coupled) | 0.5 | — | 1.2 | V |
| $V_{RX\text{-}CM\text{-}AC}$ | Input common mode range (AC coupled)[3] | 0 | — | 1.5 | V |
| $T_{RX\text{-}RELOCK}$ | CDR re-lock time[2] | — | — | 3000 | Bits |
| $Z_{RX\text{-}TERM}$ | Input termination 50/75 Ohm/High Z | — | 50 | | Ohms |
| $RL_{RX\text{-}RL}$ | Return loss (without package) | — | 9 | — | dB |

1. This is the number of bits allowed without a transition on the incoming data stream when using DC coupling.
2. This is the typical number of bit times to re-lock to a new phase of frequency within +/- 300 ppm, assuming 8b10b encoded data and the CDR is in lock state. When CDR is in un-lock state, or reset is applied, the total re-lock settling time will be approximately 4ms including analog settle time, calibration time, and acquisition time.
3. AC coupling is used to interface to LVPECL and LVDS.

## Input Data Jitter Tolerance

A receiver's ability to tolerate incoming signal jitter is very dependent on jitter type. High speed serial interface standards have recognized the dependency on jitter type and have recently modified specifications to indicate tolerance levels for different jitter types as they relate to specific protocols (e.g. FC, etc.). Sinusoidal jitter is considered to be a worst case jitter type.

***Table 3-12. Receiver Total Jitter Tolerance Specification[1]***

| Description | Frequency | Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| Deterministic | 3.125 Gbps | 600 mV differential eye | — | — | 0.54 | UI, p-p |
| Random | | 600 mV differential eye | — | — | 0.26 | UI, p-p |
| Total | | 600 mV differential eye | — | — | 0.80 | UI, p-p |
| Deterministic | 2.5 Gbps | 600 mV differential eye | — | — | 0.61 | UI, p-p |
| Random | | 600 mV differential eye | — | — | 0.22 | UI, p-p |
| Total | | 600 mV differential eye | — | — | 0.81 | UI, p-p |
| Deterministic | 1.25 Gbps | 600 mV differential eye | — | — | 0.53 | UI, p-p |
| Random | | 600 mV differential eye | — | — | 0.22 | UI, p-p |
| Total | | 600 mV differential eye | — | — | 0.80 | UI, p-p |
| Deterministic | 250 Mbps[2] | 600 mV differential eye | — | — | 0.42 | UI, p-p |
| Random | | 600 mV differential eye | — | — | 0.10 | UI, p-p |
| Total | | 600 mV differential eye | — | — | 0.60 | UI, p-p |

1. Values are measured with PRBS $2^7$-1, all channels operating, FPGA Logic active, I/Os around SERDES pins quiet, voltages are nominal, room temperature.
2. Jitter specification is limited by measurement equipment capability.

## LatticeECP2M Pin Information Summary, LFE2M20 and LFE2M35

| Pin Type | | LFE2M20 | | LFE2M35 | | |
|---|---|---|---|---|---|---|
| | | 256 fpBGA | 484 fpBGA | 256 fpBGA | 484 fpBGA | 672 fpBGA |
| Single Ended User I/O | | 140 | 304 | 140 | 303 | 410 |
| Differential Pair User I/O | | 70 | 152 | 70 | 151 | 199 |
| Configuration | TAP Pins | 5 | 5 | 5 | 5 | 5 |
| | Muxed Pins | 14 | 14 | 14 | 14 | 14 |
| | Dedicated Pins (Non TAP) | 7 | 7 | 7 | 7 | 7 |
| Non Configuration | Muxed Pins | 64 | 84 | 60 | 84 | 89 |
| | Dedicated Pins | 3 | 3 | 3 | 3 | 3 |
| VCC | | 6 | 16 | 6 | 16 | 29 |
| VCCAUX | | 4 | 8 | 4 | 8 | 17 |
| VCCPLL | | 1 | 4 | 1 | 4 | 8 |
| VCCIO | Bank0 | 1 | 4 | 1 | 4 | 5 |
| | Bank1 | 1 | 3 | 1 | 3 | 4 |
| | Bank2 | 2 | 4 | 2 | 4 | 5 |
| | Bank3 | 2 | 4 | 2 | 4 | 5 |
| | Bank4 | 2 | 4 | 2 | 4 | 4 |
| | Bank5 | 2 | 4 | 2 | 4 | 5 |
| | Bank6 | 2 | 4 | 2 | 4 | 5 |
| | Bank7 | 2 | 4 | 2 | 4 | 5 |
| | Bank8 | 1 | 2 | 1 | 2 | 2 |
| GND, GND0 to GND7 | | 22 | 57 | 22 | 57 | 80 |
| NC | | 17 | 11 | 17 | 12 | 37 |
| Single Ended/ Differential I/O Pairs per Bank (including emulated with resistors) | Bank0 | 0/0 | 36/18 | 0/0 | 36/18 | 63/31 |
| | Bank1 | 0/0 | 18/9 | 0/0 | 18/9 | 18/9 |
| | Bank2 | 14/7 | 30/15 | 14/7 | 30/15 | 50/25 |
| | Bank3 | 16/8 | 36/18 | 16/8 | 36/18 | 43/21 |
| | Bank4 | 32/16 | 62/31 | 32/16 | 62/31 | 50/21 |
| | Bank5 | 20/10 | 28/14 | 20/10 | 28/14 | 60/30 |
| | Bank6 | 16/8 | 40/20 | 16/8 | 39/19 | 52/25 |
| | Bank7 | 28/14 | 40/20 | 28/14 | 40/20 | 60/30 |
| | Bank8 | 14/7 | 14/7 | 14/7 | 14/7 | 14/7 |
| True LVDS I/O Pairs per Bank | Bank0 (Top Edge) | 0 | 0 | 0 | 0 | 0 |
| | Bank1 (Top Edge) | 0 | 0 | 0 | 0 | 0 |
| | Bank2 (Right Edge) | 3 | 7 | 3 | 7 | 12 |
| | Bank3 (Right Edge) | 4 | 9 | 4 | 9 | 11 |
| | Bank4 (Bottom Edge) | 0 | 0 | 0 | 0 | 0 |
| | Bank5 (Bottom Edge) | 0 | 0 | 0 | 0 | 0 |
| | Bank6 (Left Edge) | 4 | 10 | 4 | 10 | 14 |
| | Bank7 (Left Edge) | 7 | 10 | 7 | 10 | 15 |
| | Bank8 (Right Edge) | 0 | 0 | 0 | 0 | 0 |

## Available Device Resources by Package, LatticeECP2

| Resource | Device | 256 fpBGA | 484 fpBGA | 672 fpBGA | 900 fpBGA |
|---|---|---|---|---|---|
| PLL/DLL | ECP2-6 | 4 | — | — | — |
| | ECP2-12 | 4 | 4 | — | — |
| | ECP2-20 | 4 | 4 | 4 | — |
| | ECP2-35 | — | 4 | 4 | — |
| | ECP2-50 | — | 6 | 6 | — |
| | ECP2-70 | — | — | 8 | 8 |

## Available Device Resources by Package, LatticeECP2M

| Resource | Device | 256 fpBGA | 484 fpBGA | 672 fpBGA | 900 fpBGA | 1152 fpBGA |
|---|---|---|---|---|---|---|
| PLL/DLL | ECP2M20 | 10 | 10 | — | — | — |
| | ECP2M35 | 10 | 10 | 10 | — | — |
| | ECP2M50 | — | 10 | 10 | 10 | — |
| | ECP2M70 | — | — | — | 10 | 10 |
| | ECP2M100 | — | — | — | 10 | 10 |

## LatticeECP2M Power Supply and NC (Cont.)

| Signal | 1152 fpBGA |
|---|---|
| $V_{CC}$ | AA13, AA14, AA15, AA16, AA17, AA18, AA19, AA20, AA21, AA22, AB14, AB15, AB20, AB21, N14, N15, N20, N21, P13, P14, P15, P16, P17, P18, P19, P20, P21, P22, R13, R14, R21, R22, T14, T21, U14, U21, V14, V21, W14, W21, Y13, Y14, Y21, Y22 |
| $V_{CCIO0}$ | C12, C16, E14, H12, H16, M14, M15 |
| $V_{CCIO1}$ | C19, C23, E21, H19, H23, M20, M21 |
| $V_{CCIO2}$ | G32, K28, K32, N27, N32, P23, R23, T27, T32 |
| $V_{CCIO3}$ | AA23, AB27, AB32, AE28, AE32, AH32, W27, W32, Y23 |
| $V_{CCIO4}$ | AC20, AC21, AG19, AG23, AK21, AM19, AM23 |
| $V_{CCIO5}$ | AC14, AC15, AG12, AG16, AK14, AM12, AM16 |
| $V_{CCIO6}$ | AA12, AB3, AB8, AE3, AE7, AH3, W3, W8, Y12 |
| $V_{CCIO7}$ | G3, K3, K7, N3, N8, P12, R12, T3, T8 |
| $V_{CCIO8}$ | AD28, AG32 |
| $V_{CCJ}$ | AK3 |
| $V_{CCAUX}$ | AB12, AB13, AB22, AB23, AC13, AC22, M13, M22, N12, N13, N22, N23 |
| $V_{CCPLL}$ | R15, R20, Y15, Y20 |
| SERDES Power[3] | D7, B9, B8, D9, B7, E7, B6, D8, E6, D6, D4, B5, D3, B4, C1, B3, B1, B2, B33, B34, B32, C34, B31, D32, B30, D31, E29, D29, D27, B29, E28, B28, D26, B27, B26, D28, AL28, AN26, AN27, AL26, AN28, AK28, AN29, AL27, AL29, AK29, AL31, AN30, AL32, AN31, AM34, AN32, AN34, AN33, AN2, AN1, AN3, AM1, AN4, AL3, AN5, AL4, AL6, AK6, AL8, AN6, AK7, AN7, AL9, AN8, AN9, AL7 |
| GND[1] | A1, A10, A13, A22, A25, A34, AB16, AB17, AB18, AB19, AB26, AB31, AB4, AB9, AC16, AC17, AC18, AC19, AD27, AE27, AE31, AE4, AE8, AF12, AF16, AF19, AF23, AG31, AH31, AH4, AJ14, AJ21, AK27, AK8, AL10, AL16, AL19, AL2, AL25, AL33, AP1, AP10, AP13, AP22, AP25, AP34, D10, D16, D19, D2, D25, D33, E27, E8, F14, F21, G31, G4, J12, J16, J19, J23, K27, K31, K4, K8, M16, M17, M18, M19, N16, N17, N18, N19, N26, N31, N4, N9, R16, R17, R18, R19, T12, T13, T15, T16, T17, T18, T19, T20, T22, T23, T26, T31, T4, T9, U12, U13, U15, U16, U17, U18, U19, U20, U22, U23, V12, V13, V15, V16, V17, V18, V19, V20, V22, V23, W12, W13, W15, W16, W17, W18, W19, W20, W22, W23, W26, W31, W4, W9, Y16, Y17, Y18, Y19 |
| NC[2] | **LFE2M70:** H2, H1, G5, G6, M9, M10, H3, H4, P3, P4, P9, M7, P1, P2, N7, P7, AC7, AC5, AC6, AD5, AD4, AD3, AD10, AD8, AD2, AD1, AD9, AC11, AD6, AD7, AE1, AE2, AJ12, AH12, AL13, AK13, AE14, AG13, AH22, AH21, AG22, AG21, AF33, AF34, AC27, AC28, AD29, AD30, AE33, AE34, AD32, AD31, AB25, AC25, AB28, AA26, AD33, AD34, P30, P29, P31, P32, R25, T24, N34, N33, F24, G23, J22, G22, H21, K21, L19, L20, L18, K19, J14, L15, H14, K14, F12, D11, F11, E11, A11, A12, A23, A24, AA11, AB11, AC26, AC30, AD11, AD12, AD13, AD14, AD15, AD19, AD21, AD22, AD23, AE10, AE11, AE12, AE13, AE19, AE21, AE22, AE23, AF11, AF21, AF22, AF24, AF8, AF9, AG10, AG11, AG24, AG25, AG26, AG3, AG7, AG8, AG9, AH10, AH11, AH13, AH24, AH25, AH26, AH27, AH5, AH6, AH7, AH8, AH9, AJ10, AJ11, AJ13, AJ24, AJ25, AJ26, AJ27, AJ3, AJ4, AJ5, AJ6, AJ7, AJ8, AJ9, AK10, AK11, AK12, AK24, AK25, AK26, AK4, AK9, AL11, AL12, AL34, AM10, AM11, AM13, AM25, AN10, AN11, AN12, AN13, AN24, AN25, AP11, AP12, AP24, B10, B11, B12, B13, B22, B23, B24, B25, C10, C11, C13, C22, C24, C25, D1, D15, D24, D34, E10, E24, E25, E26, E3, E31, E32, E33, E34, E4, E9, F10, F25, F26, F27, F28, F29, F30, F31, F32, F33, F34, F5, F6, F7, F8, F9, G10, G11, G24, G25, G26, G27, G28, G29, G30, G33, G34, G7, G8, G9, H10, H11, H24, H25, H26, H27, H28, H29, H8, H9, J10, J11, J24, J25, J26, J9, K10, K11, K12, K13, K23, K24, K25, K26, L11, L12, L13, L14, L21, L22, L23, L24, L25, L26, M11, M24, M25, M6, M8, N10, N11, P10, P25, P26, R9, T11, U11, W11, Y10, Y11<br><br>**LFE2M100:** A11, A12, A23, A24, AA11, AB11, AC26, AC30, AD11, AD12, AD13, AD14, AD15, AD19, AD21, AD22, AD23, AE10, AE11, AE12, AE13, AE19, AE21, AE22, AE23, AF11, AF21, AF22, AF24, AF8, AF9, AG10, AG11, AG24, AG25, AG26, AG3, AG7, AG8, AG9, AH10, AH11, AH13, AH24, AH25, AH26, AH27, AH5, AH6, AH7, AH8, AH9, AJ10, AJ11, AJ13, AJ24, AJ25, AJ26, AJ27, AJ3, AJ4, AJ5, AJ6, AJ7, AJ8, AJ9, AK10, AK11, AK12, AK24, AK25, AK26, AK4, AK9, AL11, AL12, AL34, AM10, AM11, AM13, AM25, AN10, AN11, AN12, AN13, AN24, AN25, AP11, AP12, AP24, B10, B11, B12, B13, B22, B23, B24, B25, C10, C11, C13, C22, C24, C25, D1, D15, D24, D34, E10, E24, E25, E26, E3, E31, E32, E33, E34, E4, E9, F10, F25, F26, F27, F28, F29, F30, F31, F32, F33, F34, F5, F6, F7, F8, F9, G10, G11,G24, G25, G26, G27, G28, G29, G30, G33, G34, G7, G8, G9, H10, H11, H24, H25, H26, H27, H28, H29, H8, H9, J10, J11, J24, J25, J26, J9, K10, K11, K12, K13, K23, K24, K25, K26, L11, L12, L13, L14, L21, L22, L23, L24, L25, L26, M11, M24, M25, M6, M8, N10, N11, P10, P25, P26, R9, T11, U11, W11, Y10, Y11 |

1. All grounds must be electrically connected at the board level. For fpBGA packages, the total number of GND balls is less than the actual number of GND logic connections from the die to the common package GND plane.
2. NC pins should not be connected to any active signals, VCC or GND.
3. For package migration across device densities, the designer must comprehend the package pin requirements for the SERDES blocks. Specifically, the SERDES power pins of the largest density device must be accounted to accommodate migration to other smaller devices using the same package. Please refer to TN1160, LatticeECP2/M Density Migration for more details.

# LFE2-12E/SE and LFE2-20E/SE Logic Signal Connections: 208 PQFP (Cont.)

| LFE2-12E/SE | | | | | LFE2-20E/SE | | | |
|---|---|---|---|---|---|---|---|---|
| Pin Number | Pin/Pad Function | Bank | Dual Function | Differential | Pin/Pad Function | Bank | Dual Function | Differential |
| 138 | PR15A | 3 | PCLKT3_0 | T (LVDS)* | PR21A | 3 | PCLKT3_0/RDQ25 | T (LVDS)* |
| 139 | GND | - | | | GND | - | | |
| 140 | VCC | - | | | VCC | - | | |
| 141 | PR13B | 2 | PCLKC2_0/RDQ10 | C | PR19B | 2 | PCLKC2_0/RDQ16 | C |
| 142 | PR13A | 2 | PCLKT2_0/RDQ10 | T | PR19A | 2 | PCLKT2_0/RDQ16 | T |
| 143 | VCCIO2 | 2 | | | VCCIO2 | 2 | | |
| 144 | PR12A | 2 | RDQ10 | | PR16A | 2 | RDQS16 | |
| 145 | GND | - | | | GND | - | | |
| 146 | VCC | - | | | VCC | - | | |
| 147 | PR8B | 2 | RDQ10 | C (LVDS)* | PR14B | 2 | RDQ16 | C (LVDS)* |
| 148 | VCCIO2 | 2 | | | VCCIO2 | 2 | | |
| 149 | PR8A | 2 | RDQ10 | T (LVDS)* | PR14A | 2 | RDQ16 | T (LVDS)* |
| 150 | PR6B | 2 | RDQ10 | C (LVDS)* | PR12B | 2 | RDQ16 | C (LVDS)* |
| 151 | VCCAUX | - | | | VCCAUX | - | | |
| 152 | PR6A | 2 | RDQ10 | T (LVDS)* | PR12A | 2 | RDQ16 | T (LVDS)* |
| 153 | PR4B | 2 | | C (LVDS)* | PR6B | 2 | RDQ8 | C (LVDS)* |
| 154 | PR4A | 2 | | T (LVDS)* | PR6A | 2 | RDQ8 | T (LVDS)* |
| 155 | PR2B | 2 | VREF2_2 | C (LVDS)* | PR2B | 2 | VREF2_2 | C (LVDS)* |
| 156 | PR2A | 2 | VREF1_2 | T (LVDS)* | PR2A | 2 | VREF1_2 | T (LVDS)* |
| 157 | PT55B | 1 | VREF2_1 | C | PT64B | 1 | VREF2_1 | C |
| 158 | PT55A | 1 | VREF1_1 | T | PT64A | 1 | VREF1_1 | T |
| 159 | GND | - | | | GND | - | | |
| 160 | PT54B | 1 | | C | PT62B | 1 | | C |
| 161 | PT54A | 1 | | T | PT62A | 1 | | T |
| 162 | VCCIO1 | 1 | | | VCCIO1 | 1 | | |
| 163 | PT52B | 1 | | C | PT60B | 1 | | C |
| 164 | PT52A | 1 | | T | PT60A | 1 | | T |
| 165 | PT50B | 1 | | C | PT58B | 1 | | C |
| 166 | PT50A | 1 | | T | PT58A | 1 | | T |
| 167 | PT48B | 1 | | C | PT56B | 1 | | C |
| 168 | PT48A | 1 | | T | PT56A | 1 | | T |
| 169 | GND | - | | | GND | - | | |
| 170 | VCCIO1 | 1 | | | VCCIO1 | 1 | | |
| 171 | VCC | - | | | VCC | - | | |
| 172 | PT40B | 1 | | C | PT50B | 1 | | C |
| 173 | PT40A | 1 | | T | PT50A | 1 | | T |
| 174 | VCCAUX | - | | | VCCAUX | - | | |
| 175 | GND | - | | | GND | - | | |
| 176 | PT36B | 1 | | C | PT44B | 1 | | C |
| 177 | PT36A | 1 | | T | PT44A | 1 | | T |
| 178 | PT34B | 1 | | C | PT42B | 1 | | C |
| 179 | PT34A | 1 | | T | PT42A | 1 | | T |
| 180 | PT30B | 1 | PCLKC1_0 | C | PT39B | 1 | PCLKC1_0 | C |
| 181 | PT30A | 1 | PCLKT1_0 | T | PT39A | 1 | PCLKT1_0 | T |
| 182 | XRES | 1 | | | XRES | 1 | | |
| 183 | PT28B | 0 | PCLKC0_0 | C | PT37B | 0 | PCLKC0_0 | C |

# LFE2-35E/SE and LFE2-50E/SE Logic Signal Connections: 484 fpBGA (Cont.)

| LFE2-35E/SE | | | | | LFE2-50E/SE | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| W13 | PB46A | 4 | BDQ42 | T | PB55A | 4 | BDQ51 | T |
| GNDIO | GNDIO4 | - | | | GNDIO4 | - | | |
| W14 | PB46B | 4 | BDQ42 | C | PB55B | 4 | BDQ51 | C |
| AB18 | PB48A | 4 | BDQ51 | T | PB57A | 4 | BDQ60 | T |
| AB19 | PB48B | 4 | BDQ51 | C | PB57B | 4 | BDQ60 | C |
| V14 | PB49A | 4 | BDQ51 | T | PB58A | 4 | BDQ60 | T |
| W15 | PB49B | 4 | BDQ51 | C | PB58B | 4 | BDQ60 | C |
| VCCIO | VCCIO4 | 4 | | | VCCIO | 4 | | |
| Y15 | PB50A | 4 | BDQ51 | T | PB59A | 4 | BDQ60 | T |
| AA15 | PB50B | 4 | BDQ51 | C | PB59B | 4 | BDQ60 | C |
| GNDIO | GNDIO4 | - | | | GNDIO4 | - | | |
| AA16 | PB51A | 4 | BDQS51 | T | PB60A | 4 | BDQS60 | T |
| AA17 | PB51B | 4 | BDQ51 | C | PB60B | 4 | BDQ60 | C |
| AB20 | PB52A | 4 | BDQ51 | T | PB61A | 4 | BDQ60 | T |
| AB21 | PB52B | 4 | BDQ51 | C | PB61B | 4 | BDQ60 | C |
| U15 | PB53A | 4 | BDQ51 | T | PB62A | 4 | BDQ60 | T |
| U16 | PB53B | 4 | BDQ51 | C | PB62B | 4 | BDQ60 | C |
| VCCIO | VCCIO4 | 4 | | | VCCIO | 4 | | |
| Y16 | PB54A | 4 | BDQ51 | T | PB63A | 4 | BDQ60 | T |
| W16 | PB54B | 4 | BDQ51 | C | PB63B | 4 | BDQ60 | C |
| AA18 | PB55A | 4 | BDQ51 | T | PB64A | 4 | BDQ60 | T |
| AA20 | PB55B | 4 | BDQ51 | C | PB64B | 4 | BDQ60 | C |
| GNDIO | GNDIO4 | - | | | GNDIO4 | - | | |
| VCCIO | VCCIO4 | 4 | | | VCCIO | 4 | | |
| AA21 | PB66A | 4 | BDQ69 | T | PB75A | 4 | BDQ78 | T |
| AA22 | PB66B | 4 | BDQ69 | C | PB75B | 4 | BDQ78 | C |
| V16 | PB67A | 4 | BDQ69 | T | PB76A | 4 | BDQ78 | T |
| V17 | PB67B | 4 | BDQ69 | C | PB76B | 4 | BDQ78 | C |
| VCCIO | VCCIO4 | 4 | | | VCCIO | 4 | | |
| Y18 | PB68A | 4 | BDQ69 | T | PB77A | 4 | BDQ78 | T |
| Y17 | PB68B | 4 | BDQ69 | C | PB77B | 4 | BDQ78 | C |
| GNDIO | GNDIO4 | - | | | GNDIO4 | - | | |
| Y19 | PB69A | 4 | BDQS69 | T | PB78A | 4 | BDQS78 | T |
| Y20 | PB69B | 4 | BDQ69 | C | PB78B | 4 | BDQ78 | C |
| W17 | PB70A | 4 | BDQ69 | T | PB79A | 4 | BDQ78 | T |
| W18 | PB70B | 4 | BDQ69 | C | PB79B | 4 | BDQ78 | C |
| Y21 | PB71A | 4 | BDQ69 | T | PB80A | 4 | BDQ78 | T |
| Y22 | PB71B | 4 | BDQ69 | C | PB80B | 4 | BDQ78 | C |
| VCCIO | VCCIO4 | 4 | | | VCCIO | 4 | | |
| U18 | PB72A | 4 | BDQ69 | T | PB81A | 4 | BDQ78 | T |
| V18 | PB72B | 4 | BDQ69 | C | PB81B | 4 | BDQ78 | C |
| T15 | PB73A | 4 | VREF2_4/BDQ69 | T | PB82A | 4 | VREF2_4/BDQ78 | T |
| T16 | PB73B | 4 | VREF1_4/BDQ69 | C | PB82B | 4 | VREF1_4/BDQ78 | C |
| GNDIO | GNDIO4 | - | | | GNDIO4 | - | | |
| W19 | CFG2 | 8 | | | CFG2 | 8 | | |
| V19 | CFG1 | 8 | | | CFG1 | 8 | | |

# LFE2-35E/SE and LFE2-50E/SE Logic Signal Connections: 484 fpBGA (Cont.)

| LFE2-35E/SE | | | | | LFE2-50E/SE | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| D15 | PT52A | 1 | | T | PT61A | 1 | | T |
| E15 | PT51B | 1 | | C | PT60B | 1 | | C |
| F15 | PT51A | 1 | | T | PT60A | 1 | | T |
| GNDIO | GNDIO1 | - | | | GNDIO1 | - | | |
| B15 | PT49B | 1 | | C | PT58B | 1 | | C |
| VCCIO | VCCIO1 | 1 | | | VCCIO | 1 | | |
| A15 | PT49A | 1 | | T | PT58A | 1 | | T |
| B14 | PT48B | 1 | | C | PT57B | 1 | | C |
| A14 | PT48A | 1 | | T | PT57A | 1 | | T |
| D14 | PT46B | 1 | | C | PT55B | 1 | | C |
| C13 | PT46A | 1 | | T | PT55A | 1 | | T |
| GNDIO | GNDIO1 | - | | | GNDIO1 | - | | |
| E14 | PT45B | 1 | | C | PT54B | 1 | | C |
| F14 | PT45A | 1 | | T | PT54A | 1 | | T |
| A13 | PT44B | 1 | | C | PT53B | 1 | | C |
| B13 | PT44A | 1 | | T | PT53A | 1 | | T |
| VCCIO | VCCIO1 | 1 | | | VCCIO | 1 | | |
| E13 | PT43B | 1 | | C | PT52B | 1 | | C |
| D13 | PT43A | 1 | | T | PT52A | 1 | | T |
| E12 | PT42B | 1 | | C | PT51B | 1 | | C |
| D12 | PT42A | 1 | | T | PT51A | 1 | | T |
| GNDIO | GNDIO1 | - | | | GNDIO1 | - | | |
| A12 | PT40B | 1 | | C | PT49B | 1 | | C |
| A11 | PT40A | 1 | | T | PT49A | 1 | | T |
| VCCIO | VCCIO1 | 1 | | | VCCIO | 1 | | |
| B12 | PT39B | 1 | PCLKC1_0 | C | PT48B | 1 | PCLKC1_0 | C |
| C12 | PT39A | 1 | PCLKT1_0 | T | PT48A | 1 | PCLKT1_0 | T |
| F12 | XRES | 1 | | | XRES | 1 | | |
| B10 | PT37B | 0 | PCLKC0_0 | C | PT46B | 0 | PCLKC0_0 | C |
| GNDIO | GNDIO0 | - | | | GNDIO0 | 0 | | |
| B11 | PT37A | 0 | PCLKT0_0 | T | PT46A | 0 | PCLKT0_0 | T |
| A10 | PT36B | 0 | | C | PT45B | 0 | | C |
| A9 | PT36A | 0 | | T | PT45A | 0 | | T |
| C11 | PT35B | 0 | | C | PT44B | 0 | | C |
| VCCIO | VCCIO0 | 0 | | | VCCIO | 0 | | |
| C10 | PT35A | 0 | | T | PT44A | 0 | | T |
| E11 | PT34B | 0 | | C | PT43B | 0 | | C |
| F11 | PT34A | 0 | | T | PT43A | 0 | | T |
| A8 | PT33B | 0 | | C | PT42B | 0 | | C |
| A7 | PT33A | 0 | | T | PT42A | 0 | | T |
| B8 | PT32B | 0 | | C | PT41B | 0 | | C |
| GNDIO | GNDIO0 | - | | | GNDIO0 | 0 | | |
| B9 | PT32A | 0 | | T | PT41A | 0 | | T |
| VCCIO | VCCIO0 | 0 | | | VCCIO | 0 | | |
| B7 | PT30B | 0 | | C | PT39B | 0 | | C |
| A6 | PT30A | 0 | | T | PT39A | 0 | | T |

## LFE2-70E/SE Logic Signal Connections: 900 fpBGA (Cont.)

| LFE2-70E/SE | | | | |
|---|---|---|---|---|
| **Ball Number** | **Ball/Pad Function** | **Bank** | **Dual Function** | **Differential** |
| K28 | PR25A | 2 | RDQ29 | T (LVDS)* |
| J24 | PR24B | 2 | RDQ21 | C |
| J26 | PR24A | 2 | RDQ21 | T |
| GND | GNDIO2 | - | | |
| K29 | PR23B | 2 | RDQ21 | C (LVDS)* |
| K30 | PR23A | 2 | RDQ21 | T (LVDS)* |
| J23 | PR22B | 2 | RDQ21 | C |
| J25 | PR22A | 2 | RDQ21 | T |
| VCCIO | VCCIO2 | 99 | | |
| J27 | PR21B | 2 | RDQ21 | C (LVDS)* |
| J28 | PR21A | 2 | RDQS21 | T (LVDS)* |
| H26 | PR20B | 2 | RDQ21 | C |
| GND | GNDIO2 | - | | |
| H24 | PR20A | 2 | RDQ21 | T |
| J29 | PR19B | 2 | RDQ21 | C (LVDS)* |
| J30 | PR19A | 2 | RDQ21 | T (LVDS)* |
| H25 | PR18B | 2 | RDQ21 | C |
| VCCIO | VCCIO2 | 2 | | |
| H23 | PR18A | 2 | RDQ21 | T |
| G27 | PR15B | 2 | RUM1_SPLLC_FB_A/RDQ12 | C |
| GND | GNDIO2 | - | | |
| H27 | PR15A | 2 | RUM1_SPLLT_FB_A/RDQ12 | T |
| G29 | PR14B | 2 | RUM1_SPLLC_IN_A/RDQ12 | C (LVDS)* |
| G28 | PR14A | 2 | RUM1_SPLLT_IN_A/RDQ12 | T (LVDS)* |
| VCCIO | VCCIO2 | 2 | | |
| GND | GNDIO2 | - | | |
| G26 | PR6B | 2 | | C (LVDS)* |
| G25 | PR6A | 2 | | T (LVDS)* |
| G30 | PR5B | 2 | | C |
| F30 | PR5A | 2 | | T |
| VCCIO | VCCIO2 | 2 | | |
| F26 | PR4B | 2 | | C (LVDS)* |
| F27 | PR4A | 2 | | T (LVDS)* |
| F29 | PR3B | 2 | | C |
| GND | GNDIO2 | - | | |
| F28 | PR3A | 2 | | T |
| H29 | PR2B | 2 | VREF2_2 | C (LVDS)* |
| H30 | PR2A | 2 | VREF1_2 | T (LVDS)* |
| VCCIO | VCCIO2 | 2 | | |
| B26 | PT100B | 1 | VREF2_1 | C |
| A26 | PT100A | 1 | VREF1_1 | T |
| GND | GNDIO1 | - | | |
| C25 | PT99B | 1 | | C |

## LFE2-70E/SE Logic Signal Connections: 900 fpBGA (Cont.)

| LFE2-70E/SE | | | | |
|---|---|---|---|---|
| **Ball Number** | **Ball/Pad Function** | **Bank** | **Dual Function** | **Differential** |
| E27 | NC | - | | |
| E28 | NC | - | | |
| E29 | NC | - | | |
| E3 | NC | - | | |
| E30 | NC | - | | |
| E4 | NC | - | | |
| E5 | NC | - | | |
| E6 | NC | - | | |
| F25 | NC | - | | |
| F5 | NC | - | | |
| F6 | NC | - | | |
| G6 | NC | - | | |
| G7 | NC | - | | |
| K10 | NC | - | | |
| K9 | NC | - | | |
| N27 | NC | - | | |
| N4 | NC | - | | |
| R1 | NC | - | | |
| R2 | NC | - | | |
| V27 | NC | - | | |
| V4 | NC | - | | |
| P22 | VCCPLL | - | | |
| P8 | VCCPLL | - | | |
| T22 | VCCPLL | - | | |
| Y7 | VCCPLL | - | | |

* Supports true LVDS. Other differential signals must be emulated with external resistors.
** These dedicated input pins can be used for GPLLs or GDLLs within the respective quadrant.
***Due to packaging bond out option, this DQS does not have all the necessary DQ pins bonded out for a full 8-bit data width.

Note: VCCIO and GND pads are used to determine the average DC current drawn by I/Os between GND/VCCIO connections, or between the last GND/VCCIO in an I/O bank and the end of an I/O bank. The substrate pads listed in the Pin Table do not necessarily have a one to one connection with a package ball or pin.

# LFE2M-20E/SE and LFE2M-35E/SE Logic Signal Connections: 256 fpBGA (Cont.)

| LFE2M20E/SE | | | | | LFE2M35E/SE | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| GNDIO | GNDIO6 | - | | | GNDIO6 | - | | |
| L1 | PL42A | 6 | LLM0_GPLLT_IN_A | T (LVDS)* | PL57A | 6 | LLM0_GPLLT_IN_A**/LDQS57*** | T (LVDS)* |
| GNDIO | GNDIO6 | - | | | GNDIO6 | - | | |
| L2 | PL42B | 6 | LLM0_GPLLC_IN_A | C (LVDS)* | PL57B | 6 | LLM0_GPLLC_IN_A**/LDQ57 | C(LVDS)* |
| L3 | PL43A | 6 | LLM0_GPLLT_FB_A | T | PL58A | 6 | LLM0_GPLLT_FB_A/LDQ57 | T |
| L4 | PL43B | 6 | LLM0_GPLLC_FB_A | C | PL58B | 6 | LLM0_GPLLC_FB_A/LDQ57 | C |
| VCCIO | VCCIO6 | 6 | | | VCCIO6 | 6 | | |
| M1 | PL44A | 6 | LLM0_GDLLT_IN_A | T (LVDS)* | PL59A | 6 | LLM0_GDLLT_IN_A**/LDQ57 | T (LVDS)* |
| N1 | PL44B | 6 | LLM0_GDLLC_IN_A | C (LVDS)* | PL59B | 6 | LLM0_GDLLC_IN_A**/LDQ57 | C(LVDS)* |
| N2 | PL45A | 6 | LLM0_GDLLT_FB_A | T | PL60A | 6 | LLM0_GDLLT_FB_A/LDQ57 | T |
| N3 | PL45B | 6 | LLM0_GDLLC_FB_A | C | PL60B | 6 | LLM0_GDLLC_FB_A/LDQ57 | C |
| GNDIO | GNDIO6 | - | | | GNDIO6 | - | | |
| M4 | LLM0_PLLCAP | 6 | | | LLM0_PLLCAP | 6 | | |
| VCCIO | VCCIO6 | 6 | | | VCCIO6 | 6 | | |
| GNDIO | GNDIO6 | - | | | GNDIO6 | - | | |
| K6 | TCK | - | | | TCK | - | | |
| L5 | TDI | - | | | TDI | - | | |
| N4 | TMS | - | | | TMS | - | | |
| N6 | TDO | - | | | TDO | - | | |
| K7 | VCCJ | - | | | VCCJ | - | | |
| M5 | PB2A | 5 | BDQ6 | T | PB2A | 5 | BDQ6 | T |
| N5 | PB2B | 5 | BDQ6 | C | PB2B | 5 | BDQ6 | C |
| L6 | PB3A | 5 | BDQ6 | T | PB3A | 5 | BDQ6 | T |
| M6 | PB3B | 5 | BDQ6 | C | PB3B | 5 | BDQ6 | C |
| P3 | PB4A | 5 | BDQ6 | T | PB4A | 5 | BDQ6 | T |
| VCCIO | VCCIO5 | 5 | | | VCCIO5 | 5 | | |
| P4 | PB4B | 5 | BDQ6 | C | PB4B | 5 | BDQ6 | C |
| P2 | PB5A | 5 | BDQ6 | T | PB5A | 5 | BDQ6 | T |
| P1 | PB5B | 5 | BDQ6 | C | PB5B | 5 | BDQ6 | C |
| R1 | PB6A | 5 | BDQS6 | T | PB6A | 5 | BDQS6 | T |
| GNDIO | GNDIO5 | - | | | GNDIO5 | - | | |
| R2 | PB6B | 5 | BDQ6 | C | PB6B | 5 | BDQ6 | C |
| R3 | PB7A | 5 | BDQ6 | T | PB7A | 5 | BDQ6 | T |
| T2 | PB7B | 5 | BDQ6 | C | PB7B | 5 | BDQ6 | C |
| R4 | PB8A | 5 | BDQ6 | T | PB8A | 5 | BDQ6 | T |
| VCCIO | VCCIO5 | 5 | | | VCCIO5 | 5 | | |
| T3 | PB8B | 5 | BDQ6 | C | PB8B | 5 | BDQ6 | C |
| T4 | PB10A | 5 | BDQ6 | T | PB10A | 5 | BDQ6 | T |
| GNDIO | GNDIO5 | - | | | GNDIO5 | - | | |
| T5 | PB10B | 5 | BDQ6 | C | PB10B | 5 | BDQ6 | C |
| VCCIO | VCCIO5 | 5 | | | VCCIO5 | 5 | | |
| GNDIO | GNDIO5 | - | | | GNDIO5 | - | | |
| T6 | PB16A | 5 | VREF2_5/BDQ15 | T | PB34A | 5 | VREF2_5/BDQ33 | T |
| R6 | PB16B | 5 | VREF1_5/BDQ15 | C | PB34B | 5 | VREF1_5/BDQ33 | C |
| P6 | PB17A | 5 | PCLKT5_0/BDQ15 | T | PB35A | 5 | PCLKT5_0/BDQ33 | T |
| P7 | PB17B | 5 | PCLKC5_0/BDQ15 | C | PB35B | 5 | PCLKC5_0/BDQ33 | C |
| VCCIO | VCCIO5 | 5 | | | VCCIO5 | 5 | | |
| GNDIO | GNDIO5 | - | | | GNDIO5 | - | | |

# LFE2M-20E/SE and LFE2M-35E/SE Logic Signal Connections: 256 fpBGA (Cont.)

| LFE2M20E/SE | | | | | LFE2M35E/SE | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| N11 | CCLK | 8 | | | CCLK | 8 | | |
| M11 | INITN | 8 | | | INITN | 8 | | |
| N13 | DONE | 8 | | | DONE | 8 | | |
| GNDIO | GNDIO8 | - | | | GNDIO8 | - | | |
| M12 | PR53B | 8 | WRITEN | C | PR68B | 8 | WRITEN | C |
| M13 | PR53A | 8 | CS1N | T | PR68A | 8 | CS1N | T |
| N14 | PR52B | 8 | CSN | C | PR67B | 8 | CSN | C |
| N15 | PR52A | 8 | D0/SPIFASTN | T | PR67A | 8 | D0/SPIFASTN | T |
| VCCIO | VCCIO8 | 8 | | | VCCIO8 | 8 | | |
| N16 | PR51B | 8 | D1 | C | PR66B | 8 | D1 | C |
| M16 | PR51A | 8 | D2 | T | PR66A | 8 | D2 | T |
| L12 | PR50B | 8 | D3 | C | PR65B | 8 | D3 | C |
| GNDIO | GNDIO8 | - | | | GNDIO8 | - | | |
| L13 | PR50A | 8 | D4 | T | PR65A | 8 | D4 | T |
| L16 | PR49B | 8 | D5 | C | PR64B | 8 | D5 | C |
| K16 | PR49A | 8 | D6 | T | PR64A | 8 | D6 | T |
| L14 | PR48B | 8 | D7/SPID0*** | C | PR63B | 8 | D7/SPID0*** | C |
| VCCIO | VCCIO8 | 8 | | | VCCIO8 | 8 | | |
| L15 | PR48A | 8 | DI/CSSPI0N | T | PR63A | 8 | DI/CSSPI0N | T |
| K13 | PR47B | 8 | DOUT/CSON/CSSPI1N | C | PR62B | 8 | DOUT/CSON/CSSPI1N | C |
| K14 | PR47A | 8 | BUSY/SISPI | T | PR62A | 8 | BUSY/SISPI | T |
| K11 | RLM0_PLLCAP | 3 | | | RLM0_PLLCAP | 3 | | |
| K15 | PR45B | 3 | RLM0_GDLLC_FB_A | C | PR60B | 3 | RLM0_GDLLC_FB_A/RDQ57 | C |
| GNDIO | GNDIO3 | - | | | GNDIO3 | - | | |
| J16 | PR45A | 3 | RLM0_GDLLT_FB_A | T | PR60A | 3 | RLM0_GDLLT_FB_A/RDQ57 | T |
| H16 | PR44B | 3 | RLM0_GDLLC_IN_A | C (LVDS)* | PR59B | 3 | RLM0_GDLLC_IN_A**/RDQ57 | C(LVDS)* |
| J15 | PR44A | 3 | RLM0_GDLLT_IN_A | T (LVDS)* | PR59A | 3 | RLM0_GDLLT_IN_A**/RDQ57 | T (LVDS)* |
| J14 | PR43B | 3 | RLM0_GPLLC_IN_A | C | PR58B | 3 | RLM0_GPLLC_IN_A**/RDQ57 | C |
| VCCIO | VCCIO3 | 3 | | | VCCIO3 | 3 | | |
| J13 | PR43A | 3 | RLM0_GPLLT_IN_A | T | PR58A | 3 | RLM0_GPLLT_IN_A**/RDQ57 | T |
| H13 | PR42B | 3 | RLM0_GPLLC_FB_A | C (LVDS)* | PR57B | 3 | RLM0_GPLLC_FB_A/RDQ57 | C(LVDS)* |
| H12 | PR42A | 3 | RLM0_GPLLT_FB_A | T (LVDS)* | PR57A | 3 | RLM0_GPLLT_FB_A/RDQS57*** | T (LVDS)* |
| GNDIO | GNDIO3 | - | | | GNDIO3 | - | | |
| VCCIO | VCCIO3 | 3 | | | VCCIO3 | 3 | | |
| G16 | PR32B | 3 | RLM1_SPLLC_FB_A | C | PR42B | 3 | RLM2_SPLLC_FB_A | C |
| VCCIO | VCCIO3 | 3 | | | VCCIO3 | 3 | | |
| H15 | PR32A | 3 | RLM1_SPLLT_FB_A | T | PR42A | 3 | RLM2_SPLLT_FB_A | T |
| E16 | PR31B | 3 | RLM1_SPLLC_IN_A | C (LVDS)* | PR41B | 3 | RLM2_SPLLC_IN_A | C(LVDS)* |
| F15 | PR31A | 3 | RLM1_SPLLT_IN_A | T (LVDS)* | PR41A | 3 | RLM2_SPLLT_IN_A | T (LVDS)* |
| GNDIO | GNDIO3 | - | | | GNDIO3 | - | | |
| VCCIO | VCCIO3 | 3 | | | VCCIO3 | 3 | | |
| F16 | PR28B | 3 | VREF2_3 | C | PR38B | 3 | VREF2_3 | C |
| G15 | PR28A | 3 | VREF1_3 | T | PR38A | 3 | VREF1_3 | T |
| J11 | PR27B | 3 | PCLKC3_0 | C (LVDS)* | PR37B | 3 | PCLKC3_0 | C(LVDS)* |
| J12 | PR27A | 3 | PCLKT3_0 | T (LVDS)* | PR37A | 3 | PCLKT3_0 | T (LVDS)* |
| G14 | PR25B | 2 | PCLKC2_0/RDQ22 | C | PR35B | 2 | PCLKC2_0/RDQ32 | C |
| G13 | PR25A | 2 | PCLKT2_0/RDQ22 | T | PR35A | 2 | PCLKT2_0/RDQ32 | T |
| GNDIO | GNDIO2 | - | | | GNDIO2 | - | | |

## LFE2M50E/SE Logic Signal Connections: 484 fpBGA

| LFE2M50E/SE | | | | |
|---|---|---|---|---|
| **Ball Number** | **Ball/Pad Function** | **Bank** | **Dual Function** | **Differential** |
| D1 | PL2A | 7 | LDQ6 | T (LVDS)* |
| E1 | PL2B | 7 | LDQ6 | C (LVDS)* |
| F1 | PL3A | 7 | LDQ6 | T |
| F2 | PL3B | 7 | LDQ6 | C |
| F5 | PL4A | 7 | LDQ6 | T (LVDS)* |
| VCCIO | VCCIO7 | 7 | | |
| G6 | PL4B | 7 | LDQ6 | C (LVDS)* |
| F4 | PL5A | 7 | LDQ6 | T |
| F3 | PL5B | 7 | LDQ6 | C |
| G1 | PL6A | 7 | LDQS6 | T (LVDS)* |
| GNDIO | GNDIO7 | - | | |
| G2 | PL6B | 7 | LDQ6 | C (LVDS)* |
| H1 | PL7A | 7 | LDQ6 | T |
| H2 | PL7B | 7 | LDQ6 | C |
| VCCIO | VCCIO7 | 7 | | |
| H7 | PL8A | 7 | LDQ6 | T (LVDS)* |
| H6 | PL8B | 7 | LDQ6 | C (LVDS)* |
| G3 | PL9A | 7 | VREF2_7/LDQ6 | T |
| H3 | PL9B | 7 | VREF1_7/LDQ6 | C |
| GNDIO | GNDIO7 | - | | |
| VCCIO | VCCIO7 | 7 | | |
| H5 | PL11A | 7 | LUM0_SPLLT_IN_A | T (LVDS)* |
| H4 | PL11B | 7 | LUM0_SPLLC_IN_A | C (LVDS)* |
| J1 | PL12A | 7 | LUM0_SPLLT_FB_A | T |
| J2 | PL12B | 7 | LUM0_SPLLC_FB_A | C |
| GNDIO | GNDIO7 | - | | |
| J3 | PL13A | 7 | | T (LVDS)* |
| J4 | PL13B | 7 | | C (LVDS)* |
| J7 | PL14A | 7 | | T |
| VCCIO | VCCIO7 | 7 | | |
| J6 | PL14B | 7 | | C |
| GNDIO | GNDIO7 | - | | |
| VCCIO | VCCIO7 | 7 | | |
| K1 | PL32A | 7 | LUM3_SPLLT_IN_A/LDQ36 | T (LVDS)* |
| K2 | PL32B | 7 | LUM3_SPLLC_IN_A/LDQ36 | C (LVDS)* |
| J5 | PL33A | 7 | LUM3_SPLLT_FB_A/LDQ36 | T |
| K5 | PL33B | 7 | LUM3_SPLLC_FB_A/LDQ36 | C |
| VCCIO | VCCIO7 | 7 | | |
| K7 | PL34A | 7 | LDQ36 | T (LVDS)* |
| K6 | PL34B | 7 | LDQ36 | C (LVDS)* |
| L6 | PL35A | 7 | LDQ36 | T |
| L7 | PL35B | 7 | LDQ36 | C |

## LFE2M50E/SE Logic Signal Connections: 484 fpBGA (Cont.)

| LFE2M50E/SE | | | | |
|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential |
| C12 | URC_SQ_VCCIB2 | 12 | | |
| B12 | URC_SQ_HDINN2 | 12 | | C |
| C11 | URC_SQ_VCCRX2 | 12 | | |
| A15 | URC_SQ_HDOUTP2 | 12 | | T |
| C15 | URC_SQ_VCCOB2 | 12 | | |
| B15 | URC_SQ_HDOUTN2 | 12 | | C |
| C14 | URC_SQ_VCCTX2 | 12 | | |
| B14 | URC_SQ_HDOUTN3 | 12 | | C |
| A13 | URC_SQ_VCCOB3 | 12 | | |
| A14 | URC_SQ_HDOUTP3 | 12 | | T |
| C13 | URC_SQ_VCCTX3 | 12 | | |
| B11 | URC_SQ_HDINN3 | 12 | | C |
| B10 | URC_SQ_VCCIB3 | 12 | | |
| A11 | URC_SQ_HDINP3 | 12 | | T |
| C10 | URC_SQ_VCCRX3 | 12 | | |
| GNDIO | GNDIO1 | - | | |
| VCCIO | VCCIO1 | 1 | | |
| E13 | PT55B | 1 | | C |
| D12 | PT55A | 1 | | T |
| GNDIO | GNDIO1 | - | | |
| A9 | PT54B | 1 | | C |
| A8 | PT54A | 1 | | T |
| A7 | PT53B | 1 | | C |
| A6 | PT53A | 1 | | T |
| VCCIO | VCCIO1 | 1 | | |
| E12 | PT52B | 1 | | C |
| F12 | PT52A | 1 | | T |
| A5 | PT51B | 1 | | C |
| A4 | PT51A | 1 | | T |
| GNDIO | GNDIO1 | - | | |
| B7 | PT50B | 1 | | C |
| B8 | PT50A | 1 | | T |
| G11 | PT49B | 1 | | C |
| E11 | PT49A | 1 | | T |
| VCCIO | VCCIO1 | 1 | | |
| D11 | PT48B | 1 | VREF2_1 | C |
| D10 | PT48A | 1 | VREF1_1 | T |
| G10 | PT47B | 1 | PCLKC1_0 | C |
| F11 | PT47A | 1 | PCLKT1_0 | T |
| G9 | PT46B | 0 | PCLKC0_0 | C |
| GNDIO | GNDIO0 | - | | |
| F9 | PT46A | 0 | PCLKT0_0 | T |
| C9 | PT45B | 0 | VREF2_0 | C |

# LFE2M35E/SE and LFE2M50E/SE Logic Signal Connections: 672 fpBGA (Cont.)

| LFE2M35E/SE | | | | | LFE2M50E/SE | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| C15 | URC_SQ_VCCIB2 | 12 | | | URC_SQ_VCCIB2 | 12 | | |
| B15 | URC_SQ_HDINN2 | 12 | | C | URC_SQ_HDINN2 | 12 | | C |
| C14 | URC_SQ_VCCRX2 | 12 | | | URC_SQ_VCCRX2 | 12 | | |
| A18 | URC_SQ_HDOUTP2 | 12 | | T | URC_SQ_HDOUTP2 | 12 | | T |
| C18 | URC_SQ_VCCOB2 | 12 | | | URC_SQ_VCCOB2 | 12 | | |
| B18 | URC_SQ_HDOUTN2 | 12 | | C | URC_SQ_HDOUTN2 | 12 | | C |
| C17 | URC_SQ_VCCTX2 | 12 | | | URC_SQ_VCCTX2 | 12 | | |
| B17 | URC_SQ_HDOUTN3 | 12 | | C | URC_SQ_HDOUTN3 | 12 | | C |
| A16 | URC_SQ_VCCOB3 | 12 | | | URC_SQ_VCCOB3 | 12 | | |
| A17 | URC_SQ_HDOUTP3 | 12 | | T | URC_SQ_HDOUTP3 | 12 | | T |
| C16 | URC_SQ_VCCTX3 | 12 | | | URC_SQ_VCCTX3 | 12 | | |
| B14 | URC_SQ_HDINN3 | 12 | | C | URC_SQ_HDINN3 | 12 | | C |
| B13 | URC_SQ_VCCIB3 | 12 | | | URC_SQ_VCCIB3 | 12 | | |
| A14 | URC_SQ_HDINP3 | 12 | | T | URC_SQ_HDINP3 | 12 | | T |
| C13 | URC_SQ_VCCRX3 | 12 | | | URC_SQ_VCCRX3 | 12 | | |
| - | - | - | | | GNDIO1 | - | | |
| - | - | - | | | VCCIO1 | 1 | | |
| E17 | PT46B | 1 | | C | PT55B | 1 | | C |
| D17 | PT46A | 1 | | T | PT55A | 1 | | T |
| GNDIO | GNDIO1 | - | | | GNDIO1 | - | | |
| F17 | PT45B | 1 | | C | PT54B | 1 | | C |
| D16 | PT45A | 1 | | T | PT54A | 1 | | T |
| F19 | PT44B | 1 | | C | PT53B | 1 | | C |
| F18 | PT44A | 1 | | T | PT53A | 1 | | T |
| VCCIO | VCCIO1 | 1 | | | VCCIO1 | 1 | | |
| E16 | PT43B | 1 | | C | PT52B | 1 | | C |
| D15 | PT43A | 1 | | T | PT52A | 1 | | T |
| G18 | PT42B | 1 | | C | PT51B | 1 | | C |
| E15 | PT42A | 1 | | T | PT51A | 1 | | T |
| GNDIO | GNDIO1 | - | | | GNDIO1 | - | | |
| G17 | PT41B | 1 | | C | PT50B | 1 | | C |
| E14 | PT41A | 1 | | T | PT50A | 1 | | T |
| D14 | PT40B | 1 | | C | PT49B | 1 | | C |
| D13 | PT40A | 1 | | T | PT49A | 1 | | T |
| VCCIO | VCCIO1 | 1 | | | VCCIO1 | 1 | | |
| F15 | PT39B | 1 | VREF2_1 | C | PT48B | 1 | VREF2_1 | C |
| E12 | PT39A | 1 | VREF1_1 | T | PT48A | 1 | VREF1_1 | T |
| H17 | PT38B | 1 | PCLKC1_0 | C | PT47B | 1 | PCLKC1_0 | C |
| E13 | PT38A | 1 | PCLKT1_0 | T | PT47A | 1 | PCLKT1_0 | T |
| C12 | PT37B | 0 | PCLKC0_0 | C | PT46B | 0 | PCLKC0_0 | C |
| GNDIO | GNDIO0 | - | | | GNDIO0 | - | | |
| G15 | PT37A | 0 | PCLKT0_0 | T | PT46A | 0 | PCLKT0_0 | T |
| C11 | PT36B | 0 | VREF2_0 | C | PT45B | 0 | VREF2_0 | C |
| F14 | PT36A | 0 | VREF1_0 | T | PT45A | 0 | VREF1_0 | T |

# LFE2M35E/SE and LFE2M50E/SE Logic Signal Connections: 672 fpBGA (Cont.)

| LFE2M35E/SE | | | | | LFE2M50E/SE | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| F11 | VCCIO0 | 0 | | | VCCIO0 | 0 | | |
| J13 | VCCIO0 | 0 | | | VCCIO0 | 0 | | |
| K12 | VCCIO0 | 0 | | | VCCIO0 | 1 | | |
| D18 | VCCIO1 | 1 | | | VCCIO1 | 1 | | |
| F16 | VCCIO1 | 1 | | | VCCIO1 | 1 | | |
| J14 | VCCIO1 | 1 | | | VCCIO1 | 1 | | |
| K15 | VCCIO1 | 1 | | | VCCIO1 | 1 | | |
| G25 | VCCIO2 | 2 | | | VCCIO2 | 2 | | |
| L21 | VCCIO2 | 2 | | | VCCIO2 | 2 | | |
| M17 | VCCIO2 | 2 | | | VCCIO2 | 2 | | |
| M25 | VCCIO2 | 2 | | | VCCIO2 | 2 | | |
| N18 | VCCIO2 | 2 | | | VCCIO2 | 2 | | |
| P18 | VCCIO3 | 3 | | | VCCIO3 | 3 | | |
| R17 | VCCIO3 | 3 | | | VCCIO3 | 3 | | |
| R25 | VCCIO3 | 3 | | | VCCIO3 | 3 | | |
| T21 | VCCIO3 | 3 | | | VCCIO3 | 3 | | |
| Y25 | VCCIO3 | 3 | | | VCCIO3 | 3 | | |
| AA16 | VCCIO4 | 4 | | | VCCIO4 | 4 | | |
| AC18 | VCCIO4 | 4 | | | VCCIO4 | 4 | | |
| U15 | VCCIO4 | 4 | | | VCCIO4 | 4 | | |
| V14 | VCCIO4 | 4 | | | VCCIO4 | 4 | | |
| AA11 | VCCIO5 | 5 | | | VCCIO5 | 5 | | |
| V13 | VCCIO5 | 5 | | | VCCIO5 | 5 | | |
| AE12 | VCCIO5 | 5 | | | VCCIO5 | 5 | | |
| AE7 | VCCIO5 | 5 | | | VCCIO5 | 5 | | |
| U12 | VCCIO5 | 5 | | | VCCIO5 | 5 | | |
| P9 | VCCIO6 | 6 | | | VCCIO6 | 6 | | |
| R10 | VCCIO6 | 6 | | | VCCIO6 | 6 | | |
| R2 | VCCIO6 | 6 | | | VCCIO6 | 6 | | |
| T6 | VCCIO6 | 6 | | | VCCIO6 | 6 | | |
| Y2 | VCCIO6 | 6 | | | VCCIO6 | 6 | | |
| G2 | VCCIO7 | 7 | | | VCCIO7 | 7 | | |
| L6 | VCCIO7 | 7 | | | VCCIO7 | 7 | | |
| M10 | VCCIO7 | 7 | | | VCCIO7 | 7 | | |
| M2 | VCCIO7 | 7 | | | VCCIO7 | 7 | | |
| N9 | VCCIO7 | 7 | | | VCCIO7 | 7 | | |
| AC24 | VCCIO8 | 8 | | | VCCIO8 | 8 | | |
| U17 | VCCIO8 | 8 | | | VCCIO8 | 8 | | |
| J11 | VCCAUX | - | | | VCCAUX | - | | |
| J12 | VCCAUX | - | | | VCCAUX | - | | |
| J15 | VCCAUX | - | | | VCCAUX | - | | |
| J16 | VCCAUX | - | | | VCCAUX | - | | |
| L18 | VCCAUX | - | | | VCCAUX | - | | |
| L9 | VCCAUX | - | | | VCCAUX | - | | |
| M18 | VCCAUX | - | | | VCCAUX | - | | |
| M9 | VCCAUX | - | | | VCCAUX | - | | |
| R18 | VCCAUX | - | | | VCCAUX | - | | |
| R9 | VCCAUX | - | | | VCCAUX | - | | |

# LFE2M50E/SE and LFE2M70E/SE Logic Signal Connections: 900 fpBGA (Cont.)

| LFE2M50E/SE | | | | | LFE2M70E/SE | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| AH25 | LRC_SQ_VCCOB1 | 13 | | | LRC_SQ_VCCOB1 | 13 | | |
| AJ25 | LRC_SQ_HDOUTN1 | 13 | | C | LRC_SQ_HDOUTN1 | 13 | | C |
| AH26 | LRC_SQ_VCCTX1 | 13 | | | LRC_SQ_VCCTX1 | 13 | | |
| AJ26 | LRC_SQ_HDOUTN0 | 13 | | C | LRC_SQ_HDOUTN0 | 13 | | C |
| AK27 | LRC_SQ_VCCOB0 | 13 | | | LRC_SQ_VCCOB0 | 13 | | |
| AK26 | LRC_SQ_HDOUTP0 | 13 | | T | LRC_SQ_HDOUTP0 | 13 | | T |
| AH27 | LRC_SQ_VCCTX0 | 13 | | | LRC_SQ_VCCTX0 | 13 | | |
| AJ29 | LRC_SQ_HDINN0 | 13 | | C | LRC_SQ_HDINN0 | 13 | | C |
| AJ30 | LRC_SQ_VCCIB0 | 13 | | | LRC_SQ_VCCIB0 | 13 | | |
| AK29 | LRC_SQ_HDINP0 | 13 | | T | LRC_SQ_HDINP0 | 13 | | T |
| AH30 | LRC_SQ_VCCRX0 | 13 | | | LRC_SQ_VCCRX0 | 13 | | |
| AG27 | CFG2 | 8 | | | CFG2 | 8 | | |
| AD25 | CFG1 | 8 | | | CFG1 | 8 | | |
| AG28 | CFG0 | 8 | | | CFG0 | 8 | | |
| AG30 | PROGRAMN | 8 | | | PROGRAMN | 8 | | |
| AG29 | CCLK | 8 | | | CCLK | 8 | | |
| AC24 | INITN | 8 | | | INITN | 8 | | |
| AF27 | DONE | 8 | | | DONE | 8 | | |
| GNDIO | GNDIO8 | - | | | GNDIO8 | - | | |
| AF28 | WRITEN*** | 8 | | | WRITEN*** | 8 | | |
| AE26 | CS1N*** | 8 | | | CS1N*** | 8 | | |
| AB23 | CSN*** | 8 | | | CSN*** | 8 | | |
| AF29 | D0/SPIFASTN*** | 8 | | | D0/SPIFASTN*** | 8 | | |
| VCCIO | VCCIO8 | 8 | | | VCCIO8 | 8 | | |
| AF30 | D1*** | 8 | | | D1*** | 8 | | |
| AD26 | D2*** | 8 | | | D2*** | 8 | | |
| AE29 | D3*** | 8 | | | D3*** | 8 | | |
| GNDIO | GNDIO8 | - | | | GNDIO8 | - | | |
| AE30 | D4*** | 8 | | | D4*** | 8 | | |
| AD29 | D5*** | 8 | | | D5*** | 8 | | |
| AC25 | D6*** | 8 | | | D6*** | 8 | | |
| AD30 | D7/SPID0*** | 8 | | | D7/SPID0*** | 8 | | |
| VCCIO | VCCIO8 | 8 | | | VCCIO8 | 8 | | |
| AA22 | DI/CSSPI0N*** | 8 | | | DI/CSSPI0N*** | 8 | | |
| AC26 | DOUT/CSON/ CSSPI1N*** | 8 | | | DOUT/CSON/ CSSPI1N*** | 8 | | |
| AA23 | BUSY/SISPI*** | 8 | | | BUSY/SISPI*** | 8 | | |
| AB22 | RLM0_PLLCAP | 3 | | | RLM0_PLLCAP | 3 | | |
| AC27 | PR65B | 3 | RLM0_GDLLC_FB_A | C | PR85B | 3 | RLM0_GDLLC_FB_A/RDQ82 | C |
| GNDIO | GNDIO3 | - | | | GNDIO3 | - | | |
| AC28 | PR65A | 3 | RLM0_GDLLT_FB_A | T | PR85A | 3 | RLM0_GDLLT_FB_A/RDQ82 | T |
| AC29 | PR64B | 3 | RLM0_GDLLC_IN_A** | C (LVDS)* | PR84B | 3 | RLM0_GDLLC_IN_A**/RDQ82 | C (LVDS)* |
| AC30 | PR64A | 3 | RLM0_GDLLT_IN_A** | T (LVDS)* | PR84A | 3 | RLM0_GDLLT_IN_A**/RDQ82 | T (LVDS)* |
| AB30 | PR63B | 3 | RLM0_GPLLC_IN_A** | C | PR83B | 3 | RLM0_GPLLC_IN_A**/RDQ82 | C |
| VCCIO | VCCIO3 | 3 | | | VCCIO3 | 3 | | |
| AA30 | PR63A | 3 | RLM0_GPLLT_IN_A** | T | PR83A | 3 | RLM0_GPLLT_IN_A**/RDQ82 | T |
| AB29 | PR62B | 3 | RLM0_GPLLC_FB_A | C (LVDS)* | PR82B | 3 | RLM0_GPLLC_FB_A/RDQ82 | C (LVDS)* |
| AB28 | PR62A | 3 | RLM0_GPLLT_FB_A | T (LVDS)* | PR82A | 3 | RLM0_GPLLT_FB_A/RDQS82 | T (LVDS)* |
| GNDIO | GNDIO3 | - | | | GNDIO3 | - | | |