# Lattice Semiconductor Corporation - LFE2M50E-6FN484C Datasheet


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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

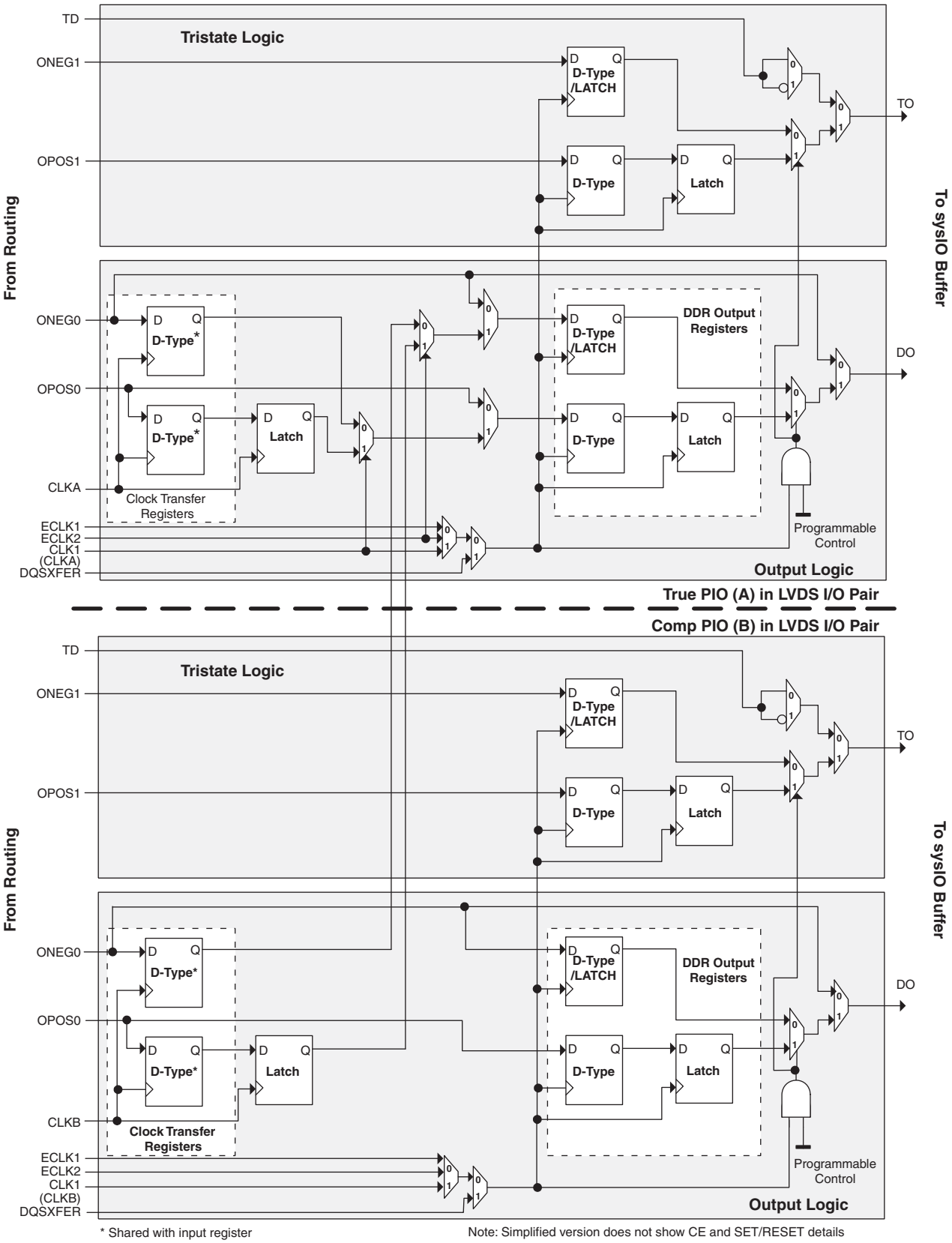
Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Active |
| Number of LABs/CLBs | 6000 |
| Number of Logic Elements/Cells | 48000 |
| Total RAM Bits | 4246528 |
| Number of I/O | 270 |
| Number of Gates | - |
| Voltage - Supply | 1.14V ~ 1.26V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 85°C (TJ) |
| Package / Case | 484-BBGA |
| Supplier Device Package | 484-FPBGA (23x23) |
| Purchase URL | https://www.e-xfl.com/product-detail/lattice-semiconductor/lfe2m50e-6fn484c |

*Figure 2-31. Output and Tristate Block for Left, Right and Bottom Edges*

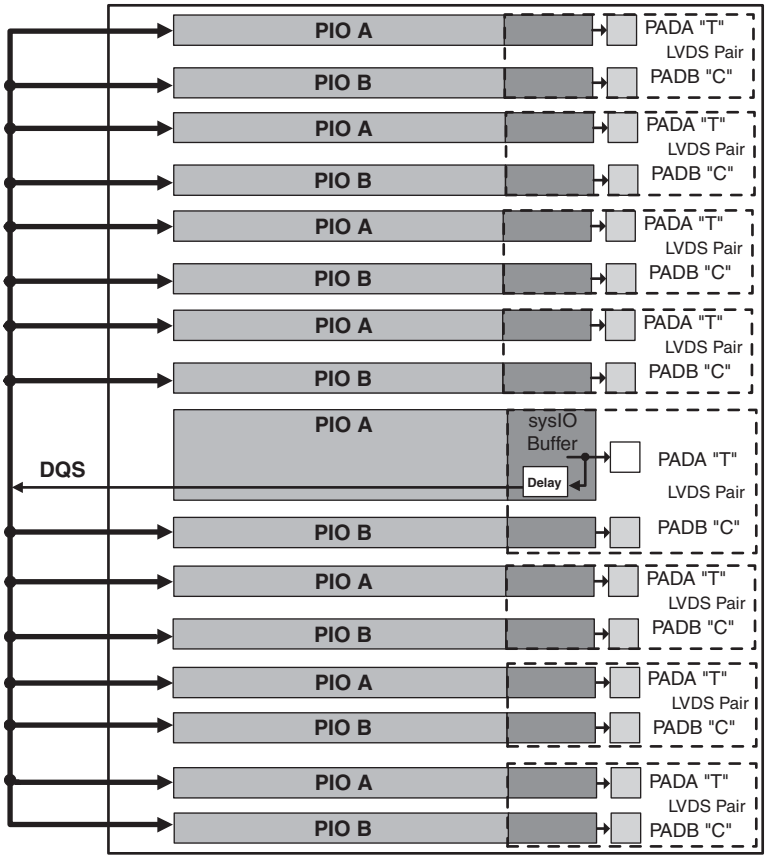


## Top Edge

The PICs on the top edge are different from PIOs on the left, right and bottom edges. PIOs on this edge do not have DDR registers or DQS signals.

The exact DQS pins are shown in a dual function in the Logic Signal Connections table in this data sheet. Additional detail is provided in the Signal Descriptions table. The DQS signal from the bus is used to strobe the DDR data from the memory into input register blocks. Interfaces on the left and right edges are designed for DDR memories that support 16 bits of data, whereas interfaces on the bottom are designed for memories that support 18 bits of data.

***Figure 2-33. DQS Input Routing for the Left and Right Edges of the Device***



# DC Electrical Characteristics

**Over Recommended Operating Conditions**

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $I_{IL}$, $I_{IH}$[1, 2] | Input or I/O Low Leakage | $0 \le V_{IN} \le (V_{CCIO} - 0.2V)$ | — | — | 10 | µA |
| $I_{IH}$[1, 3] | Input or I/O High Leakage | $(V_{CCIO} - 0.2V) < V_{IN} \le 3.6V$ | — | — | 150 | µA |
| $I_{PU}$ | I/O Active Pull-up Current | $0 \le V_{IN} \le 0.7\ V_{CCIO}$ | -30 | — | -210 | µA |
| $I_{PD}$ | I/O Active Pull-down Current | $V_{IL}$ (MAX) $\le V_{IN} \le V_{IH}$ (MAX) | 30 | — | 210 | µA |
| $I_{BHLS}$ | Bus Hold Low Sustaining Current | $V_{IN} = V_{IL}$ (MAX) | 30 | — | — | µA |
| $I_{BHHS}$ | Bus Hold High Sustaining Current | $V_{IN} = 0.7\ V_{CCIO}$ | -30 | — | — | µA |
| $I_{BHLO}$ | Bus Hold Low Overdrive Current | $0 \le V_{IN} \le V_{CCIO}$ | — | — | 210 | µA |
| $I_{BHHO}$ | Bus Hold High Overdrive Current | $0 \le V_{IN} \le V_{CCIO}$ | — | — | -210 | µA |
| $V_{BHT}$ | Bus Hold Trip Points | $0 \le V_{IN} \le V_{IH}$ (MAX) | $V_{IL}$ (MAX) | — | $V_{IH}$ (MIN) | V |
| C1[4] | I/O Capacitance | $V_{CCIO}$ = 3.3V, 2.5V, 1.8V, 1.5V, 1.2V, $V_{CC}$ = 1.2V, $V_{IO}$ = 0 to $V_{IH}$ (MAX) | — | 5 | 8 | pf |
| C2[4] | Dedicated Input Capacitance | $V_{CCIO}$ = 3.3V, 2.5V, 1.8V, 1.5V, 1.2V, $V_{CC}$ = 1.2V, $V_{IO}$ = 0 to $V_{IH}$ (MAX) | — | 5 | 6 | pf |

1. Input or I/O leakage current is measured with the pin configured as an input or as an I/O with the output driver tri-stated. It is not measured with the output driver active. Bus maintenance circuits are disabled.
2. When used as $V_{REF}$, maximum leakage = 25uA
3. Applicable to general purpose I/Os in top and bottom banks.
4. $T_A$ 25°C, f = 1.0MHz.

# Typical Building Block Function Performance[1]

## Pin-to-Pin Performance (LVCMOS25 12mA Drive)

| Function | -7 Timing | Units |
|---|---|---|
| **Basic Functions** | | |
| 16-bit Decoder | 3.8 | ns |
| 32-bit Decoder | 4.5 | ns |
| 64-bit Decoder | 5.0 | ns |
| 4:1 MUX | 3.2 | ns |
| 8:1 MUX | 3.4 | ns |
| 16:1 MUX | 3.5 | ns |
| 32:1 MUX | 4.0 | ns |

1. These timing numbers were generated using the ispLEVER 8.0 design tool. Exact performance may vary with device and tool version. The tool uses internal parameters that have been characterized but are not tested on every device.

## Register-to-Register Performance

| Function | -7 Timing | Units |
|---|---|---|
| **Basic Functions** | | |
| 16-bit Decoder | 599 | MHz |
| 32-bit Decoder | 542 | MHz |
| 64-bit Decoder | 417 | MHz |
| 4:1 MUX | 847 | MHz |
| 8:1 MUX | 803 | MHz |
| 16:1 MUX | 660 | MHz |
| 32:1 MUX | 577 | MHz |
| 8-bit Adder | 591 | MHz |
| 16-bit Adder | 500 | MHz |
| 64-bit Adder | 306 | MHz |
| 16-bit Counter | 488 | MHz |
| 32-bit Counter | 378 | MHz |
| 64-bit Counter | 260 | MHz |
| 64-bit Accumulator | 253 | MHz |
| **Embedded Memory Functions** | | |
| 512x36 Single Port RAM, EBR Output Registers | 370 | MHz |
| 1024x18 True-Dual Port RAM (Write Through or Normal, EBR Output Registers) | 370 | MHz |
| 1024x18 True-Dual Port RAM (Write Through or Normal, PLC Output Registers) | 280 | MHz |
| **Distributed Memory Functions** | | |
| 16x4 Pseudo-Dual Port RAM (One PFU) | 819 | MHz |
| 32x4 Pseudo-Dual Port RAM | 521 | MHz |
| 64x8 Pseudo-Dual Port RAM | 435 | MHz |
| **DSP Functions** | | |
| 18x18 Multiplier (All Registers) | 420 | MHz |
| 9x9 Multiplier (All Registers) | 420 | MHz |

## LatticeECP2/M Family Timing Adders[1, 2, 3]

**Over Recommended Operating Conditions**

| Buffer Type | Description | -7 | -6 | -5 | Units |
|---|---|---|---|---|---|
| **Input Adjusters** | | | | | |
| LVDS25 | LVDS | -0.04 | -0.02 | 0.00 | ns |
| BLVDS25 | BLVDS | -0.04 | -0.09 | -0.15 | ns |
| MLVDS | LVDS | -0.15 | -0.15 | -0.15 | ns |
| RSDS | RSDS | -0.15 | -0.15 | -0.15 | ns |
| LVPECL33 | LVPECL | 0.16 | 0.15 | 0.13 | ns |
| HSTL18_I | HSTL_18 class I | 0.01 | -0.01 | -0.04 | ns |
| HSTL18_II | HSTL_18 class II | 0.01 | -0.01 | -0.04 | ns |
| HSTL18D_I | Differential HSTL 18 class I | 0.01 | -0.01 | -0.04 | ns |
| HSTL18D_II | Differential HSTL 18 class II | 0.01 | -0.01 | -0.04 | ns |
| HSTL15_I | HSTL_15 class I | 0.01 | -0.01 | -0.04 | ns |
| HSTL15D_I | Differential HSTL 15 class I | 0.01 | -0.01 | -0.04 | ns |
| SSTL33_I | SSTL_3 class I | -0.03 | -0.07 | -0.10 | ns |
| SSTL33_II | SSTL_3 class II | -0.03 | -0.07 | -0.10 | ns |
| SSTL33D_I | Differential SSTL_3 class I | -0.03 | -0.07 | -0.10 | ns |
| SSTL33D_II | Differential SSTL_3 class II | -0.03 | -0.07 | -0.10 | ns |
| SSTL25_I | SSTL_2 class I | -0.04 | -0.07 | -0.10 | ns |
| SSTL25_II | SSTL_2 class II | -0.04 | -0.07 | -0.10 | ns |
| SSTL25D_I | Differential SSTL_2 class I | -0.04 | -0.07 | -0.10 | ns |
| SSTL25D_II | Differential SSTL_2 class II | -0.04 | -0.07 | -0.10 | ns |
| SSTL18_I | SSTL_18 class I | -0.01 | -0.04 | -0.07 | ns |
| SSTL18_II | SSTL_18 class II | -0.01 | -0.04 | -0.07 | ns |
| SSTL18D_I | Differential SSTL_18 class I | -0.01 | -0.04 | -0.07 | ns |
| SSTL18D_II | Differential SSTL_18 class II | -0.01 | -0.04 | -0.07 | ns |
| LVTTL33 | LVTTL | -0.16 | -0.16 | -0.16 | ns |
| LVCMOS33 | LVCMOS 3.3 | -0.08 | -0.12 | -0.16 | ns |
| LVCMOS25 | LVCMOS 2.5 | 0.00 | 0.00 | 0.00 | ns |
| LVCMOS18 | LVCMOS 1.8 | -0.16 | -0.17 | -0.17 | ns |
| LVCMOS15 | LVCMOS 1.5 | -0.14 | -0.14 | -0.14 | ns |
| LVCMOS12 | LVCMOS 1.2 | -0.04 | -0.01 | 0.01 | ns |
| PCI33 | PCI | -0.08 | -0.12 | -0.16 | ns |
| **Output Adjusters** | | | | | |
| LVDS25E | LVDS 2.5 E[4] | 0.25 | 0.19 | 0.13 | ns |
| LVDS25 | LVDS 2.5 | 0.10 | 0.13 | 0.17 | ns |
| BLVDS25 | BLVDS 2.5 | 0.00 | -0.01 | -0.03 | ns |
| MLVDS | MLVDS 2.5[4] | 0.00 | -0.01 | -0.03 | ns |
| RSDS | RSDS 2.5[4] | 0.25 | 0.19 | 0.13 | ns |
| LVPECL33 | LVPECL 3.3[4] | -0.02 | -0.04 | -0.06 | ns |
| HSTL18_I | HSTL_18 class I 8mA drive | -0.19 | -0.22 | -0.25 | ns |
| HSTL18_II | HSTL_18 class II | -0.30 | -0.34 | -0.37 | ns |
| HSTL18D_I | Differential HSTL 18 class I 8mA drive | -0.19 | -0.22 | -0.25 | ns |
| HSTL18D_II | Differential HSTL 18 class II | -0.30 | -0.34 | -0.37 | ns |

## SERDES External Reference Clock (LatticeECP2M Family Only)

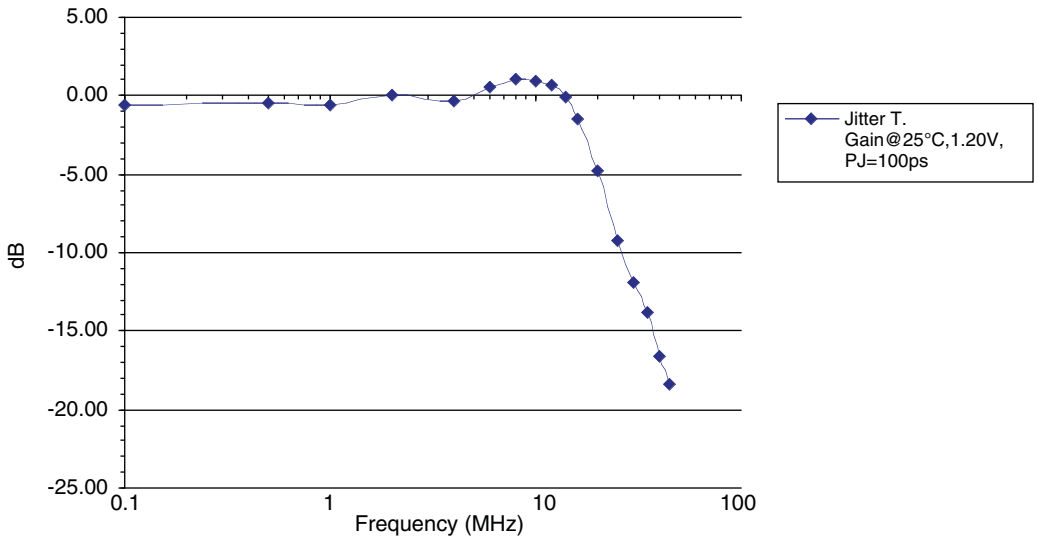
The external reference clock selection and its interface are a critical part of system applications for this product. Table 3-14 specifies reference clock requirements, over the full range of operating conditions.

***Table 3-14. External Reference Clock Specification (refclkp/refclkn)***

| Symbol | Description | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| $F_{REF}$ | Frequency range | 25 | — | 320 | MHz |
| $F_{REF-PPM}$ | Frequency tolerance | -300 | — | 300 | ppm |
| $V_{REF-IN-SE}$ | Input swing, single-ended clock[1] | 100 | — | 1200 | mV, p-p |
| $V_{REF-IN}$ | Input levels | 0 | — | $V_{CCP}$ + 0.8 | V |
| $V_{REF-CM-DC}$ | Input common mode range (DC coupled) | 0.5 | — | 1.2 | V |
| $V_{REF-CM-AC}$ | Input common mode range (AC coupled)[2] | 0 | — | 1.5 | V |
| $D_{REF}$ | Duty cycle[3] | 40 | — | 60 | % |
| $T_{REF-R}$ | Rise time (20% to 80%) | | 500 | 1000 | ps |
| $T_{REF-F}$ | Fall time (80% to 20%) | | 500 | 1000 | ps |
| $Z_{REF-IN-TERM}$ | Input termination | | 50/2K | | Ohms |
| $C_{REF-IN-CAP}$ | Input capacitance[4] | — | — | 1.5 | pF |

1. The signal swing for a single-ended input clock must be as large as the p-p differential swing of a differential input clock to get the same gain at the input receiver. Lower swings for the clock may be possible, but will tend to increase jitter.
2. When AC coupled, the input common mode range is determined by:
(Min input level) + (Peak-to-peak input swing)/2 ≤ (Input common mode voltage) ≤ (Max input level) - (Peak-to-peak input swing)/2
3. Measured at 50% amplitude.
4. Input capacitance of 1.5pF is total capacitance, including both device and package.

***Figure 3-13. Jitter Transfer***




Note: This graph is for a nominal device.

# SERDES Power-Down/Power-Up Specification

***Table 3-15. Power-Down and Power-Up Specification***

| Symbol | Description | Max. | Units |
|---|---|---|---|
| $t_{PWRDN}$ | Power-down time after all power down register bits set to '0' | 10 | µs |
| $t_{PWRUP}$ | Power-up time after all power down register bits set to '1' | 100 | µs |

# PCI Express Electrical and Timing Characteristics

## AC and DC Characteristics

***Table 3-16. Transmit[1, 2]***

| Symbol | Description | Test Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| UI | Unit interval | | 399.88 | 400 | 400.12 | ps |
| $V_{TX-DIFF\_P-P}$ | Differential peak-to-peak output voltage | | 0.8 | 1.0 | 1.2 | V |
| $V_{TX-DE-RATIO}$ | De-emphasis differential output voltage ratio | | 0 | -3.5 | -7.96 | dB |
| $V_{TX-CM-AC\_P}$ | RMS AC peak common-mode output voltage | | — | 20 | — | mV |
| $V_{TX-CM-DC-LINE-DELTA}$ | Maximum Common mode voltage delta between n and p channels | | — | — | 25 | mV |
| $V_{TX-DC-CM}$ | Tx DC common mode voltage | | 0 | — | $V_{CCOB}$ + 5% | V |
| $I_{TX-SHORT}$ | Output short circuit current | $V_{TX-D+}$=0.0V $V_{TX-D-}$=0.0V | — | — | 90 | mA |
| $Z_{TX-DIFF-DC}$ | Differential output impedance | | 80 | 100 | 120 | Ohms |
| $T_{TX-RISE}$ | Tx output rise time | 20 to 80% | 0.125 | — | — | UI |
| $T_{TX-FALL}$ | Tx output fall time | 20 to 80% | 0.125 | — | — | UI |
| $L_{TX-SKEW}$ | Lane-to-lane static output skew for all lanes in port/link | | — | — | 1.3 | ns |
| $T_{TX-EYE}$ | Transmitter eye width | | 0.75 | — | — | UI |
| $T_{TX-EYE-MEDIAN-TO-MAX-JITTER}$[3] | | | — | — | 0.125 | UI |
| $C_{TX}$ | AC coupling capacitor | | 75 | — | 200 | nF |

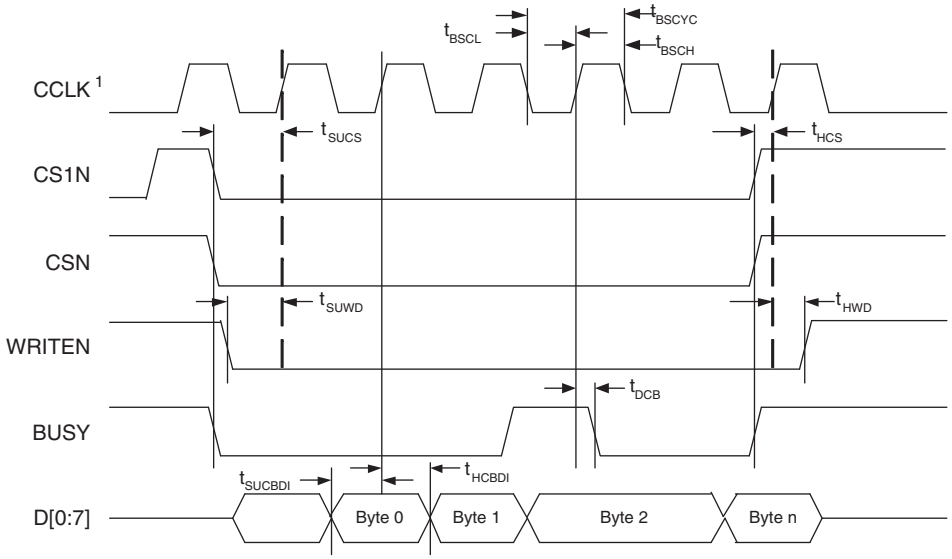
1. Values are measured at 2.5 Gbps.
2. Compliant to PCI Express v1.1.
3. Measured at 60ps with plug-in board and jitter due to socket removed.

***Table 3-17. Receive***

| Symbol | Description | Test Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| UI | Unit Interval | | 399.88 | 400 | 400.12 | ps |
| $V_{RX-DIFF\_P-P}$ | Differential peak-to-peak input voltage | | 0.175 | — | — | V |
| $V_{RX-IDLE-DET-DIFF\_P-P}$ | Idle detect threshold voltage | | 65 | — | 175 | mV |
| $Z_{RX-DIFF-DC}$ | DC differential input impedance | | 80 | 100 | 120 | Ohms |
| $Z_{RX-DC}$ | DC input impedance | | 40 | 50 | 60 | Ohms |
| $Z_{RX-HIGH-IMP-DC}$[1] | Power-down DC input impedance | | 200K | — | — | Ohms |
| $T_{RX-EYE}$ | Receiver eye width | | 0.4 | — | — | UI |
| $T_{RX-EYE-MEDIAN-TO-MAX-JITTER}$ | | | — | — | 0.3 | UI |

Notes:
1. Measured with external AC-coupling on the receiver
2. Values are measured at 2.5 Gbps

*Figure 3-15. sysCONFIG Parallel Port Write Cycle*




1. In Master Parallel Mode the FPGA provides CCLK. In Slave Parallel Mode the external device provides CCLK.

*Figure 3-16. sysCONFIG Slave Serial Port Timing*

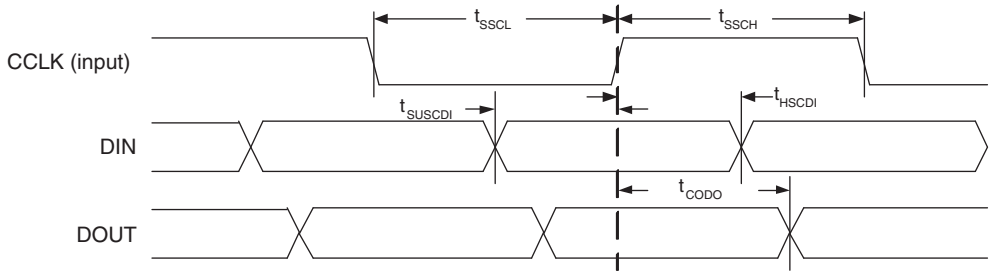
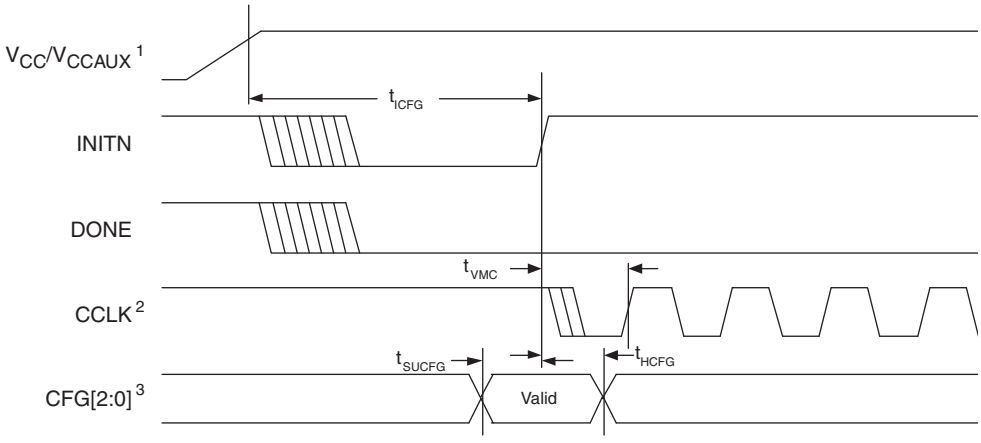



*Figure 3-17. Power-On-Reset (POR) Timing*




1. Time taken from $V_{CC}$ or $V_{CCAUX}$, whichever is the last to reach its $V_{MIN}$.
2. Device is in a Master Mode.
3. The CFG pins are normally static (hard wired).

# LFE2-12E/SE and LFE2-20E/SE Logic Signal Connections: 208 PQFP (Cont.)

| LFE2-12E/SE | | | | | LFE2-20E/SE | | | |
|---|---|---|---|---|---|---|---|---|
| Pin Number | Pin/Pad Function | Bank | Dual Function | Differential | Pin/Pad Function | Bank | Dual Function | Differential |
| 138 | PR15A | 3 | PCLKT3_0 | T (LVDS)* | PR21A | 3 | PCLKT3_0/RDQ25 | T (LVDS)* |
| 139 | GND | - | | | GND | - | | |
| 140 | VCC | - | | | VCC | - | | |
| 141 | PR13B | 2 | PCLKC2_0/RDQ10 | C | PR19B | 2 | PCLKC2_0/RDQ16 | C |
| 142 | PR13A | 2 | PCLKT2_0/RDQ10 | T | PR19A | 2 | PCLKT2_0/RDQ16 | T |
| 143 | VCCIO2 | 2 | | | VCCIO2 | 2 | | |
| 144 | PR12A | 2 | RDQ10 | | PR16A | 2 | RDQS16 | |
| 145 | GND | - | | | GND | - | | |
| 146 | VCC | - | | | VCC | - | | |
| 147 | PR8B | 2 | RDQ10 | C (LVDS)* | PR14B | 2 | RDQ16 | C (LVDS)* |
| 148 | VCCIO2 | 2 | | | VCCIO2 | 2 | | |
| 149 | PR8A | 2 | RDQ10 | T (LVDS)* | PR14A | 2 | RDQ16 | T (LVDS)* |
| 150 | PR6B | 2 | RDQ10 | C (LVDS)* | PR12B | 2 | RDQ16 | C (LVDS)* |
| 151 | VCCAUX | - | | | VCCAUX | - | | |
| 152 | PR6A | 2 | RDQ10 | T (LVDS)* | PR12A | 2 | RDQ16 | T (LVDS)* |
| 153 | PR4B | 2 | | C (LVDS)* | PR6B | 2 | RDQ8 | C (LVDS)* |
| 154 | PR4A | 2 | | T (LVDS)* | PR6A | 2 | RDQ8 | T (LVDS)* |
| 155 | PR2B | 2 | VREF2_2 | C (LVDS)* | PR2B | 2 | VREF2_2 | C (LVDS)* |
| 156 | PR2A | 2 | VREF1_2 | T (LVDS)* | PR2A | 2 | VREF1_2 | T (LVDS)* |
| 157 | PT55B | 1 | VREF2_1 | C | PT64B | 1 | VREF2_1 | C |
| 158 | PT55A | 1 | VREF1_1 | T | PT64A | 1 | VREF1_1 | T |
| 159 | GND | - | | | GND | - | | |
| 160 | PT54B | 1 | | C | PT62B | 1 | | C |
| 161 | PT54A | 1 | | T | PT62A | 1 | | T |
| 162 | VCCIO1 | 1 | | | VCCIO1 | 1 | | |
| 163 | PT52B | 1 | | C | PT60B | 1 | | C |
| 164 | PT52A | 1 | | T | PT60A | 1 | | T |
| 165 | PT50B | 1 | | C | PT58B | 1 | | C |
| 166 | PT50A | 1 | | T | PT58A | 1 | | T |
| 167 | PT48B | 1 | | C | PT56B | 1 | | C |
| 168 | PT48A | 1 | | T | PT56A | 1 | | T |
| 169 | GND | - | | | GND | - | | |
| 170 | VCCIO1 | 1 | | | VCCIO1 | 1 | | |
| 171 | VCC | - | | | VCC | - | | |
| 172 | PT40B | 1 | | C | PT50B | 1 | | C |
| 173 | PT40A | 1 | | T | PT50A | 1 | | T |
| 174 | VCCAUX | - | | | VCCAUX | - | | |
| 175 | GND | - | | | GND | - | | |
| 176 | PT36B | 1 | | C | PT44B | 1 | | C |
| 177 | PT36A | 1 | | T | PT44A | 1 | | T |
| 178 | PT34B | 1 | | C | PT42B | 1 | | C |
| 179 | PT34A | 1 | | T | PT42A | 1 | | T |
| 180 | PT30B | 1 | PCLKC1_0 | C | PT39B | 1 | PCLKC1_0 | C |
| 181 | PT30A | 1 | PCLKT1_0 | T | PT39A | 1 | PCLKT1_0 | T |
| 182 | XRES | 1 | | | XRES | 1 | | |
| 183 | PT28B | 0 | PCLKC0_0 | C | PT37B | 0 | PCLKC0_0 | C |

# LFE2-6E/SE and LFE2-12E/SE Logic Signal Connections: 256 fpBGA (Cont.)

| LFE2-6E/SE | | | | | LFE2-12E/SE | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| GND | GNDIO6 | - | | | GNDIO6 | - | | |
| L2 | PL24A | 6 | LDQ28 | T (LVDS)* | PL24A | 6 | LDQ28 | T (LVDS)* |
| K2 | PL25A | 6 | LDQ28 | T | PL25A | 6 | LDQ28 | T |
| L3 | PL24B | 6 | LDQ28 | C (LVDS)* | PL24B | 6 | LDQ28 | C (LVDS)* |
| K1 | PL25B | 6 | LDQ28 | C | PL25B | 6 | LDQ28 | C |
| VCCIO | VCCIO6 | 6 | | | VCCIO6 | 6 | | |
| L4 | PL26A | 6 | LDQ28 | T (LVDS)* | PL26A | 6 | LDQ28 | T (LVDS)* |
| L1 | PL27A | 6 | LDQ28 | T | PL27A | 6 | LDQ28 | T |
| L5 | PL26B | 6 | LDQ28 | C (LVDS)* | PL26B | 6 | LDQ28 | C (LVDS)* |
| M1 | PL27B | 6 | LDQ28 | C | PL27B | 6 | LDQ28 | C |
| GND | GNDIO6 | - | | | GNDIO6 | - | | |
| N1 | PL29A | 6 | LDQ28 | T | PL29A | 6 | LDQ28 | T |
| N2 | PL28A | 6 | LDQS28 | T (LVDS)* | PL28A | 6 | LDQS28 | T (LVDS)* |
| P1 | PL29B | 6 | LDQ28 | C | PL29B | 6 | LDQ28 | C |
| VCCIO | VCCIO6 | 6 | | | VCCIO6 | 6 | | |
| P2 | PL28B | 6 | LDQ28 | C (LVDS)* | PL28B | 6 | LDQ28 | C (LVDS)* |
| R1 | PL30A | 6 | LDQ28 | T (LVDS)* | PL30A | 6 | LDQ28 | T (LVDS)* |
| GND | GNDIO6 | - | | | GNDIO6 | - | | |
| R2 | PL30B | 6 | LDQ28 | C (LVDS)* | PL30B | 6 | LDQ28 | C (LVDS)* |
| N4 | TDI | - | | | TDI | - | | |
| M4 | TCK | - | | | TCK | - | | |
| P3 | TDO | - | | | TDO | - | | |
| N3 | TMS | - | | | TMS | - | | |
| K7 | VCCJ | - | | | VCCJ | - | | |
| M5 | PB2A | 5 | VREF2_5/BDQ6 | T | PB2A | 5 | VREF2_5/BDQ6 | T |
| K6 | NC | - | | | PB3A | 5 | BDQ6 | |
| M6 | PB2B | 5 | VREF1_5/BDQ6 | C | PB2B | 5 | VREF1_5/BDQ6 | C |
| R3 | NC | - | | | PB5A | 5 | BDQ6 | T |
| P4 | NC | - | | | PB5B | 5 | BDQ6 | C |
| - | - | - | | | VCCIO | 5 | | |
| - | - | - | | | GNDIO5 | 5 | | |
| N5 | PB3A | 5 | BDQ6 | T | PB21A | 5 | BDQ24 | T |
| N6 | PB3B | 5 | BDQ6 | C | PB21B | 5 | BDQ24 | C |
| T2 | PB4A | 5 | BDQ6 | T | PB22A | 5 | BDQ24 | T |
| P6 | PB5A | 5 | BDQ6 | T | PB23A | 5 | BDQ24 | T |
| VCCIO | VCCIO5 | 5 | | | VCCIO5 | 5 | | |
| T3 | PB4B | 5 | BDQ6 | C | PB22B | 5 | BDQ24 | C |
| R6 | PB5B | 5 | BDQ6 | C | PB23B | 5 | BDQ24 | C |
| GND | GNDIO5 | - | | | GNDIO5 | - | | |
| R4 | PB6A | 5 | BDQS6 | T | PB24A | 5 | BDQS24 | T |
| L6 | PB7A | 5 | BDQ6 | T | PB25A | 5 | BDQ24 | T |
| T4 | PB6B | 5 | BDQ6 | C | PB24B | 5 | BDQ24 | C |
| L7 | PB7B | 5 | BDQ6 | C | PB25B | 5 | BDQ24 | C |
| N7 | PB8A | 5 | PCLKT5_0/BDQ6 | T | PB26A | 5 | PCLKT5_0/BDQ24 | T |
| VCCIO | VCCIO5 | 5 | | | VCCIO5 | 5 | | |

# LFE2-20E/SE and LFE2-35E/SE Logic Signal Connections: 672 fpBGA (Cont.)

| LFE2-20E/20SE | | | | | LFE2-35E/35SE | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| G24 | PR6B | 2 | RDQ8 | C (LVDS)* | PR12B | 2 | RDQ14 | C (LVDS)* |
| G23 | PR6A | 2 | RDQ8 | T (LVDS)* | PR12A | 2 | RDQ14 | T (LVDS)* |
| VCCIO | VCCIO2 | 2 | | | VCCIO2 | 2 | | |
| K19 | PR5B | 2 | RDQ8 | C | PR11B | 2 | RDQ14 | C |
| J19 | PR5A | 2 | RDQ8 | T | PR11A | 2 | RDQ14 | T |
| D26 | PR4B | 2 | RDQ8 | C (LVDS)* | PR10B | 2 | RDQ14 | C (LVDS)* |
| C26 | PR4A | 2 | RDQ8 | T (LVDS)* | PR10A | 2 | RDQ14 | T (LVDS)* |
| F22 | NC | - | | | PR9B | 2 | RDQ6 | C |
| E24 | NC | - | | | PR9A | 2 | RDQ6 | T |
| GND | GNDIO2 | - | | | GNDIO2 | - | | |
| D25 | NC | - | | | PR8B | 2 | RDQ6 | C (LVDS)* |
| C25 | NC | - | | | PR8A | 2 | RDQ6 | T (LVDS)* |
| D24 | NC | - | | | PR7B | 2 | RDQ6 | C |
| B25 | NC | - | | | PR7A | 2 | RDQ6 | T |
| VCCIO | VCCIO2 | 2 | | | VCCIO2 | 2 | | |
| H21 | NC | - | | | PR6B | 2 | RDQ6 | C (LVDS)* |
| G22 | NC | - | | | PR6A | 2 | RDQS6 | T (LVDS)* |
| B24 | NC | - | | | PR5B | 2 | RDQ6 | C |
| GND | GNDIO2 | - | | | GNDIO2 | - | | |
| C24 | NC | - | | | PR5A | 2 | RDQ6 | T |
| D23 | NC | - | | | PR4B | 2 | RDQ6 | C (LVDS)* |
| C23 | NC | - | | | PR4A | 2 | RDQ6 | T (LVDS)* |
| G21 | PR3B | 2 | | C | PR3B | 2 | RDQ6 | C |
| VCCIO | VCCIO2 | 2 | | | VCCIO2 | 2 | | |
| H20 | PR3A | 2 | | T | PR3A | 2 | RDQ6 | T |
| GND | GNDIO2 | - | | | GNDIO2 | - | | |
| E22 | PR2B | 2 | VREF2_2 | C (LVDS)* | PR2B | 2 | VREF2_2/RDQ6 | C (LVDS)* |
| F21 | PR2A | 2 | VREF1_2 | T (LVDS)* | PR2A | 2 | VREF1_2/RDQ6 | T (LVDS)* |
| E23 | PT64B | 1 | VREF2_1 | C | PT73B | 1 | VREF2_1 | C |
| GND | GNDIO1 | - | | | GNDIO1 | - | | |
| D22 | PT64A | 1 | VREF1_1 | T | PT73A | 1 | VREF1_1 | T |
| G20 | PT63B | 1 | | C | PT72B | 1 | | C |
| J18 | PT63A | 1 | | T | PT72A | 1 | | T |
| F20 | PT62B | 1 | | C | PT71B | 1 | | C |
| VCCIO | VCCIO1 | 1 | | | VCCIO1 | 1 | | |
| H19 | PT62A | 1 | | T | PT71A | 1 | | T |
| A24 | PT61B | 1 | | C | PT70B | 1 | | C |
| A23 | PT61A | 1 | | T | PT70A | 1 | | T |
| E21 | PT60B | 1 | | C | PT69B | 1 | | C |
| F19 | PT60A | 1 | | T | PT69A | 1 | | T |
| C22 | PT59B | 1 | | C | PT68B | 1 | | C |
| GND | GNDIO1 | - | | | GNDIO1 | - | | |
| E20 | PT59A | 1 | | T | PT68A | 1 | | T |
| B22 | PT58B | 1 | | C | PT67B | 1 | | C |
| VCCIO | VCCIO1 | 1 | | | VCCIO1 | 1 | | |
| B23 | PT58A | 1 | | T | PT67A | 1 | | T |

## LFE2-70E/SE Logic Signal Connections: 900 fpBGA (Cont.)

| LFE2-70E/SE | | | | |
|---|---|---|---|---|
| **Ball Number** | **Ball/Pad Function** | **Bank** | **Dual Function** | **Differential** |
| P3 | PL54B | 7 | LDQ54 | C (LVDS)* |
| R6 | PL55A | 7 | LDQ54 | T |
| VCCIO | VCCIO7 | 7 | | |
| R8 | PL55B | 7 | LDQ54 | C |
| P2 | PL56A | 7 | LDQ54 | T (LVDS)* |
| P1 | PL56B | 7 | LDQ54 | C (LVDS)* |
| R5 | PL57A | 7 | PCLKT7_0/LDQ54 | T |
| GND | GNDIO7 | - | | |
| R7 | PL57B | 7 | PCLKC7_0/LDQ54 | C |
| R4 | PL59A | 6 | PCLKT6_0/LDQ63 | T (LVDS)* |
| R3 | PL59B | 6 | PCLKC6_0/LDQ63 | C (LVDS)* |
| T5 | PL60A | 6 | VREF2_6/LDQ63 | T |
| T7 | PL60B | 6 | VREF1_6/LDQ63 | C |
| T3 | PL61A | 6 | LDQ63 | T (LVDS)* |
| VCCIO | VCCIO6 | 6 | | |
| T4 | PL61B | 6 | LDQ63 | C (LVDS)* |
| T6 | PL62A | 6 | LDQ63 | T |
| T8 | PL62B | 6 | LDQ63 | C |
| T2 | PL63A | 6 | LDQS63 | T (LVDS)* |
| GND | GNDIO6 | - | | |
| T1 | PL63B | 6 | LDQ63 | C (LVDS)* |
| U7 | PL64A | 6 | LDQ63 | T |
| U5 | PL64B | 6 | LDQ63 | C |
| VCCIO | VCCIO6 | 6 | | |
| U4 | PL65A | 6 | LDQ63 | T (LVDS)* |
| U3 | PL65B | 6 | LDQ63 | C (LVDS)* |
| U8 | PL66A | 6 | LDQ63 | T |
| U6 | PL66B | 6 | LDQ63 | C |
| GND | GNDIO6 | - | | |
| U2 | PL67A | 6 | LDQ71 | T (LVDS)* |
| U1 | PL67B | 6 | LDQ71 | C (LVDS)* |
| V7 | PL68A | 6 | LDQ71 | T |
| V5 | PL68B | 6 | LDQ71 | C |
| VCCIO | VCCIO6 | 6 | | |
| V2 | PL69A | 6 | LDQ71 | T (LVDS)* |
| V1 | PL69B | 6 | LDQ71 | C (LVDS)* |
| V8 | PL70A | 6 | LDQ71 | T |
| V6 | PL70B | 6 | LDQ71 | C |
| GND | GNDIO6 | - | | |
| W1 | PL71A | 6 | LDQS71 | T (LVDS)* |
| W2 | PL71B | 6 | LDQ71 | C (LVDS)* |
| W5 | PL72A | 6 | LDQ71 | T |
| VCCIO | VCCIO6 | 6 | | |

## LFE2-70E/SE Logic Signal Connections: 900 fpBGA (Cont.)

| LFE2-70E/SE | | | | |
|---|---|---|---|---|
| **Ball Number** | **Ball/Pad Function** | **Bank** | **Dual Function** | **Differential** |
| AB24 | PR87B | 8 | D3 | C |
| GND | GNDIO4 | - | | |
| AB23 | PR87A | 8 | D4 | T |
| AB25 | PR86B | 8 | D5 | C |
| AB26 | PR86A | 8 | D6 | T |
| AC27 | PR85B | 8 | D7/SPID0 | C |
| VCCIO | VCCIO8 | 8 | | |
| AB27 | PR85A | 8 | DI/CSSPI0N | T |
| AD29 | PR84B | 8 | DOUT/CSON | C |
| AD30 | PR84A | 8 | BUSY/SISPI | T |
| AA25 | PR83B | 3 | RDQ80 | C |
| GND | GNDIO3 | - | | |
| AA23 | PR83A | 3 | RDQ80 | T |
| AC29 | PR82B | 3 | RDQ80 | C (LVDS)* |
| AC30 | PR82A | 3 | RDQ80 | T (LVDS)* |
| AA26 | PR81B | 3 | RDQ80 | C |
| VCCIO | VCCIO3 | 3 | | |
| AA24 | PR81A | 3 | RDQ80 | T |
| AB29 | PR80B | 3 | RDQ80 | C (LVDS)* |
| AB30 | PR80A | 3 | RDQS80 | T (LVDS)* |
| GND | GNDIO3 | - | | |
| Y23 | PR79B | 3 | RDQ80 | C |
| Y25 | PR79A | 3 | RDQ80 | T |
| AA27 | PR78B | 3 | RDQ80 | C (LVDS)* |
| AA28 | PR78A | 3 | RDQ80 | T (LVDS)* |
| VCCIO | VCCIO3 | 3 | | |
| Y24 | PR77B | 3 | RLM0_GPLLC_FB_A/RDQ80 | C |
| Y26 | PR77A | 3 | RLM0_GPLLT_FB_A/RDQ80 | T |
| AA29 | PR76B | 3 | RLM0_GPLLC_IN_A**/RDQ80 | C (LVDS)* |
| AA30 | PR76A | 3 | RLM0_GPLLT_IN_A**/RDQ80 | T (LVDS)* |
| R22 | RLM0_PLLCAP | 3 | | |
| W23 | PR74B | 3 | RLM0_GDLLC_FB_A/RDQ71 | C |
| W25 | PR74A | 3 | RLM0_GDLLT_FB_A/RDQ71 | T |
| GND | GNDIO3 | - | | |
| Y27 | PR73B | 3 | RLM0_GDLLC_IN_A**/RDQ71 | C (LVDS)* |
| Y28 | PR73A | 3 | RLM0_GDLLT_IN_A**/RDQ71 | T (LVDS)* |
| W24 | PR72B | 3 | RDQ71 | C |
| W26 | PR72A | 3 | RDQ71 | T |
| VCCIO | VCCIO3 | 3 | | |
| Y29 | PR71B | 3 | RDQ71 | C (LVDS)* |
| Y30 | PR71A | 3 | RDQS71 | T (LVDS)* |
| V25 | PR70B | 3 | RDQ71 | C |
| GND | GNDIO3 | - | | |

## LFE2M50E/SE Logic Signal Connections: 484 fpBGA (Cont.)

| LFE2M50E/SE | | | | |
|---|---|---|---|---|
| **Ball Number** | **Ball/Pad Function** | **Bank** | **Dual Function** | **Differential** |
| F20 | PR30A | 2 | RDQ27 | T |
| GNDIO | GNDIO2 | - | | |
| G17 | PR29B | 2 | RDQ27 | C (LVDS)* |
| F17 | PR29A | 2 | RDQ27 | T (LVDS)* |
| VCCIO | VCCIO2 | 2 | | |
| GNDIO | GNDIO2 | - | | |
| E22 | PR14B | 2 | | C |
| D22 | PR14A | 2 | | T |
| VCCIO | VCCIO2 | - | | |
| E20 | PR13B | 2 | | C (LVDS)* |
| D20 | PR13A | 2 | | T (LVDS)* |
| D19 | PR12B | 2 | RUM0_SPLLC_FB_A | C |
| GNDIO | GNDIO2 | - | | |
| E19 | PR12A | 2 | RUM0_SPLLT_FB_A | T |
| F18 | PR11B | 2 | RUM0_SPLLC_IN_A | C (LVDS)* |
| F19 | PR11A | 2 | RUM0_SPLLT_IN_A | T (LVDS)* |
| VCCIO | VCCIO2 | - | | |
| E18 | PR9B | 2 | VREF2_2 | C |
| GNDIO | GNDIO2 | - | | |
| D18 | PR9A | 2 | VREF1_2 | T |
| VCCIO | VCCIO2 | 2 | | |
| F16 | XRES | - | | |
| C22 | URC_SQ_VCCRX0 | 12 | | |
| A21 | URC_SQ_HDINP0 | 12 | | T |
| B22 | URC_SQ_VCCIB0 | 12 | | |
| B21 | URC_SQ_HDINN0 | 12 | | C |
| C19 | URC_SQ_VCCTX0 | 12 | | |
| A18 | URC_SQ_HDOUTP0 | 12 | | T |
| A19 | URC_SQ_VCCOB0 | 12 | | |
| B18 | URC_SQ_HDOUTN0 | 12 | | C |
| C18 | URC_SQ_VCCTX1 | 12 | | |
| B17 | URC_SQ_HDOUTN1 | 12 | | C |
| C17 | URC_SQ_VCCOB1 | 12 | | |
| A17 | URC_SQ_HDOUTP1 | 12 | | T |
| C21 | URC_SQ_VCCRX1 | 12 | | |
| B20 | URC_SQ_HDINN1 | 12 | | C |
| C20 | URC_SQ_VCCIB1 | 12 | | |
| A20 | URC_SQ_HDINP1 | 12 | | T |
| B16 | URC_SQ_VCCAUX33 | 12 | | |
| E17 | URC_SQ_REFCLKN | 12 | | C |
| D17 | URC_SQ_REFCLKP | 12 | | T |
| C16 | URC_SQ_VCCP | 12 | | |
| A12 | URC_SQ_HDINP2 | 12 | | T |

# LFE2M50E/SE and LFE2M70E/SE Logic Signal Connections: 900 fpBGA (Cont.)

| LFE2M50E/SE | | | | | LFE2M70E/SE | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| M26 | PR27A | 2 | RDQS27 | T (LVDS)* | PR37A | 2 | RDQS37 | T (LVDS)* |
| L30 | PR26B | 2 | RDQ27 | C | PR36B | 2 | RDQ37 | C |
| GNDIO | GNDIO2 | - | | | GNDIO2 | - | | |
| L29 | PR26A | 2 | RDQ27 | T | PR36A | 2 | RDQ37 | T |
| L28 | PR25B | 2 | RDQ27 | C (LVDS)* | PR35B | 2 | RDQ37 | C (LVDS)* |
| L27 | PR25A | 2 | RDQ27 | T (LVDS)* | PR35A | 2 | RDQ37 | T (LVDS)* |
| H29 | PR24B | 2 | RDQ27 | C | PR34B | 2 | RDQ37 | C |
| VCCIO | VCCIO2 | 2 | | | VCCIO2 | 2 | | |
| G29 | PR24A | 2 | RDQ27 | T | PR34A | 2 | RDQ37 | T |
| L22 | PR23B | 2 | RDQ27 | C (LVDS)* | PR33B | 2 | RDQ37 | C (LVDS)* |
| M22 | PR23A | 2 | RDQ27 | T (LVDS)* | PR33A | 2 | RDQ37 | T (LVDS)* |
| F30 | PR21B | 2 | | C | PR31B | 2 | RDQ28 | C |
| GNDIO | GNDIO2 | - | | | GNDIO2 | - | | |
| F29 | PR21A | 2 | | T | PR31A | 2 | RDQ28 | T |
| - | - | - | | | - | - | | |
| - | - | - | | | - | - | | |
| E30 | PR20B | 2 | | C (LVDS)* | PR30B | 2 | RDQ28 | C (LVDS)* |
| E29 | PR20A | 2 | | T (LVDS)* | PR30A | 2 | RDQ28 | T (LVDS)* |
| VCCIO | VCCIO2 | 2 | | | - | - | | |
| L25 | PR19B | 2 | | C | PR29B | 2 | RDQ28 | C |
| L26 | PR19A | 2 | | T | PR29A | 2 | RDQ28 | T |
| - | - | - | | | VCCIO2 | 2 | | |
| H28 | PR18B | 2 | | C (LVDS)* | PR28B | 2 | RDQ28 | C (LVDS)* |
| J28 | PR18A | 2 | | T (LVDS)* | PR28A | 2 | RDQS28 | T (LVDS)* |
| G28 | PR16B | 2 | | C | PR27B | 2 | RDQ28 | C |
| GNDIO | GNDIO2 | - | | | GNDIO2 | - | | |
| G27 | PR16A | 2 | | T | PR27A | 2 | RDQ28 | T |
| L24 | NC | - | | | PR26B | 2 | RDQ28 | C (LVDS)* |
| L23 | NC | - | | | PR26A | 2 | RDQ28 | T (LVDS)* |
| D30 | NC | - | | | PR25B | 2 | RDQ28 | C |
| - | - | - | | | VCCIO2 | 2 | | |
| D29 | NC | - | | | PR25A | 2 | RDQ28 | T |
| K24 | NC | - | | | PR24B | 2 | RDQ28 | C (LVDS)* |
| K25 | NC | - | | | PR24A | 2 | RDQ28 | T (LVDS)* |
| J27 | NC | - | | | PR22B | 2 | | C |
| - | - | - | | | GNDIO2 | - | | |
| K26 | NC | - | | | PR22A | 2 | | T |
| K23 | PR15B | 2 | | C (LVDS)* | PR21B | 2 | | C (LVDS)* |
| K22 | PR15A | 2 | | T (LVDS)* | PR21A | 2 | | T (LVDS)* |
| J22 | PR14B | 2 | | C | PR20B | 2 | | C |
| VCCIO | VCCIO2 | - | | | VCCIO2 | 2 | | |
| J23 | PR14A | 2 | | T | PR20A | 2 | | T |
| - | - | - | | | GNDIO2 | - | | |
| - | - | - | | | - | - | | |
| J26 | NC | - | | | PR17B | 2 | RDQ15 | C (LVDS)* |
| H26 | NC | - | | | PR17A | 2 | RDQ15 | T (LVDS)* |
| H27 | NC | - | | | PR16B | 2 | RDQ15 | C |
| G26 | NC | - | | | PR16A | 2 | RDQ15 | T |

# LFE2M50E/SE and LFE2M70E/SE Logic Signal Connections: 900 fpBGA (Cont.)

| LFE2M50E/SE | | | | | LFE2M70E/SE | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| A21 | URC_SQ_VCCOB3 | 12 | | | URC_SQ_VCCOB3 | 12 | | |
| A22 | URC_SQ_HDOUTP3 | 12 | | T | URC_SQ_HDOUTP3 | 12 | | T |
| C21 | URC_SQ_VCCTX3 | 12 | | | URC_SQ_VCCTX3 | 12 | | |
| B19 | URC_SQ_HDINN3 | 12 | | C | URC_SQ_HDINN3 | 12 | | C |
| B18 | URC_SQ_VCCIB3 | 12 | | | URC_SQ_VCCIB3 | 12 | | |
| A19 | URC_SQ_HDINP3 | 12 | | T | URC_SQ_HDINP3 | 12 | | T |
| C18 | URC_SQ_VCCRX3 | 12 | | | URC_SQ_VCCRX3 | 12 | | |
| D23 | PT73B | 1 | | C | PT82B | 1 | | C |
| GNDIO | GNDIO1 | - | | | GNDIO1 | - | | |
| E21 | PT73A | 1 | | T | PT82A | 1 | | T |
| D26 | PT72B | 1 | | C | PT81B | 1 | | C |
| E26 | PT72A | 1 | | T | PT81A | 1 | | T |
| E23 | PT71B | 1 | | C | PT80B | 1 | | C |
| - | - | - | | | VCCIO1 | 1 | | |
| G22 | PT71A | 1 | | T | PT80A | 1 | | T |
| VCCIO | VCCIO1 | 1 | | | - | - | | |
| D22 | PT70B | 1 | | C | PT79B | 1 | | C |
| F21 | PT70A | 1 | | T | PT79A | 1 | | T |
| G18 | PT69B | 1 | | C | PT78B | 1 | | C |
| H18 | PT69A | 1 | | T | PT78A | 1 | | T |
| D20 | PT68B | 1 | | C | PT77B | 1 | | C |
| GNDIO | GNDIO1 | - | | | GNDIO1 | - | | |
| D21 | PT68A | 1 | | T | PT77A | 1 | | T |
| E20 | PT67B | 1 | | C | PT76B | 1 | | C |
| E19 | PT67A | 1 | | T | PT76A | 1 | | T |
| D19 | PT66B | 1 | | C | PT75B | 1 | | C |
| VCCIO | VCCIO1 | 1 | | | VCCIO1 | 1 | | |
| E18 | PT66A | 1 | | T | PT75A | 1 | | T |
| D18 | PT65B | 1 | | C | PT74B | 1 | | C |
| C17 | PT65A | 1 | | T | PT74A | 1 | | T |
| A17 | PT64B | 1 | | C | PT73B | 1 | | C |
| B17 | PT64A | 1 | | T | PT73A | 1 | | T |
| GNDIO | GNDIO1 | - | | | GNDIO1 | - | | |
| VCCIO | VCCIO1 | 1 | | | VCCIO1 | 1 | | |
| J18 | NC | - | | | PT66B | 1 | | C |
| J19 | NC | - | | | PT66A | 1 | | T |
| H17 | NC | - | | | PT65B | 1 | | C |
| J17 | NC | - | | | PT65A | 1 | | T |
| F18 | NC | - | | | PT64B | 1 | | C |
| F17 | NC | - | | | PT64A | 1 | | T |
| - | - | - | | | GNDIO1 | - | | |
| A16 | PT54B | 1 | | C | PT63B | 1 | | C |
| B16 | PT54A | 1 | | T | PT63A | 1 | | T |
| G17 | PT53B | 1 | | C | PT62B | 1 | | C |
| G16 | PT53A | 1 | | T | PT62A | 1 | | T |
| VCCIO | VCCIO1 | 1 | | | VCCIO1 | 1 | | |
| H16 | PT52B | 1 | | C | PT61B | 1 | | C |
| F16 | PT52A | 1 | | T | PT61A | 1 | | T |

## LFE2M100E/SE Logic Signal Connections: 900 fpBGA (Cont.)

| LFE2M100E/SE | | | | |
|---|---|---|---|---|
| **Ball Number** | **Ball/Pad Function** | **Bank** | **Dual Function** | **Differential** |
| AA1 | PL81A | 6 | LDQS81 | T (LVDS)* |
| GNDIO | GNDIO6 | - | | |
| AA2 | PL81B | 6 | LDQ81 | C (LVDS)* |
| Y3 | PL82A | 6 | LDQ81 | T |
| AB1 | PL82B | 6 | LDQ81 | C |
| VCCIO | VCCIO6 | 6 | | |
| Y9 | PL83A | 6 | LDQ81 | T (LVDS)* |
| Y8 | PL83B | 6 | LDQ81 | C (LVDS)* |
| Y7 | PL84A | 6 | LDQ81 | T |
| AA7 | PL84B | 6 | LDQ81 | C |
| GNDIO | GNDIO6 | - | | |
| VCCIO | VCCIO6 | 6 | | |
| AB2 | PL95A | 6 | LDQ99 | T (LVDS)* |
| AB3 | PL95B | 6 | LDQ99 | C (LVDS)* |
| AA5 | PL96A | 6 | LDQ99 | T |
| AA6 | PL96B | 6 | LDQ99 | C |
| AB4 | PL97A | 6 | LDQ99 | T (LVDS)* |
| VCCIO | VCCIO6 | 6 | | |
| AB5 | PL97B | 6 | LDQ99 | C (LVDS)* |
| AA8 | PL98A | 6 | LDQ99 | T |
| AA9 | PL98B | 6 | LDQ99 | C |
| AC1 | PL99A | 6 | LLM0_GPLLT_IN_A**/LDQS99 | T (LVDS)* |
| GNDIO | GNDIO6 | - | | |
| AC2 | PL99B | 6 | LLM0_GPLLC_IN_A**/LDQ99 | C (LVDS)* |
| AC4 | PL100A | 6 | LLM0_GPLLT_FB_A/LDQ99 | T |
| AC3 | PL100B | 6 | LLM0_GPLLC_FB_A/LDQ99 | C |
| VCCIO | VCCIO6 | 6 | | |
| AC7 | PL101A | 6 | LLM0_GDLLT_IN_A**/LDQ99 | T (LVDS)* |
| AC6 | PL101B | 6 | LLM0_GDLLC_IN_A**/LDQ99 | C (LVDS)* |
| AC5 | PL102A | 6 | LLM0_GDLLT_FB_A/LDQ99 | T |
| AD3 | PL102B | 6 | LLM0_GDLLC_FB_A/LDQ99 | C |
| GNDIO | GNDIO6 | - | | |
| AB8 | LLM0_PLLCAP | 6 | | |
| AD2 | PL104A | 6 | | T |
| AD1 | PL104B | 6 | | C |
| AE2 | TCK | - | | |
| AE1 | TDI | - | | |
| AF2 | TMS | - | | |
| AF1 | TDO | - | | |
| AG1 | VCCJ | - | | |
| AH1 | LLC_SQ_VCCRX3 | 14 | | |
| AK2 | LLC_SQ_HDINP3 | 14 | | T |
| AJ1 | LLC_SQ_VCCIB3 | 14 | | |

## LFE2M100E/SE Logic Signal Connections: 900 fpBGA (Cont.)

| LFE2M100E/SE | | | | |
|---|---|---|---|---|
| **Ball Number** | **Ball/Pad Function** | **Bank** | **Dual Function** | **Differential** |
| AG2 | PB34A | 5 | BDQ33 | T |
| AG3 | PB34B | 5 | BDQ33 | C |
| AD13 | PB35A | 5 | BDQ33 | T |
| VCCIO | VCCIO5 | 5 | | |
| AC13 | PB35B | 5 | BDQ33 | C |
| AE14 | PB36A | 5 | BDQ33 | T |
| AC14 | PB36B | 5 | BDQ33 | C |
| AF3 | PB37A | 5 | BDQ33 | T |
| GNDIO | GNDIO5 | - | | |
| AF4 | PB37B | 5 | BDQ33 | C |
| - | - | - | | |
| AG4 | PB38A | 5 | BDQ42 | T |
| AG5 | PB38B | 5 | BDQ42 | C |
| GNDIO | GNDIO5 | - | | |
| - | - | - | | |
| AD11 | PB48A | 5 | BDQ51 | T |
| AF13 | PB48B | 5 | BDQ51 | C |
| AF12 | PB49A | 5 | BDQ51 | T |
| VCCIO | VCCIO5 | 5 | | |
| AD14 | PB49B | 5 | BDQ51 | C |
| AG8 | PB50A | 5 | BDQ51 | T |
| AF8 | PB50B | 5 | BDQ51 | C |
| AE15 | PB51A | 5 | BDQS51**** | T |
| GNDIO | GNDIO5 | - | | |
| - | - | - | | |
| AC15 | PB51B | 5 | BDQ51 | C |
| VCCIO | VCCIO5 | 5 | | |
| GNDIO | GNDIO5 | - | | |
| AD15 | PB56A | 5 | BDQ60 | T |
| AF15 | PB56B | 5 | BDQ60 | C |
| AG10 | PB57A | 5 | BDQ60 | T |
| AG9 | PB57B | 5 | BDQ60 | C |
| AH14 | PB58A | 5 | BDQ60 | T |
| AG12 | PB58B | 5 | BDQ60 | C |
| VCCIO | VCCIO5 | 5 | | |
| AG15 | PB59A | 5 | BDQ60 | T |
| AG13 | PB59B | 5 | BDQ60 | C |
| GNDIO | GNDIO5 | - | | |
| AF16 | PB60A | 5 | BDQS60 | T |
| AH15 | PB60B | 5 | BDQ60 | C |
| AC16 | PB61A | 5 | VREF2_5/BDQ60 | T |
| AE16 | PB61B | 5 | VREF1_5/BDQ60 | C |
| AG11 | PB62A | 5 | PCLKT5_0/BDQ60 | T |

# LFE2M70E/SE and LFE2M100E/SE Logic Signal Connections: 1152 fpBGA (Cont.)

| LFE2M70E/SE | | | | LFE2M100E/SE | | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| K11 | NC | - | | | NC | - | | |
| K12 | NC | - | | | NC | - | | |
| K13 | NC | - | | | NC | - | | |
| K23 | NC | - | | | NC | - | | |
| K24 | NC | - | | | NC | - | | |
| K25 | NC | - | | | NC | - | | |
| K26 | NC | - | | | NC | - | | |
| L11 | NC | - | | | NC | - | | |
| L12 | NC | - | | | NC | - | | |
| L13 | NC | - | | | NC | - | | |
| L14 | NC | - | | | NC | - | | |
| L21 | NC | - | | | NC | - | | |
| L22 | NC | - | | | NC | - | | |
| L23 | NC | - | | | NC | - | | |
| L24 | NC | - | | | NC | - | | |
| L25 | NC | - | | | NC | - | | |
| L26 | NC | - | | | NC | - | | |
| M11 | NC | - | | | NC | - | | |
| M24 | NC | - | | | NC | - | | |
| M25 | NC | - | | | NC | - | | |
| M6 | NC | - | | | NC | - | | |
| M8 | NC | - | | | NC | - | | |
| N10 | NC | - | | | NC | - | | |
| N11 | NC | - | | | NC | - | | |
| P10 | NC | - | | | NC | - | | |
| P25 | NC | - | | | NC | - | | |
| P26 | NC | - | | | NC | - | | |
| R9 | NC | - | | | NC | - | | |
| T11 | NC | - | | | NC | - | | |
| U11 | NC | - | | | NC | - | | |
| W11 | NC | - | | | NC | - | | |
| Y10 | NC | - | | | NC | - | | |
| Y11 | NC | - | | | NC | - | | |
| R15 | VCCPLL | - | | | VCCPLL | - | | |
| R20 | VCCPLL | - | | | VCCPLL | - | | |
| Y15 | VCCPLL | - | | | VCCPLL | - | | |
| Y20 | VCCPLL | - | | | VCCPLL | - | | |

* Supports true LVDS. Other differential signals must be emulated with external resistors.

** These dedicated input pins can be used for GPLLs or GDLLs within the respective quadrant.

*** For density migration, board design must take into account that these sysCONFIG pins are dual function for the lower density devices (ECP2M20 and ECP2M35). They can be either sysCONFIG pins or general purpose I/Os. These pins are dedicated pins for the higher density devices (ECP2M50, ECP2M70, and ECP2M100).

****Due to packaging bond out option, this DQS does not have all the necessary DQ pins bonded out for a full 8-bit data width.

Note: VCCIO and GND pads are used to determine the average DC current drawn by I/Os between GND/VCCIO connections, or between the last GND/VCCIO in an I/O bank and the end of an I/O bank. The substrate pads listed in the Pin Table do not necessarily have a one to one connection with a package ball or pin.

| Date | Version | Section | Change Summary |
|---|---|---|---|
| August 2007 (cont.) | 02.8 (cont.) | DC and Switching (cont.) | sysCLOCK GPLL timing has been updated. |
| | | Pinout Information | Added ECP2M50 (484/672/900-fpBGA), ECP2M70 (900-fpBGA) and ECP2M100 (900-fpBGA) pinout information. |
| | | Ordering Information | 1156-fpBGA package option has been removed from the LatticeECP2M family. |
| September 2007 | 02.9 | Pinout Information | Added Thermal Management text section. |
| February 2008 | 03.0 | Architecture | Added LVCMOS33D description. |
| | | DC and Switching | LatticeECP2M Supply Current has been updated. |
| | | | Typical Building Block Function Performance, External Switching Characteristics, Internal Switching Characteristics, Family Timing Adders, sysCLOCK GPLL Timing, sysCLOCK SPLL Timing, DLL Timing and sysCONFIG Port Timing Specifications have been updated (timing rev. A 0.11). |
| | | | Figure 3-9. Read/Write Mode (Normal) and Figure 3-10. Read/Write Mode with Input and Output Registers have been updated. |
| | | | Table 3-8. Channel output Jitter (Max) has been updated. |
| | | Pinout Information | Signal description has been updated. |
| | | | Added 1152-fpBGA pinouts for the ECP2M70 and ECP2M100. |
| April 2008 | 03.1 | Pinout Information | Available DDR Interfaces per I/O Bank for the LFE2M35 (484/672-fpBGA) have been updated. |
| June 2008 | 03.2 | Introduction | Family Selection Guide table - Updated number of EBR SRAM Blocks for the ECP2-70 device. |
| | | Architecture | Removed Read-Before-Write sysMEM EBR mode. |
| | | | Clarification of the operation of the secondary clock regions. |
| | | DC and Switching Characteristics | Removed Read-Before-Write sysMEM EBR mode. |
| August 2008 | 03.3 | Architecture | Clarification of the operation of the secondary clock regions. |
| | | Pinout Information | Added information for [LOC]DQ[num] to Signal Descriptions table. |
| January 2009 | 03.4 | DC and Switching Characteristics | Updated typical and max. jitter numbers in Channel Output Jitter table for x10 mode. |
| | | | Added Channel Output Jitter table for x20 mode. |
| November 2009 | 03.5 | DC and Switching Characteristics | Updated SPI/SPIm Configuration Waveforms diagram. |
| | | | Updated footnotes in LatticeECP2 Initialization Supply Current table. |
| | | | Updated footnotes in LatticeECP2M Initialization Supply Current table. |
| | | | Updated footnotes in SERDES High Speed Data Receiver (LatticeECP2M Family Only) table. |
| | | | Updated max. value for $t_{DINIT}$ parameter in LatticeECP2/M sysCONFIG Port Timing Specifications table. |
| | | | Updated Serial Output Timing and Levels table. |
| | | | Updated Figure 3-5 MLVDS |
| | | | Updated Table 3-7 Serial Output Timing and Levels |
| | | | Updated Table 3-15 Power Down/Power Up Specification |
| | | Pinout Information | Signal Descriptions table - corrected references to ULM, URM, LRM (changed to LUM, RUM and RLM), added footnote 5. |