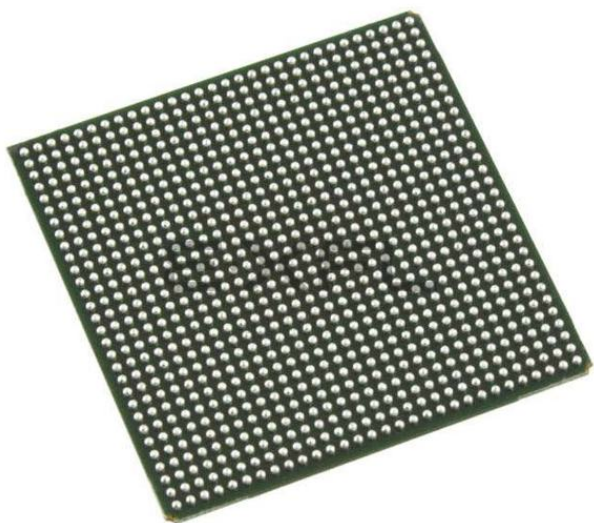




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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	6000
Number of Logic Elements/Cells	48000
Total RAM Bits	4246528
Number of I/O	410
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	900-BBGA
Supplier Device Package	900-FPBGA (31x31)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfe2m50se-5f900i

sysMEM Memory

LatticeECP2/M devices contains a number of sysMEM Embedded Block RAM (EBR). The EBR consists of an 18-Kbit RAM with dedicated input and output registers.

sysMEM Memory Block

The sysMEM block can implement single port, dual port or pseudo dual port memories. Each block can be used in a variety of depths and widths as shown in Table 2-6. FIFOs can be implemented in sysMEM EBR blocks by implementing support logic with PFUs. The EBR block facilitates parity checking by supporting an optional parity bit for each data byte. EBR blocks provide byte-enable support for configurations with 18-bit and 36-bit data widths.

Table 2-6. sysMEM Block Configurations

Memory Mode	Configurations
Single Port	16,384 x 1 8,192 x 2 4,096 x 4 2,048 x 9 1,024 x 18 512 x 36
True Dual Port	16,384 x 1 8,192 x 2 4,096 x 4 2,048 x 9 1,024 x 18
Pseudo Dual Port	16,384 x 1 8,192 x 2 4,096 x 4 2,048 x 9 1,024 x 18 512 x 36

Bus Size Matching

All of the multi-port memory modes support different widths on each of the ports. The RAM bits are mapped LSB word 0 to MSB word 0, LSB word 1 to MSB word 1, and so on. Although the word size and number of words for each port varies, this mapping scheme applies to each port.

RAM Initialization and ROM Operation

If desired, the contents of the RAM can be pre-loaded during device configuration. By preloading the RAM block during the chip configuration cycle and disabling the write controls, the sysMEM block can also be utilized as a ROM.

Memory Cascading

Larger and deeper blocks of RAM can be created using EBR sysMEM Blocks. Typically, the Lattice design tools cascade memory transparently, based on specific design inputs.

Single, Dual and Pseudo-Dual Port Modes

In all the sysMEM RAM modes the input data and address for the ports are registered at the input of the memory array. The output data of the memory is optionally registered at the output.

EBR memory supports two forms of write behavior for single port or dual port operation:

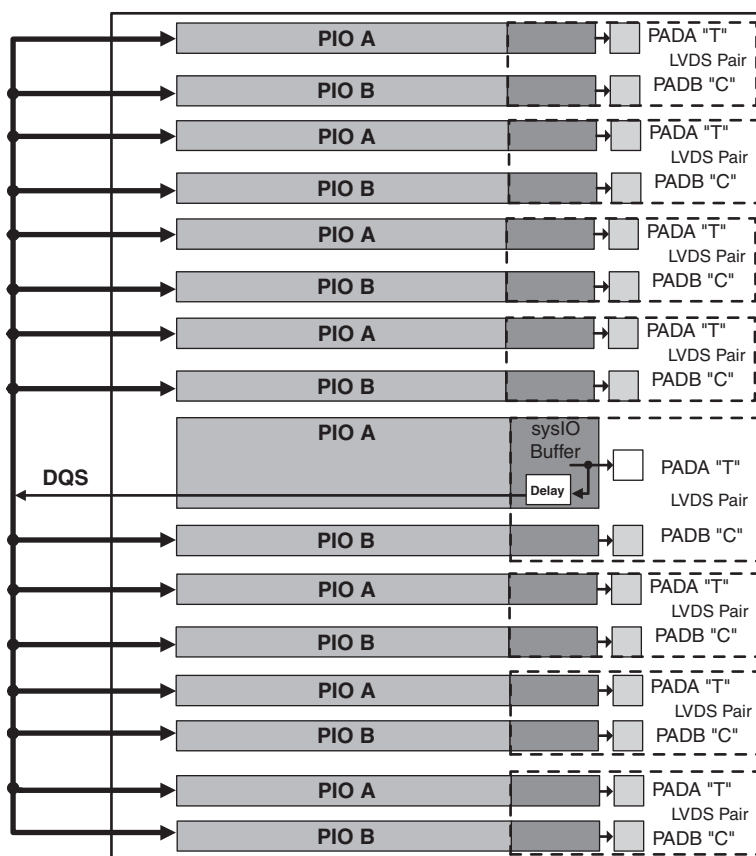
1. Normal – Data on the output appears only during a read cycle. During a write cycle, the data (at the current address) does not appear on the output. This mode is supported for all data widths.

Top Edge

The PICs on the top edge are different from PIOs on the left, right and bottom edges. PIOs on this edge do not have DDR registers or DQS signals.

The exact DQS pins are shown in a dual function in the Logic Signal Connections table in this data sheet. Additional detail is provided in the Signal Descriptions table. The DQS signal from the bus is used to strobe the DDR data from the memory into input register blocks. Interfaces on the left and right edges are designed for DDR memories that support 16 bits of data, whereas interfaces on the bottom are designed for memories that support 18 bits of data.

Figure 2-33. DQS Input Routing for the Left and Right Edges of the Device



RSDS

The LatticeECP2/M devices support differential RSDS standard. This standard is emulated using complementary LVCMOS outputs in conjunction with a parallel resistor across the driver outputs. The RSDS input standard is supported by the LVDS differential input buffer. The scheme shown in Figure 3-4 is one possible solution for RSDS standard implementation. Resistor values in Figure 3-4 are industry standard values for 1% resistors.

Figure 3-4. RSDS (Reduced Swing Differential Signaling)

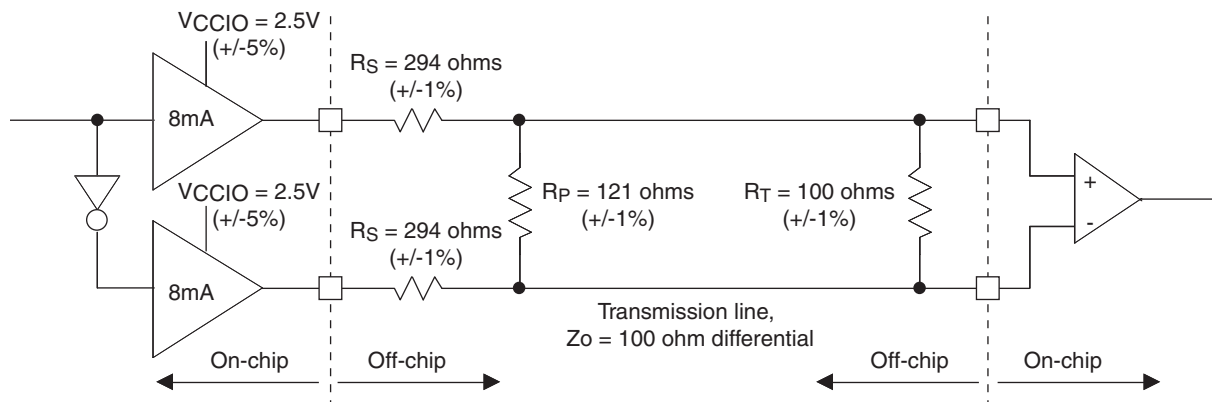


Table 3-5. RSDS DC Conditions¹

Over Recommended Operating Conditions

Parameter	Description	Typical	Units
V _{CCIO}	Output Driver Supply (+/-5%)	2.50	V
Z _{OUT}	Driver Impedance	20	Ω
R _S	Driver Series Resistor (+/-1%)	294	Ω
R _P	Driver Parallel Resistor (+/-1%)	121	Ω
R _T	Receiver Termination (+/-1%)	100	Ω
V _{OH}	Output High Voltage	1.35	V
V _{OL}	Output Low Voltage	1.15	V
V _{OD}	Output Differential Voltage	0.20	V
V _{CM}	Output Common Mode Voltage	1.25	V
Z _{BACK}	Back Impedance	101.5	Ω
I _{DC}	DC Output Current	3.66	mA

1. For input buffer, see LVDS table.

SERDES High-Speed Data Transmitter (LatticeECP2M Family Only)^{1, 2}

Table 3-7. Serial Output Timing and Levels

Symbol	Description	Frequency	Min.	Typ.	Max.	Units
V _{TX-DIFF-P-P-1}	Differential swing (1V setting) ^{1, 2}	0.25 to 3.125 Gbps	0.79	0.99	1.19	V, p-p
V _{TX-DIFF-P-P-1.25}	Differential swing (1.25V setting) ^{1, 2}	0.25 to 3.125 Gbps	1.00	1.25	1.50	V, p-p
V _{TX-DIFF-P-P-1.3}	Differential swing (1.3V setting) ^{1, 2}	0.25 to 3.125 Gbps	1.04	1.30	1.56	V, p-p
V _{TX-DIFF-P-P-1.35}	Differential swing (1.35V setting) ^{1, 2}	0.25 to 3.125 Gbps	1.08	1.35	1.62	V, p-p
V _{OCM}	Output common mode voltage	—	V _{CCOB} - 0.75	V _{CCOB} - 0.60	V _{CCOB} - 0.45	V
T _{TX-R}	Rise time (20% to 80%)	—	—	70	—	ps
T _{TX-F}	Fall time (80% to 20%)	—	—	70	—	ps
Z _{TX-OI-SE}	Output impedance 50/75/HiZ K Ohms (single-ended)	—	—	50/70 HiZ	—	Ohms
R _{TX-RL}	Return loss (with package)	—	—	9	—	dB

1. All measurements are with 50 ohm impedance.

2. See TN1124, [LatticeECP2M SERDES/PCS Usage Guide](#) for actual binary settings.

Table 3-8. Channel Output Jitter - x10 Mode

Description	Frequency	Min.	Typ.	Max.	Units
Deterministic	3.125 Gbps	—	0.08	0.12	UI, p-p
Random	3.125 Gbps	—	0.22	0.38	UI, p-p
Total	3.125 Gbps	—	0.33	0.43	UI, p-p
Deterministic	2.5 Gbps	—	0.08	0.17	UI, p-p
Random	2.5 Gbps	—	0.20	0.25	UI, p-p
Total	2.5 Gbps	—	0.25	0.35	UI, p-p
Deterministic	1.25 Gbps	—	0.03	0.10	UI, p-p
Random	1.25 Gbps	—	0.14	0.19	UI, p-p
Total	1.25 Gbps	—	0.17	0.24	UI, p-p
Deterministic	250 Mbps	—	0.04	0.17	UI, p-p
Random	250 Mbps	—	0.12	0.13	UI, p-p
Total	250 Mbps	—	0.15	0.29	UI, p-p

Note: Values are measured with PRBS 2⁷-1, all channels operating, FPGA Logic active, I/Os around SERDES pins quiet, reference clock at x10 mode.

Table 3-13. Periodic Receiver Jitter Tolerance Specification¹

Description	Frequency	Condition	Min.	Typ.	Max.	Units
Periodic	3.125 Gbps	600 mV differential eye	—	—	0.20	UI, p-p
	2.5 Gbps	600 mV differential eye	—	—	0.22	UI, p-p
	1.25 Gbps	600 mV differential eye	—	—	0.20	UI, p-p
	250 Mbps ²	600 mV differential eye	—	—	0.08	UI, p-p

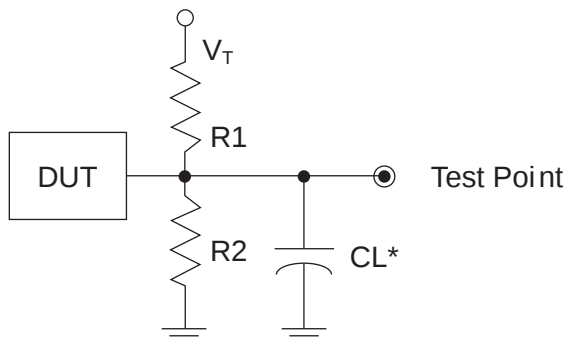
1. Values are measured with PRBS 2⁷-1, all channels operating.

2. Jitter specification is limited by measurement equipment capability.

Switching Test Conditions

Figure 3-22 shows the output test load that is used for AC testing. The specific values for resistance, capacitance, voltage, and other test conditions are shown in Table 3-19.

Figure 3-22. Output Test Load, LVTTTL and LVCMOS Standards



*CL Includes Test Fixture and Probe Capacitance

Table 3-19. Test Fixture Required Components, Non-Terminated Interfaces

Test Condition	R ₁	R ₂	C _L	Timing Ref.	V _T
LVTTTL and other LVCMOS settings (L → H, H → L)	∞	∞	0pF	LVCMOS 3.3 = 1.5V	—
				LVCMOS 2.5 = V _{CCIO} /2	—
				LVCMOS 1.8 = V _{CCIO} /2	—
				LVCMOS 1.5 = V _{CCIO} /2	—
				LVCMOS 1.2 = V _{CCIO} /2	—
LVCMOS 2.5 I/O (Z → H)	∞	1MΩ		V _{CCIO} /2	—
LVCMOS 2.5 I/O (Z → L)	1MΩ	∞		V _{CCIO} /2	V _{CCIO}
LVCMOS 2.5 I/O (H → Z)	∞	100		V _{OH} - 0.10	—
LVCMOS 2.5 I/O (L → Z)	100	∞		V _{OL} + 0.10	V _{CCIO}

Note: Output test conditions for all other interfaces are determined by the respective standards.

LFE2-6E/SE and LFE2-12E/SE Logic Signal Connections: 256 fpBGA (Cont.)

LFE2-6E/SE					LFE2-12E/SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
D5	PT2B	0	VREF2_0	C	PT2B	0	VREF2_0	C
E5	PT2A	0	VREF1_0	T	PT2A	0	VREF1_0	T
G7	VCC	-			VCC	-		
G9	VCC	-			VCC	-		
H7	VCC	-			VCC	-		
J10	VCC	-			VCC	-		
K10	VCC	-			VCC	-		
K8	VCC	-			VCC	-		
G8	VCCAUX	-			VCCAUX	-		
H10	VCCAUX	-			VCCAUX	-		
J7	VCCAUX	-			VCCAUX	-		
K9	VCCAUX	-			VCCAUX	-		
C5	VCCIO0	0			VCCIO0	0		
E7	VCCIO0	0			VCCIO0	0		
C12	VCCIO1	1			VCCIO1	1		
E10	VCCIO1	1			VCCIO1	1		
E14	VCCIO2	2			VCCIO2	2		
G12	VCCIO2	2			VCCIO2	2		
K12	VCCIO3	3			VCCIO3	3		
M14	VCCIO3	3			VCCIO3	3		
M10	VCCIO4	4			VCCIO4	4		
P12	VCCIO4	4			VCCIO4	4		
M7	VCCIO5	5			VCCIO5	5		
P5	VCCIO5	5			VCCIO5	5		
K5	VCCIO6	6			VCCIO6	6		
M3	VCCIO6	6			VCCIO6	6		
E3	VCCIO7	7			VCCIO7	7		
G5	VCCIO7	7			VCCIO7	7		
T15	VCCIO8	8			VCCIO8	8		
A1	GND	-			GND	-		
A16	GND	-			GND	-		
B12	GND	-			GND	-		
B5	GND	-			GND	-		
C8	GND	-			GND	-		
E15	GND	-			GND	-		
E2	GND	-			GND	-		
H14	GND	-			GND	-		
H8	GND	-			GND	-		
H9	GND	-			GND	-		
J3	GND	-			GND	-		
J8	GND	-			GND	-		
J9	GND	-			GND	-		
M15	GND	-			GND	-		
M2	GND	-			GND	-		
P9	GND	-			GND	-		

LFE2-20E/SE Logic Signal Connections: 256 fpBGA (Cont.)

LFE2-20E/SE					
Ball Number	Ball Number	Ball/Pad Function	Bank	Dual Function	Differential
VCCIO	VCCIO	VCCIO1	1		
D12	D12	PT62A	1		T
B14	B14	PT61B	1		C
C14	C14	PT60B	1		C
A14	A14	PT61A	1		T
D13	D13	PT60A	1		T
C13	C13	PT59B	1		C
GND	GND	GNDIO1	-		
A13	A13	PT58B	1		C
B13	B13	PT59A	1		T
VCCIO	VCCIO	VCCIO1	1		
A12	A12	PT58A	1		T
B11	B11	PT57B	1		C
D11	D11	PT56B	1		C
A11	A11	PT57A	1		T
C11	C11	PT56A	1		T
-	GND	GNDIO1	1		
-	VCC	VCCIO	1		
D10	D10	PT46B	1		C
C10	C10	PT46A	1		T
GND	GND	GNDIO1	-		
B10	B10	PT45B	1		C
A9	A9	PT44B	1		C
A10	A10	PT45A	1		T
B9	B9	PT44A	1		T
VCCIO	VCCIO	VCCIO1	1		
A8	A8	PT43B	1		C
D9	D9	PT42B	1		C
B8	B8	PT43A	1		T
C9	C9	PT42A	1		T
GND	GND	GNDIO1	-		
B7	B7	PT41B	1		C
E9	E9	PT40B	1		C
A7	A7	PT41A	1		T
D8	D8	PT40A	1		T
VCCIO	VCCIO	VCCIO1	1		
A6	A6	PT39B	1	PCLKC1_0	C
B6	B6	PT39A	1	PCLKT1_0	T
E6	E6	XRES	1		
F8	F8	PT37B	0	PCLKC0_0	C
GND	GND	GNDIO0	-		
E8	E8	PT37A	0	PCLKT0_0	T

LFE2-35E/SE and LFE2-50E/SE Logic Signal Connections: 484 fpBGA (Cont.)

LFE2-35E/SE					LFE2-50E/SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
U3	PL55A	6	LDQ56	T	PL74A	6	LDQ75	T
U4	PL55B	6	LDQ56	C	PL74B	6	LDQ75	C
GNDIO	GNDIO6	-			GNDIO6	-		
Y1	PL56A	6	LDQS56	T (LVDS)*	PL75A	6	LDQS75	T (LVDS)*
W1	PL56B	6	LDQ56	C (LVDS)*	PL75B	6	LDQ75	C (LVDS)*
R7	PL57A	6	LDQ56	T	PL76A	6	LDQ75	T
VCCIO	VCCIO6	6			VCCIO	6		
T7	PL57B	6	LDQ56	C	PL76B	6	LDQ75	C
V4	PL58A	6	LDQ56	T (LVDS)*	PL77A	6	LDQ75	T (LVDS)*
V3	PL58B	6	LDQ56	C (LVDS)*	PL77B	6	LDQ75	C (LVDS)*
AA2	PL59A	6	LDQ56	T	PL78A	6	LDQ75	T
GNDIO	GNDIO6	-			GNDIO6	-		
AA1	PL59B	6	LDQ56	C	PL78B	6	LDQ75	C
U7	TCK	-			TCK	-		
U5	TDI	-			TDI	-		
V5	TMS	-			TMS	-		
V6	TDO	-			TDO	-		
T8	VCCJ	-			VCCJ	-		
Y3	PB2A	5	VREF2_5/BDQ6	T	PB2A	5	VREF2_5/BDQ6	T
Y2	PB2B	5	VREF1_5/BDQ6	C	PB2B	5	VREF1_5/BDQ6	C
W4	PB3A	5	BDQ6	T	PB3A	5	BDQ6	T
W3	PB3B	5	BDQ6	C	PB3B	5	BDQ6	C
W5	PB4A	5	BDQ6	T	PB4A	5	BDQ6	T
W6	PB4B	5	BDQ6	C	PB4B	5	BDQ6	C
VCCIO	VCCIO5	5			VCCIO	5		
AB3	PB5A	5	BDQ6	T	PB5A	5	BDQ6	T
AB2	PB5B	5	BDQ6	C	PB5B	5	BDQ6	C
GNDIO	GNDIO5	-			GNDIO5	-		
Y4	PB6A	5	BDQS6	T	PB6A	5	BDQS6	T
AA3	PB6B	5	BDQ6	C	PB6B	5	BDQ6	C
AB5	PB7A	5	BDQ6	T	PB7A	5	BDQ6	T
AB4	PB7B	5	BDQ6	C	PB7B	5	BDQ6	C
AA5	PB8A	5	BDQ6	T	PB8A	5	BDQ6	T
Y5	PB8B	5	BDQ6	C	PB8B	5	BDQ6	C
VCCIO	VCCIO5	5			VCCIO	5		
AB6	PB9A	5	BDQ6	T	PB9A	5	BDQ6	T
AA6	PB9B	5	BDQ6	C	PB9B	5	BDQ6	C
GNDIO	GNDIO5	-			GNDIO5	-		
VCCIO	VCCIO5	5			VCCIO	5		
W7	PB20A	5	BDQ24	T	PB29A	5	BDQ33	T
W8	PB20B	5	BDQ24	C	PB29B	5	BDQ33	C
Y6	PB21A	5	BDQ24	T	PB30A	5	BDQ33	T
Y7	PB21B	5	BDQ24	C	PB30B	5	BDQ33	C
AA7	PB22A	5	BDQ24	T	PB31A	5	BDQ33	T
VCCIO	VCCIO5	5			VCCIO	5		
AB7	PB22B	5	BDQ24	C	PB31B	5	BDQ33	C

LFE2-20E/SE and LFE2-35E/SE Logic Signal Connections: 672 fpBGA (Cont.)

LFE2-20E/20SE					LFE2-35E/35SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
U1	NC	-			PL34A	6	LDQ31	T
V1	NC	-			PL34B	6	LDQ31	C
GND	GNDIO6	-			GNDIO6	-		
P3	NC	-			NC	-		
R3	NC	-			NC	-		
R4	NC	-			NC	-		
U2	NC	-			NC	-		
VCCIO	VCCIO6	6			VCCIO6	6		
V2	NC	-			NC	-		
W2	NC	-			NC	-		
T6	NC	-			PL38A	6	LDQ39	T
R5	NC	-			PL38B	6	LDQ39	C
GND	GNDIO6	-			GNDIO6	-		
R6	PL25A	6	LDQS25***	T (LVDS)*	PL39A	6	LDQS39***	T (LVDS)*
R7	PL25B	6	LDQ25	C (LVDS)*	PL39B	6	LDQ39	C (LVDS)*
W1	PL26A	6	LDQ25	T	PL40A	6	LDQ39	T
VCCIO	VCCIO6	6			VCCIO6	6		
Y2	PL26B	6	LDQ25	C	PL40B	6	LDQ39	C
Y1	PL27A	6	LLM0_GDLLT_IN_A**/LDQ25	T (LVDS)*	PL41A	6	LLM0_GDLLT_IN_A**/LDQ39	T (LVDS)*
AA2	PL27B	6	LLM0_GDLLC_IN_A**/LDQ25	C (LVDS)*	PL41B	6	LLM0_GDLLC_IN_A**/LDQ39	C (LVDS)*
T5	PL28A	6	LLM0_GDLLT_FB_A/LDQ25	T	PL42A	6	LLM0_GDLLT_FB_A/LDQ39	T
GND	GNDIO6	-			GNDIO6	-		
T7	PL28B	6	LLM0_GDLLC_FB_A/LDQ25	C	PL42B	6	LLM0_GDLLC_FB_A/LDQ39	C
R8	VCC	6			VCCPLL	6		
T8	LLM0_PLLCAP	6			LLM0_PLLCAP	6		
U3	PL30A	6	LLM0_GPLLT_IN_A**/LDQ34	T (LVDS)*	PL44A	6	LLM0_GPLLT_IN_A**/LDQ48	T (LVDS)*
U4	PL30B	6	LLM0_GPLLC_IN_A**/LDQ34	C (LVDS)*	PL44B	6	LLM0_GPLLC_IN_A**/LDQ48	C (LVDS)*
V3	PL31A	6	LLM0_GPLLT_FB_A/LDQ34	T	PL45A	6	LLM0_GPLLT_FB_A/LDQ48	T
U5	PL31B	6	LLM0_GPLLC_FB_A/LDQ34	C	PL45B	6	LLM0_GPLLC_FB_A/LDQ48	C
V4	PL32A	6	LDQ34	T (LVDS)*	PL46A	6	LDQ48	T (LVDS)*
VCCIO	VCCIO6	6			VCCIO6	6		
V5	PL32B	6	LDQ34	C (LVDS)*	PL46B	6	LDQ48	C (LVDS)*
Y3	PL33A	6	LDQ34	T	PL47A	6	LDQ48	T
Y4	PL33B	6	LDQ34	C	PL47B	6	LDQ48	C
W3	PL34A	6	LDQS34	T (LVDS)*	PL48A	6	LDQS48	T (LVDS)*
GND	GNDIO6	-			GNDIO6	-		
W4	PL34B	6	LDQ34	C (LVDS)*	PL48B	6	LDQ48	C (LVDS)*
AA1	PL35A	6	LDQ34	T	PL49A	6	LDQ48	T
AB1	PL35B	6	LDQ34	C	PL49B	6	LDQ48	C
VCCIO	VCCIO6	6			VCCIO6	6		
U8	PL36A	6	LDQ34	T (LVDS)*	PL50A	6	LDQ48	T (LVDS)*
U7	PL36B	6	LDQ34	C (LVDS)*	PL50B	6	LDQ48	C (LVDS)*
V8	PL37A	6	LDQ34	T	PL51A	6	LDQ48	T
U6	PL37B	6	LDQ34	C	PL51B	6	LDQ48	C
GND	GNDIO6	-			GNDIO6	-		
W6	PL38A	6	LDQ42	T (LVDS)*	PL52A	6	LDQ56	T (LVDS)*

LFE2-20E/SE and LFE2-35E/SE Logic Signal Connections: 672 fpBGA (Cont.)

LFE2-20E/20SE					LFE2-35E/35SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential	
AA14	PB29B	5	BDQ33	C	PB29B	5	BDQ33	C	
AE10	PB30A	5	BDQ33	T	PB30A	5	BDQ33	T	
AF10	PB30B	5	BDQ33	C	PB30B	5	BDQ33	C	
W14	PB31A	5	BDQ33	T	PB31A	5	BDQ33	T	
AB13	PB31B	5	BDQ33	C	PB31B	5	BDQ33	C	
VCCIO	VCCIO5	5			VCCIO5	5			
Y14	PB32A	5	BDQ33	T	PB32A	5	BDQ33	T	
AB14	PB32B	5	BDQ33	C	PB32B	5	BDQ33	C	
GND	GNDIO5	-			GNDIO5	-			
AE11	PB33A	5	BDQS33	T	PB33A	5	BDQS33	T	
AF11	PB33B	5	BDQ33	C	PB33B	5	BDQ33	C	
AD14	PB34A	5	BDQ33	T	PB34A	5	BDQ33	T	
AA15	PB34B	5	BDQ33	C	PB34B	5	BDQ33	C	
AE12	PB35A	5	PCLKT5_0/BDQ33	T	PB35A	5	PCLKT5_0/BDQ33	T	
AF12	PB35B	5	PCLKC5_0/BDQ33	C	PB35B	5	PCLKC5_0/BDQ33	C	
VCCIO	VCCIO5	5			VCCIO5	5			
GND	GNDIO5	-			GNDIO5	-			
AD15	PB40A	4	PCLKT4_0/BDQ42	T	PB40A	4	PCLKT4_0/BDQ42	T	
VCCIO	VCCIO4	4			VCCIO4	4			
AC15	PB40B	4	PCLKC4_0/BDQ42	C	PB40B	4	PCLKC4_0/BDQ42	C	
AE13	PB41A	4	BDQ42	T	PB41A	4	BDQ42	T	
AF13	PB41B	4	BDQ42	C	PB41B	4	BDQ42	C	
AB17	PB42A	4	BDQS42	T	PB42A	4	BDQS42	T	
GND	GNDIO4	-			GNDIO4	-			
Y15	PB42B	4	BDQ42	C	PB42B	4	BDQ42	C	
AE14	PB43A	4	BDQ42	T	PB43A	4	BDQ42	T	
AF14	PB43B	4	BDQ42	C	PB43B	4	BDQ42	C	
AA16	PB44A	4	BDQ42	T	PB44A	4	BDQ42	T	
VCCIO	VCCIO4	4			VCCIO4	4			
W15	PB44B	4	BDQ42	C	PB44B	4	BDQ42	C	
AC17	PB45A	4	BDQ42	T	PB45A	4	BDQ42	T	
AB16	PB45B	4	BDQ42	C	PB45B	4	BDQ42	C	
AE15	PB46A	4	BDQ42	T	PB46A	4	BDQ42	T	
GND	GNDIO4	-			GNDIO4	-			
AF15	PB46B	4	BDQ42	C	PB46B	4	BDQ42	C	
AE16	PB47A	4	BDQ51	T	PB47A	4	BDQ51	T	
AF16	PB47B	4	BDQ51	C	PB47B	4	BDQ51	C	
Y16	PB48A	4	BDQ51	T	PB48A	4	BDQ51	T	
AB18	PB48B	4	BDQ51	C	PB48B	4	BDQ51	C	
AD17	PB49A	4	BDQ51	T	PB49A	4	BDQ51	T	
AD18	PB49B	4	BDQ51	C	PB49B	4	BDQ51	C	
VCCIO	VCCIO4	4			VCCIO4	4			
AC18	PB50A	4	BDQ51	T	PB50A	4	BDQ51	T	
AD19	PB50B	4	BDQ51	C	PB50B	4	BDQ51	C	
GND	GNDIO4	-			GNDIO4	-			
AC19	PB51A	4	BDQS51	T	PB51A	4	BDQS51	T	

LFE2-20E/SE and LFE2-35E/SE Logic Signal Connections: 672 fpBGA (Cont.)

LFE2-20E/20SE					LFE2-35E/35SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
A7	PT26B	0		C	PT26B	0		C
B7	PT26A	0		T	PT26A	0		T
VCCIO	VCCIO0	0			VCCIO0	0		
F12	PT25B	0		C	PT25B	0		C
D10	PT25A	0		T	PT25A	0		T
H11	PT24B	0		C	PT24B	0		C
G11	PT24A	0		T	PT24A	0		T
GND	GNDIO0	-			GNDIO0	-		
A6	PT23B	0		C	PT23B	0		C
B6	PT23A	0		T	PT23A	0		T
D8	PT22B	0		C	PT22B	0		C
C8	PT22A	0		T	PT22A	0		T
VCCIO	VCCIO0	0			VCCIO0	0		
F11	PT21B	0		C	PT21B	0		C
E10	PT21A	0		T	PT21A	0		T
E9	PT20B	0		C	PT20B	0		C
D9	PT20A	0		T	PT20A	0		T
G10	PT19B	0		C	PT19B	0		C
GND	GNDIO0	-			GNDIO0	-		
H10	PT19A	0		T	PT19A	0		T
A5	PT18B	0		C	PT18B	0		C
B5	PT18A	0		T	PT18A	0		T
C7	PT17B	0		C	PT17B	0		C
VCCIO	VCCIO0	0			VCCIO0	0		
D7	PT17A	0		T	PT17A	0		T
E8	PT16B	0		C	PT16B	0		C
F10	PT16A	0		T	PT16A	0		T
F8	PT15B	0		C	PT15B	0		C
H9	PT15A	0		T	PT15A	0		T
C5	PT14B	0		C	PT14B	0		C
GND	GNDIO0	-			GNDIO0	-		
D5	PT14A	0		T	PT14A	0		T
B4	PT13B	0			PT13B	0		
VCCIO	VCCIO0	0			VCCIO0	0		
GND	GNDIO0	-			GNDIO0	-		
VCCIO	VCCIO0	0			VCCIO0	0		
GND	GNDIO0	-			GNDIO0	-		
VCCIO	VCCIO0	0			VCCIO0	0		
C4	PT10B	0		C	PT10B	0		C
GND	GNDIO0	-			GNDIO0	-		
C3	PT10A	0		T	PT10A	0		T
A4	PT9B	0		C	PT9B	0		C
A3	PT9A	0		T	PT9A	0		T
B3	PT8B	0		C	PT8B	0		C
VCCIO	VCCIO0	0			VCCIO0	0		
B2	PT8A	0		T	PT8A	0		T

LFE2-20E/SE and LFE2-35E/SE Logic Signal Connections: 672 fpBGA (Cont.)

LFE2-20E/20SE					LFE2-35E/35SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
N15	GND	-			GND	-		
N17	GND	-			GND	-		
P10	GND	-			GND	-		
P12	GND	-			GND	-		
P13	GND	-			GND	-		
P14	GND	-			GND	-		
P15	GND	-			GND	-		
P17	GND	-			GND	-		
R13	GND	-			GND	-		
R14	GND	-			GND	-		
T10	GND	-			GND	-		
T11	GND	-			GND	-		
T16	GND	-			GND	-		
T17	GND	-			GND	-		
T24	GND	-			GND	-		
T3	GND	-			GND	-		
U10	GND	-			GND	-		
U11	GND	-			GND	-		
U13	GND	-			GND	-		
U14	GND	-			GND	-		
U16	GND	-			GND	-		
U17	GND	-			GND	-		
V13	GND	-			GND	-		
V14	GND	-			GND	-		
V21	GND	-			GND	-		
V6	GND	-			GND	-		
M3	NC	-			NC	-		
N6	NC	-			NC	-		
P24	NC	-			NC	-		

* Supports true LVDS. Other differential signals must be emulated with external resistors.

** These dedicated input pins can be used for GPLLs or GDLLs within the respective quadrant.

***Due to packaging bond out option, this DQS does not have all the necessary DQ pins bonded out for a full 8-bit data width.

Note: VCCIO and GND pads are used to determine the average DC current drawn by I/Os between GND/VCCIO connections, or between the last GND/VCCIO in an I/O bank and the end of an I/O bank. The substrate pads listed in the Pin Table do not necessarily have a one to one connection with a package ball or pin.

LFE2M-20E/SE and LFE2M-35E/SE Logic Signal Connections: 256 fpBGA (Cont.)

LFE2M20E/SE					LFE2M35E/SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
T7	PB22A	4	PCLKT4_0/BDQ24	T	PB40A	4	PCLKT4_0/BDQ42	T
VCCIO	VCCIO4	4			VCCIO4	4		
T8	PB22B	4	PCLKC4_0/BDQ24	C	PB40B	4	PCLKC4_0/BDQ42	C
L7	PB23A	4	VREF2_4/BDQ24	T	PB41A	4	VREF2_4/BDQ42	T
L8	PB23B	4	VREF1_4/BDQ24	C	PB41B	4	VREF1_4/BDQ42	C
GNDIO	GNDIO4	-			GNDIO4	-		
VCCIO	VCCIO4	4			VCCIO4	4		
GNDIO	GNDIO4	-			GNDIO4	-		
P8	PB29A	4	BDQ33	T	PB47A	4	BDQ51	T
N8	PB29B	4	BDQ33	C	PB47B	4	BDQ51	C
R7	PB30A	4	BDQ33	T	PB48A	4	BDQ51	T
R8	PB30B	4	BDQ33	C	PB48B	4	BDQ51	C
N7	PB31A	4	BDQ33	T	PB49A	4	BDQ51	T
M8	PB31B	4	BDQ33	C	PB49B	4	BDQ51	C
VCCIO	VCCIO4	4			VCCIO4	4		
R9	PB32A	4	BDQ33	T	PB50A	4	BDQ51	T
T9	PB32B	4	BDQ33	C	PB50B	4	BDQ51	C
GNDIO	GNDIO4	-			GNDIO4	-		
T10	PB33A	4	BDQS33	T	PB51A	4	BDQS51	T
R10	PB33B	4	BDQ33	C	PB51B	4	BDQ51	C
N9	PB34A	4	BDQ33	T	PB52A	4	BDQ51	T
P10	PB34B	4	BDQ33	C	PB52B	4	BDQ51	C
VCCIO	VCCIO4	4			VCCIO4	4		
GNDIO	GNDIO4	-			GNDIO4	-		
L9	PB47A	4	BDQ51	T	PB65A	4	BDQ69	T
M9	PB47B	4	BDQ51	C	PB65B	4	BDQ69	C
T11	PB49A	4	BDQ51	T	PB67A	4	BDQ69	T
R11	PB49B	4	BDQ51	C	PB67B	4	BDQ69	C
VCCIO	VCCIO4	4			VCCIO4	4		
T12	PB50A	4	BDQ51	T	PB68A	4	BDQ69	T
T13	PB50B	4	BDQ51	C	PB68B	4	BDQ69	C
GNDIO	GNDIO4	-			GNDIO4	-		
P11	PB51A	4	BDQS51	T	PB69A	4	BDQS69	T
N10	PB51B	4	BDQ51	C	PB69B	4	BDQ69	C
T14	PB52A	4	BDQ51	T	PB70A	4	BDQ69	T
R13	PB52B	4	BDQ51	C	PB70B	4	BDQ69	C
R15	PB53A	4	BDQ51	T	PB71A	4	BDQ69	T
R16	PB53B	4	BDQ51	C	PB71B	4	BDQ69	C
VCCIO	VCCIO4	4			VCCIO4	4		
R14	PB54A	4	BDQ51	T	PB72A	4	BDQ69	T
P15	PB54B	4	BDQ51	C	PB72B	4	BDQ69	C
P16	PB55A	4	BDQ51	T	PB73A	4	BDQ69	T
P14	PB55B	4	BDQ51	C	PB73B	4	BDQ69	C
GNDIO	GNDIO4	-			GNDIO4	-		
L11	CFG2	8			CFG2	8		
L10	CFG1	8			CFG1	8		
P13	CFG0	8			CFG0	8		
N12	PROGRAMN	8			PROGRAMN	8		

LFE2M50E/SE Logic Signal Connections: 484 fpBGA (Cont.)

LFE2M50E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential
L11	GND	-		
L12	GND	-		
L13	GND	-		
M10	GND	-		
M11	GND	-		
M12	GND	-		
M13	GND	-		
N10	GND	-		
N11	GND	-		
N12	GND	-		
N13	GND	-		
N15	GND	-		
N20	GND	-		
N3	GND	-		
N8	GND	-		
P14	GND	-		
P9	GND	-		
R10	GND	-		
R13	GND	-		
T19	GND	-		
T4	GND	-		
W16	GND	-		
W2	GND	-		
W21	GND	-		
W7	GND	-		
Y10	GND	-		
Y13	GND	-		
Y15	NC	-		
W15	NC	-		
AB20	NC	-		
AB21	NC	-		
AA21	NC	-		
AA20	NC	-		
AB19	NC	-		
AB18	NC	-		
Y22	NC	-		
Y21	NC	-		
Y17	NC	-		
Y18	NC	-		
Y16	NC	-		
W17	NC	-		
Y19	NC	-		
Y20	NC	-		

LFE2M35E/SE and LFE2M50E/SE Logic Signal Connections: 672 fpBGA (Cont.)

LFE2M35E/SE					LFE2M50E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential	
C15	URC_SQ_VCCIB2	12			URC_SQ_VCCIB2	12			
B15	URC_SQ_HDINN2	12		C	URC_SQ_HDINN2	12		C	
C14	URC_SQ_VCCRX2	12			URC_SQ_VCCRX2	12			
A18	URC_SQ_HDOUTP2	12		T	URC_SQ_HDOUTP2	12		T	
C18	URC_SQ_VCCOB2	12			URC_SQ_VCCOB2	12			
B18	URC_SQ_HDOUTN2	12		C	URC_SQ_HDOUTN2	12		C	
C17	URC_SQ_VCCTX2	12			URC_SQ_VCCTX2	12			
B17	URC_SQ_HDOUTN3	12		C	URC_SQ_HDOUTN3	12		C	
A16	URC_SQ_VCCOB3	12			URC_SQ_VCCOB3	12			
A17	URC_SQ_HDOUTP3	12		T	URC_SQ_HDOUTP3	12		T	
C16	URC_SQ_VCCTX3	12			URC_SQ_VCCTX3	12			
B14	URC_SQ_HDINN3	12		C	URC_SQ_HDINN3	12		C	
B13	URC_SQ_VCCIB3	12			URC_SQ_VCCIB3	12			
A14	URC_SQ_HDINP3	12		T	URC_SQ_HDINP3	12		T	
C13	URC_SQ_VCCRX3	12			URC_SQ_VCCRX3	12			
-	-	-			GNDIO1	-			
-	-	-			VCCIO1	1			
E17	PT46B	1		C	PT55B	1		C	
D17	PT46A	1		T	PT55A	1		T	
GNDIO	GNDIO1	-			GNDIO1	-			
F17	PT45B	1		C	PT54B	1		C	
D16	PT45A	1		T	PT54A	1		T	
F19	PT44B	1		C	PT53B	1		C	
F18	PT44A	1		T	PT53A	1		T	
VCCIO	VCCIO1	1			VCCIO1	1			
E16	PT43B	1		C	PT52B	1		C	
D15	PT43A	1		T	PT52A	1		T	
G18	PT42B	1		C	PT51B	1		C	
E15	PT42A	1		T	PT51A	1		T	
GNDIO	GNDIO1	-			GNDIO1	-			
G17	PT41B	1		C	PT50B	1		C	
E14	PT41A	1		T	PT50A	1		T	
D14	PT40B	1		C	PT49B	1		C	
D13	PT40A	1		T	PT49A	1		T	
VCCIO	VCCIO1	1			VCCIO1	1			
F15	PT39B	1	VREF2_1	C	PT48B	1	VREF2_1	C	
E12	PT39A	1	VREF1_1	T	PT48A	1	VREF1_1	T	
H17	PT38B	1	PCLKC1_0	C	PT47B	1	PCLKC1_0	C	
E13	PT38A	1	PCLKT1_0	T	PT47A	1	PCLKT1_0	T	
C12	PT37B	0	PCLKC0_0	C	PT46B	0	PCLKC0_0	C	
GNDIO	GNDIO0	-			GNDIO0	-			
G15	PT37A	0	PCLKT0_0	T	PT46A	0	PCLKT0_0	T	
C11	PT36B	0	VREF2_0	C	PT45B	0	VREF2_0	C	
F14	PT36A	0	VREF1_0	T	PT45A	0	VREF1_0	T	

LFE2M100E/SE Logic Signal Connections: 900 fpBGA (Cont.)

LFE2M100E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential
M23	GND	-		
M8	GND	-		
N14	GND	-		
N15	GND	-		
N16	GND	-		
N17	GND	-		
N27	GND	-		
N4	GND	-		
P11	GND	-		
P13	GND	-		
P14	GND	-		
P15	GND	-		
P16	GND	-		
P17	GND	-		
P18	GND	-		
P20	GND	-		
R10	GND	-		
R11	GND	-		
R13	GND	-		
R14	GND	-		
R15	GND	-		
R16	GND	-		
R17	GND	-		
R18	GND	-		
R20	GND	-		
R21	GND	-		
R24	GND	-		
R7	GND	-		
T10	GND	-		
T11	GND	-		
T13	GND	-		
T14	GND	-		
T15	GND	-		
T16	GND	-		
T17	GND	-		
T18	GND	-		
T20	GND	-		
T21	GND	-		
T24	GND	-		
T7	GND	-		
U11	GND	-		
U13	GND	-		
U14	GND	-		

LFE2M100E/SE Logic Signal Connections: 900 fpBGA (Cont.)

LFE2M100E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential
V18	VCCPLL	-		

* Supports true LVDS. Other differential signals must be emulated with external resistors.

** These dedicated input pins can be used for GPLLs or GDLLs within the respective quadrant.

*** These sysCONFIG pins are dedicated I/O pins for configuration. The outputs are actively driven during normal device operation.

****Due to packaging bond out option, this DQS does not have all the necessary DQ pins bonded out for a full 8-bit data width.

Note: VCCIO and GND pads are used to determine the average DC current drawn by I/Os between GND/VCCIO connections, or between the last GND/VCCIO in an I/O bank and the end of an I/O bank. The substrate pads listed in the Pin Table do not necessarily have a one to one connection with a package ball or pin.

LFE2M70E/SE and LFE2M100E/SE Logic Signal Connections: 1152 fpBGA (Cont.)

LFE2M70E/SE				LFE2M100E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
U8	PL43B	7	LUM3_SPLLC_FB_A/LDQ46	C	PL51B	7	LUM3_SPLLC_FB_A/LDQ54	C
VCCIO	VCCIO7	7			VCCIO7	7		
T6	PL44A	7	LDQ46	T (LVDS)*	PL52A	7	LDQ54	T (LVDS)*
R6	PL44B	7	LDQ46	C (LVDS)*	PL52B	7	LDQ54	C (LVDS)*
U9	PL45A	7	LDQ46	T	PL53A	7	LDQ54	T
T7	PL45B	7	LDQ46	C	PL53B	7	LDQ54	C
GNDIO	GNDIO7	-			GNDIO7	-		
U5	PL46A	7	LDQS46	T (LVDS)*	PL54A	7	LDQS54	T (LVDS)*
U6	PL46B	7	LDQ46	C (LVDS)*	PL54B	7	LDQ54	C (LVDS)*
U7	PL47A	7	LDQ46	T	PL55A	7	LDQ54	T
VCCIO	VCCIO7	7			VCCIO7	7		
V9	PL47B	7	LDQ46	C	PL55B	7	LDQ54	C
V11	PL48A	7	LDQ46	T (LVDS)*	PL56A	7	LDQ54	T (LVDS)*
V10	PL48B	7	LDQ46	C (LVDS)*	PL56B	7	LDQ54	C (LVDS)*
U4	PL49A	7	PCLKT7_0/LDQ46	T	PL57A	7	PCLKT7_0/LDQ54	T
GNDIO	GNDIO7	-			GNDIO7	-		
U3	PL49B	7	PCLKC7_0/LDQ46	C	PL57B	7	PCLKC7_0/LDQ54	C
U2	PL51A	6	PCLKT6_0/LDQ55	T (LVDS)*	PL59A	6	PCLKT6_0/LDQ63	T (LVDS)*
U1	PL51B	6	PCLKC6_0/LDQ55	C (LVDS)*	PL59B	6	PCLKC6_0/LDQ63	C (LVDS)*
V5	PL52A	6	VREF2_6/LDQ55	T	PL60A	6	VREF2_6/LDQ63	T
V6	PL52B	6	VREF1_6/LDQ55	C	PL60B	6	VREF1_6/LDQ63	C
V7	PL53A	6	LDQ55	T (LVDS)*	PL61A	6	LDQ63	T (LVDS)*
VCCIO	VCCIO6	6			VCCIO6	6		
V8	PL53B	6	LDQ55	C (LVDS)*	PL61B	6	LDQ63	C (LVDS)*
V4	PL54A	6	LDQ55	T	PL62A	6	LDQ63	T
V3	PL54B	6	LDQ55	C	PL62B	6	LDQ63	C
V2	PL55A	6	LDQS55	T (LVDS)*	PL63A	6	LDQS63	T (LVDS)*
GNDIO	GNDIO6	-			GNDIO6	-		
V1	PL55B	6	LDQ55	C (LVDS)*	PL63B	6	LDQ63	C (LVDS)*
W7	PL56A	6	LDQ55	T	PL64A	6	LDQ63	T
W5	PL56B	6	LDQ55	C	PL64B	6	LDQ63	C
VCCIO	VCCIO6	6			VCCIO6	6		
W2	PL57A	6	LLM3_SPLLT_IN_A/LDQ55	T (LVDS)*	PL65A	6	LLM4_SPLLT_IN_A/LDQ63	T (LVDS)*
W1	PL57B	6	LLM3_SPLLC_IN_A/LDQ55	C (LVDS)*	PL65B	6	LLM4_SPLLC_IN_A/LDQ63	C (LVDS)*
Y6	PL58A	6	LLM3_SPLLT_FB_A/LDQ55	T	PL66A	6	LLM4_SPLLT_FB_A/LDQ63	T
W6	PL58B	6	LLM3_SPLLC_FB_A/LDQ55	C	PL66B	6	LLM4_SPLLC_FB_A/LDQ63	C
GNDIO	GNDIO6	-			GNDIO6	-		
Y1	PL60A	6	LDQ64	T (LVDS)*	PL68A	6	LDQ72	T (LVDS)*
Y2	PL60B	6	LDQ64	C (LVDS)*	PL68B	6	LDQ72	C (LVDS)*
Y7	PL61A	6	LDQ64	T	PL69A	6	LDQ72	T
Y5	PL61B	6	LDQ64	C	PL69B	6	LDQ72	C
VCCIO	VCCIO6	6			VCCIO6	6		
W10	PL62A	6	LDQ64	T (LVDS)*	PL70A	6	LDQ72	T (LVDS)*
Y8	PL62B	6	LDQ64	C (LVDS)*	PL70B	6	LDQ72	C (LVDS)*
Y4	PL63A	6	LDQ64	T	PL71A	6	LDQ72	T
Y3	PL63B	6	LDQ64	C	PL71B	6	LDQ72	C
GNDIO	GNDIO6	-			GNDIO6	-		
AA1	PL64A	6	LDQS64	T (LVDS)*	PL72A	6	LDQS72	T (LVDS)*
AA2	PL64B	6	LDQ64	C (LVDS)*	PL72B	6	LDQ72	C (LVDS)*

LatticeECP2 Standard Series Devices, Lead-Free Packaging

Commercial

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2-6E-5TN144C	90	1.2V	-5	Lead-Free TQFP	144	COM	6
LFE2-6E-6TN144C	90	1.2V	-6	Lead-Free TQFP	144	COM	6
LFE2-6E-7TN144C	90	1.2V	-7	Lead-Free TQFP	144	COM	6
LFE2-6E-5FN256C	190	1.2V	-5	Lead-Free fpBGA	256	COM	6
LFE2-6E-6FN256C	190	1.2V	-6	Lead-Free fpBGA	256	COM	6
LFE2-6E-7FN256C	190	1.2V	-7	Lead-Free fpBGA	256	COM	6

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2-12E-5TN144C	93	1.2V	-5	Lead-Free TQFP	144	COM	12
LFE2-12E-6TN144C	93	1.2V	-6	Lead-Free TQFP	144	COM	12
LFE2-12E-7TN144C	93	1.2V	-7	Lead-Free TQFP	144	COM	12
LFE2-12E-5QN208C	131	1.2V	-5	Lead-Free PQFP	208	COM	12
LFE2-12E-6QN208C	131	1.2V	-6	Lead-Free PQFP	208	COM	12
LFE2-12E-7QN208C	131	1.2V	-7	Lead-Free PQFP	208	COM	12
LFE2-12E-5FN256C	193	1.2V	-5	Lead-Free fpBGA	256	COM	12
LFE2-12E-6FN256C	193	1.2V	-6	Lead-Free fpBGA	256	COM	12
LFE2-12E-7FN256C	193	1.2V	-7	Lead-Free fpBGA	256	COM	12
LFE2-12E-5FN484C	297	1.2V	-5	Lead-Free fpBGA	484	COM	12
LFE2-12E-6FN484C	297	1.2V	-6	Lead-Free fpBGA	484	COM	12
LFE2-12E-7FN484C	297	1.2V	-7	Lead-Free fpBGA	484	COM	12

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2-20E-5QN208C	131	1.2V	-5	Lead-Free PQFP	208	COM	20
LFE2-20E-6QN208C	131	1.2V	-6	Lead-Free PQFP	208	COM	20
LFE2-20E-7QN208C	131	1.2V	-7	Lead-Free PQFP	208	COM	20
LFE2-20E-5FN256C	193	1.2V	-5	Lead-Free fpBGA	256	COM	20
LFE2-20E-6FN256C	193	1.2V	-6	Lead-Free fpBGA	256	COM	20
LFE2-20E-7FN256C	193	1.2V	-7	Lead-Free fpBGA	256	COM	20
LFE2-20E-5FN484C	331	1.2V	-5	Lead-Free fpBGA	484	COM	20
LFE2-20E-6FN484C	331	1.2V	-6	Lead-Free fpBGA	484	COM	20
LFE2-20E-7FN484C	331	1.2V	-7	Lead-Free fpBGA	484	COM	20
LFE2-20E-5FN672C	402	1.2V	-5	Lead-Free fpBGA	672	COM	20
LFE2-20E-6FN672C	402	1.2V	-6	Lead-Free fpBGA	672	COM	20
LFE2-20E-7FN672C	402	1.2V	-7	Lead-Free fpBGA	672	COM	20