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Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

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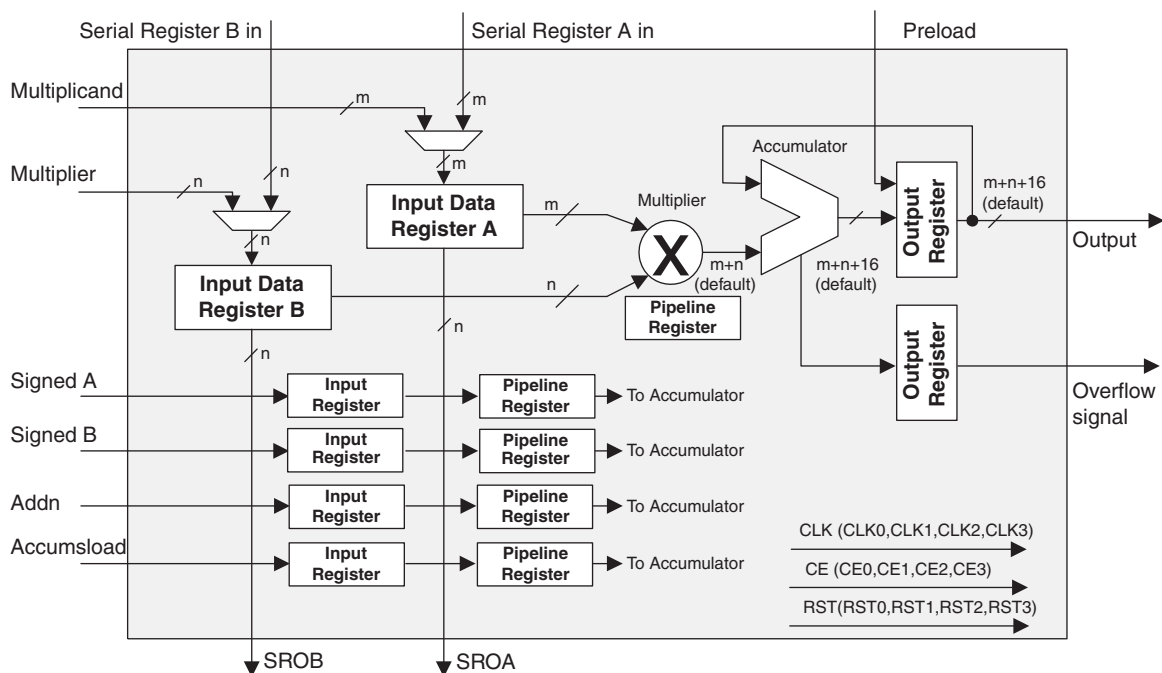
Details

Product Status	Active
Number of LABs/CLBs	6000
Number of Logic Elements/Cells	48000
Total RAM Bits	4246528
Number of I/O	270
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	484-BBGA
Supplier Device Package	484-FPBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfe2m50se-5fn484i

MAC sysDSP Element

In this case, the two operands, A and B, are multiplied and the result is added with the previous accumulated value. This accumulated value is available at the output. The user can enable the input and pipeline registers, but the output register is always enabled. The output register is used to store the accumulated value. The Accumulators in the DSP blocks in the LatticeECP2/M family can be initialized dynamically. A registered overflow signal is also available. The overflow conditions are provided later in this document. Figure 2-24 shows the MAC sysDSP element.

Figure 2-24. MAC sysDSP



LatticeECP2/M External Switching Characteristics⁹ (Continued)

Over Recommended Operating Conditions

Parameter	Description	Device	-7		-6		-5		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
t _{DIBSPI}	Data Invalid Before Clock (Transmit)	ECP2-20	—	280	—	280	—	280	ps
		ECP2-35	—	280	—	280	—	280	ps
		ECP2-50	—	280	—	280	—	280	ps
		ECP2-70	—	280	—	280	—	280	ps
		ECP2M20	—	230	—	230	—	230	ps
		ECP2M35	—	230	—	230	—	230	ps
		ECP2M50	—	230	—	230	—	230	ps
		ECP2M70	—	230	—	230	—	230	ps
		ECP2M100	—	230	—	230	—	230	ps
XGMII I/O Pin Parameters (312 Mbps) ⁵									
t _{SUXGMII}	Data Setup Before Read Clock	ECP2/M	480	—	480	—	480	—	ps
t _{HXGMII}	Data Hold After Read Clock	ECP2/M	480	—	480	—	480	—	ps
t _{DVBCKXGMII}	Data Valid Before Clock	ECP2/M	960	—	960	—	960	—	ps
t _{DVACKXGMII}	Data Valid After Clock	ECP2/M	960	—	960	—	960	—	ps
Primary									
f _{MAX_PRI} ⁷	Frequency for Primary Clock Tree	ECP2/M	—	420	—	357	—	311	MHz
t _{W_PRI}	Clock Pulse Width for Primary Clock	ECP2/M	0.95	—	1.19	—	2.00	—	ns
t _{SKEW_PRI}	Primary Clock Skew Within a Bank	ECP2/M	—	300	—	360	—	420	ps
Edge Clock									
f _{MAX_EDGE} ⁷	Frequency for Edge Clock	ECP2/M	—	420	—	357	—	311	MHz
t _{W_EDGE}	Clock Pulse Width for Edge Clock	ECP2/M	0.95	—	1.19	—	2.00	—	ns
t _{SKEW_EDGE}	Edge Clock Skew Within an Edge of the Device	ECP2/M	—	300	—	360	—	420	ps

- General timing numbers based on LVCMOS 2.5, 12mA, 0pf load.
- DDR timing numbers based on SSTL25 for BGA packages only.
- DDR2 timing numbers based on SSTL18 for BGA packages only.
- SPI4.2 and SFI4 timing numbers based on LVDS25 for BGA packages only.
- XGMII timing numbers based on HSTL class I. A corresponding left/right dedicated clock buffer is used when using the SPI4.2 interface to the left or right edge of the device. For SPI4.2 mode, the software tool will help in selecting the appropriate clock buffer.
- IP will be used to support DDR and DDR2 memory data rates down to 95MHz. This approach uses a free-running clock and PFU register to sample the data instead of the hardwired DDR memory interface.
- Using the LVDS I/O standard.
- ECP2-6 and ECP2-12 do not support SPI4.2
- The AC numbers do not apply to PCLK6 and PCLK7.
- Applies to CLKOP only.
- Please refer to TN1159, [LatticeECP2/M Pin Assignment Recommendations](#) for best performance.

LatticeECP2 Pin Information Summary, LFE2-20 and LFE2-35 (Cont.)

Pin Type		LFE2-20				LFE2-35	
		208 PQFP	256 fpBGA	484 fpBGA	672 fpBGA	484 fpBGA	672 fpBGA
Available DDR-Interfaces per I/O Bank ¹	Bank0	0	0	0	0	0	0
	Bank1	0	0	0	0	0	0
	Bank2	0	1	2	2	2	3
	Bank3	0	0	0	2	0	2
	Bank4	0	2	3	3	3	3
	Bank5	0	1	3	4	3	4
	Bank6	0	1	2	3	1	3
	Bank7	0	1	2	2	2	3
	Bank8	0	0	0	0	0	0
PCI Capable I/Os per Bank	Bank0	0	0	0	0	0	0
	Bank1	0	0	0	0	0	0
	Bank2	0	0	0	0	0	0
	Bank3	0	0	0	0	0	0
	Bank4	19	32	46	50	46	54
	Bank5	18	17	46	68	46	68
	Bank6	0	0	0	0	0	0
	Bank7	0	0	0	0	0	0
	Bank8	0	0	0	0	0	0

1. Minimum requirement to implement a fully functional 8-bit wide DDR bus. Available DDR interface consists of at least 12 I/Os (1 DQS + 1 DQSB + 8 DQs + 1 DM + Bank VREF1).

LatticeECP2M Power Supply and NC (Cont.)

Signal	672 fpBGA	900 fpBGA
GND ¹	A13, A19, A2, A25, AA2, AA25, AB18, AB22, AB5, AB9, AE1, AE11, AE16, AE22, AE26, AE6, AF13, AF19, AF2, AF25, B1, B11, B16, B22, B26, B6, E18, E22, E5, E9, F2, F25, G11, G16, J22, J5, K11, K13, K14, K16, L10, L11, L16, L17, L2, L20, L25, L7, M13, M14, N10, N12, N13, N14, N15, N17, P10, P12, P13, P14, P15, P17, R13, R14, T10, T11, T16, T17, T2, T20, T25, T7, U11, U13, U14, U16, V22, V5, Y11, Y16	LFE2M50: A1, A13, A18, A24, A30, A7, AA14, AA15, AA16, AA17, AA24, AA27, AA4, AB24, AB7, AD12, AD19, AD27, AE22, AE27, AE4, AE9, AF14, AF17, AF25, AF6, AJ10, AJ21, AJ27, AJ4, AK1, AK13, AK18, AK24, AK30, AK7, B10, B21, B27, B4, D25, D6, E14, E17, F22, F27, F4, F9, G12, G19, J24, J7, K14, K15, K16, K17, K27, K4, L14, L15, L16, L17, M23, M8, N14, N15, N16, N17, N27, N4, P11, P13, P14, P15, P16, P17, P18, P20, R10, R11, R13, R14, R15, R16, R17, R18, R20, R21, R24, R7, T10, T11, T13, T14, T15, T16, T17, T18, T20, T21, T24, T7, U11, U13, U14, U15, U16, U17, U18, U20, V14, V15, V16, V17, V27, V4, W23, W8, Y14, Y15, Y16, Y17 LFE2M70/LFE2M100: A1, A13, A18, A24, A30, A7, AA14, AA15, AA16, AA17, AA24, AA27, AA4, AB24, AB7, AD12, AD19, AD27, AE22, AE27, AE4, AE9, AF14, AF17, AF25, AF6, AJ10, AJ21, AJ27, AJ4, AK1, AK13, AK18, AK24, AK30, AK7, B10, B21, B27, B4, D25, D6, E14, E17, F22, F27, F4, F9, G12, G19, J24, J7, K14, K15, K16, K17, K27, K4, L14, L15, L16, L17, M23, M8, N14, N15, N16, N17, N27, N4, P11, P13, P14, P15, P16, P17, P18, P20, R10, R11, R13, R14, R15, R16, R17, R18, R20, R21, R24, R7, T10, T11, T13, T14, T15, T16, T17, T18, T20, T21, T24, T7, U11, U13, U14, U15, U16, U17, U18, U20, V14, V15, V16, V17, V27, V4, W23, W8, Y14, Y15, Y16, Y17
NC ²	LFE2M35: AB3, AB4, AC1, AC2, AD15, AD18, AD20, AD23, AE13, AE25, AF16, AF22, B4, B5, C26, D20, D21, D22, D23, D24, D25, D26, E20, E21, E25, E26, F20, G20, K10, K17, R4, U10, U23, V10, W7, N7, V7 LFE2M50: AB3, AB4, AC1, AC2, B4, B5, C26, D20, D21, D22, D23, D24, D25, D26, E20, E21, E25, E26, F20, G20, K10, K17, R4, U10, U23, V10, W7, AB21, AC20, AC21, AC22, AC23, AC25, AD26, W20	LFE2M50: G5, G4, K7, K8, E1, F2, F1, G3, G2, G1, L9, L7, K6, K5, L8, L6, AA1, AA2, Y3, AB1, Y9, Y8, Y7, AA7, AB2, AB3, AA5, AA6, AB4, AB5, AA8, AA9, AJ1, AK4, AH6, AH3, AH11, AH8, AK10, AJ13, AB26, AB27, Y24, Y25, AA29, Y28, Y30, Y29, W22, V22, Y27, Y26, W30, W29, W25, W26, L24, L23, D30, D29, K24, K25, J27, K26, J26, H26, H27, G26, H23, H24, D28, E28, J18, J19, H17, J17, F18, F17, B13, A10, C8, C11, C3, C6, A4, B1, AA26, AB11, AB12, AB13, AB14, AB15, AB16, AB17, AB19, AB20, AB21, AC11, AC21, AC22, AD21, AD22, AE23, AF20, AF23, AG23, AG26, F20, F23, G10, G20, G21, H19, H20, H21, H22, J20, J21, R9, U22, W9 LFE2M70/LFE2M100: AA26, AB10, AB11, AB12, AB13, AB14, AB15, AB16, AB17, AB19, AB20, AB21, AB9, AC10, AC11, AC21, AC22, AC8, AC9, AD21, AD22, AD4, AD5, AD6, AD7, AD8, AE23, AE5, AE6, AE7, AF20, AF23, AF5, AG23, AG26, D10, E10, E11, F10, F20, F23, F8, G10, G20, G21, G7, G8, G9, H19, H20, H21, H22, H6, H8, H9, J10, J20, J21, J9, K9, R9, U22, W9

1. All grounds must be electrically connected at the board level. For fpBGA packages, the total number of GND balls is less than the actual number of GND logic connections from the die to the common package GND plane.
2. NC pins should not be connected to any active signals, VCC or GND.
3. For package migration across device densities, the designer must comprehend the package pin requirements for the SERDES blocks. Specifically, the SERDES power pins of the largest density device must be accounted to accommodate migration to other smaller devices using the same package. Please refer to TN1160, [LatticeECP2/M Density Migration](#) for more details.

LFE2-6E/SE and LFE2-12E/SE Logic Signal Connections: 256 fpBGA (Cont.)

LFE2-6E/SE					LFE2-12E/SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
F15	PR11B	2	RDQ10	C	PR11B	2	RDQ10	C
G11	PR12B	2	RDQ10	C (LVDS)*	PR12B	2	RDQ10	C (LVDS)*
F14	PR11A	2	RDQ10	T	PR11A	2	RDQ10	T
VCCIO	VCCIO2	2			VCCIO2	2		
F12	PR12A	2	RDQ10	T (LVDS)*	PR12A	2	RDQ10	T (LVDS)*
G14	PR10B	2	RDQ10	C (LVDS)*	PR10B	2	RDQ10	C (LVDS)*
G13	PR10A	2	RDQS10	T (LVDS)*	PR10A	2	RDQS10	T (LVDS)*
GND	GNDIO2	-			GNDIO2	-		
F16	PR8B	2	RDQ10	C (LVDS)*	PR8B	2	RDQ10	C (LVDS)*
F9	PR9B	2	RDQ10	C	PR9B	2	RDQ10	C
E16	PR8A	2	RDQ10	T (LVDS)*	PR8A	2	RDQ10	T (LVDS)*
F10	PR9A	2	RDQ10	T	PR9A	2	RDQ10	T
VCCIO	VCCIO2	2			VCCIO2	2		
D16	PR7B	2	RDQ10	C	PR7B	2	RDQ10	C
D15	PR7A	2	RDQ10	T	PR7A	2	RDQ10	T
C15	PR4B	2		C (LVDS)*	PR4B	2		C (LVDS)*
C16	PR5B	2		C	PR5B	2		C
GND	GNDIO2	-			GNDIO2	-		
D14	PR4A	2		T (LVDS)*	PR4A	2		T (LVDS)*
B16	PR5A	2		T	PR5A	2		T
F13	PR2B	2	VREF2_2	C (LVDS)*	PR2B	2	VREF2_2	C (LVDS)*
VCCIO	VCCIO2	2			VCCIO2	2		
E13	PR2A	2	VREF1_2	T (LVDS)*	PR2A	2	VREF1_2	T (LVDS)*
F11	PT28B	1	VREF2_1	C	PT55B	1	VREF2_1	C
E11	PT28A	1	VREF1_1	T	PT55A	1	VREF1_1	T
GND	GNDIO1	-			GNDIO1	-		
A15	PT27B	1		C	PT54B	1		C
E12	PT26B	1		C	PT53B	1		C
B15	PT27A	1		T	PT54A	1		T
VCCIO	VCCIO1	1			VCCIO1	1		
D12	PT26A	1		T	PT53A	1		T
B14	PT25B	1		C	PT52B	1		C
C14	PT24B	1		C	PT51B	1		C
A14	PT25A	1		T	PT52A	1		T
D13	PT24A	1		T	PT51A	1		T
C13	PT23B	1		C	PT50B	1		C
GND	GNDIO1	-			GNDIO1	-		
A13	PT22B	1		C	PT49B	1		C
B13	PT23A	1		T	PT50A	1		T
VCCIO	VCCIO1	1			VCCIO1	1		
A12	PT22A	1		T	PT49A	1		T
B11	PT21B	1		C	PT48B	1		C
D11	PT20B	1		C	PT47B	1		C
A11	PT21A	1		T	PT48A	1		T
C11	PT20A	1		T	PT47A	1		T

LFE2-20E/SE and LFE2-35E/SE Logic Signal Connections: 672 fpBGA (Cont.)

LFE2-20E/20SE					LFE2-35E/35SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
A2	GND	-			GND	-		
A25	GND	-			GND	-		
AA18	GND	-			GND	-		
AA24	GND	-			GND	-		
AA3	GND	-			GND	-		
AA9	GND	-			GND	-		
AD11	GND	-			GND	-		
AD16	GND	-			GND	-		
AD21	GND	-			GND	-		
AD6	GND	-			GND	-		
AE1	GND	-			GND	-		
AE26	GND	-			GND	-		
AF2	GND	-			GND	-		
AF25	GND	-			GND	-		
B1	GND	-			GND	-		
B26	GND	-			GND	-		
C11	GND	-			GND	-		
C16	GND	-			GND	-		
C21	GND	-			GND	-		
C6	GND	-			GND	-		
F18	GND	-			GND	-		
F24	GND	-			GND	-		
F3	GND	-			GND	-		
F9	GND	-			GND	-		
J13	GND	-			GND	-		
J14	GND	-			GND	-		
J21	GND	-			GND	-		
J6	GND	-			GND	-		
K10	GND	-			GND	-		
K11	GND	-			GND	-		
K13	GND	-			GND	-		
K14	GND	-			GND	-		
K16	GND	-			GND	-		
K17	GND	-			GND	-		
L10	GND	-			GND	-		
L11	GND	-			GND	-		
L16	GND	-			GND	-		
L17	GND	-			GND	-		
L24	GND	-			GND	-		
L3	GND	-			GND	-		
M13	GND	-			GND	-		
M14	GND	-			GND	-		
N10	GND	-			GND	-		
N12	GND	-			GND	-		
N13	GND	-			GND	-		
N14	GND	-			GND	-		

LFE2-50E/SE and LFE2-70E/SE Logic Signal Connections: 672 fpBGA (Cont.)

LFE2-50E/SE					LFE2-70E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential	
U24	PR63B	3	RLM0_GPLL_C_IN_A**/RDQ67	C (LVDS)*	PR76B	3	RLM0_GPLL_C_IN_A**/RDQ80	C (LVDS)*	
U25	PR63A	3	RLM0_GPLL_T_IN_A**/RDQ67	T (LVDS)*	PR76A	3	RLM0_GPLL_T_IN_A**/RDQ80	T (LVDS)*	
R20	RLM0_PLLCAP	3			RLM0_PLLCAP	3			
P18	VCCPLL	3			VCCPLL	-			
T19	PR61B	3	RLM0_GDLLC_FB_A/RDQ58	C	PR74B	3	RLM0_GDLLC_FB_A/RDQ71	C	
U20	PR61A	3	RLM0_GDLLT_FB_A/RDQ58	T	PR74A	3	RLM0_GDLLT_FB_A/RDQ71	T	
GND	GNDIO3	-			GNDIO3	-			
T25	PR60B	3	RLM0_GDLLC_IN_A**/RDQ58	C (LVDS)*	PR73B	3	RLM0_GDLLC_IN_A**/RDQ71	C (LVDS)*	
T26	PR60A	3	RLM0_GDLLT_IN_A**/RDQ58	T (LVDS)*	PR73A	3	RLM0_GDLLT_IN_A**/RDQ71	T (LVDS)*	
T20	PR59B	3	RDQ58	C	PR72B	3	RDQ71	C	
T22	PR59A	3	RDQ58	T	PR72A	3	RDQ71	T	
VCCIO	VCCIO3	3			VCCIO3	3			
R26	PR58B	3	RDQ58	C (LVDS)*	PR71B	3	RDQ71	C (LVDS)*	
R25	PR58A	3	RDQS58	T (LVDS)*	PR71A	3	RDQS71	T (LVDS)*	
R22	PR57B	3	RDQ58	C	PR70B	3	RDQ71	C	
GND	GNDIO3	-			GNDIO3	-			
T21	PR57A	3	RDQ58	T	PR70A	3	RDQ71	T	
P26	PR56B	3	RDQ58	C (LVDS)*	PR69B	3	RDQ71	C (LVDS)*	
P25	PR56A	3	RDQ58	T (LVDS)*	PR69A	3	RDQ71	T (LVDS)*	
R24	PR55B	3	RDQ58	C	PR68B	3	RDQ71	C	
VCCIO	VCCIO3	3			VCCIO3	3			
R23	PR55A	3	RDQ58	T	PR68A	3	RDQ71	T	
P20	PR54B	3	RDQ58	C (LVDS)*	PR67B	3	RDQ71	C (LVDS)*	
R19	PR54A	3	RDQ58	T (LVDS)*	PR67A	3	RDQ71	T (LVDS)*	
P21	PR53B	3	RDQ50	C	PR66B	3	RDQ63	C	
GND	GNDIO3	-			GNDIO3	-			
P19	PR53A	3	RDQ50	T	PR66A	3	RDQ63	T	
P23	PR52B	3	RDQ50	C (LVDS)*	PR65B	3	RDQ63	C (LVDS)*	
P22	PR52A	3	RDQ50	T (LVDS)*	PR65A	3	RDQ63	T (LVDS)*	
N22	PR51B	3	RDQ50	C	PR64B	3	RDQ63	C	
VCCIO	VCCIO3	3			VCCIO3	3			
R21	PR51A	3	RDQ50	T	PR64A	3	RDQ63	T	
N26	PR50B	3	RDQ50	C (LVDS)*	PR63B	3	RDQ63	C (LVDS)*	
N25	PR50A	3	RDQS50	T (LVDS)*	PR63A	3	RDQS63	T (LVDS)*	
GND	GNDIO3	-			GNDIO3	-			
N19	PR49B	3	RDQ50	C	PR62B	3	RDQ63	C	
N20	PR49A	3	RDQ50	T	PR62A	3	RDQ63	T	
M26	PR48B	3	RDQ50	C (LVDS)*	PR61B	3	RDQ63	C (LVDS)*	
M25	PR48A	3	RDQ50	T (LVDS)*	PR61A	3	RDQ63	T (LVDS)*	
VCCIO	VCCIO3	3			VCCIO3	3			
N18	PR47B	3	VREF2_3/RDQ50	C	PR60B	3	VREF2_3/RDQ63	C	
N21	PR47A	3	VREF1_3/RDQ50	T	PR60A	3	VREF1_3/RDQ63	T	
L26	PR46B	3	PCLKC3_0/RDQ50	C (LVDS)*	PR59B	3	PCLKC3_0/RDQ63	C (LVDS)*	
L25	PR46A	3	PCLKT3_0/RDQ50	T (LVDS)*	PR59A	3	PCLKT3_0/RDQ63	T (LVDS)*	
N24	PR44B	2	PCLKC2_0/RDQ41	C	PR57B	2	PCLKC2_0/RDQ54	C	
M23	PR44A	2	PCLKT2_0/RDQ41	T	PR57A	2	PCLKT2_0/RDQ54	T	

LFE2-50E/SE and LFE2-70E/SE Logic Signal Connections: 672 fpBGA (Cont.)

LFE2-50E/SE					LFE2-70E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential	
D4	PT7B	0		C	PT7B	0		C	
D3	PT7A	0		T	PT7A	0		T	
C2	PT6B	0		C	PT6B	0		C	
C1	PT6A	0		T	PT6A	0		T	
G8	PT5B	0		C	PT5B	0		C	
GND	GNDIO0	-			GNDIO0	-			
G7	PT5A	0		T	PT5A	0		T	
E7	PT4B	0		C	PT4B	0		C	
VCCIO	VCCIO0	0			VCCIO0	0			
F7	PT4A	0		T	PT4A	0		T	
E6	PT3B	0		C	PT3B	0		C	
E5	PT3A	0		T	PT3A	0		T	
G6	PT2B	0	VREF2_0	C	PT2B	0	VREF2_0	C	
G5	PT2A	0	VREF1_0	T	PT2A	0	VREF1_0	T	
L12	VCC	-			VCC	-			
L13	VCC	-			VCC	-			
L14	VCC	-			VCC	-			
L15	VCC	-			VCC	-			
M11	VCC	-			VCC	-			
M12	VCC	-			VCC	-			
M15	VCC	-			VCC	-			
M16	VCC	-			VCC	-			
N11	VCC	-			VCC	-			
N16	VCC	-			VCC	-			
P11	VCC	-			VCC	-			
P16	VCC	-			VCC	-			
R11	VCC	-			VCC	-			
R12	VCC	-			VCC	-			
R15	VCC	-			VCC	-			
R16	VCC	-			VCC	-			
T12	VCC	-			VCC	-			
T13	VCC	-			VCC	-			
T14	VCC	-			VCC	-			
T15	VCC	-			VCC	-			
D11	VCCIO0	0			VCCIO0	0			
D6	VCCIO0	0			VCCIO0	0			
G9	VCCIO0	0			VCCIO0	0			
K12	VCCIO0	0			VCCIO0	0			
J12	VCCIO0	0			VCCIO0	0			
D16	VCCIO1	1			VCCIO1	1			
D21	VCCIO1	1			VCCIO1	1			
G18	VCCIO1	1			VCCIO1	1			
J15	VCCIO1	1			VCCIO1	1			
K15	VCCIO1	1			VCCIO1	1			
F23	VCCIO2	2			VCCIO2	2			
J20	VCCIO2	2			VCCIO2	2			

LFE2-70E/SE Logic Signal Connections: 900 fpBGA (Cont.)

LFE2-70E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential
AD18	PB66A	4	BDQ69	T
AF18	PB66B	4	BDQ69	C
AC18	PB67A	4	BDQ69	T
AE18	PB67B	4	BDQ69	C
VCCIO	VCCIO4	4		
AG19	PB68A	4	BDQ69	T
AH19	PB68B	4	BDQ69	C
GND	GNDIO4	-		
AE19	PB69A	4	BDQS69	T
AF19	PB69B	4	BDQ69	C
AC19	PB70A	4	BDQ69	T
AD19	PB70B	4	BDQ69	C
AJ19	PB71A	4	BDQ69	T
AK19	PB71B	4	BDQ69	C
VCCIO	VCCIO4	4		
AF20	PB72A	4	BDQ69	T
AH20	PB72B	4	BDQ69	C
AE20	PB73A	4	BDQ69	T
AG20	PB73B	4	BDQ69	C
GND	GNDIO4	-		
AD20	PB74A	4	BDQ78	T
AC20	PB74B	4	BDQ78	C
AH21	PB75A	4	BDQ78	T
AF21	PB75B	4	BDQ78	C
AJ20	PB76A	4	BDQ78	T
VCCIO	VCCIO4	4		
AK20	PB76B	4	BDQ78	C
AG21	PB77A	4	BDQ78	T
AE21	PB77B	4	BDQ78	C
AD21	PB78A	4	BDQS78	T
GND	GNDIO4	-		
AC21	PB78B	4	BDQ78	C
AD22	PB79A	4	BDQ78	T
AB21	PB79B	4	BDQ78	C
AJ21	PB80A	4	BDQ78	T
VCCIO	VCCIO4	4		
AK21	PB80B	4	BDQ78	C
GND	GNDIO4	-		
VCCIO	VCCIO4	4		
AJ25	PB87A	4	BDQS87***	T
AK24	PB87B	4	BDQ87	C
AJ24	PB88A	4	BDQ87	T
AK25	PB88B	4	BDQ87	C

LFE2-70E/SE Logic Signal Connections: 900 fpBGA (Cont.)

LFE2-70E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential
K28	PR25A	2	RDQ29	T (LVDS)*
J24	PR24B	2	RDQ21	C
J26	PR24A	2	RDQ21	T
GND	GNDIO2	-		
K29	PR23B	2	RDQ21	C (LVDS)*
K30	PR23A	2	RDQ21	T (LVDS)*
J23	PR22B	2	RDQ21	C
J25	PR22A	2	RDQ21	T
VCCIO	VCCIO2	99		
J27	PR21B	2	RDQ21	C (LVDS)*
J28	PR21A	2	RDQS21	T (LVDS)*
H26	PR20B	2	RDQ21	C
GND	GNDIO2	-		
H24	PR20A	2	RDQ21	T
J29	PR19B	2	RDQ21	C (LVDS)*
J30	PR19A	2	RDQ21	T (LVDS)*
H25	PR18B	2	RDQ21	C
VCCIO	VCCIO2	2		
H23	PR18A	2	RDQ21	T
G27	PR15B	2	RUM1_SPLLC_FB_A/RDQ12	C
GND	GNDIO2	-		
H27	PR15A	2	RUM1_SPLLT_FB_A/RDQ12	T
G29	PR14B	2	RUM1_SPLLC_IN_A/RDQ12	C (LVDS)*
G28	PR14A	2	RUM1_SPLLT_IN_A/RDQ12	T (LVDS)*
VCCIO	VCCIO2	2		
GND	GNDIO2	-		
G26	PR6B	2		C (LVDS)*
G25	PR6A	2		T (LVDS)*
G30	PR5B	2		C
F30	PR5A	2		T
VCCIO	VCCIO2	2		
F26	PR4B	2		C (LVDS)*
F27	PR4A	2		T (LVDS)*
F29	PR3B	2		C
GND	GNDIO2	-		
F28	PR3A	2		T
H29	PR2B	2	VREF2_2	C (LVDS)*
H30	PR2A	2	VREF1_2	T (LVDS)*
VCCIO	VCCIO2	2		
B26	PT100B	1	VREF2_1	C
A26	PT100A	1	VREF1_1	T
GND	GNDIO1	-		
C25	PT99B	1		C

LFE2M20E/SE and LFE2M35E/SE Logic Signal Connections: 484 fpBGA (Cont.)

LFE2M20E/SE					LFE2M35E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential	
GNDIO	GNDIO0	-			GNDIO0	-			
F7	PT9B	0		C	PT9B	0		C	
G7	PT9A	0		T	PT9A	0		T	
C3	PT8B	0		C	PT8B	0		C	
D4	PT8A	0		T	PT8A	0		T	
VCCIO	VCCIO0	0			VCCIO0	0			
F6	PT7B	0		C	PT7B	0		C	
E6	PT7A	0		T	PT7A	0		T	
E5	PT6B	0		C	PT6B	0		C	
D6	PT6A	0		T	PT6A	0		T	
GNDIO	GNDIO0	-			GNDIO0	-			
D3	PT5B	0		C	PT5B	0		C	
E3	PT5A	0		T	PT5A	0		T	
D5	PT4B	0		C	PT4B	0		C	
E4	PT4A	0		T	PT4A	0		T	
VCCIO	VCCIO0	0			VCCIO0	0			
C2	PT3B	0		C	PT3B	0		C	
B2	PT3A	0		T	PT3A	0		T	
B1	PT2B	0		C	PT2B	0		C	
C1	PT2A	0		T	PT2A	0		T	
R8	VCCPLL	-			VCCPLL	-			
H15	VCCPLL	-			VCCPLL	-			
H8	VCCPLL	-			VCCPLL	-			
R15	VCCPLL	-			VCCPLL	-			
J10	VCC	-			VCC	-			
J11	VCC	-			VCC	-			
J12	VCC	-			VCC	-			
J13	VCC	-			VCC	-			
K14	VCC	-			VCC	-			
K9	VCC	-			VCC	-			
L14	VCC	-			VCC	-			
L9	VCC	-			VCC	-			
M14	VCC	-			VCC	-			
M9	VCC	-			VCC	-			
N14	VCC	-			VCC	-			
N9	VCC	-			VCC	-			
P10	VCC	-			VCC	-			
P11	VCC	-			VCC	-			
P12	VCC	-			VCC	-			
P13	VCC	-			VCC	-			
B5	VCCIO0	0			VCCIO0	0			
B9	VCCIO0	0			VCCIO0	0			
E7	VCCIO0	0			VCCIO0	0			
H9	VCCIO0	0			VCCIO0	0			
D13	VCCIO1	1			VCCIO1	1			
E16	VCCIO1	1			VCCIO1	1			
H14	VCCIO1	1			VCCIO1	1			
E21	VCCIO2	2			VCCIO2	2			

LFE2M50E/SE Logic Signal Connections: 484 fpBGA

LFE2M50E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential
D1	PL2A	7	LDQ6	T (LVDS)*
E1	PL2B	7	LDQ6	C (LVDS)*
F1	PL3A	7	LDQ6	T
F2	PL3B	7	LDQ6	C
F5	PL4A	7	LDQ6	T (LVDS)*
VCCIO	VCCIO7	7		
G6	PL4B	7	LDQ6	C (LVDS)*
F4	PL5A	7	LDQ6	T
F3	PL5B	7	LDQ6	C
G1	PL6A	7	LDQS6	T (LVDS)*
GNDIO	GNDIO7	-		
G2	PL6B	7	LDQ6	C (LVDS)*
H1	PL7A	7	LDQ6	T
H2	PL7B	7	LDQ6	C
VCCIO	VCCIO7	7		
H7	PL8A	7	LDQ6	T (LVDS)*
H6	PL8B	7	LDQ6	C (LVDS)*
G3	PL9A	7	VREF2_7/LDQ6	T
H3	PL9B	7	VREF1_7/LDQ6	C
GNDIO	GNDIO7	-		
VCCIO	VCCIO7	7		
H5	PL11A	7	LUM0_SPLLT_IN_A	T (LVDS)*
H4	PL11B	7	LUM0_SPLLC_IN_A	C (LVDS)*
J1	PL12A	7	LUM0_SPLLT_FB_A	T
J2	PL12B	7	LUM0_SPLLC_FB_A	C
GNDIO	GNDIO7	-		
J3	PL13A	7		T (LVDS)*
J4	PL13B	7		C (LVDS)*
J7	PL14A	7		T
VCCIO	VCCIO7	7		
J6	PL14B	7		C
GNDIO	GNDIO7	-		
VCCIO	VCCIO7	7		
K1	PL32A	7	LUM3_SPLLT_IN_A/LDQ36	T (LVDS)*
K2	PL32B	7	LUM3_SPLLC_IN_A/LDQ36	C (LVDS)*
J5	PL33A	7	LUM3_SPLLT_FB_A/LDQ36	T
K5	PL33B	7	LUM3_SPLLC_FB_A/LDQ36	C
VCCIO	VCCIO7	7		
K7	PL34A	7	LDQ36	T (LVDS)*
K6	PL34B	7	LDQ36	C (LVDS)*
L6	PL35A	7	LDQ36	T
L7	PL35B	7	LDQ36	C

LFE2M50E/SE Logic Signal Connections: 484 fpBGA (Cont.)

LFE2M50E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential
Y6	PB8A	5	BDQ6	T
Y5	PB8B	5	BDQ6	C
VCCIO	VCCIO5	5		
AB3	PB9A	5	BDQ6	T
AB4	PB9B	5	BDQ6	C
AB5	PB10A	5	BDQ6	T
AA6	PB10B	5	BDQ6	C
GNDIO	GNDIO5	-		
VCCIO	VCCIO5	5		
V9	PB40A	5	BDQ42	T
U9	PB40B	5	BDQ42	C
VCCIO	VCCIO5	5		
U10	PB41A	5	BDQ42	T
T10	PB41B	5	BDQ42	C
GNDIO	GNDIO5	-		
W9	PB42A	5	BDQS42****	T
Y8	PB42B	5	BDQ42	C
AA7	PB43A	5	VREF2_5/BDQ42	T
Y7	PB43B	5	VREF1_5/BDQ42	C
AB6	PB44A	5	PCLKT5_0/BDQ42	T
AB7	PB44B	5	PCLKC5_0/BDQ42	C
VCCIO	VCCIO5	5		
GNDIO	GNDIO5	-		
AA8	PB49A	4	PCLKT4_0/BDQ51	T
VCCIO	VCCIO4	4		
AB8	PB49B	4	PCLKC4_0/BDQ51	C
AA9	PB50A	4	VREF2_4/BDQ51	T
Y9	PB50B	4	VREF1_4/BDQ51	C
AB9	PB51A	4	BDQS51****	T
GNDIO	GNDIO4	-		
AB10	PB51B	4	BDQ51	C
AA10	PB52A	4	BDQ51	T
Y11	PB52B	4	BDQ51	C
VCCIO	VCCIO4	4		
GNDIO	GNDIO4	-		
V10	PB56A	4	BDQ60	T
U11	PB56B	4	BDQ60	C
V11	PB57A	4	BDQ60	T
W11	PB57B	4	BDQ60	C
AA11	PB58A	4	BDQ60	T
AB11	PB58B	4	BDQ60	C
VCCIO	VCCIO4	4		
T11	PB59A	4	BDQ60	T

LFE2M50E/SE and LFE2M70E/SE Logic Signal Connections: 900 fpBGA (Cont.)

LFE2M50E/SE					LFE2M70E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential	
-	-	-			VCCIO2	2			
H23	NC	-			PR15B	2	RDQ15	C (LVDS)*	
H24	NC	-			PR15A	2	RDQS15	T (LVDS)*	
D28	NC	-			PR14B	2	RDQ15	C	
-	-	-			GNDIO2	-			
E28	NC	-			PR14A	2	RDQ15	T	
G24	PR13B	2		C (LVDS)*	PR13B	2	RDQ15	C (LVDS)*	
H25	PR13A	2		T (LVDS)*	PR13A	2	RDQ15	T (LVDS)*	
D27	PR12B	2	RUM0_SPLLC_FB_A	C	PR12B	2	RUM0_SPLLC_FB_A/RDQ15	C	
GNDIO	GNDIO2	-			VCCIO2	2			
E27	PR12A	2	RUM0_SPLLT_FB_A	T	PR12A	2	RUM0_SPLLT_FB_A/RDQ15	T	
F26	PR11B	2	RUM0_SPLLC_IN_A	C (LVDS)*	PR11B	2	RUM0_SPLLC_IN_A/RDQ15	C (LVDS)*	
G25	PR11A	2	RUM0_SPLLT_IN_A	T (LVDS)*	PR11A	2	RUM0_SPLLT_IN_A/RDQ15	T (LVDS)*	
F24	PR9B	2	VREF2_2	C	PR9B	2	VREF2_2	C	
VCCIO	VCCIO2	-			-	-			
GNDIO	GNDIO2	-			GNDIO2	-			
F25	PR9A	2	VREF1_2	T	PR9A	2	VREF1_2	T	
VCCIO	VCCIO2	2			VCCIO2	2			
G23	XRES	-			XRES	1			
C30	URC_SQ_VCCR_X0	12			URC_SQ_VCCR_X0	12			
A29	URC_SQ_HDIN_P0	12		T	URC_SQ_HDIN_P0	12		T	
B30	URC_SQ_VCCIB0	12			URC_SQ_VCCIB0	12			
B29	URC_SQ_HDINN0	12		C	URC_SQ_HDINN0	12		C	
C27	URC_SQ_VCCTX0	12			URC_SQ_VCCTX0	12			
A26	URC_SQ_HDOUT_P0	12		T	URC_SQ_HDOUT_P0	12		T	
A27	URC_SQ_VCCOB0	12			URC_SQ_VCCOB0	12			
B26	URC_SQ_HDOUTN0	12		C	URC_SQ_HDOUTN0	12		C	
C26	URC_SQ_VCCTX1	12			URC_SQ_VCCTX1	12			
B25	URC_SQ_HDOUTN1	12		C	URC_SQ_HDOUTN1	12		C	
C25	URC_SQ_VCCOB1	12			URC_SQ_VCCOB1	12			
A25	URC_SQ_HDOUT_P1	12		T	URC_SQ_HDOUT_P1	12		T	
C29	URC_SQ_VCCR_X1	12			URC_SQ_VCCR_X1	12			
B28	URC_SQ_HDINN1	12		C	URC_SQ_HDINN1	12		C	
C28	URC_SQ_VCCIB1	12			URC_SQ_VCCIB1	12			
A28	URC_SQ_HDIN_P1	12		T	URC_SQ_HDIN_P1	12		T	
B24	URC_SQ_VCCAUX33	12			URC_SQ_VCCAUX33	12			
E24	URC_SQ_REFCLK_N	12		C	URC_SQ_REFCLK_N	12		C	
D24	URC_SQ_REFCLK_P	12		T	URC_SQ_REFCLK_P	12		T	
C24	URC_SQ_VCCP	12			URC_SQ_VCCP	12			
A20	URC_SQ_HDIN_P2	12		T	URC_SQ_HDIN_P2	12		T	
C20	URC_SQ_VCCIB2	12			URC_SQ_VCCIB2	12			
B20	URC_SQ_HDINN2	12		C	URC_SQ_HDINN2	12		C	
C19	URC_SQ_VCCR_X2	12			URC_SQ_VCCR_X2	12			
A23	URC_SQ_HDOUT_P2	12		T	URC_SQ_HDOUT_P2	12		T	
C23	URC_SQ_VCCOB2	12			URC_SQ_VCCOB2	12			
B23	URC_SQ_HDOUTN2	12		C	URC_SQ_HDOUTN2	12		C	
C22	URC_SQ_VCCTX2	12			URC_SQ_VCCTX2	12			
B22	URC_SQ_HDOUTN3	12		C	URC_SQ_HDOUTN3	12		C	

LFE2M50E/SE and LFE2M70E/SE Logic Signal Connections: 900 fpBGA (Cont.)

LFE2M50E/SE					LFE2M70E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential	
G7	PL8A	7	LDQ6	T (LVDS)*	NC	-			
G8	PL6A	7	LDQS6****	T (LVDS)*	NC	-			
G9	PL5A	7	LDQ6	T	NC	-			
H19	NC	-			NC	-			
H20	NC	-			NC	-			
H21	NC	-			NC	-			
H22	NC	-			NC	-			
H6	PL8B	7	LDQ6	C (LVDS)*	NC	-			
H8	PL5B	7	LDQ6	C	NC	-			
H9	PL2A	7	LDQ6	T (LVDS)*	NC	-			
J10	PL2B	7	LDQ6	C (LVDS)*	NC	-			
J20	NC	-			NC	-			
J21	NC	-			NC	-			
J9	PL4A	7	LDQ6	T (LVDS)*	NC	-			
K9	PL4B	7	LDQ6	C (LVDS)*	NC	-			
R9	NC	-			NC	-			
U22	NC	-			NC	-			
W9	NC	-			NC	-			
N13	VCCPLL	-			VCCPLL	-			
N18	VCCPLL	-			VCCPLL	-			
V13	VCCPLL	-			VCCPLL	-			
V18	VCCPLL	-			VCCPLL	-			

* Supports true LVDS. Other differential signals must be emulated with external resistors.

** These dedicated input pins can be used for GPLLs or GDLLs within the respective quadrant.

*** These sysCONFIG pins are dedicated I/O pins for configuration. The outputs are actively driven during normal device operation.

****Due to packaging bond out option, this DQS does not have all the necessary DQ pins bonded out for a full 8-bit data width.

Note: VCCIO and GND pads are used to determine the average DC current drawn by I/Os between GND/VCCIO connections, or between the last GND/VCCIO in an I/O bank and the end of an I/O bank. The substrate pads listed in the Pin Table do not necessarily have a one to one connection with a package ball or pin.

LFE2M100E/SE Logic Signal Connections: 900 fpBGA (Cont.)

LFE2M100E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential
AC19	PB96A	4	BDQS96	T
AD20	PB96B	4	BDQ96	C
AB18	PB97A	4	BDQ96	T
AC20	PB97B	4	BDQ96	C
AE20	PB98A	4	BDQ96	T
AE21	PB98B	4	BDQ96	C
VCCIO	VCCIO4	4		
AC23	PB99A	4	BDQ96	T
AD23	PB99B	4	BDQ96	C
GNDIO	GNDIO4	-		
AH18	LRC_SQ_VCCR3	13		
AK19	LRC_SQ_HDINP3	13		T
AJ18	LRC_SQ_VCCIB3	13		
AJ19	LRC_SQ_HDINN3	13		C
AH21	LRC_SQ_VCCTX3	13		
AK22	LRC_SQ_HDOUTP3	13		T
AK21	LRC_SQ_VCCOB3	13		
AJ22	LRC_SQ_HDOUTN3	13		C
AH22	LRC_SQ_VCCTX2	13		
AJ23	LRC_SQ_HDOUTN2	13		C
AH23	LRC_SQ_VCCOB2	13		
AK23	LRC_SQ_HDOUTP2	13		T
AH19	LRC_SQ_VCCR2	13		
AJ20	LRC_SQ_HDINN2	13		C
AH20	LRC_SQ_VCCIB2	13		
AK20	LRC_SQ_HDINP2	13		T
AH24	LRC_SQ_VCCP	13		
AG24	LRC_SQ_REFCLKP	13		T
AF24	LRC_SQ_REFCLKN	13		C
AJ24	LRC_SQ_VCCAUX33	13		
AK28	LRC_SQ_HDINP1	13		T
AH28	LRC_SQ_VCCIB1	13		
AJ28	LRC_SQ_HDINN1	13		C
AH29	LRC_SQ_VCCR1	13		
AK25	LRC_SQ_HDOUTP1	13		T
AH25	LRC_SQ_VCCOB1	13		
AJ25	LRC_SQ_HDOUTN1	13		C
AH26	LRC_SQ_VCCTX1	13		
AJ26	LRC_SQ_HDOUTN0	13		C
AK27	LRC_SQ_VCCOB0	13		
AK26	LRC_SQ_HDOUTP0	13		T
AH27	LRC_SQ_VCCTX0	13		
AJ29	LRC_SQ_HDINN0	13		C

LFE2M100E/SE Logic Signal Connections: 900 fpBGA (Cont.)

LFE2M100E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential
VCCIO	VCCIO3	3		
T22	PR69A	3	RDQ72	T
T29	PR68B	3	RDQ72	C (LVDS)*
T28	PR68A	3	RDQ72	T (LVDS)*
R23	PR66B	3	RLM4_SPLLC_FB_A/RDQ63	C
GNDIO	GNDIO3	-		
-	-	-		
R22	PR66A	3	RLM4_SPLLT_FB_A/RDQ63	T
P30	PR65B	3	RLM4_SPLLC_IN_A/RDQ63	C (LVDS)*
R29	PR65A	3	RLM4_SPLLT_IN_A/RDQ63	T (LVDS)*
T27	PR64B	3	RDQ63	C
VCCIO	VCCIO3	3		
T26	PR64A	3	RDQ63	T
GNDIO	GNDIO3	-		
N30	PR61B	3	RDQ63	C (LVDS)*
N29	PR61A	3	RDQ63	T (LVDS)*
VCCIO	VCCIO3	3		
R27	PR60B	3	VREF2_3/RDQ63	C
R28	PR60A	3	VREF1_3/RDQ63	T
P29	PR59B	3	PCLKC3_0/RDQ63	C (LVDS)*
P28	PR59A	3	PCLKT3_0/RDQ63	T (LVDS)*
M30	PR57B	2	PCLKC2_0/RDQ54	C
M29	PR57A	2	PCLKT2_0/RDQ54	T
GNDIO	GNDIO2	-		
P23	PR56B	2	RDQ54	C (LVDS)*
P24	PR56A	2	RDQ54	T (LVDS)*
R26	PR55B	2	RDQ54	C
P27	PR55A	2	RDQ54	T
VCCIO	VCCIO2	2		
P25	PR54B	2	RDQ54	C (LVDS)*
P26	PR54A	2	RDQS54	T (LVDS)*
K30	PR53B	2	RDQ54	C
GNDIO	GNDIO2	-		
K29	PR53A	2	RDQ54	T
N22	PR52B	2	RDQ54	C (LVDS)*
P22	PR52A	2	RDQ54	T (LVDS)*
J30	PR51B	2	RUM3_SPLLC_FB_A/RDQ54	C
VCCIO	VCCIO2	2		
J29	PR51A	2	RUM3_SPLLT_FB_A/RDQ54	T
N24	PR50B	2	RUM3_SPLLC_IN_A/RDQ54	C (LVDS)*
N23	PR50A	2	RUM3_SPLLT_IN_A/RDQ54	T (LVDS)*
N25	PR48B	2	RDQ45	C
N26	PR48A	2	RDQ45	T

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2-35SE-5F484C	331	1.2V	-5	fpBGA	484	Com	35
LFE2-35SE-6F484C	331	1.2V	-6	fpBGA	484	Com	35
LFE2-35SE-7F484C	331	1.2V	-7	fpBGA	484	Com	35
LFE2-35SE-5F672C	450	1.2V	-5	fpBGA	672	Com	35
LFE2-35SE-6F672C	450	1.2V	-6	fpBGA	672	Com	35
LFE2-35SE-7F672C	450	1.2V	-7	fpBGA	672	Com	35

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2-50SE-5F484C	339	1.2V	-5	fpBGA	484	Com	50
LFE2-50SE-6F484C	339	1.2V	-6	fpBGA	484	Com	50
LFE2-50SE-7F484C	339	1.2V	-7	fpBGA	484	Com	50
LFE2-50SE-5F672C	500	1.2V	-5	fpBGA	672	Com	50
LFE2-50SE-6F672C	500	1.2V	-6	fpBGA	672	Com	50
LFE2-50SE-7F672C	500	1.2V	-7	fpBGA	672	Com	50

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2-70SE-5F672C	500	1.2V	-5	fpBGA	672	Com	70
LFE2-70SE-6F672C	500	1.2V	-6	fpBGA	672	Com	70
LFE2-70SE-7F672C	500	1.2V	-7	fpBGA	672	Com	70
LFE2-70SE-5F900C	583	1.2V	-5	fpBGA	900	Com	70
LFE2-70SE-6F900C	583	1.2V	-6	fpBGA	900	Com	70
LFE2-70SE-7F900C	583	1.2V	-7	fpBGA	900	Com	70

Industrial

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2-6SE-5T144I	90	1.2V	-5	TQFP	144	Ind	6
LFE2-6SE-6T144I	90	1.2V	-6	TQFP	144	Ind	6
LFE2-6SE-5F256I	190	1.2V	-5	fpBGA	256	Ind	6
LFE2-6SE-6F256I	190	1.2V	-6	fpBGA	256	Ind	6

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2-12SE-5T144I	93	1.2V	-5	TQFP	144	Ind	12
LFE2-12SE-6T144I	93	1.2V	-6	TQFP	144	Ind	12
LFE2-12SE-5Q208I	131	1.2V	-5	PQFP	208	Ind	12
LFE2-12SE-6Q208I	131	1.2V	-6	PQFP	208	Ind	12
LFE2-12SE-5F256I	193	1.2V	-5	fpBGA	256	Ind	12
LFE2-12SE-6F256I	193	1.2V	-6	fpBGA	256	Ind	12
LFE2-12SE-5F484I	297	1.2V	-5	fpBGA	484	Ind	12
LFE2-12SE-6F484I	297	1.2V	-6	fpBGA	484	Ind	12

Industrial

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2M20SE-5F484I	304	1.2V	-5	fpBGA	484	Ind	20
LFE2M20SE-6F484I	304	1.2V	-6	fpBGA	484	Ind	20
LFE2M20SE-5F256I	140	1.2V	-5	fpBGA	256	Ind	20
LFE2M20SE-6F256I	140	1.2V	-6	fpBGA	256	Ind	20

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2M35SE-5F672I	410	1.2V	-5	fpBGA	672	Ind	35
LFE2M35SE-6F672I	410	1.2V	-6	fpBGA	672	Ind	35
LFE2M35SE-5F484I	303	1.2V	-5	fpBGA	484	Ind	35
LFE2M35SE-6F484I	303	1.2V	-6	fpBGA	484	Ind	35
LFE2M35SE-5F256I	140	1.2V	-5	fpBGA	256	Ind	35
LFE2M35SE-6F256I	140	1.2V	-6	fpBGA	256	Ind	35

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2M50SE-5F900I	410	1.2V	-5	fpBGA	900	Ind	50
LFE2M50SE-6F900I	410	1.2V	-6	fpBGA	900	Ind	50
LFE2M50SE-5F672I	372	1.2V	-5	fpBGA	672	Ind	50
LFE2M50SE-6F672I	372	1.2V	-6	fpBGA	672	Ind	50
LFE2M50SE-5F484I	270	1.2V	-5	fpBGA	484	Ind	50
LFE2M50SE-6F484I	270	1.2V	-6	fpBGA	484	Ind	50

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2M70SE-5F1152I	436	1.2V	-5	fpBGA	1152	Ind	70
LFE2M70SE-6F1152I	436	1.2V	-6	fpBGA	1152	Ind	70
LFE2M70SE-5F900I	416	1.2V	-5	fpBGA	900	Ind	70
LFE2M70SE-6F900I	416	1.2V	-6	fpBGA	900	Ind	70

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2M100SE-5F1152I	520	1.2V	-5	fpBGA	1152	Ind	100
LFE2M100SE-6F1152I	520	1.2V	-6	fpBGA	1152	Ind	100
LFE2M100SE-5F900I	416	1.2V	-5	fpBGA	900	Ind	100
LFE2M100SE-6F900I	416	1.2V	-6	fpBGA	900	Ind	100

Industrial

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2M20SE-5FN484I	304	1.2V	-5	Lead-Free fpBGA	484	Ind	20
LFE2M20SE-6FN484I	304	1.2V	-6	Lead-Free fpBGA	484	Ind	20
LFE2M20SE-5FN256I	140	1.2V	-5	Lead-Free fpBGA	256	Ind	20
LFE2M20SE-6FN256I	140	1.2V	-6	Lead-Free fpBGA	256	Ind	20

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2M35SE-5FN672I	410	1.2V	-5	Lead-Free fpBGA	672	Ind	35
LFE2M35SE-6FN672I	410	1.2V	-6	Lead-Free fpBGA	672	Ind	35
LFE2M35SE-5FN484I	303	1.2V	-5	Lead-Free fpBGA	484	Ind	35
LFE2M35SE-6FN484I	303	1.2V	-6	Lead-Free fpBGA	484	Ind	35
LFE2M35SE-5FN256I	140	1.2V	-5	Lead-Free fpBGA	256	Ind	35
LFE2M35SE-6FN256I	140	1.2V	-6	Lead-Free fpBGA	256	Ind	35

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2M50SE-5FN900I	410	1.2V	-5	Lead-Free fpBGA	900	Ind	50
LFE2M50SE-6FN900I	410	1.2V	-6	Lead-Free fpBGA	900	Ind	50
LFE2M50SE-5FN672I	372	1.2V	-5	Lead-Free fpBGA	672	Ind	50
LFE2M50SE-6FN672I	372	1.2V	-6	Lead-Free fpBGA	672	Ind	50
LFE2M50SE-5FN484I	270	1.2V	-5	Lead-Free fpBGA	484	Ind	50
LFE2M50SE-6FN484I	270	1.2V	-6	Lead-Free fpBGA	484	Ind	50

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2M70SE-5FN1152I	436	1.2V	-5	Lead-Free fpBGA	1152	Ind	70
LFE2M70SE-6FN1152I	436	1.2V	-6	Lead-Free fpBGA	1152	Ind	70
LFE2M70SE-5FN900I	416	1.2V	-5	Lead-Free fpBGA	900	Ind	70
LFE2M70SE-6FN900I	416	1.2V	-6	Lead-Free fpBGA	900	Ind	70

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2M100SE-5FN1152I	520	1.2V	-5	Lead-Free fpBGA	1152	Ind	100
LFE2M100SE-6FN1152I	520	1.2V	-6	Lead-Free fpBGA	1152	Ind	100
LFE2M100SE-5FN900I	416	1.2V	-5	Lead-Free fpBGA	900	Ind	100
LFE2M100SE-6FN900I	416	1.2V	-6	Lead-Free fpBGA	900	Ind	100