



Welcome to [E-XFL.COM](https://www.e-xfl.com)

Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

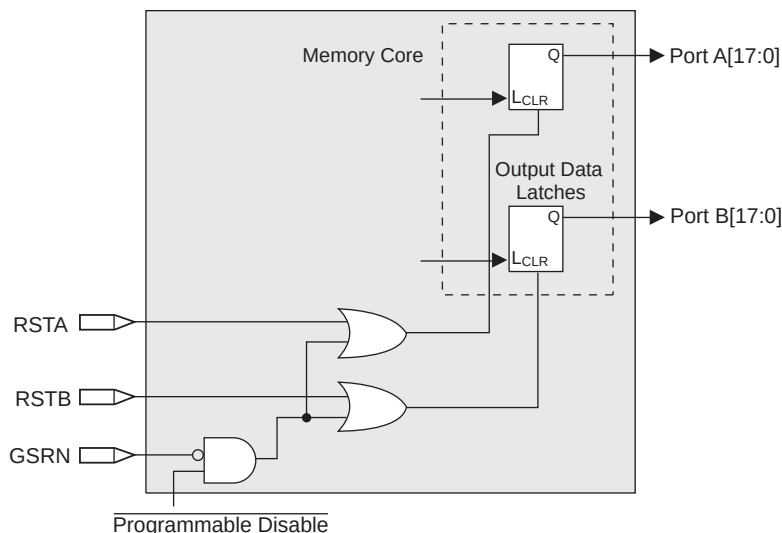
Product Status	Active
Number of LABs/CLBs	6000
Number of Logic Elements/Cells	48000
Total RAM Bits	4246528
Number of I/O	372
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	672-BBGA
Supplier Device Package	672-FPBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfe2m50se-5fn672i

2. Write Through – A copy of the input data appears at the output of the same port during a write cycle. This mode is supported for all data widths.

Memory Core Reset

The memory array in the EBR utilizes latches at the A and B output ports. These latches can be reset asynchronously or synchronously. RSTA and RSTB are local signals, which reset the output latches associated with Port A and Port B, respectively. The Global Reset (GSRN) signal resets both ports. The output data latches and associated resets for both ports are as shown in Figure 2-20.

Figure 2-20. Memory Core Reset

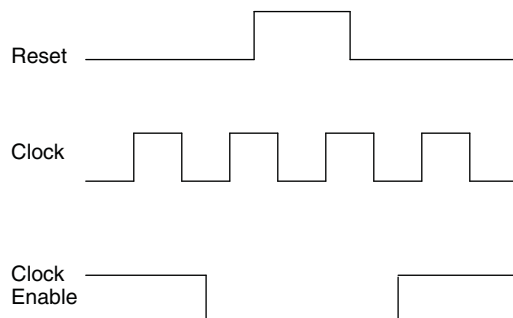


For further information about the sysMEM EBR block, please see the the list of additional technical documentation at the end of this data sheet.

EBR Asynchronous Reset

EBR asynchronous reset or GSR (if used) can only be applied if all clock enables are low for a clock cycle before the reset is applied and released a clock cycle after the reset is released, as shown in Figure 2-21. The GSR input to the EBR is always asynchronous.

Figure 2-21. EBR Asynchronous Reset (Including GSR) Timing Diagram



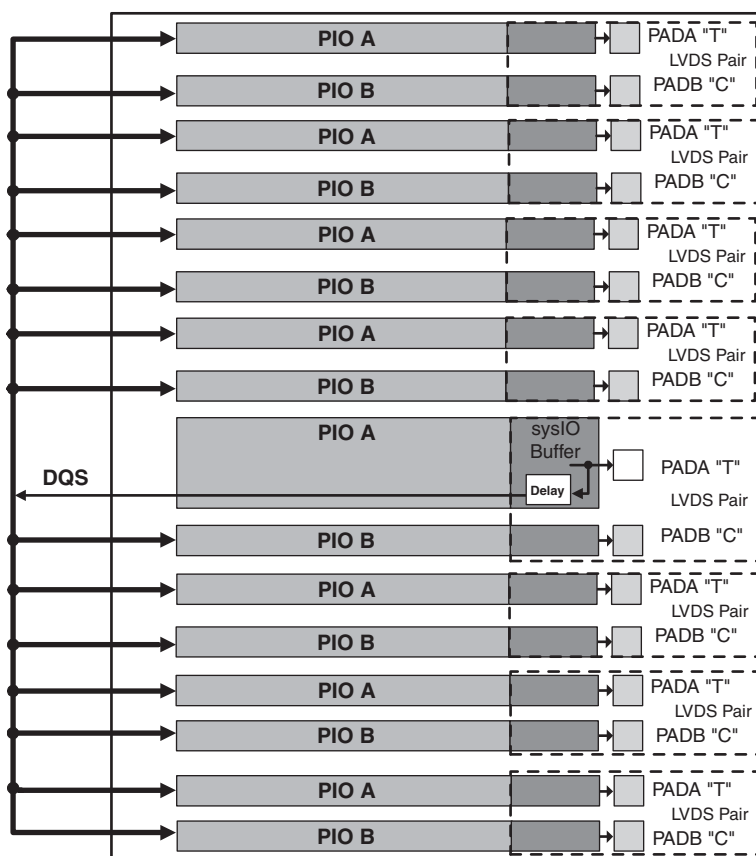
If all clock enables remain enabled, the EBR asynchronous reset or GSR may only be applied and released after the EBR read and write clock inputs are in a steady state condition for a minimum of $1/f_{MAX}$ (EBR clock). The reset release must adhere to the EBR synchronous reset setup time before the next active read or write clock edge.

Top Edge

The PICs on the top edge are different from PIOs on the left, right and bottom edges. PIOs on this edge do not have DDR registers or DQS signals.

The exact DQS pins are shown in a dual function in the Logic Signal Connections table in this data sheet. Additional detail is provided in the Signal Descriptions table. The DQS signal from the bus is used to strobe the DDR data from the memory into input register blocks. Interfaces on the left and right edges are designed for DDR memories that support 16 bits of data, whereas interfaces on the bottom are designed for memories that support 18 bits of data.

Figure 2-33. DQS Input Routing for the Left and Right Edges of the Device



LatticeECP2M Power Supply and NC (Cont.)

Signal	1152 fpBGA
V _{CC}	AA13, AA14, AA15, AA16, AA17, AA18, AA19, AA20, AA21, AA22, AB14, AB15, AB20, AB21, N14, N15, N20, N21, P13, P14, P15, P16, P17, P18, P19, P20, P21, P22, R13, R14, R21, R22, T14, T21, U14, U21, V14, V21, W14, W21, Y13, Y14, Y21, Y22
V _{CCIO0}	C12, C16, E14, H12, H16, M14, M15
V _{CCIO1}	C19, C23, E21, H19, H23, M20, M21
V _{CCIO2}	G32, K28, K32, N27, N32, P23, R23, T27, T32
V _{CCIO3}	AA23, AB27, AB32, AE28, AE32, AH32, W27, W32, Y23
V _{CCIO4}	AC20, AC21, AG19, AG23, AK21, AM19, AM23
V _{CCIO5}	AC14, AC15, AG12, AG16, AK14, AM12, AM16
V _{CCIO6}	AA12, AB3, AB8, AE3, AE7, AH3, W3, W8, Y12
V _{CCIO7}	G3, K3, K7, N3, N8, P12, R12, T3, T8
V _{CCIO8}	AD28, AG32
V _{CCJ}	AK3
V _{CCAUX}	AB12, AB13, AB22, AB23, AC13, AC22, M13, M22, N12, N13, N22, N23
V _{CCPLL}	R15, R20, Y15, Y20
SERDES Power ³	D7, B9, B8, D9, B7, E7, B6, D8, E6, D6, D4, B5, D3, B4, C1, B3, B1, B2, B33, B34, B32, C34, B31, D32, B30, D31, E29, D29, D27, B29, E28, B28, D26, B27, B26, D28, AL28, AN26, AN27, AL26, AN28, AK28, AN29, AL27, AL29, AK29, AL31, AN30, AL32, AN31, AM34, AN32, AN34, AN33, AN2, AN1, AN3, AM1, AN4, AL3, AN5, AL4, AL6, AK6, AL8, AN6, AK7, AN7, AL9, AN8, AN9, AL7
GND ¹	A1, A10, A13, A22, A25, A34, AB16, AB17, AB18, AB19, AB26, AB31, AB4, AB9, AC16, AC17, AC18, AC19, AD27, AE27, AE31, AE4, AE8, AF12, AF16, AF19, AF23, AG31, AH31, AH4, AJ14, AJ21, AK27, AK8, AL10, AL16, AL19, AL2, AL25, AL33, AP1, AP10, AP13, AP22, AP25, AP34, D10, D16, D19, D2, D25, D33, E27, E8, F14, F21, G31, G4, J12, J16, J19, J23, K27, K31, K4, K8, M16, M17, M18, M19, N16, N17, N18, N19, N26, N31, N4, N9, R16, R17, R18, R19, T12, T13, T15, T16, T17, T18, T19, T20, T22, T23, T26, T31, T4, T9, U12, U13, U15, U16, U17, U18, U19, U20, U22, U23, V12, V13, V15, V16, V17, V18, V19, V20, V22, V23, W12, W13, W15, W16, W17, W18, W19, W20, W22, W23, W26, W31, W4, W9, Y16, Y17, Y18, Y19
NC ²	LFE2M70: H2, H1, G5, G6, M9, M10, H3, H4, P3, P4, P9, M7, P1, P2, N7, P7, AC7, AC5, AC6, AD5, AD4, AD3, AD10, AD8, AD2, AD1, AD9, AC11, AD6, AD7, AE1, AE2, AJ12, AH12, AL13, AK13, AE14, AG13, AH22, AH21, AG22, AG21, AF33, AF34, AC27, AC28, AD29, AD30, AE33, AE34, AD32, AD31, AB25, AC25, AB28, AA26, AD33, AD34, P30, P29, P31, P32, R25, T24, N34, N33, F24, G23, J22, G22, H21, K21, L19, L20, L18, K19, J14, L15, H14, K14, F12, D11, F11, E11, A11, A12, A23, A24, AA11, AB11, AC26, AC30, AD11, AD12, AD13, AD14, AD15, AD19, AD21, AD22, AD23, AE10, AE11, AE12, AE13, AE19, AE21, AE22, AE23, AF11, AF21, AF22, AF24, AF8, AF9, AG10, AG11, AG24, AG25, AG26, AG3, AG7, AG8, AG9, AH10, AH11, AH13, AH24, AH25, AH26, AH27, AH5, AH6, AH7, AH8, AH9, AJ10, AJ11, AJ13, AJ24, AJ25, AJ26, AJ27, AJ3, AJ4, AJ5, AJ6, AJ7, AJ8, AJ9, AK10, AK11, AK12, AK24, AK25, AK26, AK4, AK9, AL11, AL12, AL34, AM10, AM11, AM13, AM25, AN10, AN11, AN12, AN13, AN24, AN25, AP11, AP12, AP24, B10, B11, B12, B13, B22, B23, B24, B25, C10, C11, C13, C22, C24, C25, D1, D15, D24, D34, E10, E24, E25, E26, E3, E31, E32, E33, E34, E4, E9, F10, F25, F26, F27, F28, F29, F30, F31, F32, F33, F34, F5, F6, F7, F8, F9, G10, G11, G24, G25, G26, G27, G28, G29, G30, G33, G34, G7, G8, G9, H10, H11, H24, H25, H26, H27, H28, H29, H8, H9, J10, J11, J24, J25, J26, J9, K10, K11, K12, K13, K23, K24, K25, K26, L11, L12, L13, L14, L21, L22, L23, L24, L25, L26, M11, M24, M25, M6, M8, N10, N11, P10, P25, P26, R9, T11, U11, W11, Y10, Y11 LFE2M100: A11, A12, A23, A24, AA11, AB11, AC26, AC30, AD11, AD12, AD13, AD14, AD15, AD19, AD21, AD22, AD23, AE10, AE11, AE12, AE13, AE19, AE21, AE22, AE23, AF11, AF21, AF22, AF24, AF8, AF9, AG10, AG11, AG24, AG25, AG26, AG3, AG7, AG8, AG9, AH10, AH11, AH13, AH24, AH25, AH26, AH27, AH5, AH6, AH7, AH8, AH9, AJ10, AJ11, AJ13, AJ24, AJ25, AJ26, AJ27, AJ3, AJ4, AJ5, AJ6, AJ7, AJ8, AJ9, AK10, AK11, AK12, AK24, AK25, AK26, AK4, AK9, AL11, AL12, AL34, AM10, AM11, AM13, AM25, AN10, AN11, AN12, AN13, AN24, AN25, AP11, AP12, AP24, B10, B11, B12, B13, B22, B23, B24, B25, C10, C11, C13, C22, C24, C25, D1, D15, D24, D34, E10, E24, E25, E26, E3, E31, E32, E33, E34, E4, E9, F10, F25, F26, F27, F28, F29, F30, F31, F32, F33, F34, F5, F6, F7, F8, F9, G10, G11, G24, G25, G26, G27, G28, G29, G30, G33, G34, G7, G8, G9, H10, H11, H24, H25, H26, H27, H28, H29, H8, H9, J10, J11, J24, J25, J26, J9, K10, K11, K12, K13, K23, K24, K25, K26, L11, L12, L13, L14, L21, L22, L23, L24, L25, L26, M11, M24, M25, M6, M8, N10, N11, P10, P25, P26, R9, T11, U11, W11, Y10, Y11

1. All grounds must be electrically connected at the board level. For fpBGA packages, the total number of GND balls is less than the actual number of GND logic connections from the die to the common package GND plane.
2. NC pins should not be connected to any active signals, VCC or GND.
3. For package migration across device densities, the designer must comprehend the package pin requirements for the SERDES blocks. Specifically, the SERDES power pins of the largest density device must be accounted to accommodate migration to other smaller devices using the same package. Please refer to TN1160, [LatticeECP2/M Density Migration](#) for more details.

LFE2-6E/SE and LFE2-12E/SE Logic Signal Connections: 256 fpBGA (Cont.)

LFE2-6E/SE					LFE2-12E/SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
R12	GND	-			GND	-		
R5	GND	-			GND	-		
T1	GND	-			GND	-		
T16	GND	-			GND	-		

* Supports true LVDS. Other differential signals must be emulated with external resistors.

** These dedicated input pins can be used for GPLLs or GDLLs within the respective quadrant.

Note: VCCIO and GND pads are used to determine the average DC current drawn by I/Os between GND/VCCIO connections, or between the last GND/VCCIO in an I/O bank and the end of an I/O bank. The substrate pads listed in the Pin Table do not necessarily have a one to one connection with a package ball or pin.

LFE2-12E/SE and LFE2-20E/SE Logic Signal Connections: 484 fpBGA (Cont.)

LFE2-12E/12SE					LFE2-20E/20SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
W19	CFG2	8			CFG2	8		
V19	CFG1	8			CFG1	8		
V20	PROGRAMN	8			PROGRAMN	8		
W20	CFG0	8			CFG0	8		
U22	PR28B	8	D1	C	PR42B	8	D1	C
V22	INITN	8			INITN	8		
R16	PR30B	8	WRITEN	C	PR44B	8	WRITEN	C
GNDIO	GNDIO8	-			GNDIO8	-		
W22	CCLK	8			CCLK	8		
R17	PR30A	8	CS1N	T	PR44A	8	CS1N	T
V21	DONE	8			DONE	8		
VCCIO	VCCIO8	8			VCCIO8	8		
U19	PR29B	8	CSN	C	PR43B	8	CSN	C
T17	PR26B	8	D5	C	PR40B	8	D5	C
U20	PR29A	8	D0/SPIFASTN	T	PR43A	8	D0/SPIFASTN	T
U21	PR28A	8	D2	T	PR42A	8	D2	T
GNDIO	GNDIO8	-			GNDIO8	-		
T18	PR26A	8	D6	T	PR40A	8	D6	T
T20	PR27B	8	D3	C	PR41B	8	D3	C
T21	PR25B	8	D7/SPID0	C	PR39B	8	D7/SPID0	C
T19	PR27A	8	D4	T	PR41A	8	D4	T
VCCIO	VCCIO8	8			VCCIO8	8		
T22	PR25A	8	DI/CSSPI0N	T	PR39A	8	DI/CSSPI0N	T
R18	PR24B	8	DOUT/CSN	C	PR38B	8	DOUT/CSN	C
R19	PR24A	8	BUSY/SISPI	T	PR38A	8	BUSY/SISPI	T
-	-	-			VCCIO3	3		
GNDIO	GNDIO3	-			GNDIO3	-		
P18	PR22B	3		C (LVDS)*	PR32B	3	RDQ34	C (LVDS)*
R22	PR23B	3		C	PR33B	3	RDQ34	C
P19	PR22A	3		T (LVDS)*	PR32A	3	RDQ34	T (LVDS)*
R21	PR23A	3		T	PR33A	3	RDQ34	T
VCCIO	VCCIO3	3			VCCIO3	3		
R20	PR21B	3	RLM0_GPLL_C_FB_A	C	PR31B	3	RLM0_GPLL_C_FB_A/RDQ34	C
P22	PR21A	3	RLM0_GPLLT_FB_A	T	PR31A	3	RLM0_GPLLT_FB_A/RDQ34	T
P21	PR20B	3	RLM0_GPLL_C_IN_A**	C (LVDS)*	PR30B	3	RLM0_GPLL_C_IN_A**/RDQ34	C (LVDS)*
N21	PR20A	3	RLM0_GPLLT_IN_A**	T (LVDS)*	PR30A	3	RLM0_GPLLT_IN_A**/RDQ34	T (LVDS)*
N17	RLM0_PLLCAP	3			RLM0_PLLCAP	3		
N22	PR18B	3	RLM0_GDLL_C_FB_A	C	PR28B	3	RLM0_GDLL_C_FB_A/RDQ25	C
M22	PR17B	3	RLM0_GDLL_C_IN_A**	C (LVDS)*	PR27B	3	RLM0_GDLL_C_IN_A**/RDQ25	C (LVDS)*
GNDIO	GNDIO3	-			GNDIO3	-		
N20	PR18A	3	RLM0_GDLLT_FB_A	T	PR28A	3	RLM0_GDLLT_FB_A/RDQ25	T
M21	PR17A	3	RLM0_GDLLT_IN_A**	T (LVDS)*	PR27A	3	RLM0_GDLLT_IN_A**/RDQ25	T (LVDS)*
N19	NC	-			PR26B	3	RDQ25	C
-	-	-			VCCIO3	3		

LFE2-12E/SE and LFE2-20E/SE Logic Signal Connections: 484 fpBGA (Cont.)

LFE2-12E/12SE					LFE2-20E/20SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
H16	NC	-			NC	-		
H20	NC	-			NC	-		
H18	NC	-			NC	-		
K6	NC	-			NC	-		
J16	NC	-			NC	-		
N18	VCC	-			VCC	-		
N6	VCC	-			VCC	-		

* Supports true LVDS. Other differential signals must be emulated with external resistors.

** These dedicated input pins can be used for GPLLs or GDLLs within the respective quadrant.

Note: VCCIO and GND pads are used to determine the average DC current drawn by I/Os between GND/VCCIO connections, or between the last GND/VCCIO in an I/O bank and the end of an I/O bank. The substrate pads listed in the Pin Table do not necessarily have a one to one connection with a package ball or pin.

LFE2-20E/SE and LFE2-35E/SE Logic Signal Connections: 672 fpBGA (Cont.)

LFE2-20E/20SE					LFE2-35E/35SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential	
C20	PT57B	1		C	PT66B	1		C	
D20	PT57A	1		T	PT66A	1		T	
A22	PT56B	1		C	PT65B	1		C	
A21	PT56A	1		T	PT65A	1		T	
GND	GNDIO1	-			GNDIO1	-			
E19	NC	-			NC	-			
C19	NC	-			NC	-			
VCCIO	VCCIO1	1			VCCIO1	1			
B21	NC	-			NC	-			
B20	NC	-			NC	-			
D19	NC	-			NC	-			
B19	NC	-			NC	-			
GND	GNDIO1	-			GNDIO1	-			
G17	NC	-			NC	-			
E18	NC	-			NC	-			
G19	NC	-			NC	-			
F17	NC	-			NC	-			
VCCIO	VCCIO1	1			VCCIO1	1			
A20	NC	-			NC	-			
A19	NC	-			NC	-			
E17	NC	-			NC	-			
D18	NC	-			NC	-			
B18	PT55B	1		C	PT55B	1		C	
GND	GNDIO1	-			GNDIO1	-			
A18	PT55A	1		T	PT55A	1		T	
E16	PT54B	1		C	PT54B	1		C	
G16	PT54A	1		T	PT54A	1		T	
F16	PT53B	1		C	PT53B	1		C	
VCCIO	VCCIO1	1			VCCIO1	1			
H18	PT53A	1		T	PT53A	1		T	
A17	PT52B	1		C	PT52B	1		C	
B17	PT52A	1		T	PT52A	1		T	
C18	PT51B	1		C	PT51B	1		C	
B16	PT51A	1		T	PT51A	1		T	
C17	PT50B	1		C	PT50B	1		C	
GND	GNDIO1	-			GNDIO1	-			
D17	PT50A	1		T	PT50A	1		T	
E15	PT49B	1		C	PT49B	1		C	
VCCIO	VCCIO1	1			VCCIO1	1			
G15	PT49A	1		T	PT49A	1		T	
A16	PT48B	1		C	PT48B	1		C	
B15	PT48A	1		T	PT48A	1		T	
D15	PT47B	1		C	PT47B	1		C	
F15	PT47A	1		T	PT47A	1		T	
A14	PT46B	1		C	PT46B	1		C	
B14	PT46A	1		T	PT46A	1		T	

LFE2-20E/SE and LFE2-35E/SE Logic Signal Connections: 672 fpBGA (Cont.)

LFE2-20E/20SE					LFE2-35E/35SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
D4	PT7B	0		C	PT7B	0		C
D3	PT7A	0		T	PT7A	0		T
C2	PT6B	0		C	PT6B	0		C
C1	PT6A	0		T	PT6A	0		T
G8	PT5B	0		C	PT5B	0		C
GND	GNDIO0	-			GNDIO0	-		
G7	PT5A	0		T	PT5A	0		T
E7	PT4B	0		C	PT4B	0		C
VCCIO	VCCIO0	0			VCCIO0	0		
F7	PT4A	0		T	PT4A	0		T
E6	PT3B	0		C	PT3B	0		C
E5	PT3A	0		T	PT3A	0		T
G6	PT2B	0	VREF2_0	C	PT2B	0	VREF2_0	C
G5	PT2A	0	VREF1_0	T	PT2A	0	VREF1_0	T
L12	VCC	-			VCC	-		
L13	VCC	-			VCC	-		
L14	VCC	-			VCC	-		
L15	VCC	-			VCC	-		
M11	VCC	-			VCC	-		
M12	VCC	-			VCC	-		
M15	VCC	-			VCC	-		
M16	VCC	-			VCC	-		
N11	VCC	-			VCC	-		
N16	VCC	-			VCC	-		
P11	VCC	-			VCC	-		
P16	VCC	-			VCC	-		
R11	VCC	-			VCC	-		
R12	VCC	-			VCC	-		
R15	VCC	-			VCC	-		
R16	VCC	-			VCC	-		
T12	VCC	-			VCC	-		
T13	VCC	-			VCC	-		
T14	VCC	-			VCC	-		
T15	VCC	-			VCC	-		
D11	VCCIO0	0			VCCIO0	0		
D6	VCCIO0	0			VCCIO0	0		
G9	VCCIO0	0			VCCIO0	0		
K12	VCCIO0	0			VCCIO0	0		
J12	VCCIO0	0			VCCIO0	0		
D16	VCCIO1	1			VCCIO1	1		
D21	VCCIO1	1			VCCIO1	1		
G18	VCCIO1	1			VCCIO1	1		
J15	VCCIO1	1			VCCIO1	1		
K15	VCCIO1	1			VCCIO1	1		
F23	VCCIO2	2			VCCIO2	2		
J20	VCCIO2	2			VCCIO2	2		

LFE2-50E/SE and LFE2-70E/SE Logic Signal Connections: 672 fpBGA (Cont.)

LFE2-50E/SE					LFE2-70E/SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
C20	PT75B	1		C	PT93B	1		C
D20	PT75A	1		T	PT93A	1		T
A22	PT74B	1		C	PT92B	1		C
A21	PT74A	1		T	PT92A	1		T
GND	GNDIO1	-			GNDIO1	-		
E19	PT71B	1		C	PT85B	1		C
C19	PT71A	1		T	PT85A	1		T
VCCIO	VCCIO1	1			VCCIO1	1		
B21	PT70B	1		C	PT79B	1		C
B20	PT70A	1		T	PT79A	1		T
D19	PT69B	1		C	PT78B	1		C
B19	PT69A	1		T	PT78A	1		T
GND	GNDIO1	-			GNDIO1	-		
G17	PT68B	1		C	PT77B	1		C
E18	PT68A	1		T	PT77A	1		T
G19	PT67B	1		C	PT76B	1		C
F17	PT67A	1		T	PT76A	1		T
VCCIO	VCCIO1	1			VCCIO1	1		
A20	PT66B	1		C	PT75B	1		C
A19	PT66A	1		T	PT75A	1		T
E17	PT65B	1		C	PT74B	1		C
D18	PT65A	1		T	PT74A	1		T
B18	PT64B	1		C	PT73B	1		C
GND	GNDIO1	-			GNDIO1	-		
A18	PT64A	1		T	PT73A	1		T
E16	PT63B	1		C	PT72B	1		C
G16	PT63A	1		T	PT72A	1		T
F16	PT62B	1		C	PT71B	1		C
VCCIO	VCCIO1	1			VCCIO1	1		
H18	PT62A	1		T	PT71A	1		T
A17	PT61B	1		C	PT70B	1		C
B17	PT61A	1		T	PT70A	1		T
C18	PT60B	1		C	PT69B	1		C
B16	PT60A	1		T	PT69A	1		T
C17	PT59B	1		C	PT68B	1		C
GND	GNDIO1	-			GNDIO1	-		
D17	PT59A	1		T	PT68A	1		T
E15	PT58B	1		C	PT67B	1		C
VCCIO	VCCIO1	1			VCCIO1	1		
G15	PT58A	1		T	PT67A	1		T
A16	PT57B	1		C	PT66B	1		C
B15	PT57A	1		T	PT66A	1		T
D15	PT56B	1		C	PT65B	1		C
F15	PT56A	1		T	PT65A	1		T
A14	PT55B	1		C	PT64B	1		C
B14	PT55A	1		T	PT64A	1		T

LFE2-50E/SE and LFE2-70E/SE Logic Signal Connections: 672 fpBGA (Cont.)

LFE2-50E/SE					LFE2-70E/SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
N15	GND	-			GND	-		
N17	GND	-			GND	-		
P10	GND	-			GND	-		
P12	GND	-			GND	-		
P13	GND	-			GND	-		
P14	GND	-			GND	-		
P15	GND	-			GND	-		
P17	GND	-			GND	-		
R13	GND	-			GND	-		
R14	GND	-			GND	-		
T10	GND	-			GND	-		
T11	GND	-			GND	-		
T16	GND	-			GND	-		
T17	GND	-			GND	-		
T24	GND	-			GND	-		
T3	GND	-			GND	-		
U10	GND	-			GND	-		
U11	GND	-			GND	-		
U13	GND	-			GND	-		
U14	GND	-			GND	-		
U16	GND	-			GND	-		
U17	GND	-			GND	-		
V13	GND	-			GND	-		
V14	GND	-			GND	-		
V21	GND	-			GND	-		
V6	GND	-			GND	-		
M3	NC	-			NC	-		
N6	NC	-			NC	-		
P24	NC	-			NC	-		

* Supports true LVDS. Other differential signals must be emulated with external resistors.

** These dedicated input pins can be used for GPLLs or GDLLs within the respective quadrant.

***Due to packaging bond out option, this DQS does not have all the necessary DQ pins bonded out for a full 8-bit data width.

Note: VCCIO and GND pads are used to determine the average DC current drawn by I/Os between GND/VCCIO connections, or between the last GND/VCCIO in an I/O bank and the end of an I/O bank. The substrate pads listed in the Pin Table do not necessarily have a one to one connection with a package ball or pin.

LFE2-70E/SE Logic Signal Connections: 900 fpBGA

LFE2-70E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential
VCCIO	VCCIO7	7		
F4	PL2A	7	VREF2_7	T (LVDS)*
F3	PL2B	7	VREF1_7	C (LVDS)*
H4	PL3A	7		T
G5	PL3B	7		C
GND	GNDIO7	-		
D2	PL4A	7		T (LVDS)*
D1	PL4B	7		C (LVDS)*
E2	PL5A	7		T
VCCIO	VCCIO7	7		
E1	PL5B	7		C
GND	GNDIO7	-		
VCCIO	VCCIO7	7		
F1	PL14A	7	LUM1_SPLLT_IN_A/LDQ12	T (LVDS)*
F2	PL14B	7	LUM1_SPLLC_IN_A/LDQ12	C (LVDS)*
G1	PL15A	7	LUM1_SPLLT_FB_A/LDQ12	T
G2	PL15B	7	LUM1_SPLLC_FB_A/LDQ12	C
GND	GNDIO7	-		
H8	PL18A	7	LDQ21	T
H6	PL18B	7	LDQ21	C
VCCIO	VCCIO7	7		
G4	PL19A	7	LDQ21	T (LVDS)*
G3	PL19B	7	LDQ21	C (LVDS)*
H7	PL20A	7	LDQ21	T
H5	PL20B	7	LDQ21	C
GND	GNDIO7	-		
H2	PL21A	7	LDQS21	T (LVDS)*
H1	PL21B	7	LDQ21	C (LVDS)*
J6	PL22A	7	LDQ21	T
VCCIO	VCCIO7	7		
J8	PL22B	7	LDQ21	C
J2	PL23A	7	LDQ21	T (LVDS)*
J1	PL23B	7	LDQ21	C (LVDS)*
J5	PL24A	7	LDQ21	T
GND	GNDIO7	-		
J7	PL24B	7	LDQ21	C
J4	PL25A	7	LDQ29	T (LVDS)*
J3	PL25B	7	LDQ29	C (LVDS)*
K6	PL26A	7	LDQ29	T
K8	PL26B	7	LDQ29	C
VCCIO	VCCIO7	7		
K2	PL27A	7	LDQ29	T (LVDS)*

LFE2-70E/SE Logic Signal Connections: 900 fpBGA (Cont.)

LFE2-70E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential
W7	PL72B	6	LDQ71	C
W4	PL73A	6	LLM0_GDLLT_IN_A**/LDQ71	T (LVDS)*
W3	PL73B	6	LLM0_GDLLC_IN_A**/LDQ71	C (LVDS)*
W6	PL74A	6	LLM0_GDLLT_FB_A/LDQ71	T
GND	GNDIO6	-		
W8	PL74B	6	LLM0_GDLLC_FB_D/LDQ71	C
Y8	LLM0_PLLCAP	6		
Y1	PL76A	6	LLM0_GPLLT_IN_A**/LDQ80	T (LVDS)*
Y2	PL76B	6	LLM0_GPLLC_IN_A**/LDQ80	C (LVDS)*
Y5	PL77A	6	LLM0_GPLLT_FB_A/LDQ80	T
Y6	PL77B	6	LLM0_GPLLC_FB_A/LDQ80	C
Y4	PL78A	6	LDQ80	T (LVDS)*
VCCIO	VCCIO6	6		
Y3	PL78B	6	LDQ80	C (LVDS)*
AA6	PL79A	6	LDQ80	T
AA8	PL79B	6	LDQ80	C
AA2	PL80A	6	LDQS80	T (LVDS)*
GND	GNDIO6	-		
AA1	PL80B	6	LDQ80	C (LVDS)*
AA7	PL81A	6	LDQ80	T
AA5	PL81B	6	LDQ80	C
VCCIO	VCCIO6	6		
AA4	PL82A	6	LDQ80	T (LVDS)*
AA3	PL82B	6	LDQ80	C (LVDS)*
AB7	PL83A	6	LDQ80	T
AB5	PL83B	6	LDQ80	C
GND	GNDIO6	-		
AB2	PL84A	6	LDQ88	T (LVDS)*
AB1	PL84B	6	LDQ88	C (LVDS)*
AB8	PL85A	6	LDQ88	T
AB6	PL85B	6	LDQ88	C
VCCIO	VCCIO6	6		
AB4	PL86A	6	LDQ88	T (LVDS)*
AB3	PL86B	6	LDQ88	C (LVDS)*
AC7	PL87A	6	LDQ88	T
AC5	PL87B	6	LDQ88	C
GND	GNDIO6	-		
AC2	PL88A	6	LDQS88	T (LVDS)*
AC1	PL88B	6	LDQ88	C (LVDS)*
AC6	PL89A	6	LDQ88	T
VCCIO	VCCIO6	6		
AD6	PL89B	6	LDQ88	C
AD1	PL90A	6	LDQ88	T (LVDS)*

LFE2-70E/SE Logic Signal Connections: 900 fpBGA (Cont.)

LFE2-70E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential
AD18	PB66A	4	BDQ69	T
AF18	PB66B	4	BDQ69	C
AC18	PB67A	4	BDQ69	T
AE18	PB67B	4	BDQ69	C
VCCIO	VCCIO4	4		
AG19	PB68A	4	BDQ69	T
AH19	PB68B	4	BDQ69	C
GND	GNDIO4	-		
AE19	PB69A	4	BDQS69	T
AF19	PB69B	4	BDQ69	C
AC19	PB70A	4	BDQ69	T
AD19	PB70B	4	BDQ69	C
AJ19	PB71A	4	BDQ69	T
AK19	PB71B	4	BDQ69	C
VCCIO	VCCIO4	4		
AF20	PB72A	4	BDQ69	T
AH20	PB72B	4	BDQ69	C
AE20	PB73A	4	BDQ69	T
AG20	PB73B	4	BDQ69	C
GND	GNDIO4	-		
AD20	PB74A	4	BDQ78	T
AC20	PB74B	4	BDQ78	C
AH21	PB75A	4	BDQ78	T
AF21	PB75B	4	BDQ78	C
AJ20	PB76A	4	BDQ78	T
VCCIO	VCCIO4	4		
AK20	PB76B	4	BDQ78	C
AG21	PB77A	4	BDQ78	T
AE21	PB77B	4	BDQ78	C
AD21	PB78A	4	BDQS78	T
GND	GNDIO4	-		
AC21	PB78B	4	BDQ78	C
AD22	PB79A	4	BDQ78	T
AB21	PB79B	4	BDQ78	C
AJ21	PB80A	4	BDQ78	T
VCCIO	VCCIO4	4		
AK21	PB80B	4	BDQ78	C
GND	GNDIO4	-		
VCCIO	VCCIO4	4		
AJ25	PB87A	4	BDQS87***	T
AK24	PB87B	4	BDQ87	C
AJ24	PB88A	4	BDQ87	T
AK25	PB88B	4	BDQ87	C

LFE2-70E/SE Logic Signal Connections: 900 fpBGA (Cont.)

LFE2-70E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential
G12	PT40B	0		C
E12	PT40A	0		T
VCCIO	VCCIO0	0		
B13	PT39B	0		C
A13	PT39A	0		T
H12	PT38B	0		C
F12	PT38A	0		T
C12	PT37B	0		C
GND	GNDIO0	-		
D12	PT37A	0		T
B12	PT36B	0		C
A12	PT36A	0		T
E11	PT35B	0		C
VCCIO	VCCIO0	0		
G11	PT35A	0		T
F11	PT34B	0		C
H11	PT34A	0		T
C11	PT33B	0		C
D11	PT33A	0		T
B11	PT32B	0		C
GND	GNDIO0	-		
A11	PT32A	0		T
E10	PT31B	0		C
VCCIO	VCCIO0	0		
G10	PT31A	0		T
F10	PT30B	0		C
H10	PT30A	0		T
D10	PT29B	0		C
C10	PT29A	0		T
GND	GNDIO0	-		
VCCIO	VCCIO0	0		
A7	PT16B	0		C
B7	PT16A	0		T
A6	PT15B	0		C
B6	PT15A	0		T
C7	PT14B	0		C
GND	GNDIO0	-		
D7	PT14A	0		T
D8	PT13B	0		C
VCCIO	VCCIO0	0		
E7	PT13A	0		T
C6	PT12B	0		C
D6	PT12A	0		T

LFE2M50E/SE Logic Signal Connections: 484 fpBGA (Cont.)

LFE2M50E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential
T1	PL65A	6	LLM0_GDLLT_FB_A	T
T2	PL65B	6	LLM0_GDLLC_FB_A	C
GNDIO	GNDIO6	-		
R7	LLM0_PLLCAP	6		
T6	PL67A	6	LDQ71	T (LVDS)*
T7	PL67B	6	LDQ71	C (LVDS)*
U1	PL68A	6	LDQ71	T
U2	PL68B	6	LDQ71	C
VCCIO	VCCIO6	6		
T3	PL69A	6	LDQ71	T (LVDS)*
U3	PL69B	6	LDQ71	C (LVDS)*
U6	PL70A	6	LDQ71	T
U5	PL70B	6	LDQ71	C
GNDIO	GNDIO6	-		
V5	PL71A	6	LDQS71	T (LVDS)*
U4	PL71B	6	LDQ71	C (LVDS)*
V1	PL72A	6	LDQ71	T
VCCIO	VCCIO6	6		
V3	PL72B	6	LDQ71	C
W1	PL73A	6	LDQ71	T (LVDS)*
Y1	PL73B	6	LDQ71	C (LVDS)*
AA1	PL74A	6	LDQ71	T
GNDIO	GNDIO6	-		
AA2	PL74B	6	LDQ71	C
V4	TCK	-		
Y2	TDI	-		
Y3	TMS	-		
W3	TDO	-		
W4	VCCJ	-		
W5	PB2A	5	BDQ6	T
Y4	PB2B	5	BDQ6	C
W6	PB3A	5	BDQ6	T
V6	PB3B	5	BDQ6	C
AA3	PB4A	5	BDQ6	T
AB2	PB4B	5	BDQ6	C
VCCIO	VCCIO5	5		
T8	PB5A	5	BDQ6	T
U7	PB5B	5	BDQ6	C
GNDIO	GNDIO5	-		
U8	PB6A	5	BDQS6	T
T9	PB6B	5	BDQ6	C
V8	PB7A	5	BDQ6	T
W8	PB7B	5	BDQ6	C

LFE2M50E/SE and LFE2M70E/SE Logic Signal Connections: 900 fpBGA (Cont.)

LFE2M50E/SE					LFE2M70E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential	
L13	VCC	-			VCC	-			
L18	VCC	-			VCC	-			
L19	VCC	-			VCC	-			
M11	VCC	-			VCC	-			
M12	VCC	-			VCC	-			
M13	VCC	-			VCC	-			
M14	VCC	-			VCC	-			
M15	VCC	-			VCC	-			
M16	VCC	-			VCC	-			
M17	VCC	-			VCC	-			
M18	VCC	-			VCC	-			
M19	VCC	-			VCC	-			
M20	VCC	-			VCC	-			
N11	VCC	-			VCC	-			
N12	VCC	-			VCC	-			
N19	VCC	-			VCC	-			
N20	VCC	-			VCC	-			
P12	VCC	-			VCC	-			
P19	VCC	-			VCC	-			
R12	VCC	-			VCC	-			
R19	VCC	-			VCC	-			
T12	VCC	-			VCC	-			
T19	VCC	-			VCC	-			
U12	VCC	-			VCC	-			
U19	VCC	-			VCC	-			
V11	VCC	-			VCC	-			
V12	VCC	-			VCC	-			
V19	VCC	-			VCC	-			
V20	VCC	-			VCC	-			
W11	VCC	-			VCC	-			
W12	VCC	-			VCC	-			
W13	VCC	-			VCC	-			
W14	VCC	-			VCC	-			
W15	VCC	-			VCC	-			
W16	VCC	-			VCC	-			
W17	VCC	-			VCC	-			
W18	VCC	-			VCC	-			
W19	VCC	-			VCC	-			
W20	VCC	-			VCC	-			
Y12	VCC	-			VCC	-			
Y13	VCC	-			VCC	-			
Y18	VCC	-			VCC	-			
Y19	VCC	-			VCC	-			
D14	VCCIO0	0			VCCIO0	0			
E6	VCCIO0	0			VCCIO0	0			
E9	VCCIO0	0			VCCIO0	0			
F12	VCCIO0	0			VCCIO0	0			
K12	VCCIO0	0			VCCIO0	0			

LFE2M50E/SE and LFE2M70E/SE Logic Signal Connections: 900 fpBGA (Cont.)

LFE2M50E/SE					LFE2M70E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential	
K13	VCCIO0	0			VCCIO0	0			
D17	VCCIO1	1			VCCIO1	1			
E22	VCCIO1	1			VCCIO1	1			
E25	VCCIO1	1			VCCIO1	1			
F19	VCCIO1	1			VCCIO1	1			
K18	VCCIO1	1			VCCIO1	1			
K19	VCCIO1	1			VCCIO1	1			
F28	VCCIO2	2			VCCIO2	2			
J25	VCCIO2	2			VCCIO2	2			
K28	VCCIO2	2			VCCIO2	2			
M21	VCCIO2	2			VCCIO2	2			
M24	VCCIO2	2			VCCIO2	2			
N21	VCCIO2	2			VCCIO2	2			
N28	VCCIO2	2			VCCIO2	2			
P21	VCCIO2	2			VCCIO2	2			
R25	VCCIO2	2			VCCIO2	2			
AA28	VCCIO3	3			VCCIO3	3			
AB25	VCCIO3	3			VCCIO3	3			
AE28	VCCIO3	3			VCCIO3	3			
T25	VCCIO3	3			VCCIO3	3			
U21	VCCIO3	3			VCCIO3	3			
V21	VCCIO3	3			VCCIO3	3			
V28	VCCIO3	3			VCCIO3	3			
W21	VCCIO3	3			VCCIO3	3			
W24	VCCIO3	3			VCCIO3	3			
AA18	VCCIO4	4			VCCIO4	4			
AA19	VCCIO4	4			VCCIO4	4			
AE19	VCCIO4	4			VCCIO4	4			
AF22	VCCIO4	4			VCCIO4	4			
AG17	VCCIO4	4			VCCIO4	4			
AG25	VCCIO4	4			VCCIO4	4			
AA12	VCCIO5	5			VCCIO5	5			
AA13	VCCIO5	5			VCCIO5	5			
AE12	VCCIO5	5			VCCIO5	5			
AF9	VCCIO5	5			VCCIO5	5			
AG14	VCCIO5	5			VCCIO5	5			
AG6	VCCIO5	5			VCCIO5	5			
AA3	VCCIO6	6			VCCIO6	6			
AB6	VCCIO6	6			VCCIO6	6			
AE3	VCCIO6	6			VCCIO6	6			
T6	VCCIO6	6			VCCIO6	6			
U10	VCCIO6	6			VCCIO6	6			
V10	VCCIO6	6			VCCIO6	6			
V3	VCCIO6	6			VCCIO6	6			
W10	VCCIO6	6			VCCIO6	6			
W7	VCCIO6	6			VCCIO6	6			
F3	VCCIO7	7			VCCIO7	7			
J6	VCCIO7	7			VCCIO7	7			

LFE2M100E/SE Logic Signal Connections: 900 fpBGA (Cont.)

LFE2M100E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential
AB27	PR97A	3	RDQ99	T (LVDS)*
VCCIO	VCCIO3	3		
Y24	PR96B	3	RDQ99	C
Y25	PR96A	3	RDQ99	T
AA29	PR95B	3	RDQ99	C (LVDS)*
Y28	PR95A	3	RDQ99	T (LVDS)*
Y30	PR93B	3	RDQ90	C
Y29	PR93A	3	RDQ90	T
GNDIO	GNDIO3	-		
VCCIO	VCCIO3	3		
W22	PR83B	3	RDQ81	C (LVDS)*
V22	PR83A	3	RDQ81	T (LVDS)*
Y27	PR82B	3	RDQ81	C
VCCIO	VCCIO3	3		
Y26	PR82A	3	RDQ81	T
W30	PR81B	3	RDQ81	C (LVDS)*
W29	PR81A	3	RDQS81	T (LVDS)*
GNDIO	GNDIO3	-		
W25	PR80B	3	RDQ81	C
W26	PR80A	3	RDQ81	T
U29	PR79B	3	RDQ81	C (LVDS)*
V29	PR79A	3	RDQ81	T (LVDS)*
VCCIO	VCCIO3	3		
V30	PR78B	3	RDQ81	C
U30	PR78A	3	RDQ81	T
W27	PR77B	3	RDQ81	C (LVDS)*
W28	PR77A	3	RDQ81	T (LVDS)*
V24	PR75B	3	RDQ72	C
V25	PR75A	3	RDQ72	T
GNDIO	GNDIO3	-		
U28	PR74B	3	RDQ72	C (LVDS)*
U27	PR74A	3	RDQ72	T (LVDS)*
U23	PR73B	3	RDQ72	C
V23	PR73A	3	RDQ72	T
VCCIO	VCCIO3	3		
V26	PR72B	3	RDQ72	C (LVDS)*
U26	PR72A	3	RDQS72	T (LVDS)*
U25	PR71B	3	RDQ72	C
GNDIO	GNDIO3	-		
U24	PR71A	3	RDQ72	T
T30	PR70B	3	RDQ72	C (LVDS)*
R30	PR70A	3	RDQ72	T (LVDS)*
T23	PR69B	3	RDQ72	C

LFE2M70E/SE and LFE2M100E/SE Logic Signal Connections: 1152 fpBGA (Cont.)

LFE2M70E/SE				LFE2M100E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
AK12	NC	-			NC	-		
AK24	NC	-			NC	-		
AK25	NC	-			NC	-		
AK26	NC	-			NC	-		
AK4	NC	-			NC	-		
AK9	NC	-			NC	-		
AL11	NC	-			NC	-		
AL12	NC	-			NC	-		
AL34	NC	-			NC	-		
AM10	NC	-			NC	-		
AM11	NC	-			NC	-		
AM13	NC	-			NC	-		
AM25	NC	-			NC	-		
AN10	NC	-			NC	-		
AN11	NC	-			NC	-		
AN12	NC	-			NC	-		
AN13	NC	-			NC	-		
AN24	NC	-			NC	-		
AN25	NC	-			NC	-		
AP11	NC	-			NC	-		
AP12	NC	-			NC	-		
AP24	NC	-			NC	-		
B10	NC	-			NC	-		
B11	NC	-			NC	-		
B12	NC	-			NC	-		
B13	NC	-			NC	-		
B22	NC	-			NC	-		
B23	NC	-			NC	-		
B24	NC	-			NC	-		
B25	NC	-			NC	-		
C10	NC	-			NC	-		
C11	NC	-			NC	-		
C13	NC	-			NC	-		
C22	NC	-			NC	-		
C24	NC	-			NC	-		
C25	NC	-			NC	-		
D1	NC	-			NC	-		
D15	NC	-			NC	-		
D24	NC	-			NC	-		
D34	NC	-			NC	-		
E10	NC	-			NC	-		
E24	NC	-			NC	-		
E25	NC	-			NC	-		
E26	NC	-			NC	-		
E3	NC	-			NC	-		
E31	NC	-			NC	-		
E32	NC	-			NC	-		
E33	NC	-			NC	-		
E34	NC	-			NC	-		

Date	Version	Section	Change Summary
November 2009 (cont.)	03.5 (cont.)	Pinout Information (cont.)	LatticeECP2M Pin Information Summary, LFE2M50, LFE2M70 and LFE2M100 table - corrected values for LFE2M50, 672 fpBGA in Available DDR-Interfaces per I/O Bank.
			Minor corrections in LFE2M20E/SE and LFE2M35E/SE Logic Signal Connections: 484 fpBGA table.
			Minor corrections in LFE2M50E/SE and LFE2M70E/SE Logic Signal Connections: 900 fpBGA table.
			Minor corrections in LFE2M100E/SE Logic Signal Connections: 900 fpBGA table.
			Updated LFE2-6E/SE and LFE2-12E/SE Logical Signal Connections (changed D1/SPIDS to D1).
		Ordering Information	Updated LatticeECP2M Part Number Description diagram.
March 2010	03.6	DC and Switching Characteristics	Footnote for SED operating frequency added to the sysCONFIG Port Timing Specifications table.
		Pinout Information	Changed Dual Function pin E7 to be D7/SPDI0 in Logic Signal Connections tables. Changed footnote (***) in Logic Signal Connections table.
July 2010	03.7	Architecture	Updated the Typical sysIO Behavior During Power-up text section.
		Pinout Information	Added reference to powerup information.
			Corrected reference to footnote for pins 131 and 132 for the LFE-20E/SE, 208 PQFP.
			Referenced footnote (***) for all D7/SPID0.
			Changed D7*** to D7/SPID0.
			Corrected *** footnote.
		All Sections	Included references to Lattice Diamond design software wherever ispLEVER and ispLeverCORE is specified.
April 2011	03.8	DC and Switching Characteristics	DC Electrical Characteristics table: - Added footnote 3 to I_{IH} - Added footnote 2 to I_{IL} , I_{IH} - Updated C1 and C2 typ. and max. data.
			DLL Timing table – Removed line for t_R and t_F
			LatticeECP2/M sysCONFIG Port Timing Specifications table – added footnote to t_{DINIT} .
			Figure 3-18 – Corrected label to be PRGM (not PRGMRJ).
		Pinout Information	LFE2-12E/SE and LFE-20/SE Logical Signal Connections for 208 PQFP – Corrected Dual Function information for pins 112, 114, 117, 119.
January 2012	03.9	Multiple	Removed references to ispLEVER design software.
		Architecture	Corrected information regarding SED support.
		DC and Switching Characteristics	Added reference to ESD information.
June 2013	04.0	All	Updated document with new corporate logo.
		Architecture	Architecture Overview – Added information on the state of the register on power up and after configuration.