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Applications of Embedded - FPGAs

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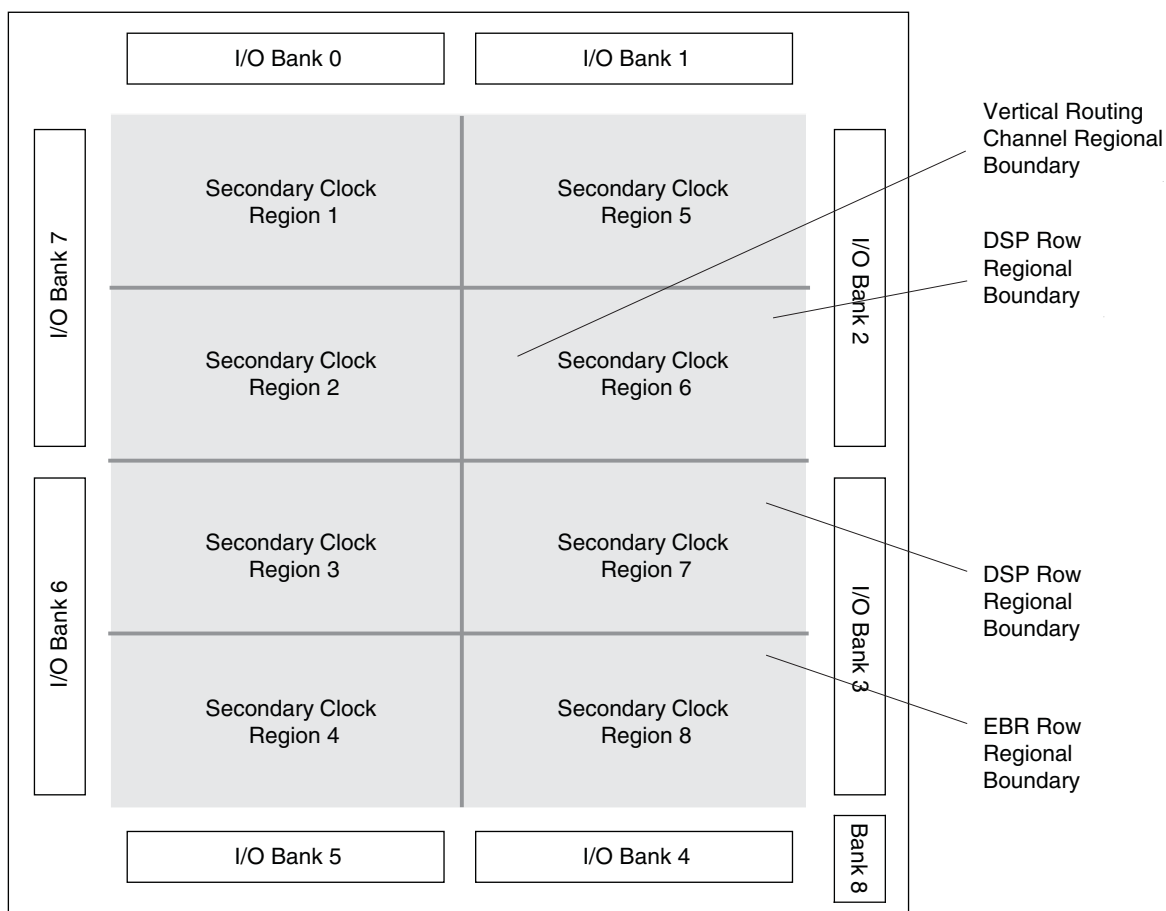
Details

Product Status	Active
Number of LABs/CLBs	6000
Number of Logic Elements/Cells	48000
Total RAM Bits	4246528
Number of I/O	410
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	900-BBGA
Supplier Device Package	900-FPBGA (31x31)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfe2m50se-5fn900c

this special vertical routing channel and the eight secondary clock regions for the ECP2-50. LatticeECP2 devices have four secondary clocks (SC0 to SC3) which are distributed to every region.

The secondary clock muxes are located in the center of the device. Figure 2-16 shows the mux structure of the secondary clock routing. Secondary clocks SC0 to SC3 are used for clock and control and SC4 to SC7 are used for high fan-out signals.

Figure 2-15. Secondary Clock Regions ECP2-50



one clock is selected for each input register, pipeline register and output register. Similarly Clock enable (CE) and Reset (RST) are selected from their four respective sources (CE0, CE1, CE2, CE3 and RST0, RST1, RST2, RST3) at each input register, pipeline register and output register.

Signed and Unsigned with Different Widths

The DSP block supports different widths of signed and unsigned multipliers besides x9, x18 and x36 widths. For unsigned operands, unused upper data bits should be filled to create a valid x9, x18 or x36 operand. For signed two's complement operands, sign extension of the most significant bit should be performed until x9, x18 or x36 width is reached. Table 2-8 provides an example of this.

Table 2-8. Sign Extension Example

Number	Unsigned	Unsigned 9-bit	Unsigned 18-bit	Signed	Two's Complement Signed 9 Bits	Two's Complement Signed 18 Bits
+5	0101	000000101	0000000000000000101	0101	000000101	0000000000000000101
-6	N/A	N/A	N/A	1010	11111010	111111111111111010

OVERFLOW Flag from MAC

The sysDSP block provides an overflow output to indicate that the accumulator has overflowed. When two unsigned numbers are added and the result is a smaller number than the accumulator, “roll-over” is said to have occurred and an overflow signal is indicated. When two positive numbers are added with a negative sum and when two negative numbers are added with a positive sum, then the accumulator “roll-over” is said to have occurred and an overflow signal is indicated. Note that when overflow occurs the overflow flag is present for only one cycle. By counting these overflow pulses in FPGA logic, larger accumulators can be constructed. The conditions overflow signals for signed and unsigned operands are listed in Figure 2-27.

Figure 2-27. Accumulator Overflow/Underflow

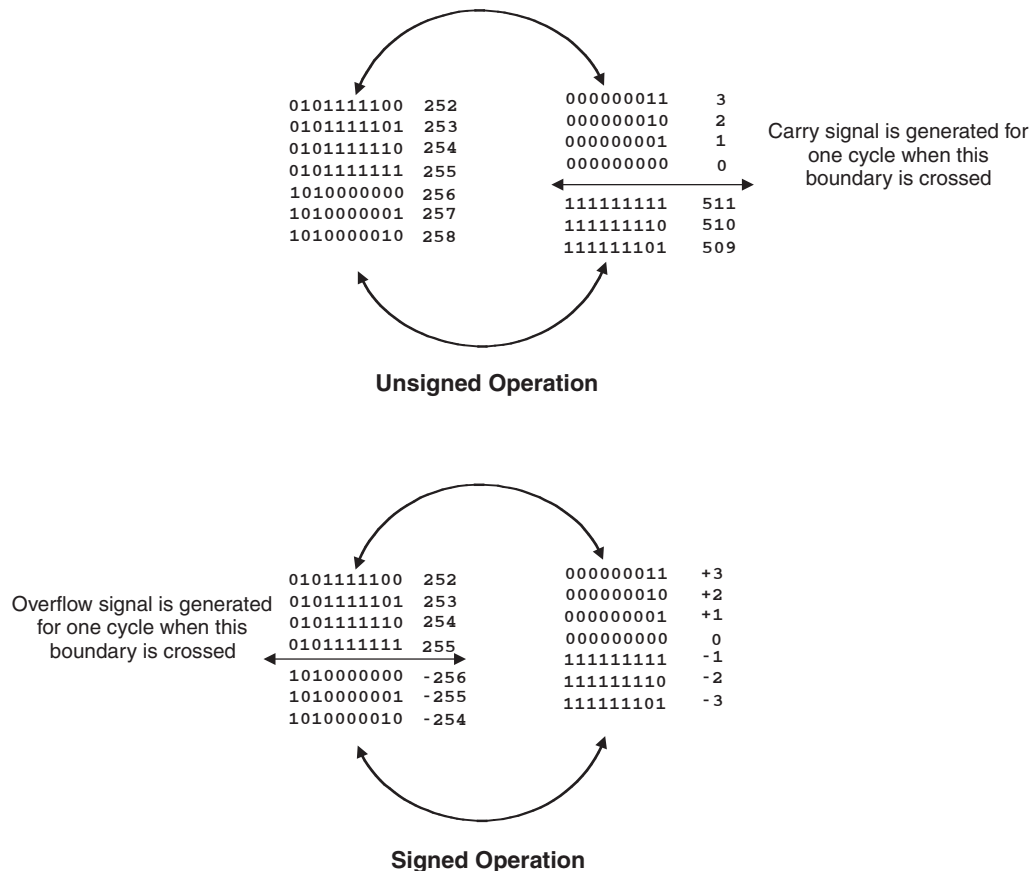
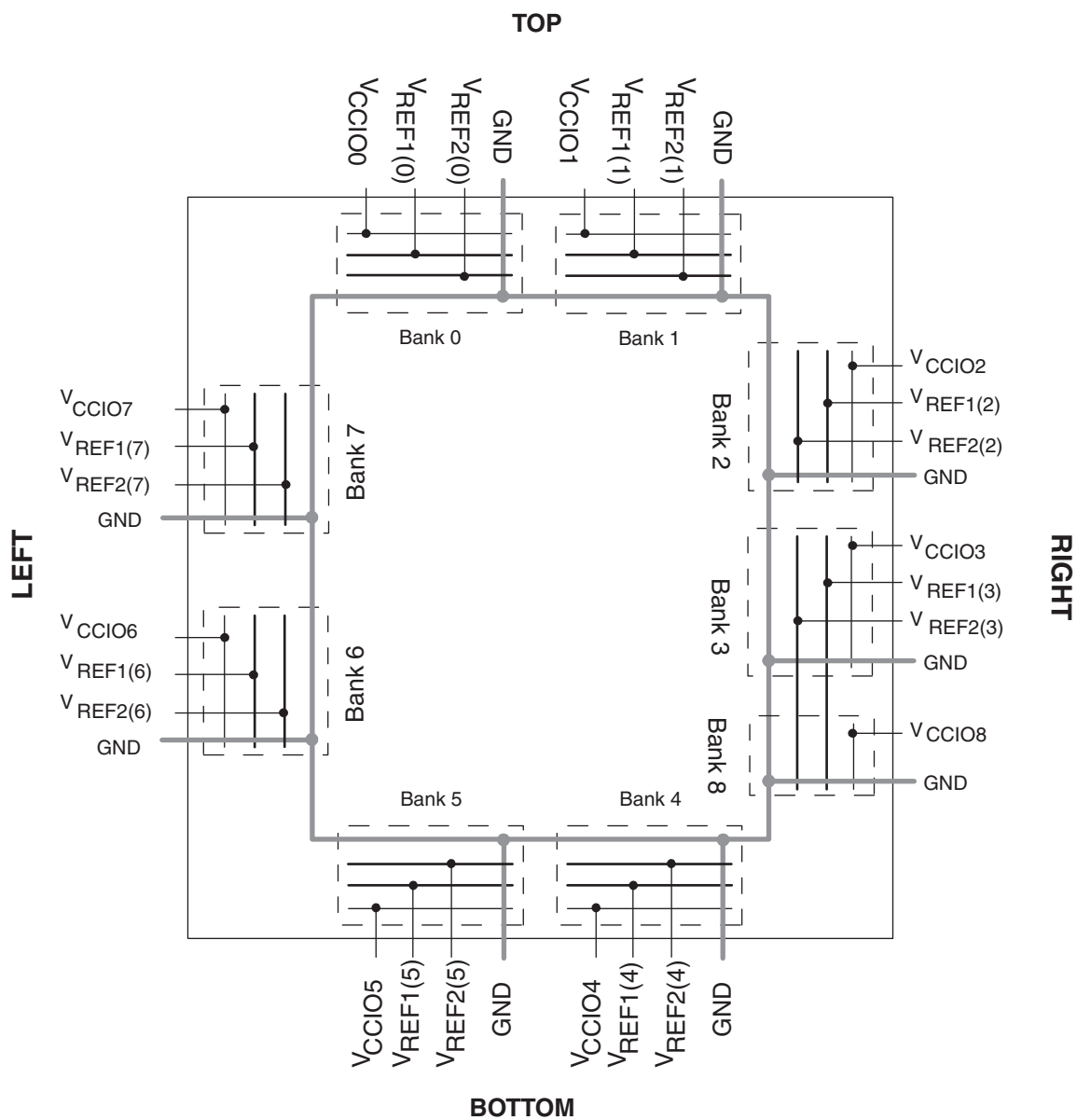


Figure 2-37. LatticeECP2 Banks



DC Electrical Characteristics

Over Recommended Operating Conditions

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
$I_{IL}, I_{IH}^{1,2}$	Input or I/O Low Leakage	$0 \leq V_{IN} \leq (V_{CCIO} - 0.2V)$	—	—	10	μA
$I_{IH}^{1,3}$	Input or I/O High Leakage	$(V_{CCIO} - 0.2V) < V_{IN} \leq 3.6V$	—	—	150	μA
I_{PU}	I/O Active Pull-up Current	$0 \leq V_{IN} \leq 0.7 V_{CCIO}$	-30	—	-210	μA
I_{PD}	I/O Active Pull-down Current	$V_{IL} (MAX) \leq V_{IN} \leq V_{IH} (MAX)$	30	—	210	μA
I_{BHLS}	Bus Hold Low Sustaining Current	$V_{IN} = V_{IL} (MAX)$	30	—	—	μA
I_{BHHS}	Bus Hold High Sustaining Current	$V_{IN} = 0.7 V_{CCIO}$	-30	—	—	μA
I_{BHLO}	Bus Hold Low Overdrive Current	$0 \leq V_{IN} \leq V_{CCIO}$	—	—	210	μA
I_{BHHO}	Bus Hold High Overdrive Current	$0 \leq V_{IN} \leq V_{CCIO}$	—	—	-210	μA
V_{BHT}	Bus Hold Trip Points	$0 \leq V_{IN} \leq V_{IH} (MAX)$	$V_{IL} (MAX)$	—	$V_{IH} (MIN)$	V
$C1^4$	I/O Capacitance	$V_{CCIO} = 3.3V, 2.5V, 1.8V, 1.5V, 1.2V,$ $V_{CC} = 1.2V, V_{IO} = 0 \text{ to } V_{IH} (MAX)$	—	5	8	pf
$C2^4$	Dedicated Input Capacitance	$V_{CCIO} = 3.3V, 2.5V, 1.8V, 1.5V, 1.2V,$ $V_{CC} = 1.2V, V_{IO} = 0 \text{ to } V_{IH} (MAX)$	—	5	6	pf

1. Input or I/O leakage current is measured with the pin configured as an input or as an I/O with the output driver tri-stated. It is not measured with the output driver active. Bus maintenance circuits are disabled.
2. When used as V_{REF} maximum leakage = 25 μA
3. Applicable to general purpose I/Os in top and bottom banks.
4. T_A 25°C, $f = 1.0MHz$.

SERDES High-Speed Data Transmitter (LatticeECP2M Family Only)^{1, 2}

Table 3-7. Serial Output Timing and Levels

Symbol	Description	Frequency	Min.	Typ.	Max.	Units
V _{TX-DIFF-P-P-1}	Differential swing (1V setting) ^{1, 2}	0.25 to 3.125 Gbps	0.79	0.99	1.19	V, p-p
V _{TX-DIFF-P-P-1.25}	Differential swing (1.25V setting) ^{1, 2}	0.25 to 3.125 Gbps	1.00	1.25	1.50	V, p-p
V _{TX-DIFF-P-P-1.3}	Differential swing (1.3V setting) ^{1, 2}	0.25 to 3.125 Gbps	1.04	1.30	1.56	V, p-p
V _{TX-DIFF-P-P-1.35}	Differential swing (1.35V setting) ^{1, 2}	0.25 to 3.125 Gbps	1.08	1.35	1.62	V, p-p
V _{OCM}	Output common mode voltage	—	V _{CCOB} - 0.75	V _{CCOB} - 0.60	V _{CCOB} - 0.45	V
T _{TX-R}	Rise time (20% to 80%)	—	—	70	—	ps
T _{TX-F}	Fall time (80% to 20%)	—	—	70	—	ps
Z _{TX-OI-SE}	Output impedance 50/75/HiZ K Ohms (single-ended)	—	—	50/70 HiZ	—	Ohms
R _{TX-RL}	Return loss (with package)	—	—	9	—	dB

1. All measurements are with 50 ohm impedance.

2. See TN1124, [LatticeECP2M SERDES/PCS Usage Guide](#) for actual binary settings.

Table 3-8. Channel Output Jitter - x10 Mode

Description	Frequency	Min.	Typ.	Max.	Units
Deterministic	3.125 Gbps	—	0.08	0.12	UI, p-p
Random	3.125 Gbps	—	0.22	0.38	UI, p-p
Total	3.125 Gbps	—	0.33	0.43	UI, p-p
Deterministic	2.5 Gbps	—	0.08	0.17	UI, p-p
Random	2.5 Gbps	—	0.20	0.25	UI, p-p
Total	2.5 Gbps	—	0.25	0.35	UI, p-p
Deterministic	1.25 Gbps	—	0.03	0.10	UI, p-p
Random	1.25 Gbps	—	0.14	0.19	UI, p-p
Total	1.25 Gbps	—	0.17	0.24	UI, p-p
Deterministic	250 Mbps	—	0.04	0.17	UI, p-p
Random	250 Mbps	—	0.12	0.13	UI, p-p
Total	250 Mbps	—	0.15	0.29	UI, p-p

Note: Values are measured with PRBS 2⁷-1, all channels operating, FPGA Logic active, I/Os around SERDES pins quiet, reference clock at x10 mode.

Signal Descriptions (Cont.)

Signal Name	I/O	Description
[LOC]DQS[num]	I/O	DQ input/output pads: T (top), R (right), B (bottom), L (left), DQS, num = ball function number.
[LOC]DQ[num]	I/O	DQ input/output pads: T (top), R (right), B (bottom), L (left), DQ, associated DQS number.
Test and Programming (Dedicated Pins)		
TMS	I	Test Mode Select input, used to control the 1149.1 state machine. Pull-up is enabled during configuration.
TCK	I	Test Clock input pin, used to clock the 1149.1 state machine. No pull-up enabled.
TDI	I	Test Data in pin. Used to load data into device using 1149.1 state machine. After power-up, this TAP port can be activated for configuration by sending appropriate command. (Note: once a configuration port is selected it is locked. Another configuration port cannot be selected until the power-up sequence). Pull-up is enabled during configuration.
TDO	O	Output pin. Test Data Out pin used to shift data out of a device using 1149.1.
VCCJ	—	Power supply pin for JTAG Test Access Port.
Configuration Pads (Used During sysCONFIG)		
CFG[2:0]	I	Mode pins used to specify configuration mode values latched on rising edge of INITN. During configuration, a pull-up is enabled. These are dedicated pins.
INITN	I/O	Open Drain pin. Indicates the FPGA is ready to be configured. During configuration, a pull-up is enabled. It is a dedicated pin.
PROGRAMN	I	Initiates configuration sequence when asserted low. This pin always has an active pull-up. This is a dedicated pin.
DONE	I/O	Open Drain pin. Indicates that the configuration sequence is complete, and the startup sequence is in progress. This is a dedicated pin.
CCLK	I/O	Configuration Clock for configuring an FPGA in sysCONFIG mode.
BUSY/SISPI	I/O	Read control command in SPI or SPI _m mode.
CSN	I	sysCONFIG chip select (active low). During configuration, a pull-up is enabled.
CS1N	I	sysCONFIG chip select (active low). During configuration, a pull-up is enabled.
WRITEN	I	Write Data on Parallel port (active low).
D[0]/SPIFASTN	I/O	sysCONFIG Port Data I/O for Parallel mode. sysCONFIG Port Data I/O for SPI or SPI _m . When using the SPI or SPI _m mode, this pin should either be tied high or low, must not be left floating.
D[1:6]	I/O	sysCONFIG Port Data I/O for Parallel
D[7]/SPID0	I/O	sysCONFIG Port Data I/O for Parallel, SPI, SPI _m
DOUT/CSN	O	Output for serial configuration data (rising edge of CCLK) when using sysCONFIG port.
DI/CSSPI0N	I/O	Input for serial configuration data (clocked with CCLK) when using sysCONFIG port. During configuration, a pull-up is enabled. Output when used in SPI/SPI _m modes.
Dedicated SERDES Signals^{1, 2, 3}		
[LOC]_SQ_VCCAUX33	—	Termination resistor switching power (3.3V). This pin must be tied to 3.3V even if the quad is unused.
[LOC]_SQ_REFCLKN	I	Negative Reference Clock Input
[LOC]_SQ_REFCLKP	I	Positive Reference Clock Input
[LOC]_SQ_VCCP	—	PLL and Reference clock buffer power (1.2V). This pin must be tied to 1.2V even if the quad is unused.

LatticeECP2M Pin Information Summary, LFE2M50, LFE2M70 and LFE2M100 (Cont.)

Pin Type		LFE2M50			LFE2M70		LFE2M100	
		484 fpBGA	672 fpBGA	900 fpBGA	900 fpBGA	1152 fpBGA	900 fpBGA	1152 fpBGA
Available DDR-Interfaces per I/O Bank ¹	Bank0	0	0	0	0	0	0	0
	Bank1	0	0	0	0	0	0	0
	Bank2	2	2	2	4	4	4	4
	Bank3	2	1	1	3	4	3	5
	Bank4	3	1	3	3	3	3	3
	Bank5	2	3	3	2	3	2	3
	Bank6	1	2	2	3	4	3	5
	Bank7	3	3	3	4	4	4	5
	Bank8	0	0	0	0	0	0	0
PCI Capable I/Os per Bank	Bank0	0	0	0	0	0	0	0
	Bank1	0	0	0	0	0	0	0
	Bank2	0	0	0	0	72	0	80
	Bank3	0	0	0	0	64	0	80
	Bank4	50	24	48	48	40	48	44
	Bank5	60	60	50	40	40	40	46
	Bank6	52	54	60	62	66	62	82
	Bank7	60	60	68	70	74	70	90
	Bank8	0	0	0	0	0	0	0

1. Minimum requirement to implement a fully functional 8-bit wide DDR bus. Available DDR interface consists of at least 12 I/Os (1 DQS + 1 DQSB + 8 DQs + 1 DM + Bank VREF1).

LFE2-6E/SE and LFE2-12E/SE Logic Signal Connections: 144 TQFP

LFE2-6E/SE					LFE2-12E/12SE				
Pin Number	Pin/Pad Function	Bank	Dual Function	Differential	Pin/Pad Function	Bank	Dual Function	Differential	
1	PL2A	7	VREF2_7	T (LVDS)*	PL2A	7	VREF2_7	T (LVDS)*	
2	PL2B	7	VREF1_7	C (LVDS)*	PL2B	7	VREF1_7	C (LVDS)*	
3	PL4A	7		T (LVDS)*	PL4A	7		T (LVDS)*	
4	PL4B	7		C (LVDS)*	PL4B	7		C (LVDS)*	
5	PL6A	7	LDQ10	T (LVDS)*	PL6A	7	LDQ10	T (LVDS)*	
6	VCCAUX	-			VCCAUX	-			
7	PL6B	7	LDQ10	C (LVDS)*	PL6B	7	LDQ10	C (LVDS)*	
8	PL8A	7	LDQ10	T (LVDS)*	PL8A	7	LDQ10	T (LVDS)*	
9	VCCIO7	7			VCCIO7	7			
10	PL8B	7	LDQ10	C (LVDS)*	PL8B	7	LDQ10	C (LVDS)*	
11	GND	-			GND	-			
12	PL12A	7	LDQ10	T (LVDS)*	PL12A	7	LDQ10	T (LVDS)*	
13	PL12B	7	LDQ10	C (LVDS)*	PL12B	7	LDQ10	C (LVDS)*	
14	PL13A	7	PCLKT7_0/LDQ10	T	PL13A	7	PCLKT7_0/LDQ10	T	
15	PL13B	7	PCLKC7_0/LDQ10	C	PL13B	7	PCLKC7_0/LDQ10	C	
16	VCC	-			VCC	-			
17	PL15A	6	PCLKT6_0	T (LVDS)*	PL15A	6	PCLKT6_0	T (LVDS)*	
18	PL15B	6	PCLKC6_0	C (LVDS)*	PL15B	6	PCLKC6_0	C (LVDS)*	
19	PL16A	6	VREF2_6	T	PL16A	6	VREF2_6	T	
20	PL16B	6	VREF1_6	C	PL16B	6	VREF1_6	C	
21	GND	-			GND	-			
22	VCC	-			VCC	-			
23	PL18A	6	LLM0_GDLLT_FB_A	T	PL18A	6	LLM0_GDLLT_FB_A	T	
24	PL18B	6	LLM0_GDLLC_FB_A	C	PL18B	6	LLM0_GDLLC_FB_A	C	
25	LLM0_PLCCAP	6			LLM0_PLCCAP	6			
26	PL20A	6	LLM0_GPLLT_IN_A**	T (LVDS)*	PL20A	6	LLM0_GPLLT_IN_A**	T (LVDS)*	
27	PL20B	6	LLM0_GPLLC_IN_A**	C (LVDS)*	PL20B	6	LLM0_GPLLC_IN_A**	C (LVDS)*	
28	PL22A	6			PL22A	6			
29	VCC	-			VCC	-			
30	GND	-			GND	-			
31	VCCIO6	6			VCCIO6	6			
32	TCK	-			TCK	-			
33	TDI	-			TDI	-			
34	TDO	-			TDO	-			
35	VCCJ	-			VCCJ	-			
36	TMS	-			TMS	-			
37	PB2A	5	VREF2_5/BDQ6	T	PB2A	5	VREF2_5/BDQ6	T	
38	PB2B	5	VREF1_5/BDQ6	C	PB2B	5	VREF1_5/BDQ6	C	
39	VCCAUX	-			VCCAUX	-			
40	PB4A	5	BDQ6	T	PB6A	5	BDQS6	T	
41	PB4B	5	BDQ6	C	PB6B	5	BDQ6	C	
42	VCCIO5	5			VCCIO5	5			
43	PB6A	5	BDQS6	T	PB12A	5	BDQ15	T	
44	PB6B	5	BDQ6	C	PB12B	5	BDQ15	C	
45	NC	5			PB16A	5	BDQ15	T	

LFE2-20E/SE and LFE2-35E/SE Logic Signal Connections: 672 fpBGA (Cont.)

LFE2-20E/20SE					LFE2-35E/35SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential	
AE17	PB51B	4	BDQ51	C	PB51B	4	BDQ51	C	
AB19	PB52A	4	BDQ51	T	PB52A	4	BDQ51	T	
AE19	PB52B	4	BDQ51	C	PB52B	4	BDQ51	C	
AF17	PB53A	4	BDQ51	T	PB53A	4	BDQ51	T	
AE18	PB53B	4	BDQ51	C	PB53B	4	BDQ51	C	
VCCIO	VCCIO4	4			VCCIO4	4			
W16	PB54A	4	BDQ51	T	PB54A	4	BDQ51	T	
AA17	PB54B	4	BDQ51	C	PB54B	4	BDQ51	C	
AF18	PB55A	4	BDQ51	T	PB55A	4	BDQ51	T	
AF19	PB55B	4	BDQ51	C	PB55B	4	BDQ51	C	
GND	GNDIO4	-			GNDIO4	-			
AA19	NC	-			PB56A	4	BDQ60	T	
W17	NC	-			PB56B	4	BDQ60	C	
Y19	NC	-			PB57A	4	BDQ60	T	
Y17	NC	-			PB57B	4	BDQ60	C	
AF20	NC	-			NC	-			
VCCIO	VCCIO4	4			VCCIO4	4			
AE20	NC	-			NC	-			
AA20	NC	-			NC	-			
W18	NC	-			NC	-			
AD20	NC	-			NC	-			
GND	GNDIO4	-			GNDIO4	-			
AE21	NC	-			NC	-			
AF21	NC	-			NC	-			
AF22	NC	-			NC	-			
VCCIO	VCCIO4	4			VCCIO4	4			
GND	GNDIO4	-			GNDIO4	-			
AE22	PB56A	4	BDQ60	T	PB65A	4	BDQ69	T	
AD22	PB56B	4	BDQ60	C	PB65B	4	BDQ69	C	
AF23	PB57A	4	BDQ60	T	PB66A	4	BDQ69	T	
AE23	PB57B	4	BDQ60	C	PB66B	4	BDQ69	C	
AD23	PB58A	4	BDQ60	T	PB67A	4	BDQ69	T	
AC23	PB58B	4	BDQ60	C	PB67B	4	BDQ69	C	
VCCIO	VCCIO4	4			VCCIO4	4			
AB20	PB59A	4	BDQ60	T	PB68A	4	BDQ69	T	
AC20	PB59B	4	BDQ60	C	PB68B	4	BDQ69	C	
GND	GNDIO4	-			GNDIO4	-			
AB21	PB60A	4	BDQS60	T	PB69A	4	BDQS69	T	
AC22	PB60B	4	BDQ60	C	PB69B	4	BDQ69	C	
W19	PB61A	4	BDQ60	T	PB70A	4	BDQ69	T	
AA21	PB61B	4	BDQ60	C	PB70B	4	BDQ69	C	
AF24	PB62A	4	BDQ60	T	PB71A	4	BDQ69	T	
AE24	PB62B	4	BDQ60	C	PB71B	4	BDQ69	C	
VCCIO	VCCIO4	4			VCCIO4	4			
Y20	PB63A	4	BDQ60	T	PB72A	4	BDQ69	T	
AB22	PB63B	4	BDQ60	C	PB72B	4	BDQ69	C	

LFE2-50E/SE and LFE2-70E/SE Logic Signal Connections: 672 fpBGA (Cont.)

LFE2-50E/SE					LFE2-70E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential	
G24	PR14B	2	RDQ16	C (LVDS)*	PR27B	2	RDQ29	C (LVDS)*	
G23	PR14A	2	RDQ16	T (LVDS)*	PR27A	2	RDQ29	T (LVDS)*	
VCCIO	VCCIO2	2			VCCIO2	2			
K19	PR13B	2	RDQ16	C	PR26B	2	RDQ29	C	
J19	PR13A	2	RDQ16	T	PR26A	2	RDQ29	T	
D26	PR12B	2	RDQ16	C (LVDS)*	PR25B	2	RDQ29	C (LVDS)*	
C26	PR12A	2	RDQ16	T (LVDS)*	PR25A	2	RDQ29	T (LVDS)*	
F22	PR11B	2	RDQ8	C	PR24B	2	RDQ21	C	
E24	PR11A	2	RDQ8	T	PR24A	2	RDQ21	T	
GND	GNDIO2	-			GNDIO2	-			
D25	PR10B	2	RDQ8	C (LVDS)*	PR23B	2	RDQ21	C (LVDS)*	
C25	PR10A	2	RDQ8	T (LVDS)*	PR23A	2	RDQ21	T (LVDS)*	
D24	PR9B	2	RDQ8	C	PR22B	2	RDQ21	C	
B25	PR9A	2	RDQ8	T	PR22A	2	RDQ21	T	
VCCIO	VCCIO2	2			VCCIO2	2			
H21	PR8B	2	RDQ8	C (LVDS)*	PR21B	2	RDQ21	C (LVDS)*	
G22	PR8A	2	RDQS8	T (LVDS)*	PR21A	2	RDQS21	T (LVDS)*	
B24	PR7B	2	RDQ8	C	PR20B	2	RDQ21	C	
GND	GNDIO2	-			GNDIO2	-			
C24	PR7A	2	RDQ8	T	PR20A	2	RDQ21	T	
D23	PR6B	2	RDQ8	C (LVDS)*	PR19B	2	RDQ21	C (LVDS)*	
C23	PR6A	2	RDQ8	T (LVDS)*	PR19A	2	RDQ21	T (LVDS)*	
G21	PR5B	2	RDQ8	C	PR18B	2	RDQ21	C	
VCCIO	VCCIO2	2			VCCIO2	2			
H20	PR5A	2	RDQ8	T	PR18A	2	RDQ21	T	
GND	GNDIO2	-			GNDIO2	-			
E22	PR2B	2	VREF2_2	C (LVDS)*	PR2B	2	VREF2_2	C (LVDS)*	
F21	PR2A	2	VREF1_2	T (LVDS)*	PR2A	2	VREF1_2	T (LVDS)*	
E23	PT82B	1	VREF2_1	C	PT100B	1	VREF2_1	C	
GND	GNDIO1	-			GNDIO1	-			
D22	PT82A	1	VREF1_1	T	PT100A	1	VREF1_1	T	
G20	PT81B	1		C	PT99B	1		C	
J18	PT81A	1		T	PT99A	1		T	
F20	PT80B	1		C	PT98B	1		C	
VCCIO	VCCIO1	1			VCCIO1	1			
H19	PT80A	1		T	PT98A	1		T	
A24	PT79B	1		C	PT97B	1		C	
A23	PT79A	1		T	PT97A	1		T	
E21	PT78B	1		C	PT96B	1		C	
F19	PT78A	1		T	PT96A	1		T	
C22	PT77B	1		C	PT95B	1		C	
GND	GNDIO1	-			GNDIO1	-			
E20	PT77A	1		T	PT95A	1		T	
B22	PT76B	1		C	PT94B	1		C	
VCCIO	VCCIO1	1			VCCIO1	1			
B23	PT76A	1		T	PT94A	1		T	

LFE2-50E/SE and LFE2-70E/SE Logic Signal Connections: 672 fpBGA (Cont.)

LFE2-50E/SE					LFE2-70E/SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
A7	PT35B	0		C	PT44B	0		C
B7	PT35A	0		T	PT44A	0		T
VCCIO	VCCIO0	0			VCCIO0	0		
F12	PT34B	0		C	PT43B	0		C
D10	PT34A	0		T	PT43A	0		T
H11	PT33B	0		C	PT42B	0		C
G11	PT33A	0		T	PT42A	0		T
GND	GNDIO0	-			GNDIO0	-		
A6	PT32B	0		C	PT41B	0		C
B6	PT32A	0		T	PT41A	0		T
D8	PT31B	0		C	PT40B	0		C
C8	PT31A	0		T	PT40A	0		T
VCCIO	VCCIO0	0			VCCIO0	0		
F11	PT30B	0		C	PT39B	0		C
E10	PT30A	0		T	PT39A	0		T
E9	PT29B	0		C	PT38B	0		C
D9	PT29A	0		T	PT38A	0		T
G10	PT28B	0		C	PT37B	0		C
GND	GNDIO0	-			GNDIO0	-		
H10	PT28A	0		T	PT37A	0		T
A5	PT27B	0		C	PT36B	0		C
B5	PT27A	0		T	PT36A	0		T
C7	PT26B	0		C	PT35B	0		C
VCCIO	VCCIO0	0			VCCIO0	0		
D7	PT26A	0		T	PT35A	0		T
E8	PT25B	0		C	PT34B	0		C
F10	PT25A	0		T	PT34A	0		T
F8	PT24B	0		C	PT33B	0		C
H9	PT24A	0		T	PT33A	0		T
C5	PT23B	0		C	PT32B	0		C
GND	GNDIO0	-			GNDIO0	-		
D5	PT23A	0		T	PT32A	0		T
B4	PT22B	0			PT31B	0		
VCCIO	VCCIO0	0			VCCIO0	0		
GND	GNDIO0	-			GNDIO0	-		
VCCIO	VCCIO0	0			VCCIO0	0		
GND	GNDIO0	-			GNDIO0	-		
VCCIO	VCCIO0	0			VCCIO0	0		
C4	PT10B	0		C	PT10B	0		C
GND	GNDIO0	-			GNDIO0	-		
C3	PT10A	0		T	PT10A	0		T
A4	PT9B	0		C	PT9B	0		C
A3	PT9A	0		T	PT9A	0		T
B3	PT8B	0		C	PT8B	0		C
VCCIO	VCCIO0	0			VCCIO0	0		
B2	PT8A	0		T	PT8A	0		T

LFE2-50E/SE and LFE2-70E/SE Logic Signal Connections: 672 fpBGA (Cont.)

LFE2-50E/SE					LFE2-70E/SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
L23	VCCIO2	2			VCCIO2	2		
M17	VCCIO2	2			VCCIO2	2		
M18	VCCIO2	2			VCCIO2	2		
AA23	VCCIO3	3			VCCIO3	3		
R17	VCCIO3	3			VCCIO3	3		
R18	VCCIO3	3			VCCIO3	3		
T23	VCCIO3	3			VCCIO3	3		
V20	VCCIO3	3			VCCIO3	3		
AC16	VCCIO4	4			VCCIO4	4		
AC21	VCCIO4	4			VCCIO4	4		
U15	VCCIO4	4			VCCIO4	4		
V15	VCCIO4	4			VCCIO4	4		
Y18	VCCIO4	4			VCCIO4	4		
AC11	VCCIO5	5			VCCIO5	5		
AC6	VCCIO5	5			VCCIO5	5		
U12	VCCIO5	5			VCCIO5	5		
V12	VCCIO5	5			VCCIO5	5		
Y9	VCCIO5	5			VCCIO5	5		
AA4	VCCIO6	6			VCCIO6	6		
R10	VCCIO6	6			VCCIO6	6		
R9	VCCIO6	6			VCCIO6	6		
T4	VCCIO6	6			VCCIO6	6		
V7	VCCIO6	6			VCCIO6	6		
F4	VCCIO7	7			VCCIO7	7		
J7	VCCIO7	7			VCCIO7	7		
L4	VCCIO7	7			VCCIO7	7		
M10	VCCIO7	7			VCCIO7	7		
M9	VCCIO7	7			VCCIO7	7		
AE25	VCCIO8	8			VCCIO8	8		
V18	VCCIO8	8			VCCIO8	8		
J10	VCCAUX	-			VCCAUX	-		
J11	VCCAUX	-			VCCAUX	-		
J16	VCCAUX	-			VCCAUX	-		
J17	VCCAUX	-			VCCAUX	-		
K18	VCCAUX	-			VCCAUX	-		
K9	VCCAUX	-			VCCAUX	-		
L18	VCCAUX	-			VCCAUX	-		
L9	VCCAUX	-			VCCAUX	-		
T18	VCCAUX	-			VCCAUX	-		
T9	VCCAUX	-			VCCAUX	-		
U18	VCCAUX	-			VCCAUX	-		
U9	VCCAUX	-			VCCAUX	-		
V10	VCCAUX	-			VCCAUX	-		
V11	VCCAUX	-			VCCAUX	-		
V16	VCCAUX	-			VCCAUX	-		
V17	VCCAUX	-			VCCAUX	-		

LFE2-70E/SE Logic Signal Connections: 900 fpBGA (Cont.)

LFE2-70E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential
E27	NC	-		
E28	NC	-		
E29	NC	-		
E3	NC	-		
E30	NC	-		
E4	NC	-		
E5	NC	-		
E6	NC	-		
F25	NC	-		
F5	NC	-		
F6	NC	-		
G6	NC	-		
G7	NC	-		
K10	NC	-		
K9	NC	-		
N27	NC	-		
N4	NC	-		
R1	NC	-		
R2	NC	-		
V27	NC	-		
V4	NC	-		
P22	VCCPLL	-		
P8	VCCPLL	-		
T22	VCCPLL	-		
Y7	VCCPLL	-		

* Supports true LVDS. Other differential signals must be emulated with external resistors.

** These dedicated input pins can be used for GPLLs or GDLLs within the respective quadrant.

***Due to packaging bond out option, this DQS does not have all the necessary DQ pins bonded out for a full 8-bit data width.

Note: VCCIO and GND pads are used to determine the average DC current drawn by I/Os between GND/VCCIO connections, or between the last GND/VCCIO in an I/O bank and the end of an I/O bank. The substrate pads listed in the Pin Table do not necessarily have a one to one connection with a package ball or pin.

LFE2M-20E/SE and LFE2M-35E/SE Logic Signal Connections: 256 fpBGA (Cont.)

LFE2M20E/SE					LFE2M35E/SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
GNDIO	GNDIO6	-			GNDIO6	-		
L1	PL42A	6	LLM0_GPLLT_IN_A	T (LVDS)*	PL57A	6	LLM0_GPLLT_IN_A**/LDQS57***	T (LVDS)*
GNDIO	GNDIO6	-			GNDIO6	-		
L2	PL42B	6	LLM0_GPLLC_IN_A	C (LVDS)*	PL57B	6	LLM0_GPLLC_IN_A**/LDQ57	C (LVDS)*
L3	PL43A	6	LLM0_GPLLT_FB_A	T	PL58A	6	LLM0_GPLLT_FB_A/LDQ57	T
L4	PL43B	6	LLM0_GPLLC_FB_A	C	PL58B	6	LLM0_GPLLC_FB_A/LDQ57	C
VCCIO	VCCIO6	6			VCCIO6	6		
M1	PL44A	6	LLM0_GDLLT_IN_A	T (LVDS)*	PL59A	6	LLM0_GDLLT_IN_A**/LDQ57	T (LVDS)*
N1	PL44B	6	LLM0_GDLLC_IN_A	C (LVDS)*	PL59B	6	LLM0_GDLLC_IN_A**/LDQ57	C (LVDS)*
N2	PL45A	6	LLM0_GDLLT_FB_A	T	PL60A	6	LLM0_GDLLT_FB_A/LDQ57	T
N3	PL45B	6	LLM0_GDLLC_FB_A	C	PL60B	6	LLM0_GDLLC_FB_A/LDQ57	C
GNDIO	GNDIO6	-			GNDIO6	-		
M4	LLM0_PLLCAP	6			LLM0_PLLCAP	6		
VCCIO	VCCIO6	6			VCCIO6	6		
GNDIO	GNDIO6	-			GNDIO6	-		
K6	TCK	-			TCK	-		
L5	TDI	-			TDI	-		
N4	TMS	-			TMS	-		
N6	TDO	-			TDO	-		
K7	VCCJ	-			VCCJ	-		
M5	PB2A	5	BDQ6	T	PB2A	5	BDQ6	T
N5	PB2B	5	BDQ6	C	PB2B	5	BDQ6	C
L6	PB3A	5	BDQ6	T	PB3A	5	BDQ6	T
M6	PB3B	5	BDQ6	C	PB3B	5	BDQ6	C
P3	PB4A	5	BDQ6	T	PB4A	5	BDQ6	T
VCCIO	VCCIO5	5			VCCIO5	5		
P4	PB4B	5	BDQ6	C	PB4B	5	BDQ6	C
P2	PB5A	5	BDQ6	T	PB5A	5	BDQ6	T
P1	PB5B	5	BDQ6	C	PB5B	5	BDQ6	C
R1	PB6A	5	BDQS6	T	PB6A	5	BDQS6	T
GNDIO	GNDIO5	-			GNDIO5	-		
R2	PB6B	5	BDQ6	C	PB6B	5	BDQ6	C
R3	PB7A	5	BDQ6	T	PB7A	5	BDQ6	T
T2	PB7B	5	BDQ6	C	PB7B	5	BDQ6	C
R4	PB8A	5	BDQ6	T	PB8A	5	BDQ6	T
VCCIO	VCCIO5	5			VCCIO5	5		
T3	PB8B	5	BDQ6	C	PB8B	5	BDQ6	C
T4	PB10A	5	BDQ6	T	PB10A	5	BDQ6	T
GNDIO	GNDIO5	-			GNDIO5	-		
T5	PB10B	5	BDQ6	C	PB10B	5	BDQ6	C
VCCIO	VCCIO5	5			VCCIO5	5		
GNDIO	GNDIO5	-			GNDIO5	-		
T6	PB16A	5	VREF2_5/BDQ15	T	PB34A	5	VREF2_5/BDQ33	T
R6	PB16B	5	VREF1_5/BDQ15	C	PB34B	5	VREF1_5/BDQ33	C
P6	PB17A	5	PCLKT5_0/BDQ15	T	PB35A	5	PCLKT5_0/BDQ33	T
P7	PB17B	5	PCLKC5_0/BDQ15	C	PB35B	5	PCLKC5_0/BDQ33	C
VCCIO	VCCIO5	5			VCCIO5	5		
GNDIO	GNDIO5	-			GNDIO5	-		

LFE2M35E/SE and LFE2M50E/SE Logic Signal Connections: 672 fpBGA (Cont.)

LFE2M35E/SE					LFE2M50E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential	
L16	GND	-			GND	-			
L17	GND	-			GND	-			
L2	GND	-			GND	-			
L20	GND	-			GND	-			
L25	GND	-			GND	-			
L7	GND	-			GND	-			
M13	GND	-			GND	-			
M14	GND	-			GND	-			
N10	GND	-			GND	-			
N12	GND	-			GND	-			
N13	GND	-			GND	-			
N14	GND	-			GND	-			
N15	GND	-			GND	-			
N17	GND	-			GND	-			
P10	GND	-			GND	-			
P12	GND	-			GND	-			
P13	GND	-			GND	-			
P14	GND	-			GND	-			
P15	GND	-			GND	-			
P17	GND	-			GND	-			
R13	GND	-			GND	-			
R14	GND	-			GND	-			
T10	GND	-			GND	-			
T11	GND	-			GND	-			
T16	GND	-			GND	-			
T17	GND	-			GND	-			
T2	GND	-			GND	-			
T20	GND	-			GND	-			
T25	GND	-			GND	-			
T7	GND	-			GND	-			
U11	GND	-			GND	-			
U13	GND	-			GND	-			
U14	GND	-			GND	-			
U16	GND	-			GND	-			
V22	GND	-			GND	-			
V5	GND	-			GND	-			
Y11	GND	-			GND	-			
Y16	GND	-			GND	-			
AB3	NC	-			NC	-			
AB4	NC	-			NC	-			
AC1	NC	-			NC	-			
AC2	NC	-			NC	-			
B4	NC	-			NC	-			
B5	NC	-			NC	-			
C26	NC	-			NC	-			
D20	NC	-			NC	-			
D21	NC	-			NC	-			
D22	NC	-			NC	-			

LFE2M50E/SE and LFE2M70E/SE Logic Signal Connections: 900 fpBGA (Cont.)

LFE2M50E/SE					LFE2M70E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential	
J16	PT51B	1		C	PT60B	1		C	
G15	PT51A	1		T	PT60A	1		T	
GNDIO	GNDIO1	-			GNDIO1	-			
C16	PT50B	1		C	PT59B	1		C	
D16	PT50A	1		T	PT59A	1		T	
J15	PT49B	1		C	PT58B	1		C	
H15	PT49A	1		T	PT58A	1		T	
VCCIO	VCCIO1	1			VCCIO1	1			
A15	PT48B	1	VREF2_1	C	PT57B	1	VREF2_1	C	
B15	PT48A	1	VREF1_1	T	PT57A	1	VREF1_1	T	
F15	PT47B	1	PCLKC1_0	C	PT56B	1	PCLKC1_0	C	
E16	PT47A	1	PCLKT1_0	T	PT56A	1	PCLKT1_0	T	
C15	PT46B	0	PCLKC0_0	C	PT55B	0	PCLKC0_0	C	
GNDIO	GNDIO0	-			GNDIO0	-			
D15	PT46A	0	PCLKT0_0	T	PT55A	0	PCLKT0_0	T	
C14	PT45B	0	VREF2_0	C	PT54B	0	VREF2_0	C	
E15	PT45A	0	VREF1_0	T	PT54A	0	VREF1_0	T	
G14	PT44B	0		C	PT53B	0		C	
VCCIO	VCCIO0	0			VCCIO0	0			
J14	PT44A	0		T	PT53A	0		T	
F14	PT43B	0		C	PT52B	0		C	
H14	PT43A	0		T	PT52A	0		T	
A14	PT42B	0		C	PT51B	0		C	
B14	PT42A	0		T	PT51A	0		T	
D13	PT41B	0		C	PT50B	0		C	
GNDIO	GNDIO0	-			GNDIO0	-			
F13	PT41A	0		T	PT50A	0		T	
G13	PT40B	0		C	PT49B	0		C	
VCCIO	VCCIO0	0			VCCIO0	0			
J11	PT40A	0		T	PT49A	0		T	
D4	PT38B	0		C	PT47B	0		C	
D5	PT38A	0		T	PT47A	0		T	
E5	PT37B	0		C	PT46B	0		C	
F6	PT37A	0		T	PT46A	0		T	
GNDIO	GNDIO0	-			GNDIO0	-			
VCCIO	VCCIO0	0			VCCIO0	0			
F7	PT34B	0		C	PT43B	0		C	
D8	PT34A	0		T	PT43A	0		T	
GNDIO	GNDIO0	-			GNDIO0	-			
J13	PT32B	0		C	PT41B	0		C	
G11	PT32A	0		T	PT41A	0		T	
H13	PT31B	0		C	PT40B	0		C	
H12	PT31A	0		T	PT40A	0		T	
VCCIO	VCCIO0	0			VCCIO0	0			
E8	PT30B	0		C	PT39B	0		C	
D9	PT30A	0		T	PT39A	0		T	
D12	PT28B	0		C	PT37B	0		C	
GNDIO	GNDIO0	-			GNDIO0	-			

LFE2M100E/SE Logic Signal Connections: 900 fpBGA (Cont.)

LFE2M100E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential
AC19	PB96A	4	BDQS96	T
AD20	PB96B	4	BDQ96	C
AB18	PB97A	4	BDQ96	T
AC20	PB97B	4	BDQ96	C
AE20	PB98A	4	BDQ96	T
AE21	PB98B	4	BDQ96	C
VCCIO	VCCIO4	4		
AC23	PB99A	4	BDQ96	T
AD23	PB99B	4	BDQ96	C
GNDIO	GNDIO4	-		
AH18	LRC_SQ_VCCR3	13		
AK19	LRC_SQ_HDINP3	13		T
AJ18	LRC_SQ_VCCIB3	13		
AJ19	LRC_SQ_HDINN3	13		C
AH21	LRC_SQ_VCCTX3	13		
AK22	LRC_SQ_HDOUTP3	13		T
AK21	LRC_SQ_VCCOB3	13		
AJ22	LRC_SQ_HDOUTN3	13		C
AH22	LRC_SQ_VCCTX2	13		
AJ23	LRC_SQ_HDOUTN2	13		C
AH23	LRC_SQ_VCCOB2	13		
AK23	LRC_SQ_HDOUTP2	13		T
AH19	LRC_SQ_VCCR2	13		
AJ20	LRC_SQ_HDINN2	13		C
AH20	LRC_SQ_VCCIB2	13		
AK20	LRC_SQ_HDINP2	13		T
AH24	LRC_SQ_VCCP	13		
AG24	LRC_SQ_REFCLKP	13		T
AF24	LRC_SQ_REFCLKN	13		C
AJ24	LRC_SQ_VCCAUX33	13		
AK28	LRC_SQ_HDINP1	13		T
AH28	LRC_SQ_VCCIB1	13		
AJ28	LRC_SQ_HDINN1	13		C
AH29	LRC_SQ_VCCR1	13		
AK25	LRC_SQ_HDOUTP1	13		T
AH25	LRC_SQ_VCCOB1	13		
AJ25	LRC_SQ_HDOUTN1	13		C
AH26	LRC_SQ_VCCTX1	13		
AJ26	LRC_SQ_HDOUTN0	13		C
AK27	LRC_SQ_VCCOB0	13		
AK26	LRC_SQ_HDOUTP0	13		T
AH27	LRC_SQ_VCCTX0	13		
AJ29	LRC_SQ_HDINN0	13		C

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2-35E-5F484C	331	1.2V	-5	fpBGA	484	COM	35
LFE2-35E-6F484C	331	1.2V	-6	fpBGA	484	COM	35
LFE2-35E-7F484C	331	1.2V	-7	fpBGA	484	COM	35
LFE2-35E-5F672C	450	1.2V	-5	fpBGA	672	COM	35
LFE2-35E-6F672C	450	1.2V	-6	fpBGA	672	COM	35
LFE2-35E-7F672C	450	1.2V	-7	fpBGA	672	COM	35

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2-50E-5F484C	339	1.2V	-5	fpBGA	484	COM	50
LFE2-50E-6F484C	339	1.2V	-6	fpBGA	484	COM	50
LFE2-50E-7F484C	339	1.2V	-7	fpBGA	484	COM	50
LFE2-50E-5F672C	500	1.2V	-5	fpBGA	672	COM	50
LFE2-50E-6F672C	500	1.2V	-6	fpBGA	672	COM	50
LFE2-50E-7F672C	500	1.2V	-7	fpBGA	672	COM	50

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2-70E-5F672C	500	1.2V	-5	fpBGA	672	COM	70
LFE2-70E-6F672C	500	1.2V	-6	fpBGA	672	COM	70
LFE2-70E-7F672C	500	1.2V	-7	fpBGA	672	COM	70
LFE2-70E-5F900C	583	1.2V	-5	fpBGA	900	COM	70
LFE2-70E-6F900C	583	1.2V	-6	fpBGA	900	COM	70
LFE2-70E-7F900C	583	1.2V	-7	fpBGA	900	COM	70

Industrial

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2-6E-5T144I	90	1.2V	-5	TQFP	144	IND	6
LFE2-6E-6T144I	90	1.2V	-6	TQFP	144	IND	6
LFE2-6E-5F256I	190	1.2V	-5	fpBGA	256	IND	6
LFE2-6E-6F256I	190	1.2V	-6	fpBGA	256	IND	6

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2-12E-5T144I	93	1.2V	-5	TQFP	144	IND	12
LFE2-12E-6T144I	93	1.2V	-6	TQFP	144	IND	12
LFE2-12E-5Q208I	131	1.2V	-5	PQFP	208	IND	12
LFE2-12E-6Q208I	131	1.2V	-6	PQFP	208	IND	12
LFE2-12E-5F256I	193	1.2V	-5	fpBGA	256	IND	12
LFE2-12E-6F256I	193	1.2V	-6	fpBGA	256	IND	12
LFE2-12E-5F484I	297	1.2V	-5	fpBGA	484	IND	12
LFE2-12E-6F484I	297	1.2V	-6	fpBGA	484	IND	12

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2M100SE-5FN1152C	520	1.2V	-5	Lead-Free fpBGA	1152	Com	100
LFE2M100SE-6FN1152C	520	1.2V	-6	Lead-Free fpBGA	1152	Com	100
LFE2M100SE-7FN1152C	520	1.2V	-7	Lead-Free fpBGA	1152	Com	100
LFE2M100SE-5FN900C	416	1.2V	-5	Lead-Free fpBGA	900	Com	100
LFE2M100SE-6FN900C	416	1.2V	-6	Lead-Free fpBGA	900	Com	100
LFE2M100SE-7FN900C	416	1.2V	-7	Lead-Free fpBGA	900	Com	100