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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

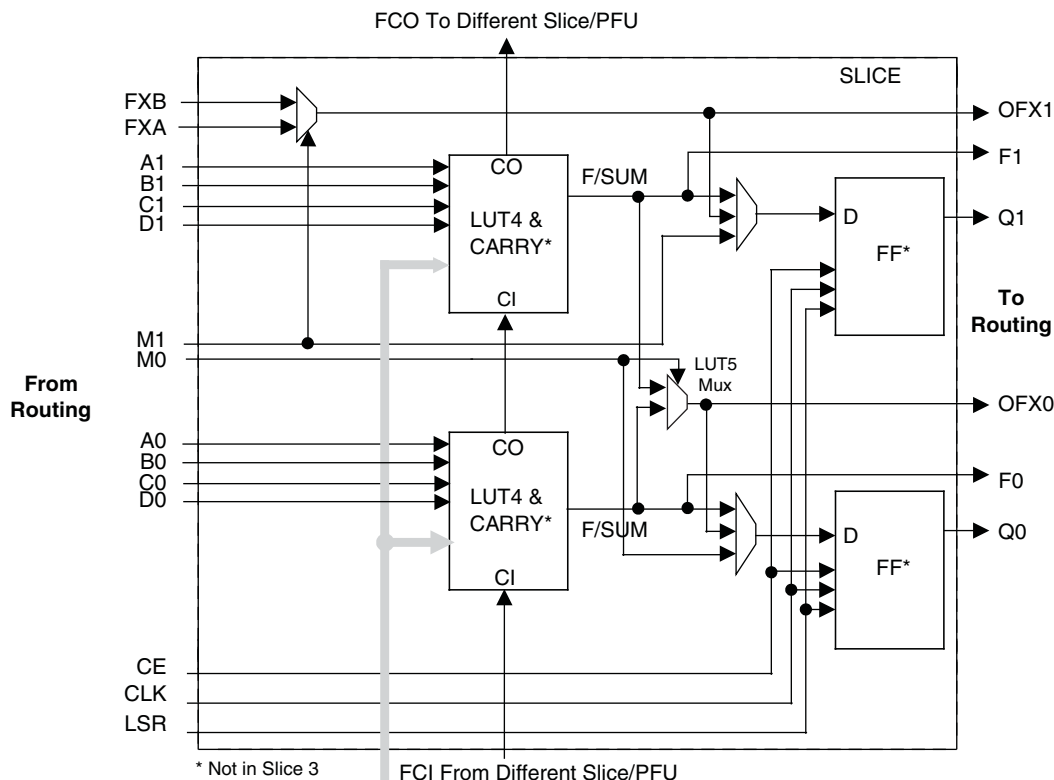
Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details

Product Status	Obsolete
Number of LABs/CLBs	6000
Number of Logic Elements/Cells	48000
Total RAM Bits	4246528
Number of I/O	372
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	672-BBGA
Supplier Device Package	672-FPBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfe2m50se-6f672c

Figure 2-4. Slice Diagram



For Slices 0 and 2, memory control signals are generated from Slice 1 as follows:

WCK is CLK
WRE is from LSR
DI[3:2] for Slice 2 and DI[1:0] for Slice 0 data
WAD [A:D] is a 4bit address from slice 1 LUT input

Table 2-2. Slice Signal Descriptions

Function	Type	Signal Names	Description
Input	Data signal	A0, B0, C0, D0	Inputs to LUT4
Input	Data signal	A1, B1, C1, D1	Inputs to LUT4
Input	Multi-purpose	M0	Multipurpose Input
Input	Multi-purpose	M1	Multipurpose Input
Input	Control signal	CE	Clock Enable
Input	Control signal	LSR	Local Set/Reset
Input	Control signal	CLK	System Clock
Input	Inter-PFU signal	FC	Fast Carry-in ¹
Input	Inter-slice signal	FXA	Intermediate signal to generate LUT6 and LUT7
Input	Inter-slice signal	FXB	Intermediate signal to generate LUT6 and LUT7
Output	Data signals	F0, F1	LUT4 output register bypass signals
Output	Data signals	Q0, Q1	Register outputs
Output	Data signals	OFX0	Output of a LUT5 MUX
Output	Data signals	OFX1	Output of a LUT6, LUT7, LUT8 ² MUX depending on the slice
Output	Inter-PFU signal	FCO	Slice 2 of each PFU is the fast carry chain output ¹

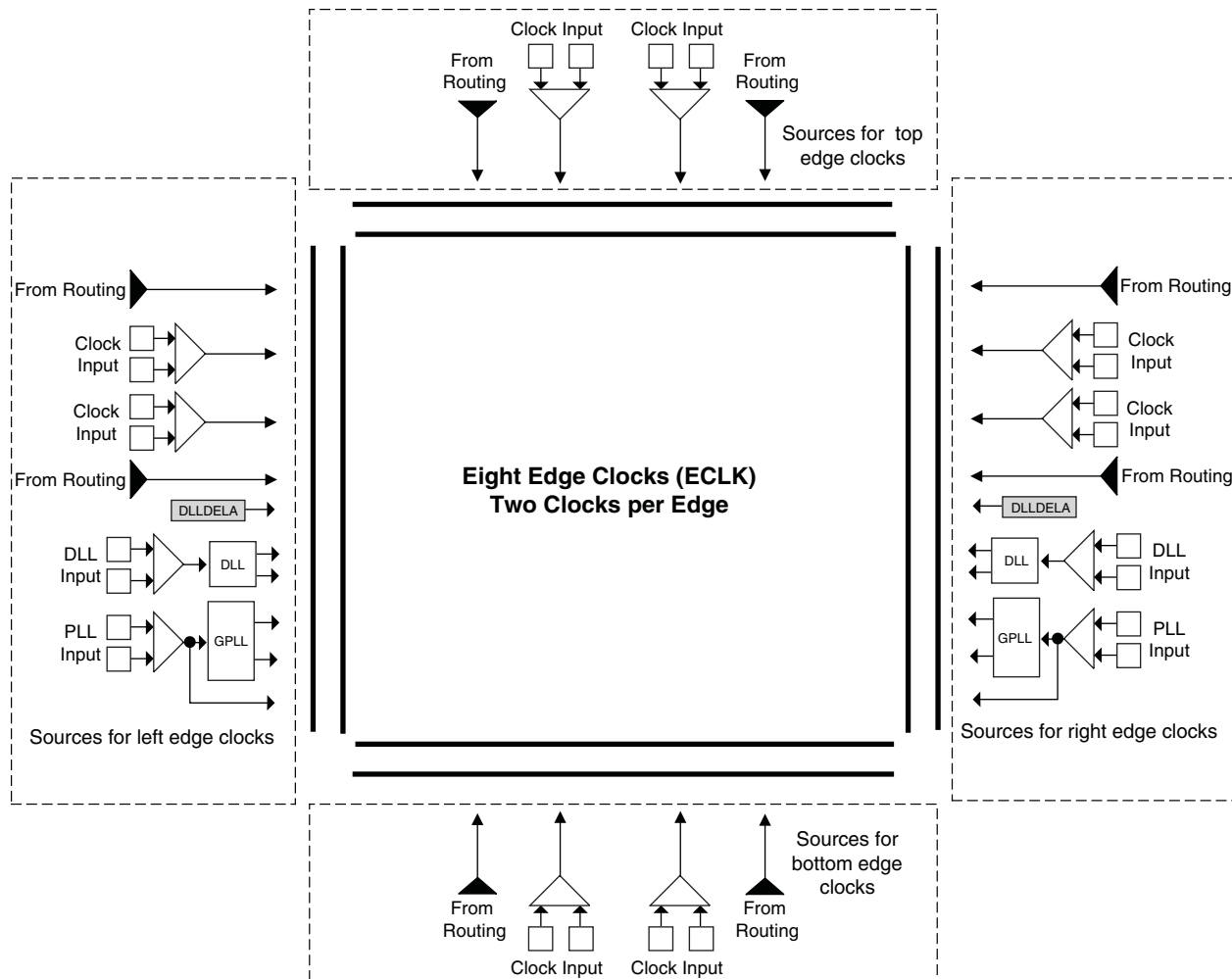
1. See Figure 2-4 for connection details.

2. Requires two PFUs.

Edge Clock Sources

Edge clock resources can be driven from a variety of sources at the same edge. Edge clock resources can be driven from adjacent edge clock PIOs, primary clock PIOs, PLLs/DLLs and clock dividers as shown in Figure 2-12.

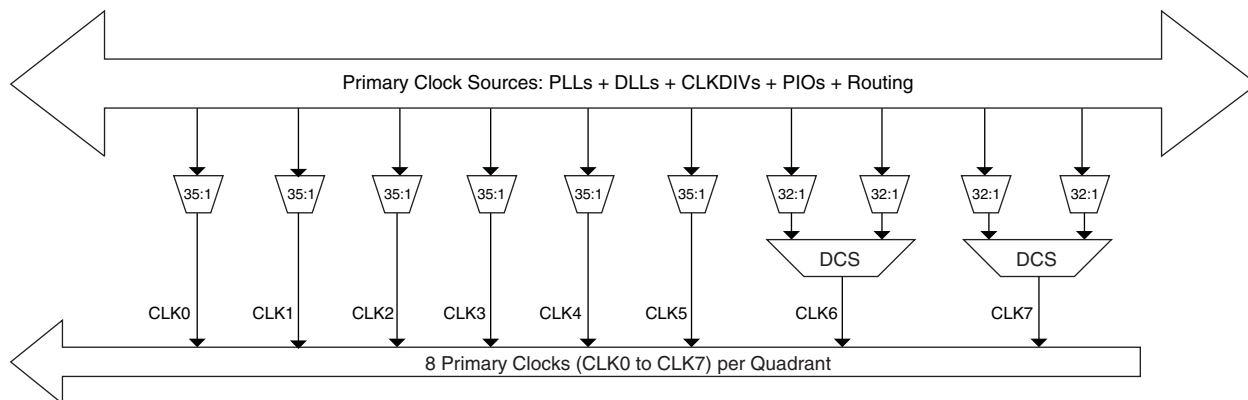
Figure 2-12. Edge Clock Sources



Primary Clock Routing

The clock routing structure in LatticeECP2/M devices consists of a network of eight primary clock lines (CLK0 through CLK7) per quadrant. The primary clocks of each quadrant are generated from muxes located in the center of the device. All the clock sources are connected to these muxes. Figure 2-13 shows the clock routing for one quadrant. Each quadrant mux is identical. If desired, any clock can be routed globally

Figure 2-13. Per Quadrant Primary Clock Selection

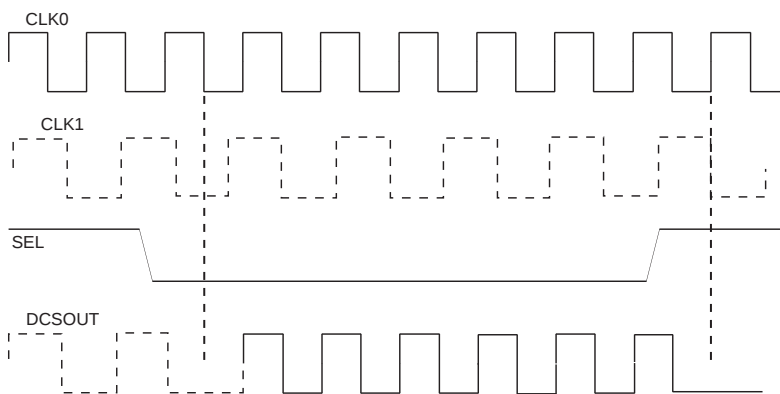


Dynamic Clock Select (DCS)

The DCS is a smart multiplexer function available in the primary clock routing. It switches between two independent input clock sources without any glitches or runt pulses. This is achieved regardless of when the select signal is toggled. There are two DCS blocks per quadrant; in total, there are eight DCS blocks per device. The inputs to the DCS block come from the center muxes. The output of the DCS is connected to primary clocks CLK6 and CLK7 (see Figure 2-13).

Figure 2-14 shows the timing waveforms of the default DCS operating mode. The DCS block can be programmed to other modes. For more information about the DCS, please see the list of additional technical documentation at the end of this data sheet.

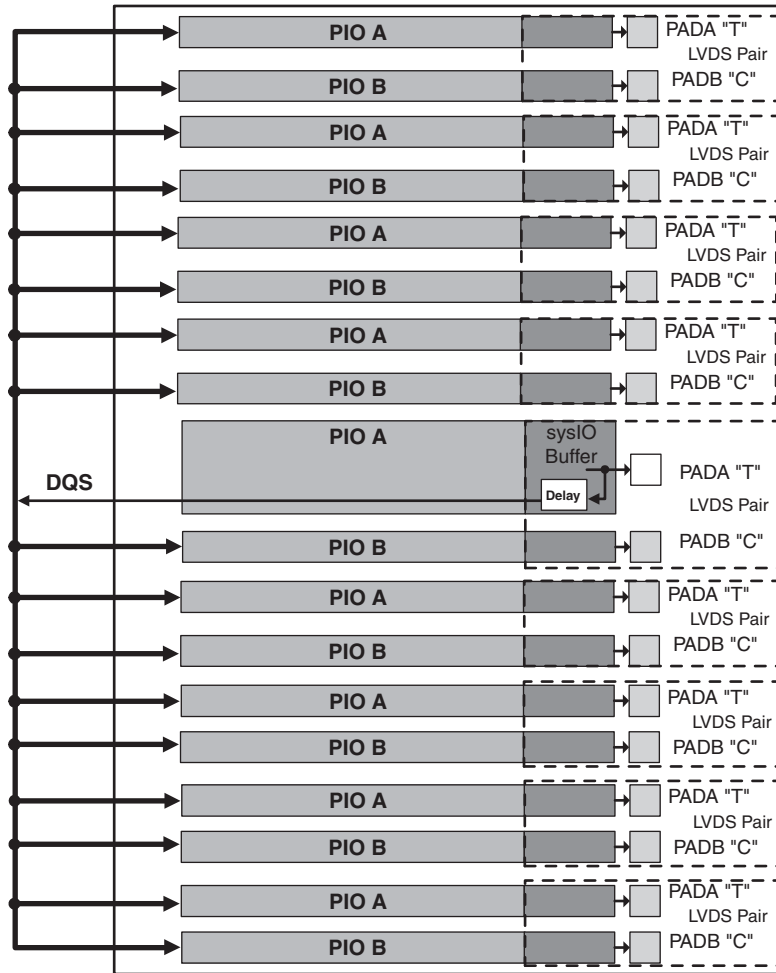
Figure 2-14. DCS Waveforms



Secondary Clock/Control Routing

Secondary clocks in the LatticeECP2 devices are region-based resources. The benefit of region-based resources is the relatively low injection delay and skew within the region, as compared to primary clocks. EBR/DSP rows and a special vertical routing channel bound the secondary clock regions. This special vertical routing channel aligns with either the left edge of the center DSP block in the DSP row or the center of the DSP row. Figure 2-15 shows

Figure 2-34. DQS Input Routing for the Bottom Edge of the Device



DLL Calibrated DQS Delay Block

Source synchronous interfaces generally require the input clock to be adjusted in order to correctly capture data at the input register. For most interfaces a PLL is used for this adjustment. However, in DDR memories the clock (referred to as DQS) is not free-running so this approach cannot be used. The DQS Delay block provides the required clock alignment for DDR memory interfaces.

The DQS signal (selected PIOs only, as shown in Figure 2-35) feeds from the PAD through a DQS delay element to a dedicated DQS routing resource. The DQS signal also feeds polarity control logic, which controls the polarity of the clock to the sync registers in the input register blocks. Figure 2-35 and Figure 2-36 show how the DQS transition signals are routed to the PIOs.

The temperature, voltage and process variations of the DQS delay block are compensated by a set of calibration (6-bit bus) signals from two dedicated DLLs (DDR_DLL) on opposite sides of the device. Each DLL compensates DQS delays in its half of the device as shown in Figure 2-35. The DLL loop is compensated for temperature, voltage and process variations by the system clock and feedback loop.

sysI/O Recommended Operating Conditions

Standard	V _{CCIO}			V _{REF} (V)		
	Min.	Typ.	Max.	Min.	Typ.	Max.
LVC MOS 3.3 ²	3.135	3.3	3.465	—	—	—
LVC MOS 2.5 ²	2.375	2.5	2.625	—	—	—
LVC MOS 1.8	1.71	1.8	1.89	—	—	—
LVC MOS 1.5	1.425	1.5	1.575	—	—	—
LVC MOS 1.2 ²	1.14	1.2	1.26	—	—	—
LVTTL ²	3.135	3.3	3.465	—	—	—
PCI	3.135	3.3	3.465	—	—	—
SSTL18 ² Class I, II	1.71	1.8	1.89	0.833	0.9	0.969
SSTL2 ² Class I, II	2.375	2.5	2.625	1.15	1.25	1.35
SSTL3 ² Class I, II	3.135	3.3	3.465	1.3	1.5	1.7
HSTL ² 15 Class I	1.425	1.5	1.575	0.68	0.75	0.9
HSTL ² 18 Class I, II	1.71	1.8	1.89	0.816	0.9	1.08
LVDS ²	2.375	2.5	2.625	—	—	—
MLVDS25 ¹	2.375	2.5	2.625	—	—	—
LVPECL33 ^{1,2}	3.135	3.3	3.465	—	—	—
BLVDS25 ^{1,2}	2.375	2.5	2.625	—	—	—
RSDS ^{1,2}	2.375	2.5	2.625	—	—	—
SSTL18D_I ² , II ²	1.71	1.8	1.89	—	—	—
SSTL25D_I ² , II ²	2.375	2.5	2.625	—	—	—
SSTL33D_I ² , II ²	3.135	3.3	3.465	—	—	—
HSTL15D_I ²	1.425	1.5	1.575	—	—	—
HSTL18D_I ² , II ²	1.71	1.8	1.89	—	—	—

1. Inputs on chip. Outputs are implemented with the addition of external resistors.

2. Input on this standard does not depend on the value of V_{CCIO}.

LVPECL

The LatticeECP2/M devices support the differential LVPECL standard. This standard is emulated using complementary LVCMOS outputs in conjunction with a parallel resistor across the driver outputs. The LVPECL input standard is supported by the LVDS differential input buffer. The scheme shown in Figure 3-3 is one possible solution for point-to-point signals.

Figure 3-3. Differential LVPECL

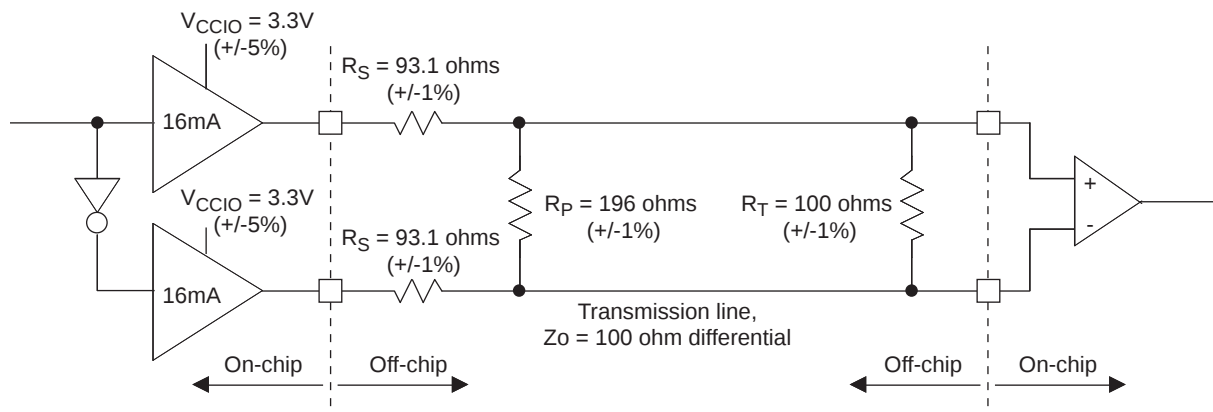


Table 3-4. LVPECL DC Conditions¹

Over Recommended Operating Conditions

Parameter	Description	Typical	Units
V_{CCIO}	Output Driver Supply (+/-5%)	3.30	V
Z_{OUT}	Driver Impedance	10	Ω
R_S	Driver Series Resistor (+/-1%)	93	Ω
R_P	Driver Parallel Resistor (+/-1%)	196	Ω
R_T	Receiver Termination (+/-1%)	100	Ω
V_{OH}	Output High Voltage	2.05	V
V_{OL}	Output Low Voltage	1.25	V
V_{OD}	Output Differential Voltage	0.80	V
V_{CM}	Output Common Mode Voltage	1.65	V
Z_{BACK}	Back Impedance	100.5	Ω
I_{DC}	DC Output Current	12.11	mA

1. For input buffer, see LVDS table.

LFE2-12E/SE and LFE2-20E/SE Logic Signal Connections: 208 PQFP (Cont.)

LFE2-12E/SE					LFE2-20E/SE				
Pin Number	Pin/Pad Function	Bank	Dual Function	Differential	Pin/Pad Function	Bank	Dual Function	Differential	
184	GND	-			GND	-			
185	PT28A	0	PCLKT0_0	T	PT37A	0	PCLKT0_0	T	
186	PT26B	0		C	PT36B	0		C	
187	PT26A	0		T	PT36A	0		T	
188	VCC	-			VCC	-			
189	PT20B	0		C	PT30B	0		C	
190	VCCAUX	-			VCCAUX	-			
191	PT20A	0		T	PT30A	0		T	
192	GND	-			GND	-			
193	PT18B	0		C	PT26B	0		C	
194	PT18A	0		T	PT26A	0		T	
195	VCCIO0	0			VCCIO0	0			
196	PT16B	0		C	PT20B	0		C	
197	PT16A	0		T	PT20A	0		T	
198	VCC	-			VCC	-			
199	PT12B	0		C	PT12B	0		C	
200	PT12A	0		T	PT12A	0		T	
201	GND	-			GND	-			
202	PT8B	0		C	PT8B	0		C	
203	PT8A	0		T	PT8A	0		T	
204	PT6B	0		C	PT6B	0		C	
205	PT6A	0		T	PT6A	0		T	
206	VCCIO0	0			VCCIO0	0			
207	PT2B	0	VREF2_0	C	PT2B	0	VREF2_0	C	
208	PT2A	0	VREF1_0	T	PT2A	0	VREF1_0	T	

* Supports true LVDS. Other differential signals must be emulated with external resistors.

** These dedicated input pins can be used for GPLLs or GDLLs within the respective quadrant.

Note: VCCIO and GND pads are used to determine the average DC current drawn by I/Os between GND/VCCIO connections, or between the last GND/VCCIO in an I/O bank and the end of an I/O bank. The substrate pads listed in the Pin Table do not necessarily have a one to one connection with a package ball or pin.

LFE2-6E/SE and LFE2-12E/SE Logic Signal Connections: 256 fpBGA (Cont.)

LFE2-6E/SE					LFE2-12E/SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
R12	GND	-			GND	-		
R5	GND	-			GND	-		
T1	GND	-			GND	-		
T16	GND	-			GND	-		

* Supports true LVDS. Other differential signals must be emulated with external resistors.

** These dedicated input pins can be used for GPLLs or GDLLs within the respective quadrant.

Note: VCCIO and GND pads are used to determine the average DC current drawn by I/Os between GND/VCCIO connections, or between the last GND/VCCIO in an I/O bank and the end of an I/O bank. The substrate pads listed in the Pin Table do not necessarily have a one to one connection with a package ball or pin.

LFE2-20E/SE and LFE2-35E/SE Logic Signal Connections: 672 fpBGA (Cont.)

LFE2-20E/20SE					LFE2-35E/35SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential	
AE17	PB51B	4	BDQ51	C	PB51B	4	BDQ51	C	
AB19	PB52A	4	BDQ51	T	PB52A	4	BDQ51	T	
AE19	PB52B	4	BDQ51	C	PB52B	4	BDQ51	C	
AF17	PB53A	4	BDQ51	T	PB53A	4	BDQ51	T	
AE18	PB53B	4	BDQ51	C	PB53B	4	BDQ51	C	
VCCIO	VCCIO4	4			VCCIO4	4			
W16	PB54A	4	BDQ51	T	PB54A	4	BDQ51	T	
AA17	PB54B	4	BDQ51	C	PB54B	4	BDQ51	C	
AF18	PB55A	4	BDQ51	T	PB55A	4	BDQ51	T	
AF19	PB55B	4	BDQ51	C	PB55B	4	BDQ51	C	
GND	GNDIO4	-			GNDIO4	-			
AA19	NC	-			PB56A	4	BDQ60	T	
W17	NC	-			PB56B	4	BDQ60	C	
Y19	NC	-			PB57A	4	BDQ60	T	
Y17	NC	-			PB57B	4	BDQ60	C	
AF20	NC	-			NC	-			
VCCIO	VCCIO4	4			VCCIO4	4			
AE20	NC	-			NC	-			
AA20	NC	-			NC	-			
W18	NC	-			NC	-			
AD20	NC	-			NC	-			
GND	GNDIO4	-			GNDIO4	-			
AE21	NC	-			NC	-			
AF21	NC	-			NC	-			
AF22	NC	-			NC	-			
VCCIO	VCCIO4	4			VCCIO4	4			
GND	GNDIO4	-			GNDIO4	-			
AE22	PB56A	4	BDQ60	T	PB65A	4	BDQ69	T	
AD22	PB56B	4	BDQ60	C	PB65B	4	BDQ69	C	
AF23	PB57A	4	BDQ60	T	PB66A	4	BDQ69	T	
AE23	PB57B	4	BDQ60	C	PB66B	4	BDQ69	C	
AD23	PB58A	4	BDQ60	T	PB67A	4	BDQ69	T	
AC23	PB58B	4	BDQ60	C	PB67B	4	BDQ69	C	
VCCIO	VCCIO4	4			VCCIO4	4			
AB20	PB59A	4	BDQ60	T	PB68A	4	BDQ69	T	
AC20	PB59B	4	BDQ60	C	PB68B	4	BDQ69	C	
GND	GNDIO4	-			GNDIO4	-			
AB21	PB60A	4	BDQS60	T	PB69A	4	BDQS69	T	
AC22	PB60B	4	BDQ60	C	PB69B	4	BDQ69	C	
W19	PB61A	4	BDQ60	T	PB70A	4	BDQ69	T	
AA21	PB61B	4	BDQ60	C	PB70B	4	BDQ69	C	
AF24	PB62A	4	BDQ60	T	PB71A	4	BDQ69	T	
AE24	PB62B	4	BDQ60	C	PB71B	4	BDQ69	C	
VCCIO	VCCIO4	4			VCCIO4	4			
Y20	PB63A	4	BDQ60	T	PB72A	4	BDQ69	T	
AB22	PB63B	4	BDQ60	C	PB72B	4	BDQ69	C	

LFE2-20E/SE and LFE2-35E/SE Logic Signal Connections: 672 fpBGA (Cont.)

LFE2-20E/20SE					LFE2-35E/35SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
A2	GND	-			GND	-		
A25	GND	-			GND	-		
AA18	GND	-			GND	-		
AA24	GND	-			GND	-		
AA3	GND	-			GND	-		
AA9	GND	-			GND	-		
AD11	GND	-			GND	-		
AD16	GND	-			GND	-		
AD21	GND	-			GND	-		
AD6	GND	-			GND	-		
AE1	GND	-			GND	-		
AE26	GND	-			GND	-		
AF2	GND	-			GND	-		
AF25	GND	-			GND	-		
B1	GND	-			GND	-		
B26	GND	-			GND	-		
C11	GND	-			GND	-		
C16	GND	-			GND	-		
C21	GND	-			GND	-		
C6	GND	-			GND	-		
F18	GND	-			GND	-		
F24	GND	-			GND	-		
F3	GND	-			GND	-		
F9	GND	-			GND	-		
J13	GND	-			GND	-		
J14	GND	-			GND	-		
J21	GND	-			GND	-		
J6	GND	-			GND	-		
K10	GND	-			GND	-		
K11	GND	-			GND	-		
K13	GND	-			GND	-		
K14	GND	-			GND	-		
K16	GND	-			GND	-		
K17	GND	-			GND	-		
L10	GND	-			GND	-		
L11	GND	-			GND	-		
L16	GND	-			GND	-		
L17	GND	-			GND	-		
L24	GND	-			GND	-		
L3	GND	-			GND	-		
M13	GND	-			GND	-		
M14	GND	-			GND	-		
N10	GND	-			GND	-		
N12	GND	-			GND	-		
N13	GND	-			GND	-		
N14	GND	-			GND	-		

LFE2-70E/SE Logic Signal Connections: 900 fpBGA (Cont.)

LFE2-70E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential
P25	PR51B	2	RDQ54	C
VCCIO	VCCIO2	2		
P23	PR51A	2	RDQ54	T
P27	PR50B	2	RDQ54	C (LVDS)*
P28	PR50A	2	RDQ54	T (LVDS)*
GND	GNDIO2	-		
VCCIO	VCCIO2	2		
N24	PR39B	2	RUM0_SPLLC_FB_A/RDQ37	C
N26	PR39A	2	RUM0_SPLLT_FB_A/RDQ37	T
N23	PR38B	2	RUM0_SPLLC_IN_A/RDQ37	C
N25	PR38A	2	RUM0_SPLLT_IN_A/RDQ37	T
VCCIO	VCCIO2	2		
P29	PR37B	2	RDQ37	C (LVDS)*
P30	PR37A	2	RDQS37	T (LVDS)*
M26	PR36B	2	RDQ37	C
GND	GNDIO2	-		
M24	PR36A	2	RDQ37	T
N29	PR35B	2	RDQ37	C (LVDS)*
N30	PR35A	2	RDQ37	T (LVDS)*
M25	PR34B	2	RDQ37	C
VCCIO	VCCIO2	2		
M23	PR34A	2	RDQ37	T
M27	PR33B	2	RDQ37	C (LVDS)*
M28	PR33A	2	RDQ37	T (LVDS)*
L26	PR32B	2	RDQ29	C
GND	GNDIO2	-		
L24	PR32A	2	RDQ29	T
M29	PR31B	2	RDQ29	C (LVDS)*
M30	PR31A	2	RDQ29	T (LVDS)*
L25	PR30B	2	RDQ29	C
VCCIO	VCCIO2	2		
L23	PR30A	2	RDQ29	T
L27	PR29B	2	RDQ29	C (LVDS)*
L28	PR29A	2	RDQS29	T (LVDS)*
GND	GNDIO2	-		
K24	PR28B	2	RDQ29	C
K26	PR28A	2	RDQ29	T
L29	PR27B	2	RDQ29	C (LVDS)*
L30	PR27A	2	RDQ29	T (LVDS)*
VCCIO	VCCIO2	2		
K23	PR26B	2	RDQ29	C
K25	PR26A	2	RDQ29	T
K27	PR25B	2	RDQ29	C (LVDS)*

LFE2M50E/SE and LFE2M70E/SE Logic Signal Connections: 900 fpBGA

LFE2M50E/SE					LFE2M70E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential	
D2	PL9A	7	VREF2_7/LDQ6	T	PL9A	7	VREF2_7	T	
D3	PL9B	7	VREF1_7/LDQ6	C	PL9B	7	VREF1_7	C	
GNDIO	GNDIO7	-			GNDIO7	-			
J8	PL11A	7	LUM0_SPLLT_IN_A	T (LVDS)*	PL11A	7	LUM0_SPLLT_IN_A/LDQ15	T (LVDS)*	
H7	PL11B	7	LUM0_SPLLC_IN_A	C (LVDS)*	PL11B	7	LUM0_SPLLC_IN_A/LDQ15	C (LVDS)*	
E3	PL12A	7	LUM0_SPLLT_FB_A	T	PL12A	7	LUM0_SPLLT_FB_A/LDQ15	T	
E4	PL12B	7	LUM0_SPLLC_FB_A	C	PL12B	7	LUM0_SPLLC_FB_A/LDQ15	C	
GNDIO	GNDIO7	-			-	-			
G6	PL13A	7		T (LVDS)*	PL13A	7	LDQ15	T (LVDS)*	
F5	PL13B	7		C (LVDS)*	PL13B	7	LDQ15	C (LVDS)*	
E2	PL14A	7		T	PL14A	7	LDQ15	T	
D1	PL14B	7		C	PL14B	7	LDQ15	C	
-	-	-			GNDIO7	-			
G5	NC	-			PL15A	7	LDQS15	T (LVDS)*	
G4	NC	-			PL15B	7	LDQ15	C (LVDS)*	
K7	NC	-			PL16A	7	LDQ15	T	
K8	NC	-			PL16B	7	LDQ15	C	
E1	NC	-			PL17A	7	LDQ15	T (LVDS)*	
F2	NC	-			PL17B	7	LDQ15	C (LVDS)*	
F1	NC	-			PL18A	7	LDQ15	T	
-	-	-			GNDIO7	-			
G3	NC	-			PL18B	7	LDQ15	C	
H5	PL15A	7		T (LVDS)*	PL21A	7		T (LVDS)*	
H4	PL15B	7		C (LVDS)*	PL21B	7		C (LVDS)*	
J5	PL16A	7		T	PL22A	7		T	
J4	PL16B	7		C	PL22B	7		C	
GNDIO	GNDIO7	-			GNDIO7	-			
G2	NC	-			PL24A	7	LDQ28	T (LVDS)*	
G1	NC	-			PL24B	7	LDQ28	C (LVDS)*	
L9	NC	-			PL25A	7	LDQ28	T	
L7	NC	-			PL25B	7	LDQ28	C	
K6	NC	-			PL26A	7	LDQ28	T (LVDS)*	
K5	NC	-			PL26B	7	LDQ28	C (LVDS)*	
L8	NC	-			PL27A	7	LDQ28	T	
L6	NC	-			PL27B	7	LDQ28	C	
-	-	-			GNDIO7	-			
H3	PL18A	7		T (LVDS)*	PL28A	7	LDQS28	T (LVDS)*	
H2	PL18B	7		C (LVDS)*	PL28B	7	LDQ28	C (LVDS)*	
N8	PL19A	7		T	PL29A	7	LDQ28	T	
M9	PL19B	7		C	PL29B	7	LDQ28	C	
J3	PL20A	7		T (LVDS)*	PL30A	7	LDQ28	T (LVDS)*	
VCCIO	VCCIO7	7			-	-			
J2	PL20B	7		C (LVDS)*	PL30B	7	LDQ28	C (LVDS)*	
H1	PL21A	7		T	PL31A	7	LDQ28	T	
GNDIO	GNDIO7	-			GNDIO7	-			
J1	PL21B	7		C	PL31B	7	LDQ28	C	
-	-	-			-	-			
-	-	-			-	-			

LFE2M50E/SE and LFE2M70E/SE Logic Signal Connections: 900 fpBGA (Cont.)

LFE2M50E/SE					LFE2M70E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential	
AC15	PB27B	5	BDQ24	C	PB42B	5	BDQ42	C	
VCCIO	VCCIO5	5			VCCIO5	5			
GNDIO	GNDIO5	-			GNDIO5	-			
AD15	PB38A	5	BDQ42	T	PB47A	5	BDQ51	T	
AF15	PB38B	5	BDQ42	C	PB47B	5	BDQ51	C	
AG10	PB39A	5	BDQ42	T	PB48A	5	BDQ51	T	
AG9	PB39B	5	BDQ42	C	PB48B	5	BDQ51	C	
AH14	PB40A	5	BDQ42	T	PB49A	5	BDQ51	T	
AG12	PB40B	5	BDQ42	C	PB49B	5	BDQ51	C	
VCCIO	VCCIO5	5			VCCIO5	5			
AG15	PB41A	5	BDQ42	T	PB50A	5	BDQ51	T	
AG13	PB41B	5	BDQ42	C	PB50B	5	BDQ51	C	
GNDIO	GNDIO5	-			GNDIO5	-			
AF16	PB42A	5	BDQS42	T	PB51A	5	BDQS51	T	
AH15	PB42B	5	BDQ42	C	PB51B	5	BDQ51	C	
AC16	PB43A	5	VREF2_5/BDQ42	T	PB52A	5	VREF2_5/BDQ51	T	
AE16	PB43B	5	VREF1_5/BDQ42	C	PB52B	5	VREF1_5/BDQ51	C	
AG11	PB44A	5	PCLKT5_0/BDQ42	T	PB53A	5	PCLKT5_0/BDQ51	T	
AF11	PB44B	5	PCLKC5_0/BDQ42	C	PB53B	5	PCLKC5_0/BDQ51	C	
VCCIO	VCCIO5	5			VCCIO5	5			
GNDIO	GNDIO5	-			GNDIO5	-			
AJ14	PB49A	4	PCLKT4_0/BDQ51	T	PB58A	4	PCLKT4_0/BDQ60	T	
VCCIO	VCCIO4	4			VCCIO4	4			
AK14	PB49B	4	PCLKC4_0/BDQ51	C	PB58B	4	PCLKC4_0/BDQ60	C	
AK15	PB50A	4	VREF2_4/BDQ51	T	PB59A	4	VREF2_4/BDQ60	T	
AK16	PB50B	4	VREF1_4/BDQ51	C	PB59B	4	VREF1_4/BDQ60	C	
AF18	PB51A	4	BDQS51	T	PB60A	4	BDQS60	T	
GNDIO	GNDIO4	-			GNDIO4	-			
AD16	PB51B	4	BDQ51	C	PB60B	4	BDQ60	C	
AJ15	PB52A	4	BDQ51	T	PB61A	4	BDQ60	T	
AG16	PB52B	4	BDQ51	C	PB61B	4	BDQ60	C	
AE17	PB53A	4	BDQ51	T	PB62A	4	BDQ60	T	
VCCIO	VCCIO4	4			VCCIO4	4			
AC17	PB53B	4	BDQ51	C	PB62B	4	BDQ60	C	
AH16	PB54A	4	BDQ51	T	PB63A	4	BDQ60	T	
AK17	PB54B	4	BDQ51	C	PB63B	4	BDQ60	C	
AG20	PB55A	4	BDQ51	T	PB64A	4	BDQ60	T	
GNDIO	GNDIO4	-			GNDIO4	-			
AG21	PB55B	4	BDQ51	C	PB64B	4	BDQ60	C	
AG18	PB56A	4	BDQ60	T	PB65A	4	BDQ69	T	
AJ16	PB56B	4	BDQ60	C	PB65B	4	BDQ69	C	
AF21	PB57A	4	BDQ60	T	PB66A	4	BDQ69	T	
AG22	PB57B	4	BDQ60	C	PB66B	4	BDQ69	C	
AD17	PB58A	4	BDQ60	T	PB67A	4	BDQ69	T	
AF19	PB58B	4	BDQ60	C	PB67B	4	BDQ69	C	
VCCIO	VCCIO4	4			VCCIO4	4			
GNDIO	GNDIO4	-			GNDIO4	-			
AH17	PB62A	4	BDQ60	T	PB71A	4	BDQ69	T	

LFE2M50E/SE and LFE2M70E/SE Logic Signal Connections: 900 fpBGA (Cont.)

LFE2M50E/SE					LFE2M70E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential	
P13	GND	-			GND	-			
P14	GND	-			GND	-			
P15	GND	-			GND	-			
P16	GND	-			GND	-			
P17	GND	-			GND	-			
P18	GND	-			GND	-			
P20	GND	-			GND	-			
R10	GND	-			GND	-			
R11	GND	-			GND	-			
R13	GND	-			GND	-			
R14	GND	-			GND	-			
R15	GND	-			GND	-			
R16	GND	-			GND	-			
R17	GND	-			GND	-			
R18	GND	-			GND	-			
R20	GND	-			GND	-			
R21	GND	-			GND	-			
R24	GND	-			GND	-			
R7	GND	-			GND	-			
T10	GND	-			GND	-			
T11	GND	-			GND	-			
T13	GND	-			GND	-			
T14	GND	-			GND	-			
T15	GND	-			GND	-			
T16	GND	-			GND	-			
T17	GND	-			GND	-			
T18	GND	-			GND	-			
T20	GND	-			GND	-			
T21	GND	-			GND	-			
T24	GND	-			GND	-			
T7	GND	-			GND	-			
U11	GND	-			GND	-			
U13	GND	-			GND	-			
U14	GND	-			GND	-			
U15	GND	-			GND	-			
U16	GND	-			GND	-			
U17	GND	-			GND	-			
U18	GND	-			GND	-			
U20	GND	-			GND	-			
V14	GND	-			GND	-			
V15	GND	-			GND	-			
V16	GND	-			GND	-			
V17	GND	-			GND	-			
V27	GND	-			GND	-			
V4	GND	-			GND	-			
W23	GND	-			GND	-			
W8	GND	-			GND	-			
Y14	GND	-			GND	-			

LFE2M100E/SE Logic Signal Connections: 900 fpBGA (Cont.)

LFE2M100E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential
H14	PT61A	0		T
A14	PT60B	0		C
B14	PT60A	0		T
D13	PT59B	0		C
GNDIO	GNDIO0	-		
F13	PT59A	0		T
G13	PT58B	0		C
VCCIO	VCCIO0	0		
J11	PT58A	0		T
D4	PT57B	0		
D5	PT56A	0		
E5	PT55B	0		C
F6	PT55A	0		T
GNDIO	GNDIO0	-		
VCCIO	VCCIO0	0		
F7	PT52B	0		C
D8	PT52A	0		T
GNDIO	GNDIO0	-		
J13	PT50B	0		C
G11	PT50A	0		T
H13	PT49B	0		C
H12	PT49A	0		T
VCCIO	VCCIO0	0		
E8	PT48B	0		C
D9	PT48A	0		T
D12	PT46B	0		C
GNDIO	GNDIO0	-		
E13	PT46A	0		T
VCCIO	VCCIO0	0		
GNDIO	GNDIO0	-		
J12	PT31B	0		C
-	-	-		
VCCIO	VCCIO0	0		
H10	PT31A	0		T
E12	PT30B	0		C
D11	PT30A	0		T
H11	PT29B	0		C
F11	PT29A	0		T
C13	ULC_SQ_VCCR0	11		
A12	ULC_SQ_HDINP0	11		T
B13	ULC_SQ_VCCIB0	11		
B12	ULC_SQ_HDINN0	11		C
C10	ULC_SQ_VCCTX0	11		

LFE2M100E/SE Logic Signal Connections: 900 fpBGA (Cont.)

LFE2M100E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential
A9	ULC_SQ_HDOUTP0	11		T
A10	ULC_SQ_VCCOB0	11		
B9	ULC_SQ_HDOUTN0	11		C
C9	ULC_SQ_VCCTX1	11		
B8	ULC_SQ_HDOUTN1	11		C
C8	ULC_SQ_VCCOB1	11		
A8	ULC_SQ_HDOUTP1	11		T
C12	ULC_SQ_VCCR1	11		
B11	ULC_SQ_HDINN1	11		C
C11	ULC_SQ_VCCIB1	11		
A11	ULC_SQ_HDINP1	11		T
B7	ULC_SQ_VCCAUX33	11		
E7	ULC_SQ_REFCLKN	11		C
D7	ULC_SQ_REFCLKP	11		T
C7	ULC_SQ_VCCP	11		
A3	ULC_SQ_HDINP2	11		T
C3	ULC_SQ_VCCIB2	11		
B3	ULC_SQ_HDINN2	11		C
C2	ULC_SQ_VCCR2	11		
A6	ULC_SQ_HDOUTP2	11		T
C6	ULC_SQ_VCCOB2	11		
B6	ULC_SQ_HDOUTN2	11		C
C5	ULC_SQ_VCCTX2	11		
B5	ULC_SQ_HDOUTN3	11		C
A4	ULC_SQ_VCCOB3	11		
A5	ULC_SQ_HDOUTP3	11		T
C4	ULC_SQ_VCCTX3	11		
B2	ULC_SQ_HDINN3	11		C
B1	ULC_SQ_VCCIB3	11		
A2	ULC_SQ_HDINP3	11		T
C1	ULC_SQ_VCCR3	11		
L12	VCC	-		
L13	VCC	-		
L18	VCC	-		
L19	VCC	-		
M11	VCC	-		
M12	VCC	-		
M13	VCC	-		
M14	VCC	-		
M15	VCC	-		
M16	VCC	-		
M17	VCC	-		
M18	VCC	-		

LFE2M100E/SE Logic Signal Connections: 900 fpBGA (Cont.)

LFE2M100E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential
U15	GND	-		
U16	GND	-		
U17	GND	-		
U18	GND	-		
U20	GND	-		
V14	GND	-		
V15	GND	-		
V16	GND	-		
V17	GND	-		
V27	GND	-		
V4	GND	-		
W23	GND	-		
W8	GND	-		
Y14	GND	-		
Y15	GND	-		
Y16	GND	-		
Y17	GND	-		
AA26	NC	-		
AB10	NC	-		
AB11	NC	-		
AB12	NC	-		
AB13	NC	-		
AB14	NC	-		
AB15	NC	-		
AB16	NC	-		
AB17	NC	-		
AB19	NC	-		
AB20	NC	-		
AB21	NC	-		
AB9	NC	-		
AC10	NC	-		
AC11	NC	-		
AC21	NC	-		
AC22	NC	-		
AC8	NC	-		
AC9	NC	-		
AD21	NC	-		
AD22	NC	-		
AD4	NC	-		
AD5	NC	-		
AD6	NC	-		
AD7	NC	-		
AD8	NC	-		

LFE2M70E/SE and LFE2M100E/SE Logic Signal Connections: 1152 fpBGA

LFE2M70E/SE				LFE2M100E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
VCCIO	VCCIO7	7			VCCIO7	7		
F4	PL9A	7	VREF2_7	T	PL9A	7	VREF2_7	T
F3	PL9B	7	VREF1_7	C	PL9B	7	VREF1_7	C
GNDIO	GNDIO7	-			GNDIO7	-		
E1	PL11A	7	LUM0_SPLLT_IN_A/LDQ15	T (LVDS)*	PL11A	7	LUM0_SPLLT_IN_A/LDQ15	T (LVDS)*
E2	PL11B	7	LUM0_SPLLC_IN_A/LDQ15	C (LVDS)*	PL11B	7	LUM0_SPLLC_IN_A/LDQ15	C (LVDS)*
K9	PL12A	7	LUM0_SPLLT_FB_A/LDQ15	T	PL12A	7	LUM0_SPLLT_FB_A/LDQ15	T
H7	PL12B	7	LUM0_SPLLC_FB_A/LDQ15	C	PL12B	7	LUM0_SPLLC_FB_A/LDQ15	C
VCCIO	VCCIO7	7			VCCIO7	7		
F1	PL13A	7	LDQ15	T (LVDS)*	PL13A	7	LDQ15	T (LVDS)*
F2	PL13B	7	LDQ15	C (LVDS)*	PL13B	7	LDQ15	C (LVDS)*
J8	PL14A	7	LDQ15	T	PL14A	7	LDQ15	T
H6	PL14B	7	LDQ15	C	PL14B	7	LDQ15	C
GNDIO	GNDIO7	-			GNDIO7	-		
G2	PL15A	7	LDQS15	T (LVDS)*	PL15A	7	LDQS15	T (LVDS)*
G1	PL15B	7	LDQ15	C (LVDS)*	PL15B	7	LDQ15	C (LVDS)*
J7	PL16A	7	LDQ15	T	PL16A	7	LDQ15	T
VCCIO	VCCIO7	7			VCCIO7	7		
L8	PL16B	7	LDQ15	C	PL16B	7	LDQ15	C
L9	PL17A	7	LDQ15	T (LVDS)*	PL17A	7	LDQ15	T (LVDS)*
L10	PL17B	7	LDQ15	C (LVDS)*	PL17B	7	LDQ15	C (LVDS)*
H5	PL18A	7	LDQ15	T	PL18A	7	LDQ15	T
GNDIO	GNDIO7	-			GNDIO7	-		
J6	PL18B	7	LDQ15	C	PL18B	7	LDQ15	C
H2	NC	-			PL19A	7	LDQ23	T (LVDS)*
H1	NC	-			PL19B	7	LDQ23	C (LVDS)*
G5	NC	-			PL20A	7	LDQ23	T
G6	NC	-			PL20B	7	LDQ23	C
M9	NC	-			PL21A	7	LDQ23	T (LVDS)*
-	-	-			VCCIO7	7		
M10	NC	-			PL21B	7	LDQ23	C (LVDS)*
H3	NC	-			PL22A	7	LDQ23	T
H4	NC	-			PL22B	7	LDQ23	C
J2	PL19A	7		T (LVDS)*	PL23A	7	LDQS23	T (LVDS)*
-	-	-			GNDIO7	-		
J1	PL19B	7		C (LVDS)*	PL23B	7	LDQ23	C (LVDS)*
K2	PL20A	7		T	PL24A	7	LDQ23	T
K1	PL20B	7		C	PL24B	7	LDQ23	C
VCCIO	VCCIO7	7			VCCIO7	7		
J4	PL21A	7		T (LVDS)*	PL25A	7	LDQ23	T (LVDS)*
J3	PL21B	7		C (LVDS)*	PL25B	7	LDQ23	C (LVDS)*
J5	PL22A	7		T	PL26A	7	LDQ23	T
K5	PL22B	7		C	PL26B	7	LDQ23	C
GNDIO	GNDIO7	-			GNDIO7	-		
L2	PL24A	7	LDQ28	T (LVDS)*	PL28A	7	LDQ32	T (LVDS)*
L1	PL24B	7	LDQ28	C (LVDS)*	PL28B	7	LDQ32	C (LVDS)*
L7	PL25A	7	LDQ28	T	PL29A	7	LDQ32	T
K6	PL25B	7	LDQ28	C	PL29B	7	LDQ32	C
VCCIO	VCCIO7	7			VCCIO7	7		

Date	Version	Section	Change Summary
August 2006 (cont.)	01.1 (cont.)	Pinout Information (cont.)	Added Information on: Available Device Resources per Packaged Device table.
		Ordering Information	Updated ordering part number table to include ECP2-12.
			Updated topside mark drawing.
September 2006	02.0	Multiple	Added information regarding LatticeECP2M support throughout.
September 2006	02.1	DC and Switching Characteristics	Added Receiver Total Jitter Tolerance Specification table.
			Removed power-up requirements for proper configuration footnote in Recommended Operating Conditions table.
December 2006	02.2	Introduction	LatticeECP2M Selection Guide table has been updated.
		Architecture	Figure 2-16. Per Region Secondary Clock Selection has been updated.
			Figure 2-39. Simplified Channel Block Diagram for SERDES and PCS has been updated.
		DC and Switching	Footnotes have been added to Recommended Operating Conditions.
			DC Electrical Characteristics table has been updated.
			Supply Current (Standby) tables have been updated.
			Initialization Supply Current table have been updated.
			Updated timing numbers to include LFE2-12E (rev A 0.08).
		Pinout Information	Updated to include the entire ECP2 device information as well as 256-fpBGA and 484-fpBGA pin information for the ECP2M35E.
		Ordering Information	Updated to include the entire ECP2 and ECP2M device ordering information.
February 2007	02.3	Architecture	Updated EBR Asynchronous Reset section.
March 2007	02.4	DC and Switching Characteristics	Power-sequencing footnotes have been added to the Recommended Operating Conditions. DDR2 performance has been updated to 266MHz.
March 2007	02.5	Introduction	Added "Security Series" to the LatticeECP2 and LatticeECP2M families.
		Architecture	Enhanced Configuration Option section updated.
		DC and Switching	Recommended Operating Conditions table - footnote 4 updated.
		Ordering Information	"Security Series" ordering part numbers added.
April 2007	02.6	Introduction	LatticeECP2M family table has been updated for user I/O counts.
		Ordering Information	LatticeECP2M family ordering part number section has been updated to add 1152-fpBGA package for the ECP2M70 and ECP2M100.
July 2007	02.7	Architecture	Updated text in Ripple Mode section.
		DC and Switching	ECP2/M Supply Current information has been updated. Typical Building Block Function Performance, External Switching Characteristics, Internal Switching Characteristics, Family Timing Adders, sysCLOCK GPLL Timing, sysCLOCK SPLN Timing, DLL Timing and sysCONFIG Port Timing Specifications have been updated (timing rev. A 0.10). SERDES timing information has been updated. PCI Express timing information has been updated.
		Pinout Information	Added LatticeECP2M20 pinout information.
August 2007	02.8	Introduction	1156-fpBGA package option has been removed from the LatticeECP2M family.
		Architecture	Table 2-16. Selectable Master Clock (CCLK) Frequencies During Configuration table has been updated.
		DC and Switching	Supply Current (Standby) table has been updated.
			DSP Function timing has been updated.

Date	Version	Section	Change Summary
November 2009 (cont.)	03.5 (cont.)	Pinout Information (cont.)	LatticeECP2M Pin Information Summary, LFE2M50, LFE2M70 and LFE2M100 table - corrected values for LFE2M50, 672 fpBGA in Available DDR-Interfaces per I/O Bank.
			Minor corrections in LFE2M20E/SE and LFE2M35E/SE Logic Signal Connections: 484 fpBGA table.
			Minor corrections in LFE2M50E/SE and LFE2M70E/SE Logic Signal Connections: 900 fpBGA table.
			Minor corrections in LFE2M100E/SE Logic Signal Connections: 900 fpBGA table.
			Updated LFE2-6E/SE and LFE2-12E/SE Logical Signal Connections (changed D1/SPIDS to D1).
		Ordering Information	Updated LatticeECP2M Part Number Description diagram.
March 2010	03.6	DC and Switching Characteristics	Footnote for SED operating frequency added to the sysCONFIG Port Timing Specifications table.
		Pinout Information	Changed Dual Function pin E7 to be D7/SPDI0 in Logic Signal Connections tables. Changed footnote (***) in Logic Signal Connections table.
July 2010	03.7	Architecture	Updated the Typical sysIO Behavior During Power-up text section.
		Pinout Information	Added reference to powerup information.
			Corrected reference to footnote for pins 131 and 132 for the LFE-20E/SE, 208 PQFP.
			Referenced footnote (***) for all D7/SPID0.
			Changed D7*** to D7/SPID0.
			Corrected *** footnote.
		All Sections	Included references to Lattice Diamond design software wherever ispLEVER and ispLeverCORE is specified.
April 2011	03.8	DC and Switching Characteristics	DC Electrical Characteristics table: - Added footnote 3 to I_{IH} - Added footnote 2 to I_{IL} , I_{IH} - Updated C1 and C2 typ. and max. data.
			DLL Timing table – Removed line for t_R and t_F
			LatticeECP2/M sysCONFIG Port Timing Specifications table – added footnote to t_{DINIT} .
			Figure 3-18 – Corrected label to be PRGM (not PRGMRJ).
		Pinout Information	LFE2-12E/SE and LFE-20/SE Logical Signal Connections for 208 PQFP – Corrected Dual Function information for pins 112, 114, 117, 119.
January 2012	03.9	Multiple	Removed references to ispLEVER design software.
		Architecture	Corrected information regarding SED support.
		DC and Switching Characteristics	Added reference to ESD information.
June 2013	04.0	All	Updated document with new corporate logo.
		Architecture	Architecture Overview – Added information on the state of the register on power up and after configuration.