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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

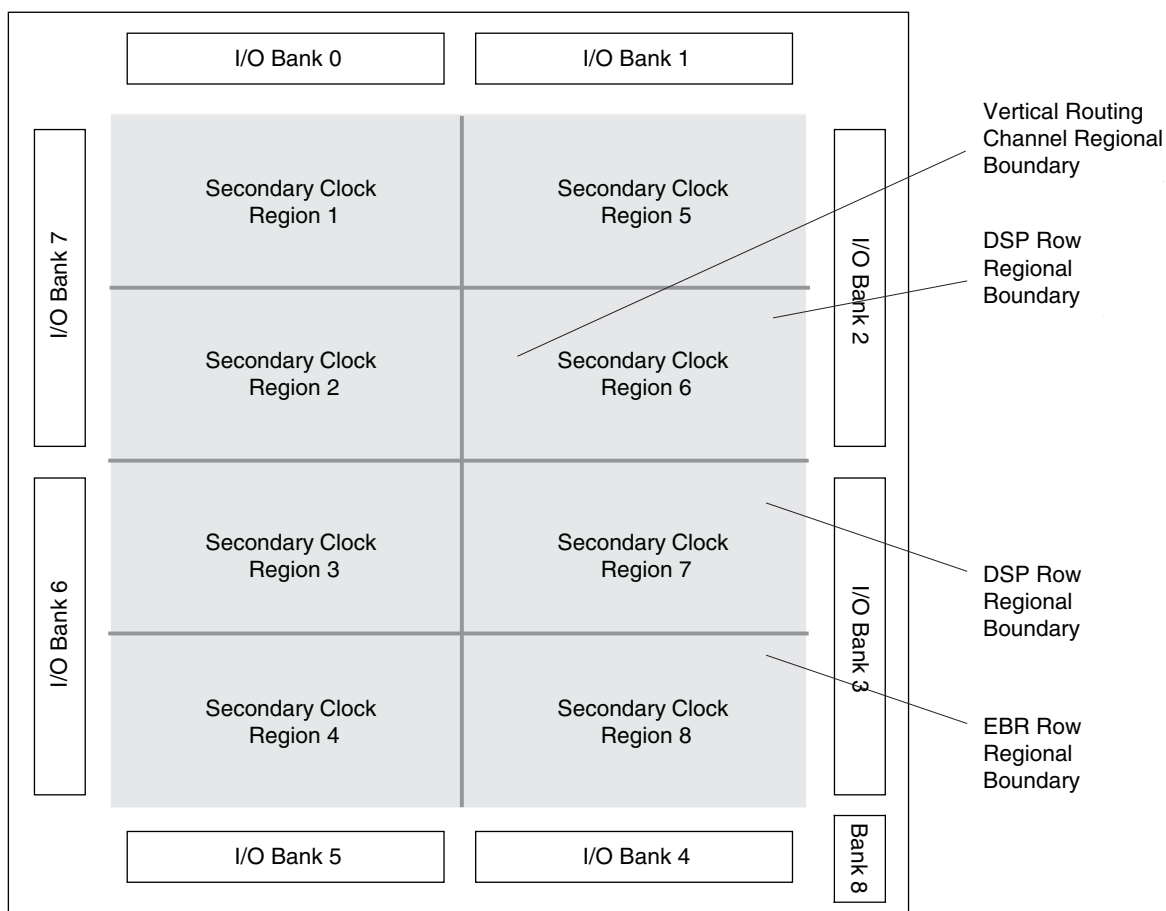
Details

Product Status	Active
Number of LABs/CLBs	6000
Number of Logic Elements/Cells	48000
Total RAM Bits	4246528
Number of I/O	270
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	484-BBGA
Supplier Device Package	484-FPBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfe2m50se-6fn484i

this special vertical routing channel and the eight secondary clock regions for the ECP2-50. LatticeECP2 devices have four secondary clocks (SC0 to SC3) which are distributed to every region.

The secondary clock muxes are located in the center of the device. Figure 2-16 shows the mux structure of the secondary clock routing. Secondary clocks SC0 to SC3 are used for clock and control and SC4 to SC7 are used for high fan-out signals.

Figure 2-15. Secondary Clock Regions ECP2-50



IPexpress™

The user can access the sysDSP block via the IPexpress tool, which provides the option to configure each DSP module (or group of modules) or by direct HDL instantiation. In addition, Lattice has partnered with The MathWorks® to support instantiation in the Simulink® tool, a graphical simulation environment. Simulink works with Diamond to dramatically shorten the DSP design cycle in Lattice FPGAs.

Optimized DSP Functions

Lattice provides a library of optimized DSP IP functions. Some of the IP cores planned for the LatticeECP2/M DSP include the Bit Correlator, Fast Fourier Transform, Finite Impulse Response (FIR) Filter, Reed-Solomon Encoder/Decoder, Turbo Encoder/Decoder and Convolutional Encoder/Decoder. Please contact Lattice to obtain the latest list of available DSP IP cores.

Resources Available in the LatticeECP2/M Family

Table 2-9 shows the maximum number of multipliers for each member of the LatticeECP2/M family. Table 2-10 shows the maximum available EBR RAM Blocks in each LatticeECP2/M device. EBR blocks, together with Distributed RAM can be used to store variables locally for fast DSP operations.

Table 2-9. Maximum Number of DSP Blocks in the LatticeECP2/M Family

Device	DSP Block	9x9 Multiplier	18x18 Multiplier	36x36 Multiplier
ECP2-6	3	24	12	3
ECP2-12	6	48	24	6
ECP2-20	7	56	28	7
ECP2-35	8	64	32	8
ECP2-50	18	144	72	18
ECP2-70	22	176	88	22
ECP2M20	6	48	24	6
ECP2M35	8	64	32	8
ECP2M50	22	176	88	22
ECP2M70	24	192	96	24
ECP2M100	42	336	168	42

Table 2-10. Embedded SRAM in the LatticeECP2/M Family

Device	EBR SRAM Block	Total EBR SRAM (Kbits)
ECP2-6	3	55
ECP2-12	12	221
ECP2-20	15	277
ECP2-35	18	332
ECP2-50	21	387
ECP2-70	60	1106
ECP2M20	66	1217
ECP2M35	114	2101
ECP2M50	225	4147
ECP2M70	246	4534
ECP2M100	288	5308

LatticeECP2M Supply Current (Standby)^{1, 2, 3, 4}
Over Recommended Operating Conditions

Symbol	Parameter	Device	Typ. ⁵	Units
I_{CC}	Core Power Supply Current	ECP2M20	25	mA
		ECP2M35	50	mA
		ECP2M50	85	mA
		ECP2M70	100	mA
		ECP2M100	100	mA
I_{CCAUX}	Auxiliary Power Supply Current	ECP2M20	24	mA
		ECP2M35	24	mA
		ECP2M50	24	mA
		ECP2M70	24	mA
		ECP2M100	24	mA
I_{CCGPLL}	GPLL Power Supply Current (per GPLL)	All Devices	0.5	mA
I_{CCSPLL}	GPLL Power Supply Current (per SPLL)	All Devices	0.5	mA
I_{CCIO}	Bank Power Supply Current (Per Bank)	ECP2M20	2	mA
		ECP2M35	2	mA
		ECP2M50	2	mA
		ECP2M70	2	mA
		ECP2M100	2	mA
I_{CCJ}	V_{CCJ} Power Supply Current	All Devices	3	mA

1. For further information about supply current, please see the list of additional technical documentation at the end of this data sheet.

2. Assumes all outputs are tristated, all inputs are configured as LVCMOS and held at the V_{CCIO} or GND.

3. Frequency 0MHz.

4. Pattern represents a "blank" configuration data file.

5. $T_J = 25^{\circ}\text{C}$, power supplies at normal voltage.

LatticeECP2M Initialization Supply Current^{1, 2, 3, 4}
Over Recommended Operating Conditions

Symbol	Parameter	Device	Typ. ^{5, 6, 7}	Units
I_{CC}	Core Power Supply Current	ECP2M20	41	mA
		ECP2M35	107	mA
		ECP2M50	169	mA
		ECP2M70	254	mA
		ECP2M100	378	mA
I_{CCAUX}	Auxiliary Power Supply Current	ECP2M20	30	mA
		ECP2M35	30	mA
		ECP2M50	30	mA
		ECP2M70	30	mA
		ECP2M100	30	mA
I_{CCGPLL}	GPLL Power Supply Current (per GPLL)	All Devices	0.5	mA
I_{CCSPLL}	SPLL Power Supply Current (per SPLL)	All Devices	0.5	mA
I_{CCIO}	Bank Power Supply Current (per Bank)	All Devices	3	mA
I_{CCJ}	VCCJ Power Supply Current	All Devices	4	mA

1. Until DONE signal is active.

2. For further information about supply current, please see the list of additional technical documentation at the end of this data sheet.

3. Assumes all outputs are tristated, all inputs are configured as LVCMOS and held at the V_{CCIO} or GND.

4. Frequency 0MHz.

5. $T_J = 25^{\circ}\text{C}$, power supplies at nominal voltage.

6. A specific configuration pattern is used that scales with the size of the device; consists of 75% PFU utilization, 50% EBR, and 25% I/O configuration.

7. Values shown in this column are the typical average DC current during configuration. Use the Power Calculator tool to find the peak startup current.

sysCLOCK GPLL Timing

Over Recommended Operating Conditions

Parameter	Description	Conditions	Min.	Typ.	Max.	Units
f _{IN}	Input Clock Frequency (CLKI, CLKFB)	Without external capacitor	20	—	420	MHz
		With external capacitor ^{5, 6}	2	—	420	MHz
f _{OUT}	Output Clock Frequency (CLKOP, CLKOS)	Without external capacitor	20	—	420	MHz
		With external capacitor ⁵	5	—	50	MHz
f _{OUT2}	K-Divider Output Frequency (CLKOK)	Without external capacitor	0.156	—	210	MHz
		With external capacitor ⁵	0.039	—	25	MHz
f _{VCO}	PLL VCO Frequency		640	—	1280	MHz
f _{PFD}	Phase Detector Input Frequency	Without external capacitor	20	—	420	MHz
		With external capacitor ^{5, 6}	2	—	50	MHz
AC Characteristics						
t _{DT}	Output Clock Duty Cycle	Default duty cycle selected ³	45	50	55	%
t _{PH} ⁴	Output Phase Accuracy		—	—	±0.05	UI
t _{OPJIT} ¹	Output Clock Period Jitter	f _{OUT} ≥ 100 MHz	—	—	±125	ps
		50 ≤ f _{OUT} < 100 MHz	—	—	0.025	UIPP
		f _{OUT} < 50 MHz	—	—	0.04	UIPP
t _{SK}	Input Clock to Output Clock Skew	N/M = integer	—	—	±250	ps
t _W	Output Clock Pulse Width	At 90% or 10%	1	—	—	ns
t _{LOCK} ²	PLL Lock-in Time	Without external capacitor	—	—	150	μs
		With external capacitor ⁵	—	—	500	μs
t _{PA}	Programmable Delay Unit		85	130	360	ps
t _{IPJIT}	Input Clock Period Jitter		—	—	±200	ps
t _{FBKDLY}	External Feedback Delay		—	—	10	ns
t _{HI}	Input Clock High Time	90% to 90%	0.5	—	—	ns
t _{LO}	Input Clock Low Time	10% to 10%	0.5	—	—	ns
t _{RST}	RST Pulse Width (RESETM/RESETK)		15	—	—	ns
	Reset Signal Pulse Width (CNTRST)	Without external capacitor	500	—	—	ns
		With external capacitor ⁵	20	—	—	μs

1. Jitter sample is taken over 10,000 samples of the primary PLL output with clean reference clock and no additional I/O pins toggling.

2. Output clock is valid after t_{LOCK} for PLL reset and dynamic delay adjustment.

3. Using LVDS output buffers.

4. Relative to CLKOP.

5. Value of external capacitor: 5.6 nF ±20%, NPO dielectric, ceramic chip capacitor, 1206 or smaller package, connected to PLLCAP pin.

6. $f_{OUT} (max) = f_{IN} * 10$ for $f_{IN} < 5$ MHz.

LatticeECP2/M sysCONFIG Port Timing Specifications

Over Recommended Operating Conditions

Parameter	Description	Min.	Max.	Units
sysCONFIG Byte Data Flow				
t_{SUCBDI}	Byte D[0:7] Setup Time to CCLK	7	—	ns
$t_{HCB DI}$	Byte D[0:7] Hold Time to CCLK	1	—	ns
t_{CODO}	CCLK to DOUT in Flowthrough Mode	—	12	ns
t_{SUCS}	CSN[0:1] Setup Time to CCLK	7	—	ns
t_{HCS}	CSN[0:1] Hold Time to CCLK	1	—	ns
t_{SUWD}	Write Signal Setup Time to CCLK	7	—	ns
t_{HWD}	Write Signal Hold Time to CCLK	1	—	ns
t_{DCB}	CCLK to BUSY Delay Time	—	12	ns
t_{CORD}	CCLK to Out for Read Data	—	12	ns
sysCONFIG Byte Slave Clocking				
t_{BSCH}	Byte Slave CCLK Minimum High Pulse	6	—	ns
t_{BSCL}	Byte Slave CCLK Minimum Low Pulse	9	—	ns
t_{BSCYC}	Byte Slave CCLK Cycle Time	15	—	ns
sysCONFIG Serial (Bit) Data Flow				
t_{SUSCDI}	DI Setup Time to CCLK Slave Mode	7	—	ns
t_{HSCDI}	DI Hold Time to CCLK Slave Mode	1	—	ns
t_{CODO}	CCLK to DOUT in Flowthrough Mode	—	12	ns
sysCONFIG Serial Slave Clocking				
t_{SSCH}	Serial Slave CCLK Minimum High Pulse	6	—	ns
t_{SSCL}	Serial Slave CCLK Minimum Low Pulse	6	—	ns
sysCONFIG POR, Initialization and Wake-up				
t_{ICFG}	Minimum Vcc to INITN High	—	28	ms
t_{VMC}	Time from t_{ICFG} to Valid Master CCLK	—	2	us
t_{PRGMRJ}	PROGRAMN Pin Pulse Rejection	—	8	ns
t_{PRGM}	PROGRAMN Low Time to Start Configuration	25	—	ns
t_{DINIT}	PROGRAMN High to INITN High Delay ¹	—	1.5	ms
$t_{DPPINIT}$	Delay Time from PROGRAMN Low to INITN Low	—	37	ns
$t_{DPPDONE}$	Delay Time from PROGRAMN Low to DONE Low	—	37	ns
t_{IODISS}	User I/O Disable from PROGRAMN Low	—	35	ns
t_{IOENSS}	User I/O Enabled Time from CCLK Edge During Wake-up Sequence	—	25	ns
t_{MWC}	Additional Wake Master Clock Signals after DONE Pin High	120	—	cycles
sysCONFIG SPI Port²				
t_{CFGX}	INITN High to CCLK Low	—	1	μs
t_{CSSPI}	INITN High to CSSPIN Low	—	2	us
t_{CSCCLK}	CCLK Low before CSSPIN Low	0	—	ns
t_{SOCDO}	CCLK Low to Output Valid	—	15	ns
t_{SOE}	CSSPIN[0:1] Active Setup Time	300	—	ns
t_{CSPID}	CSSPIN[0:1] Low to First CCLK Edge Setup Time	300+3cyc	600+6cyc	ns

LatticeECP2 Pin Information Summary, LFE2-6 and LFE2-12 (Cont.)

Pin Type		LFE2-6		LFE2-12			
		144 TQFP	256 fpBGA	144 TQFP	208 PQFP	256 fpBGA	484 fpBGA
Available DDR-Interfaces per I/O Bank ¹	Bank0	0	0	0	0	0	0
	Bank1	0	0	0	0	0	0
	Bank2	0	1	0	0	1	1
	Bank3	0	0	0	0	0	0
	Bank4	0	2	0	0	2	3
	Bank5	0	1	0	0	1	3
	Bank6	0	1	0	0	1	1
	Bank7	0	1	0	0	1	1
	Bank8	0	0	0	0	0	0
PCI Capable I/Os per Bank	Bank0	0	0	0	0	0	0
	Bank1	0	0	0	0	0	0
	Bank2	0	0	0	0	0	0
	Bank3	0	0	0	0	0	0
	Bank4	18	32	18	19	32	46
	Bank5	8	14	10	18	17	46
	Bank6	0	0	0	0	0	0
	Bank7	0	0	0	0	0	0
	Bank8	0	0	0	0	0	0

1. Minimum requirement to implement a fully functional 8-bit wide DDR bus. Available DDR interface consists of at least 12 I/Os (1 DQS + 1 DQSB + 8 DQs + 1 DM + Bank VREF1).

LFE2-12E/SE and LFE2-20E/SE Logic Signal Connections: 484 fpBGA (Cont.)

LFE2-12E/12SE					LFE2-20E/20SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
A6	PT21A	0		T	PT30A	0		T
GNDIO	GNDIO0	-			GNDIO0	-		
C7	PT17B	0		C	PT26B	0		C
D10	PT18B	0		C	PT27B	0		C
C6	PT17A	0		T	PT26A	0		T
E10	PT18A	0		T	PT27A	0		T
VCCIO	VCCIO0	0			VCCIO0	0		
F10	PT15B	0		C	PT24B	0		C
B6	PT16B	0		C	PT25B	0		C
D9	PT15A	0		T	PT24A	0		T
B5	PT16A	0		T	PT25A	0		T
GNDIO	GNDIO0	-			GNDIO0	-		
A5	PT13B	0		C	PT22B	0		C
F9	PT14B	0		C	PT23B	0		C
A4	PT13A	0		T	PT22A	0		T
E9	PT14A	0		T	PT23A	0		T
VCCIO	VCCIO0	0			VCCIO0	0		
G8	PT11B	0		C	PT20B	0		C
A3	PT12B	0		C	PT21B	0		C
E8	PT11A	0		T	PT20A	0		T
A2	PT12A	0		T	PT21A	0		T
GNDIO	GNDIO0	-			GNDIO0	-		
-	-	-			VCCIO0	0		
C3	PT10B	0		C	PT10B	0		C
B3	PT10A	0		T	PT10A	0		T
-	-	-			GNDIO0	-		
E7	PT8B	0		C	PT8B	0		C
F8	PT9B	0		C	PT9B	0		C
F7	PT8A	0		T	PT8A	0		T
D7	PT9A	0		T	PT9A	0		T
VCCIO	VCCIO0	0			VCCIO0	0		
D4	PT6B	0		C	PT6B	0		C
D5	PT7B	0		C	PT7B	0		C
C4	PT6A	0		T	PT6A	0		T
D6	PT7A	0		T	PT7A	0		T
GNDIO	GNDIO0	-			GNDIO	-		
J7	PT4B	0		C	PT4B	0		C
B2	PT5B	0		C	PT5B	0		C
H7	PT4A	0		T	PT4A	0		T
B1	PT5A	0		T	PT5A	0		T
VCCIO	VCCIO0	0			VCCIO0	0		
D1	PT2B	0	VREF2_0	C	PT2B	0	VREF2_0	C
D3	PT3B	0		C	PT3B	0		C
C1	PT2A	0	VREF1_0	T	PT2A	0	VREF1_0	T

LFE2-20E/SE and LFE2-35E/SE Logic Signal Connections: 672 fpBGA (Cont.)

LFE2-20E/20SE					LFE2-35E/35SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
G24	PR6B	2	RDQ8	C (LVDS)*	PR12B	2	RDQ14	C (LVDS)*
G23	PR6A	2	RDQ8	T (LVDS)*	PR12A	2	RDQ14	T (LVDS)*
VCCIO	VCCIO2	2			VCCIO2	2		
K19	PR5B	2	RDQ8	C	PR11B	2	RDQ14	C
J19	PR5A	2	RDQ8	T	PR11A	2	RDQ14	T
D26	PR4B	2	RDQ8	C (LVDS)*	PR10B	2	RDQ14	C (LVDS)*
C26	PR4A	2	RDQ8	T (LVDS)*	PR10A	2	RDQ14	T (LVDS)*
F22	NC	-			PR9B	2	RDQ6	C
E24	NC	-			PR9A	2	RDQ6	T
GND	GNDIO2	-			GNDIO2	-		
D25	NC	-			PR8B	2	RDQ6	C (LVDS)*
C25	NC	-			PR8A	2	RDQ6	T (LVDS)*
D24	NC	-			PR7B	2	RDQ6	C
B25	NC	-			PR7A	2	RDQ6	T
VCCIO	VCCIO2	2			VCCIO2	2		
H21	NC	-			PR6B	2	RDQ6	C (LVDS)*
G22	NC	-			PR6A	2	RDQS6	T (LVDS)*
B24	NC	-			PR5B	2	RDQ6	C
GND	GNDIO2	-			GNDIO2	-		
C24	NC	-			PR5A	2	RDQ6	T
D23	NC	-			PR4B	2	RDQ6	C (LVDS)*
C23	NC	-			PR4A	2	RDQ6	T (LVDS)*
G21	PR3B	2		C	PR3B	2	RDQ6	C
VCCIO	VCCIO2	2			VCCIO2	2		
H20	PR3A	2		T	PR3A	2	RDQ6	T
GND	GNDIO2	-			GNDIO2	-		
E22	PR2B	2	VREF2_2	C (LVDS)*	PR2B	2	VREF2_2/RDQ6	C (LVDS)*
F21	PR2A	2	VREF1_2	T (LVDS)*	PR2A	2	VREF1_2/RDQ6	T (LVDS)*
E23	PT64B	1	VREF2_1	C	PT73B	1	VREF2_1	C
GND	GNDIO1	-			GNDIO1	-		
D22	PT64A	1	VREF1_1	T	PT73A	1	VREF1_1	T
G20	PT63B	1		C	PT72B	1		C
J18	PT63A	1		T	PT72A	1		T
F20	PT62B	1		C	PT71B	1		C
VCCIO	VCCIO1	1			VCCIO1	1		
H19	PT62A	1		T	PT71A	1		T
A24	PT61B	1		C	PT70B	1		C
A23	PT61A	1		T	PT70A	1		T
E21	PT60B	1		C	PT69B	1		C
F19	PT60A	1		T	PT69A	1		T
C22	PT59B	1		C	PT68B	1		C
GND	GNDIO1	-			GNDIO1	-		
E20	PT59A	1		T	PT68A	1		T
B22	PT58B	1		C	PT67B	1		C
VCCIO	VCCIO1	1			VCCIO1	1		
B23	PT58A	1		T	PT67A	1		T

LFE2-50E/SE and LFE2-70E/SE Logic Signal Connections: 672 fpBGA

LFE2-50E/SE					LFE2-70E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential	
D2	PL2A	7	VREF2_7	T (LVDS)*	PL2A	7	VREF2_7	T (LVDS)*	
D1	PL2B	7	VREF1_7	C (LVDS)*	PL2B	7	VREF1_7	C (LVDS)*	
GND	GNDIO7	-			GNDIO7	-			
F6	PL5A	7	LDQ8	T	PL18A	7	LDQ21	T	
F5	PL5B	7	LDQ8	C	PL18B	7	LDQ21	C	
VCCIO	VCCIO7	7			VCCIO7	7			
E4	PL6A	7	LDQ8	T (LVDS)*	PL19A	7	LDQ21	T (LVDS)*	
E3	PL6B	7	LDQ8	C (LVDS)*	PL19B	7	LDQ21	C (LVDS)*	
E2	PL7A	7	LDQ8	T	PL20A	7	LDQ21	T	
E1	PL7B	7	LDQ8	C	PL20B	7	LDQ21	C	
GND	GNDIO7	-			GNDIO7	-			
H6	PL8A	7	LDQS8	T (LVDS)*	PL21A	7	LDQS21	T (LVDS)*	
H5	PL8B	7	LDQ8	C (LVDS)*	PL21B	7	LDQ21	C (LVDS)*	
F2	PL9A	7	LDQ8	T	PL22A	7	LDQ21	T	
VCCIO	VCCIO7	7			VCCIO7	7			
F1	PL9B	7	LDQ8	C	PL22B	7	LDQ21	C	
H8	PL10A	7	LDQ8	T (LVDS)*	PL23A	7	LDQ21	T (LVDS)*	
J9	PL10B	7	LDQ8	C (LVDS)*	PL23B	7	LDQ21	C (LVDS)*	
G4	PL11A	7	LDQ8	T	PL24A	7	LDQ21	T	
GND	GNDIO7	-			GNDIO7	-			
G3	PL11B	7	LDQ8	C	PL24B	7	LDQ21	C	
H7	PL12A	7	LDQ16	T (LVDS)*	PL25A	7	LDQ29	T (LVDS)*	
J8	PL12B	7	LDQ16	C (LVDS)*	PL25B	7	LDQ29	C (LVDS)*	
G2	PL13A	7	LDQ16	T	PL26A	7	LDQ29	T	
G1	PL13B	7	LDQ16	C	PL26B	7	LDQ29	C	
H3	PL14A	7	LDQ16	T (LVDS)*	PL27A	7	LDQ29	T (LVDS)*	
VCCIO	VCCIO7	7			VCCIO7	7			
H4	PL14B	7	LDQ16	C (LVDS)*	PL27B	7	LDQ29	C (LVDS)*	
J5	PL15A	7	LDQ16	T	PL28A	7	LDQ29	T	
J4	PL15B	7	LDQ16	C	PL28B	7	LDQ29	C	
J3	PL16A	7	LDQS16	T (LVDS)*	PL29A	7	LDQS29	T (LVDS)*	
GND	GNDIO7	-			GNDIO7	-			
K4	PL16B	7	LDQ16	C (LVDS)*	PL29B	7	LDQ29	C (LVDS)*	
H1	PL17A	7	LDQ16	T	PL30A	7	LDQ29	T	
H2	PL17B	7	LDQ16	C	PL30B	7	LDQ29	C	
VCCIO	VCCIO7	7			VCCIO7	7			
K6	PL18A	7	LDQ16	T (LVDS)*	PL31A	7	LDQ29	T (LVDS)*	
K7	PL18B	7	LDQ16	C (LVDS)*	PL31B	7	LDQ29	C (LVDS)*	
J1	PL19A	7	LDQ16	T	PL32A	7	LDQ29	T	
J2	PL19B	7	LDQ16	C	PL32B	7	LDQ29	C	
GND	GNDIO7	-			GNDIO7	-			
VCCIO	VCCIO7	7			VCCIO7	7			
K3	PL23A	7	LDQ24	T	PL36A	7	LDQ37	T	
K2	PL23B	7	LDQ24	C	PL36B	7	LDQ37	C	
GND	GNDIO7	-			GNDIO7	-			
K1	PL24A	7	LDQS24***	T (LVDS)*	PL37A	7	LDQS37***	T (LVDS)*	

LFE2-50E/SE and LFE2-70E/SE Logic Signal Connections: 672 fpBGA (Cont.)

LFE2-50E/SE					LFE2-70E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential	
G24	PR14B	2	RDQ16	C (LVDS)*	PR27B	2	RDQ29	C (LVDS)*	
G23	PR14A	2	RDQ16	T (LVDS)*	PR27A	2	RDQ29	T (LVDS)*	
VCCIO	VCCIO2	2			VCCIO2	2			
K19	PR13B	2	RDQ16	C	PR26B	2	RDQ29	C	
J19	PR13A	2	RDQ16	T	PR26A	2	RDQ29	T	
D26	PR12B	2	RDQ16	C (LVDS)*	PR25B	2	RDQ29	C (LVDS)*	
C26	PR12A	2	RDQ16	T (LVDS)*	PR25A	2	RDQ29	T (LVDS)*	
F22	PR11B	2	RDQ8	C	PR24B	2	RDQ21	C	
E24	PR11A	2	RDQ8	T	PR24A	2	RDQ21	T	
GND	GNDIO2	-			GNDIO2	-			
D25	PR10B	2	RDQ8	C (LVDS)*	PR23B	2	RDQ21	C (LVDS)*	
C25	PR10A	2	RDQ8	T (LVDS)*	PR23A	2	RDQ21	T (LVDS)*	
D24	PR9B	2	RDQ8	C	PR22B	2	RDQ21	C	
B25	PR9A	2	RDQ8	T	PR22A	2	RDQ21	T	
VCCIO	VCCIO2	2			VCCIO2	2			
H21	PR8B	2	RDQ8	C (LVDS)*	PR21B	2	RDQ21	C (LVDS)*	
G22	PR8A	2	RDQS8	T (LVDS)*	PR21A	2	RDQS21	T (LVDS)*	
B24	PR7B	2	RDQ8	C	PR20B	2	RDQ21	C	
GND	GNDIO2	-			GNDIO2	-			
C24	PR7A	2	RDQ8	T	PR20A	2	RDQ21	T	
D23	PR6B	2	RDQ8	C (LVDS)*	PR19B	2	RDQ21	C (LVDS)*	
C23	PR6A	2	RDQ8	T (LVDS)*	PR19A	2	RDQ21	T (LVDS)*	
G21	PR5B	2	RDQ8	C	PR18B	2	RDQ21	C	
VCCIO	VCCIO2	2			VCCIO2	2			
H20	PR5A	2	RDQ8	T	PR18A	2	RDQ21	T	
GND	GNDIO2	-			GNDIO2	-			
E22	PR2B	2	VREF2_2	C (LVDS)*	PR2B	2	VREF2_2	C (LVDS)*	
F21	PR2A	2	VREF1_2	T (LVDS)*	PR2A	2	VREF1_2	T (LVDS)*	
E23	PT82B	1	VREF2_1	C	PT100B	1	VREF2_1	C	
GND	GNDIO1	-			GNDIO1	-			
D22	PT82A	1	VREF1_1	T	PT100A	1	VREF1_1	T	
G20	PT81B	1		C	PT99B	1		C	
J18	PT81A	1		T	PT99A	1		T	
F20	PT80B	1		C	PT98B	1		C	
VCCIO	VCCIO1	1			VCCIO1	1			
H19	PT80A	1		T	PT98A	1		T	
A24	PT79B	1		C	PT97B	1		C	
A23	PT79A	1		T	PT97A	1		T	
E21	PT78B	1		C	PT96B	1		C	
F19	PT78A	1		T	PT96A	1		T	
C22	PT77B	1		C	PT95B	1		C	
GND	GNDIO1	-			GNDIO1	-			
E20	PT77A	1		T	PT95A	1		T	
B22	PT76B	1		C	PT94B	1		C	
VCCIO	VCCIO1	1			VCCIO1	1			
B23	PT76A	1		T	PT94A	1		T	

LFE2-50E/SE and LFE2-70E/SE Logic Signal Connections: 672 fpBGA (Cont.)

LFE2-50E/SE					LFE2-70E/SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
L23	VCCIO2	2			VCCIO2	2		
M17	VCCIO2	2			VCCIO2	2		
M18	VCCIO2	2			VCCIO2	2		
AA23	VCCIO3	3			VCCIO3	3		
R17	VCCIO3	3			VCCIO3	3		
R18	VCCIO3	3			VCCIO3	3		
T23	VCCIO3	3			VCCIO3	3		
V20	VCCIO3	3			VCCIO3	3		
AC16	VCCIO4	4			VCCIO4	4		
AC21	VCCIO4	4			VCCIO4	4		
U15	VCCIO4	4			VCCIO4	4		
V15	VCCIO4	4			VCCIO4	4		
Y18	VCCIO4	4			VCCIO4	4		
AC11	VCCIO5	5			VCCIO5	5		
AC6	VCCIO5	5			VCCIO5	5		
U12	VCCIO5	5			VCCIO5	5		
V12	VCCIO5	5			VCCIO5	5		
Y9	VCCIO5	5			VCCIO5	5		
AA4	VCCIO6	6			VCCIO6	6		
R10	VCCIO6	6			VCCIO6	6		
R9	VCCIO6	6			VCCIO6	6		
T4	VCCIO6	6			VCCIO6	6		
V7	VCCIO6	6			VCCIO6	6		
F4	VCCIO7	7			VCCIO7	7		
J7	VCCIO7	7			VCCIO7	7		
L4	VCCIO7	7			VCCIO7	7		
M10	VCCIO7	7			VCCIO7	7		
M9	VCCIO7	7			VCCIO7	7		
AE25	VCCIO8	8			VCCIO8	8		
V18	VCCIO8	8			VCCIO8	8		
J10	VCCAUX	-			VCCAUX	-		
J11	VCCAUX	-			VCCAUX	-		
J16	VCCAUX	-			VCCAUX	-		
J17	VCCAUX	-			VCCAUX	-		
K18	VCCAUX	-			VCCAUX	-		
K9	VCCAUX	-			VCCAUX	-		
L18	VCCAUX	-			VCCAUX	-		
L9	VCCAUX	-			VCCAUX	-		
T18	VCCAUX	-			VCCAUX	-		
T9	VCCAUX	-			VCCAUX	-		
U18	VCCAUX	-			VCCAUX	-		
U9	VCCAUX	-			VCCAUX	-		
V10	VCCAUX	-			VCCAUX	-		
V11	VCCAUX	-			VCCAUX	-		
V16	VCCAUX	-			VCCAUX	-		
V17	VCCAUX	-			VCCAUX	-		

LFE2M35E/SE and LFE2M50E/SE Logic Signal Connections: 672 fpBGA (Cont.)

LFE2M35E/SE					LFE2M50E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential	
U9	PL67B	6	LDQ66	C	PL72B	6	LDQ71	C	
AA5	PL68A	6	LDQ66	T (LVDS)*	PL73A	6	LDQ71	T*	
AA6	PL68B	6	LDQ66	C (LVDS)*	PL73B	6	LDQ71	C*	
Y7	PL69A	6	LDQ66	T	PL74A	6	LDQ71	T	
GNDIO	GNDIO6	-			GNDIO6	-			
V9	PL69B	6	LDQ66	C	PL74B	6	LDQ71	C	
AC3	TCK	-			TCK	-			
W8	TDI	-			TDI	-			
AC4	TMS	-			TMS	-			
V8	TDO	-			TDO	-			
AA7	VCCJ	-			VCCJ	-			
AB6	PB2A	5	BDQ6	T	PB2A	5	BDQ6	T	
Y8	PB2B	5	BDQ6	C	PB2B	5	BDQ6	C	
AD1	PB3A	5	BDQ6	T	PB3A	5	BDQ6	T	
AD2	PB3B	5	BDQ6	C	PB3B	5	BDQ6	C	
AC5	PB4A	5	BDQ6	T	PB4A	5	BDQ6	T	
AA8	PB4B	5	BDQ6	C	PB4B	5	BDQ6	C	
VCCIO	VCCIO5	5			VCCIO5	5			
AC6	PB5A	5	BDQ6	T	PB5A	5	BDQ6	T	
W9	PB5B	5	BDQ6	C	PB5B	5	BDQ6	C	
AB7	PB6A	5	BDQS6	T	PB6A	5	BDQS6	T	
GNDIO	GNDIO5	-			GNDIO5	-			
Y9	PB6B	5	BDQ6	C	PB6B	5	BDQ6	C	
AD3	PB7A	5	BDQ6	T	PB7A	5	BDQ6	T	
AD4	PB7B	5	BDQ6	C	PB7B	5	BDQ6	C	
AA9	PB8A	5	BDQ6	T	PB8A	5	BDQ6	T	
W10	PB8B	5	BDQ6	C	PB8B	5	BDQ6	C	
VCCIO	VCCIO5	5			VCCIO5	5			
AC7	PB9A	5	BDQ6	T	PB9A	5	BDQ6	T	
Y10	PB9B	5	BDQ6	C	PB9B	5	BDQ6	C	
AE2	PB10A	5	BDQ6	T	PB10A	5	BDQ6	T	
AD5	PB10B	5	BDQ6	C	PB10B	5	BDQ6	C	
GNDIO	GNDIO5	-			GNDIO5	-			
AE4	PB11A	5	BDQ15	T	PB11A	5	BDQ15	T	
AE3	PB11B	5	BDQ15	C	PB11B	5	BDQ15	C	
W11	PB12A	5	BDQ15	T	PB12A	5	BDQ15	T	
AB8	PB12B	5	BDQ15	C	PB12B	5	BDQ15	C	
AE5	PB13A	5	BDQ15	T	PB13A	5	BDQ15	T	
AD6	PB13B	5	BDQ15	C	PB13B	5	BDQ15	C	
VCCIO	VCCIO5	5			VCCIO5	5			
AA10	PB14A	5	BDQ15	T	PB14A	5	BDQ15	T	
AC8	PB14B	5	BDQ15	C	PB14B	5	BDQ15	C	
W12	PB15A	5	BDQS15	T	PB15A	5	BDQS15	T	
GNDIO	GNDIO5	-			GNDIO5	-			
AC9	PB15B	5	BDQ15	C	PB15B	5	BDQ15	C	
W13	PB16A	5	BDQ15	T	PB16A	5	BDQ15	T	
AB10	PB16B	5	BDQ15	C	PB16B	5	BDQ15	C	
AF3	PB17A	5	BDQ15	T	PB17A	5	BDQ15	T	

LFE2M50E/SE and LFE2M70E/SE Logic Signal Connections: 900 fpBGA (Cont.)

LFE2M50E/SE					LFE2M70E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential	
AH12	VCC	-			LLC_SQ_VCCR1	14			
AK8	PB16A	5	BDQ15	T	LLC_SQ_HDOUTP1	14		T	
AH8	NC	-			LLC_SQ_VCCOB1	14			
AJ8	PB16B	5	BDQ15	C	LLC_SQ_HDOUTN1	14		C	
AH9	VCC	-			LLC_SQ_VCCTX1	14			
AJ9	PB17B	5	BDQ15	C	LLC_SQ_HDOUTN0	14		C	
AK10	NC	-			LLC_SQ_VCCOB0	14			
AK9	PB17A	5	BDQ15	T	LLC_SQ_HDOUTP0	14		T	
AH10	VCC	-			LLC_SQ_VCCTX0	14			
AJ12	PB19B	5	BDQ15	C	LLC_SQ_HDINN0	14		C	
AJ13	NC	-			LLC_SQ_VCCIB0	14			
AK12	PB19A	5	BDQ15	T	LLC_SQ_HDINP0	14		T	
AH13	VCC	-			LLC_SQ_VCCR0	14			
AF10	PB3A	5	BDQ6	T	PB30A	5	BDQ33	T	
AE8	PB3B	5	BDQ6	C	PB30B	5	BDQ33	C	
AE11	PB4A	5	BDQ6	T	PB31A	5	BDQ33	T	
VCCIO	VCCIO5	5			VCCIO5	5			
AD9	PB4B	5	BDQ6	C	PB31B	5	BDQ33	C	
AE10	PB5A	5	BDQ6	T	PB32A	5	BDQ33	T	
AD10	PB5B	5	BDQ6	C	PB32B	5	BDQ33	C	
AE13	PB6A	5	BDQS6	T	PB33A	5	BDQS33	T	
GNDIO	GNDIO5	-			GNDIO5	-			
AC12	PB6B	5	BDQ6	C	PB33B	5	BDQ33	C	
AG2	PB7A	5	BDQ6	T	PB34A	5	BDQ33	T	
AG3	PB7B	5	BDQ6	C	PB34B	5	BDQ33	C	
AD13	PB8A	5	BDQ6	T	PB35A	5	BDQ33	T	
VCCIO	VCCIO5	5			VCCIO5	5			
AC13	PB8B	5	BDQ6	C	PB35B	5	BDQ33	C	
AE14	PB9A	5	BDQ6	T	PB36A	5	BDQ33	T	
AC14	PB9B	5	BDQ6	C	PB36B	5	BDQ33	C	
AF3	PB10A	5	BDQ6	T	PB37A	5	BDQ33	T	
GNDIO	GNDIO5	-			GNDIO5	-			
AF4	PB10B	5	BDQ6	C	PB37B	5	BDQ33	C	
VCCIO	VCCIO5	5			-	-			
AG4	PB20A	5	BDQ24	T	PB38A	5	BDQ42	T	
AG5	PB20B	5	BDQ24	C	PB38B	5	BDQ42	C	
GNDIO	GNDIO5	-			-	-			
VCCIO	VCCIO5	5			-	-			
AD11	PB24A	5	BDQS24****	T	PB39A	5	BDQ42	T	
AF13	PB24B	5	BDQ24	C	PB39B	5	BDQ42	C	
AF12	PB25A	5	BDQ24	T	PB40A	5	BDQ42	T	
-	-	-			VCCIO5	5			
AD14	PB25B	5	BDQ24	C	PB40B	5	BDQ42	C	
AG8	PB26A	5	BDQ24	T	PB41A	5	BDQ42	T	
AF8	PB26B	5	BDQ24	C	PB41B	5	BDQ42	C	
AE15	PB27A	5	BDQ24	T	PB42A	5	BDQS42****	T	
-	-	-			GNDIO5	-			
VCCIO	VCCIO5	5			-	-			

LFE2M50E/SE and LFE2M70E/SE Logic Signal Connections: 900 fpBGA (Cont.)

LFE2M50E/SE					LFE2M70E/SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
Y15	GND	-			GND	-		
Y16	GND	-			GND	-		
Y17	GND	-			GND	-		
AA26	NC	-			NC	-		
AB10	PL73B	6	LDQ71	C (LVDS)*	NC	-		
AB11	NC	-			NC	-		
AB12	NC	-			NC	-		
AB13	NC	-			NC	-		
AB14	NC	-			NC	-		
AB15	NC	-			NC	-		
AB16	NC	-			NC	-		
AB17	NC	-			NC	-		
AB19	NC	-			NC	-		
AB20	NC	-			NC	-		
AB21	NC	-			NC	-		
AB9	PL73A	6	LDQ71	T (LVDS)*	NC	-		
AC10	PL74B	6	LDQ71	C	NC	-		
AC11	NC	-			NC	-		
AC21	NC	-			NC	-		
AC22	NC	-			NC	-		
AC8	PL70B	6	LDQ71	C	NC	-		
AC9	PL74A	6	LDQ71	T	NC	-		
AD21	NC	-			NC	-		
AD22	NC	-			NC	-		
AD4	PL68A	6	LDQ71	T	NC	-		
AD5	PL68B	6	LDQ71	C	NC	-		
AD6	PL71A	6	LDQS71	T (LVDS)*	NC	-		
AD7	PL72A	6	LDQ71	T	NC	-		
AD8	PL72B	6	LDQ71	C	NC	-		
AE23	NC	-			NC	-		
AE5	PL69A	6	LDQ71	T (LVDS)*	NC	-		
AE6	PL70A	6	LDQ71	T	NC	-		
AE7	PL71B	6	LDQ71	C (LVDS)*	NC	-		
AF20	NC	-			NC	-		
AF23	NC	-			NC	-		
AF5	PL69B	6	LDQ71	C (LVDS)*	NC	-		
AG23	NC	-			NC	-		
AG26	NC	-			NC	-		
D10	PT10A	0		T	NC	-		
E10	PT9B	0		C	NC	-		
E11	PT10B	0		C	NC	-		
F10	PT9A	0		T	NC	-		
F20	NC	-			NC	-		
F23	NC	-			NC	-		
F8	PL6B	7	LDQ6	C (LVDS)*	NC	-		
G10	NC	-			NC	-		
G20	NC	-			NC	-		
G21	NC	-			NC	-		

LFE2M50E/SE and LFE2M70E/SE Logic Signal Connections: 900 fpBGA (Cont.)

LFE2M50E/SE					LFE2M70E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential	
G7	PL8A	7	LDQ6	T (LVDS)*	NC	-			
G8	PL6A	7	LDQS6****	T (LVDS)*	NC	-			
G9	PL5A	7	LDQ6	T	NC	-			
H19	NC	-			NC	-			
H20	NC	-			NC	-			
H21	NC	-			NC	-			
H22	NC	-			NC	-			
H6	PL8B	7	LDQ6	C (LVDS)*	NC	-			
H8	PL5B	7	LDQ6	C	NC	-			
H9	PL2A	7	LDQ6	T (LVDS)*	NC	-			
J10	PL2B	7	LDQ6	C (LVDS)*	NC	-			
J20	NC	-			NC	-			
J21	NC	-			NC	-			
J9	PL4A	7	LDQ6	T (LVDS)*	NC	-			
K9	PL4B	7	LDQ6	C (LVDS)*	NC	-			
R9	NC	-			NC	-			
U22	NC	-			NC	-			
W9	NC	-			NC	-			
N13	VCCPLL	-			VCCPLL	-			
N18	VCCPLL	-			VCCPLL	-			
V13	VCCPLL	-			VCCPLL	-			
V18	VCCPLL	-			VCCPLL	-			

* Supports true LVDS. Other differential signals must be emulated with external resistors.

** These dedicated input pins can be used for GPLLs or GDLLs within the respective quadrant.

*** These sysCONFIG pins are dedicated I/O pins for configuration. The outputs are actively driven during normal device operation.

****Due to packaging bond out option, this DQS does not have all the necessary DQ pins bonded out for a full 8-bit data width.

Note: VCCIO and GND pads are used to determine the average DC current drawn by I/Os between GND/VCCIO connections, or between the last GND/VCCIO in an I/O bank and the end of an I/O bank. The substrate pads listed in the Pin Table do not necessarily have a one to one connection with a package ball or pin.

LFE2M70E/SE and LFE2M100E/SE Logic Signal Connections: 1152 fpBGA (Cont.)

LFE2M70E/SE				LFE2M100E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
E23	PT82B	1		C	PT100B	1		C
GNDIO	GNDIO1	-			GNDIO1	-		
F23	PT82A	1		T	PT100A	1		T
F24	NC	-			PT99B	1		C
G23	NC	-			PT99A	1		T
D23	PT80B	1		C	PT98B	1		C
VCCIO	VCCIO1	1			VCCIO1	1		
D22	PT80A	1		T	PT98A	1		T
-	-	-			GNDIO1	-		
-	-	-			VCCIO1	1		
C21	PT79B	1		C	PT88B	1		C
D21	PT79A	1		T	PT88A	1		T
GNDIO	GNDIO1	-			GNDIO1	-		
B21	PT77B	1		C	PT86B	1		C
A21	PT77A	1		T	PT86A	1		T
F22	PT76B	1		C	PT85B	1		C
E22	PT76A	1		T	PT85A	1		T
VCCIO	VCCIO1	1			VCCIO1	1		
GNDIO	GNDIO1	-			-	-		
J22	NC	-			PT84B	1		C
G22	NC	-			PT84A	1		T
-	-	-			GNDIO1	-		
H22	PT72B	1		C	PT81B	1		C
K22	PT72A	1		T	PT81A	1		T
G21	PT71B	1		C	PT80B	1		C
VCCIO	VCCIO1	1			VCCIO1	1		
J21	PT71A	1		T	PT80A	1		T
H21	NC	-			PT79B	1		C
K21	NC	-			PT79A	1		T
D20	PT69B	1		C	PT78B	1		C
F20	PT69A	1		T	PT78A	1		T
C20	PT68B	1		C	PT77B	1		C
GNDIO	GNDIO1	-			GNDIO1	-		
E20	PT68A	1		T	PT77A	1		T
G20	PT67B	1		C	PT76B	1		C
VCCIO	VCCIO1	1			VCCIO1	1		
J20	PT67A	1		T	PT76A	1		T
A20	PT66B	1		C	PT75B	1		C
B20	PT66A	1		T	PT75A	1		T
GNDIO	GNDIO1	-			GNDIO1	-		
A19	PT63B	1		C	PT72B	1		C
B19	PT63A	1		T	PT72A	1		T
K20	PT62B	1		C	PT71B	1		C
H20	PT62A	1		T	PT71A	1		T
VCCIO	VCCIO1	1			VCCIO1	1		
L19	NC	-			PT70B	1		C
L20	NC	-			PT70A	1		T
E19	PT60B	1		C	PT69B	1		C
C18	PT60A	1		T	PT69A	1		T

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2-20E-5Q208I	131	1.2V	-5	PQFP	208	IND	20
LFE2-20E-6Q208I	131	1.2V	-6	PQFP	208	IND	20
LFE2-20E-5F256I	193	1.2V	-5	fpBGA	256	IND	20
LFE2-20E-6F256I	193	1.2V	-6	fpBGA	256	IND	20
LFE2-20E-5F484I	331	1.2V	-5	fpBGA	484	IND	20
LFE2-20E-6F484I	331	1.2V	-6	fpBGA	484	IND	20
LFE2-20E-5F672I	402	1.2V	-5	fpBGA	672	IND	20
LFE2-20E-6F672I	402	1.2V	-6	fpBGA	672	IND	20

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2-35E-5F484I	331	1.2V	-5	fpBGA	484	IND	35
LFE2-35E-6F484I	331	1.2V	-6	fpBGA	484	IND	35
LFE2-35E-5F672I	450	1.2V	-5	fpBGA	672	IND	35
LFE2-35E-6F672I	450	1.2V	-6	fpBGA	672	IND	35

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2-50E-5F484I	339	1.2V	-5	fpBGA	484	IND	50
LFE2-50E-6F484I	339	1.2V	-6	fpBGA	484	IND	50
LFE2-50E-5F672I	500	1.2V	-5	fpBGA	672	IND	50
LFE2-50E-6F672I	500	1.2V	-6	fpBGA	672	IND	50

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2-70E-5F672I	500	1.2V	-5	fpBGA	672	IND	70
LFE2-70E-6F672I	500	1.2V	-6	fpBGA	672	IND	70
LFE2-70E-5F900I	583	1.2V	-5	fpBGA	900	IND	70
LFE2-70E-6F900I	583	1.2V	-6	fpBGA	900	IND	70

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2-35SE-5FN484C	331	1.2V	-5	Lead-Free fpBGA	484	Com	35
LFE2-35SE-6FN484C	331	1.2V	-6	Lead-Free fpBGA	484	Com	35
LFE2-35SE-7FN484C	331	1.2V	-7	Lead-Free fpBGA	484	Com	35
LFE2-35SE-5FN672C	450	1.2V	-5	Lead-Free fpBGA	672	Com	35
LFE2-35SE-6FN672C	450	1.2V	-6	Lead-Free fpBGA	672	Com	35
LFE2-35SE-7FN672C	450	1.2V	-7	Lead-Free fpBGA	672	Com	35

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2-50SE-5FN484C	339	1.2V	-5	Lead-Free fpBGA	484	Com	50
LFE2-50SE-6FN484C	339	1.2V	-6	Lead-Free fpBGA	484	Com	50
LFE2-50SE-7FN484C	339	1.2V	-7	Lead-Free fpBGA	484	Com	50
LFE2-50SE-5FN672C	500	1.2V	-5	Lead-Free fpBGA	672	Com	50
LFE2-50SE-6FN672C	500	1.2V	-6	Lead-Free fpBGA	672	Com	50
LFE2-50SE-7FN672C	500	1.2V	-7	Lead-Free fpBGA	672	Com	50

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2-70SE-5FN672C	500	1.2V	-5	Lead-Free fpBGA	672	Com	70
LFE2-70SE-6FN672C	500	1.2V	-6	Lead-Free fpBGA	672	Com	70
LFE2-70SE-7FN672C	500	1.2V	-7	Lead-Free fpBGA	672	Com	70
LFE2-70SE-5FN900C	583	1.2V	-5	Lead-Free fpBGA	900	Com	70
LFE2-70SE-6FN900C	583	1.2V	-6	Lead-Free fpBGA	900	Com	70
LFE2-70SE-7FN900C	583	1.2V	-7	Lead-Free fpBGA	900	Com	70

Industrial

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2-6SE-5TN144I	90	1.2V	-5	Lead-Free TQFP	144	Ind	6
LFE2-6SE-6TN144I	90	1.2V	-6	Lead-Free TQFP	144	Ind	6
LFE2-6SE-5FN256I	190	1.2V	-5	Lead-Free fpBGA	256	Ind	6
LFE2-6SE-6FN256I	190	1.2V	-6	Lead-Free fpBGA	256	Ind	6

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2-12SE-5TN144I	93	1.2V	-5	Lead-Free TQFP	144	Ind	12
LFE2-12SE-6TN144I	93	1.2V	-6	Lead-Free TQFP	144	Ind	12
LFE2-12SE-5QN208I	131	1.2V	-5	Lead-Free PQFP	208	Ind	12
LFE2-12SE-6QN208I	131	1.2V	-6	Lead-Free PQFP	208	Ind	12
LFE2-12SE-5FN256I	193	1.2V	-5	Lead-Free fpBGA	256	Ind	12
LFE2-12SE-6FN256I	193	1.2V	-6	Lead-Free fpBGA	256	Ind	12
LFE2-12SE-5FN484I	297	1.2V	-5	Lead-Free fpBGA	484	Ind	12
LFE2-12SE-6FN484I	297	1.2V	-6	Lead-Free fpBGA	484	Ind	12

Date	Version	Section	Change Summary
August 2007 (cont.)	02.8 (cont.)	DC and Switching (cont.)	sysCLOCK GPLL timing has been updated.
		Pinout Information	Added ECP2M50 (484/672/900-fpBGA), ECP2M70 (900-fpBGA) and ECP2M100 (900-fpBGA) pinout information.
		Ordering Information	1156-fpBGA package option has been removed from the LatticeECP2M family.
September 2007	02.9	Pinout Information	Added Thermal Management text section.
February 2008	03.0	Architecture	Added LVC MOS33D description.
		DC and Switching	LatticeECP2M Supply Current has been updated.
			Typical Building Block Function Performance, External Switching Characteristics, Internal Switching Characteristics, Family Timing Adders, sysCLOCK GPLL Timing, sysCLOCK SPLL Timing, DLL Timing and sysCONFIG Port Timing Specifications have been updated (timing rev. A 0.11).
			Figure 3-9. Read/Write Mode (Normal) and Figure 3-10. Read/Write Mode with Input and Output Registers have been updated.
			Table 3-8. Channel output Jitter (Max) has been updated.
		Pinout Information	Signal description has been updated.
April 2008	03.1	Pinout Information	Added 1152-fpBGA pinouts for the ECP2M70 and ECP2M100.
June 2008	03.2	Pinout Information	Available DDR Interfaces per I/O Bank for the LFE2M35 (484/672-fpBGA) have been updated.
		Introduction	Family Selection Guide table - Updated number of EBR SRAM Blocks for the ECP2-70 device.
		Architecture	Removed Read-Before-Write sysMEM EBR mode.
		Architecture	Clarification of the operation of the secondary clock regions.
August 2008	03.3	DC and Switching Characteristics	Removed Read-Before-Write sysMEM EBR mode.
		Architecture	Clarification of the operation of the secondary clock regions.
		Pinout Information	Added information for [LOC]DQ[num] to Signal Descriptions table.
January 2009	03.4	DC and Switching Characteristics	Updated typical and max. jitter numbers in Channel Output Jitter table for x10 mode.
			Added Channel Output Jitter table for x20 mode.
November 2009	03.5	DC and Switching Characteristics	Updated SPI/SPI _m Configuration Waveforms diagram.
			Updated footnotes in LatticeECP2 Initialization Supply Current table.
			Updated footnotes in LatticeECP2M Initialization Supply Current table.
			Updated footnotes in SERDES High Speed Data Receiver (LatticeECP2M Family Only) table.
			Updated max. value for t _{DINIT} parameter in LatticeECP2/M sysCONFIG Port Timing Specifications table.
			Updated Serial Output Timing and Levels table.
			Updated Figure 3-5 MLVDS
			Updated Table 3-7 Serial Output Timing and Levels
			Updated Table 3-15 Power Down/Power Up Specification
		Pinout Information	Signal Descriptions table - corrected references to ULM, URM, LRM (changed to LUM, RUM and RLM), added footnote 5.