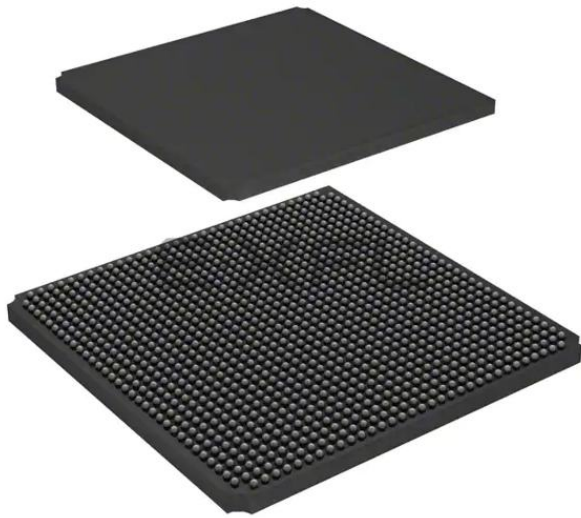




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Applications of Embedded - FPGAs

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Details

Product Status	Not For New Designs
Number of LABs/CLBs	8375
Number of Logic Elements/Cells	67000
Total RAM Bits	4642816
Number of I/O	436
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1152-BBGA
Supplier Device Package	1152-FPBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfe2m70e-7fn1152c

one clock is selected for each input register, pipeline register and output register. Similarly Clock enable (CE) and Reset (RST) are selected from their four respective sources (CE0, CE1, CE2, CE3 and RST0, RST1, RST2, RST3) at each input register, pipeline register and output register.

Signed and Unsigned with Different Widths

The DSP block supports different widths of signed and unsigned multipliers besides x9, x18 and x36 widths. For unsigned operands, unused upper data bits should be filled to create a valid x9, x18 or x36 operand. For signed two's complement operands, sign extension of the most significant bit should be performed until x9, x18 or x36 width is reached. Table 2-8 provides an example of this.

Table 2-8. Sign Extension Example

Number	Unsigned	Unsigned 9-bit	Unsigned 18-bit	Signed	Two's Complement Signed 9 Bits	Two's Complement Signed 18 Bits
+5	0101	000000101	0000000000000000101	0101	000000101	0000000000000000101
-6	N/A	N/A	N/A	1010	11111010	111111111111111010

OVERFLOW Flag from MAC

The sysDSP block provides an overflow output to indicate that the accumulator has overflowed. When two unsigned numbers are added and the result is a smaller number than the accumulator, “roll-over” is said to have occurred and an overflow signal is indicated. When two positive numbers are added with a negative sum and when two negative numbers are added with a positive sum, then the accumulator “roll-over” is said to have occurred and an overflow signal is indicated. Note that when overflow occurs the overflow flag is present for only one cycle. By counting these overflow pulses in FPGA logic, larger accumulators can be constructed. The conditions overflow signals for signed and unsigned operands are listed in Figure 2-27.

Figure 2-27. Accumulator Overflow/Underflow

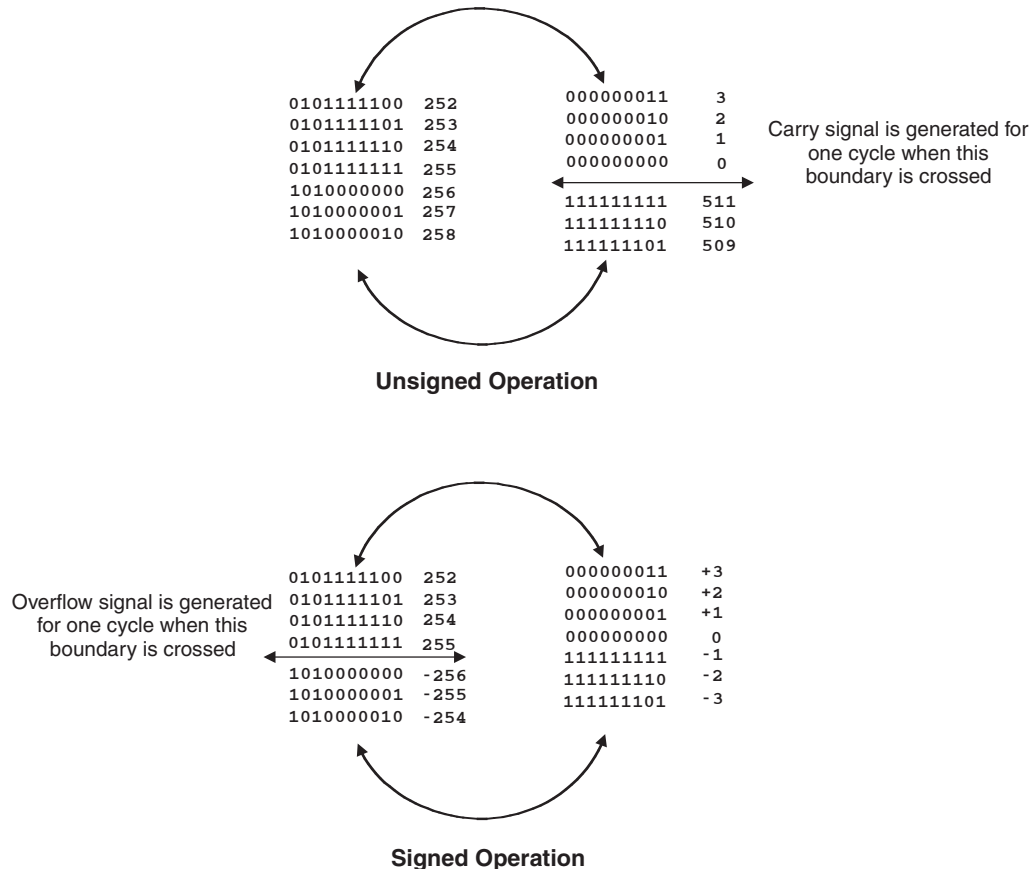
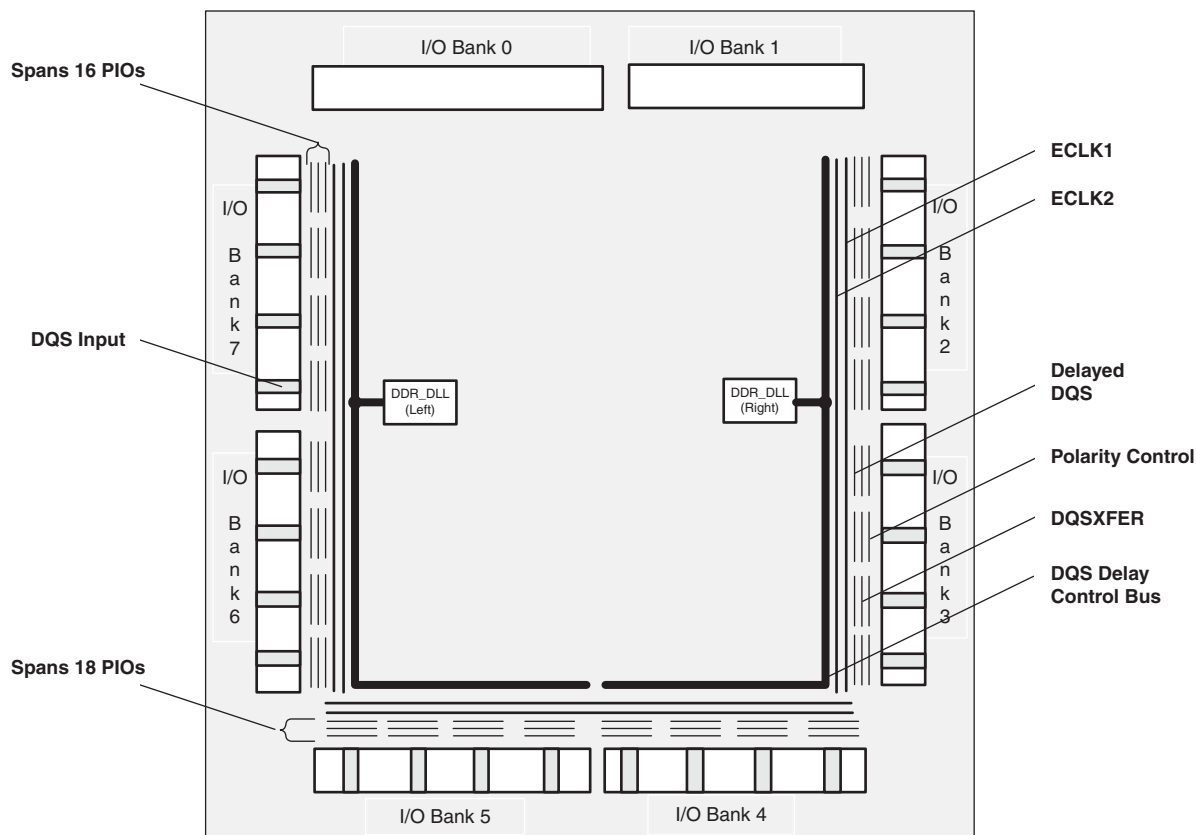
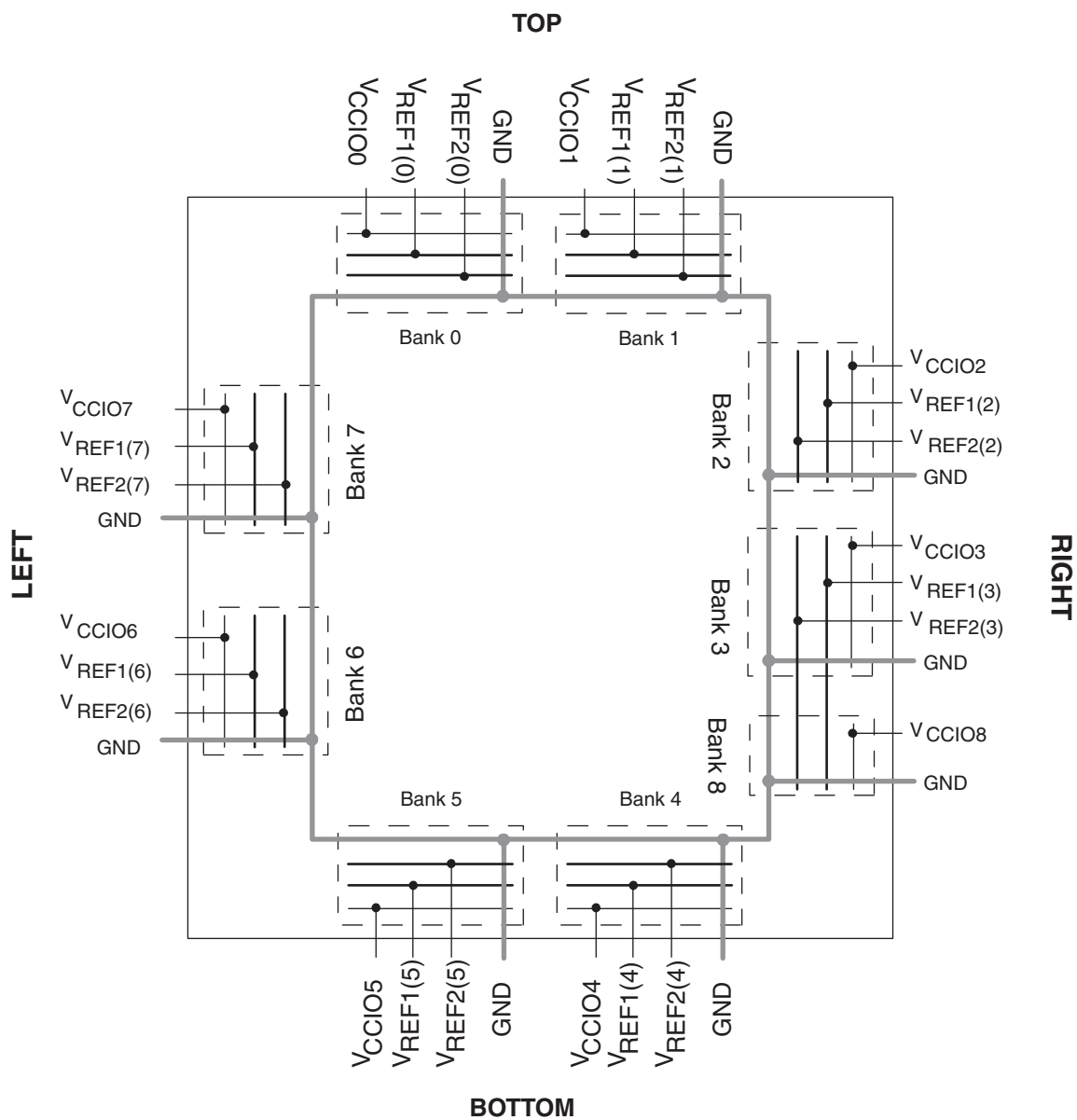


Figure 2-35. Edge Clock, DLL Calibration and DQS Local Bus Distribution



Note: Bank 8 is not shown.

Figure 2-37. LatticeECP2 Banks



LVPECL

The LatticeECP2/M devices support the differential LVPECL standard. This standard is emulated using complementary LVCMOS outputs in conjunction with a parallel resistor across the driver outputs. The LVPECL input standard is supported by the LVDS differential input buffer. The scheme shown in Figure 3-3 is one possible solution for point-to-point signals.

Figure 3-3. Differential LVPECL

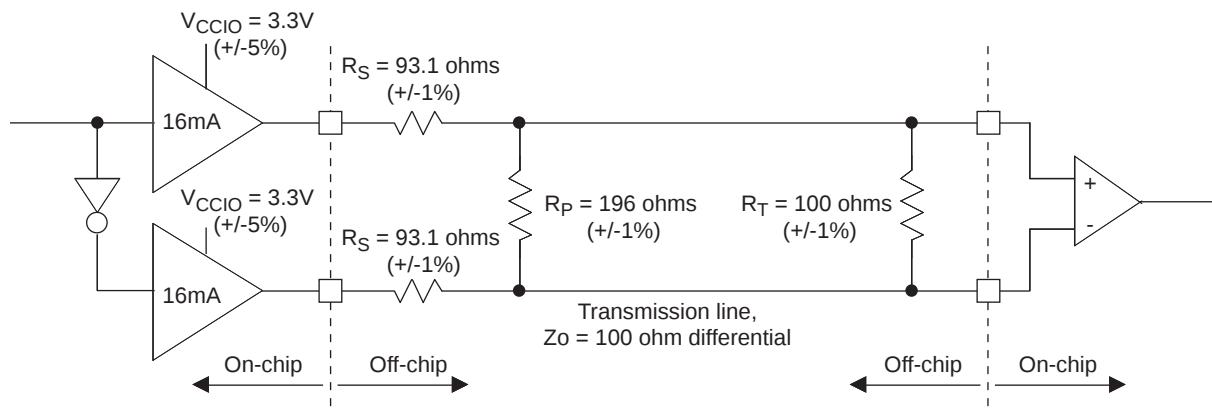


Table 3-4. LVPECL DC Conditions¹

Over Recommended Operating Conditions

Parameter	Description	Typical	Units
V_{CCIO}	Output Driver Supply (+/-5%)	3.30	V
Z_{OUT}	Driver Impedance	10	Ω
R_S	Driver Series Resistor (+/-1%)	93	Ω
R_P	Driver Parallel Resistor (+/-1%)	196	Ω
R_T	Receiver Termination (+/-1%)	100	Ω
V_{OH}	Output High Voltage	2.05	V
V_{OL}	Output Low Voltage	1.25	V
V_{OD}	Output Differential Voltage	0.80	V
V_{CM}	Output Common Mode Voltage	1.65	V
Z_{BACK}	Back Impedance	100.5	Ω
I_{DC}	DC Output Current	12.11	mA

1. For input buffer, see LVDS table.

SERDES High-Speed Data Transmitter (LatticeECP2M Family Only)^{1, 2}

Table 3-7. Serial Output Timing and Levels

Symbol	Description	Frequency	Min.	Typ.	Max.	Units
V _{TX-DIFF-P-P-1}	Differential swing (1V setting) ^{1, 2}	0.25 to 3.125 Gbps	0.79	0.99	1.19	V, p-p
V _{TX-DIFF-P-P-1.25}	Differential swing (1.25V setting) ^{1, 2}	0.25 to 3.125 Gbps	1.00	1.25	1.50	V, p-p
V _{TX-DIFF-P-P-1.3}	Differential swing (1.3V setting) ^{1, 2}	0.25 to 3.125 Gbps	1.04	1.30	1.56	V, p-p
V _{TX-DIFF-P-P-1.35}	Differential swing (1.35V setting) ^{1, 2}	0.25 to 3.125 Gbps	1.08	1.35	1.62	V, p-p
V _{OCM}	Output common mode voltage	—	V _{CCOB} - 0.75	V _{CCOB} - 0.60	V _{CCOB} - 0.45	V
T _{TX-R}	Rise time (20% to 80%)	—	—	70	—	ps
T _{TX-F}	Fall time (80% to 20%)	—	—	70	—	ps
Z _{TX-OI-SE}	Output impedance 50/75/HiZ K Ohms (single-ended)	—	—	50/70 HiZ	—	Ohms
R _{TX-RL}	Return loss (with package)	—	—	9	—	dB

1. All measurements are with 50 ohm impedance.

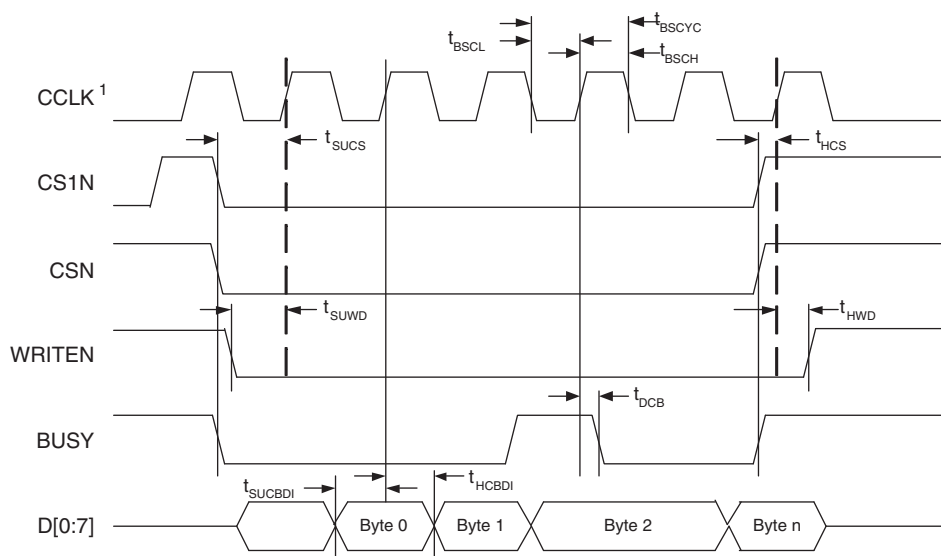
2. See TN1124, [LatticeECP2M SERDES/PCS Usage Guide](#) for actual binary settings.

Table 3-8. Channel Output Jitter - x10 Mode

Description	Frequency	Min.	Typ.	Max.	Units
Deterministic	3.125 Gbps	—	0.08	0.12	UI, p-p
Random	3.125 Gbps	—	0.22	0.38	UI, p-p
Total	3.125 Gbps	—	0.33	0.43	UI, p-p
Deterministic	2.5 Gbps	—	0.08	0.17	UI, p-p
Random	2.5 Gbps	—	0.20	0.25	UI, p-p
Total	2.5 Gbps	—	0.25	0.35	UI, p-p
Deterministic	1.25 Gbps	—	0.03	0.10	UI, p-p
Random	1.25 Gbps	—	0.14	0.19	UI, p-p
Total	1.25 Gbps	—	0.17	0.24	UI, p-p
Deterministic	250 Mbps	—	0.04	0.17	UI, p-p
Random	250 Mbps	—	0.12	0.13	UI, p-p
Total	250 Mbps	—	0.15	0.29	UI, p-p

Note: Values are measured with PRBS 2⁷-1, all channels operating, FPGA Logic active, I/Os around SERDES pins quiet, reference clock at x10 mode.

Figure 3-15. sysCONFIG Parallel Port Write Cycle



1. In Master Parallel Mode the FPGA provides CCLK. In Slave Parallel Mode the external device provides CCLK.

Figure 3-16. sysCONFIG Slave Serial Port Timing

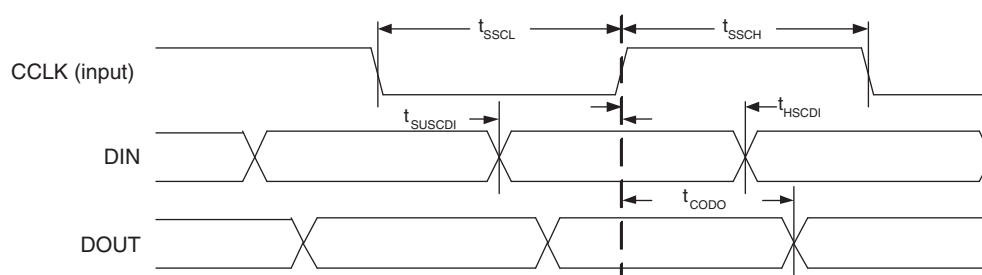
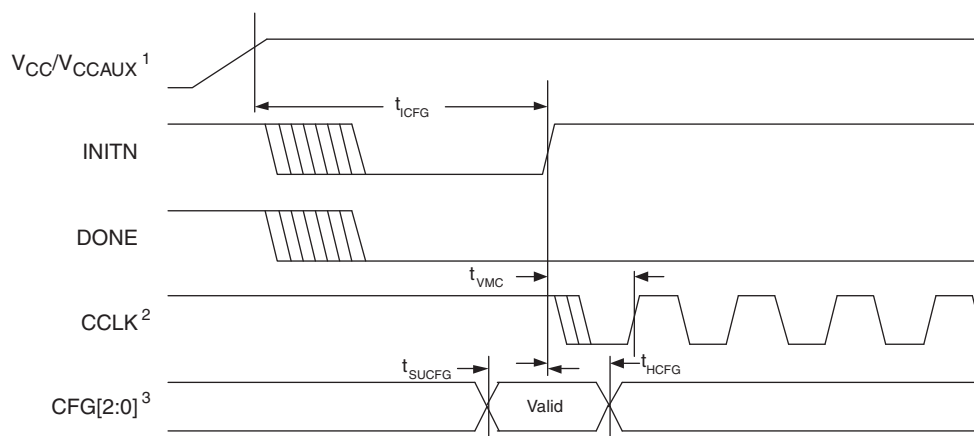


Figure 3-17. Power-On-Reset (POR) Timing



1. Time taken from V_{CC} or V_{CCAUX} , whichever is the last to reach its V_{MIN} .
2. Device is in a Master Mode.
3. The CFG pins are normally static (hard wired).

LatticeECP2 Pin Information Summary, LFE2-6 and LFE2-12

Pin Type		LFE2-6		LFE2-12			
		144 TQFP	256 fpBGA	144 TQFP	208 PQFP	256 fpBGA	484 fpBGA
Single Ended User I/O		90	190	93	131	193	297
Differential Pair User I/O		43	95	45	62	96	148
Configuration	TAP Pins	5	5	5	5	5	5
	Muxed Pins	14	14	14	14	14	14
	Dedicated Pins (Non TAP)	7	7	7	7	7	7
Non Configuration	Muxed Pins	34	54	33	40	54	57
	Dedicated Pins	3	3	3	3	3	3
VCC		10	7	10	14	7	16
VCCAUX		4	4	4	8	4	16
VCCPLL		0	0	0	0	0	0
VCCIO	Bank0	1	2	1	2	2	4
	Bank1	1	2	1	2	2	4
	Bank2	1	2	1	2	2	4
	Bank3	1	2	1	2	2	4
	Bank4	1	2	1	2	2	4
	Bank5	1	2	1	2	2	4
	Bank6	1	2	1	2	2	4
	Bank7	1	2	1	2	2	4
	Bank8	1	1	1	2	1	2
GND, GND0 to GND7		12	20	12	22	20	60
NC		4	3	1	0	0	44
Single Ended/ Differential I/O Pairs per Bank (including emulated with resistors)	Bank0	8/4	18/6	8/4	18/9	18/9	50/25
	Bank1	17/8	34/17	18/9	18/9	34/17	46/23
	Bank2	4/2	20/10	4/2	11/5	20/10	24/12
	Bank3	8/4	12/6	8/4	11/5	12/6	16/8
	Bank4	18/9	32/16	18/9	19/9	32/16	46/23
	Bank5	8/4	14/7	10/5	18/9	17/8	46/23
	Bank6	9/4	26/13	9/4	18/8	26/13	32/16
	Bank7	12/6	20/10	12/6	12/6	20/10	23/11
	Bank8	6/2	14/7	6/2	6/2	14/7	14/7
True LVDS I/O Pairs per Bank	Bank0 (Top Edge)	0	0	0	0	0	0
	Bank1 (Top Edge)	0	0	0	0	0	0
	Bank2 (Right Edge)	1	5	1	4	5	6
	Bank3 (Right Edge)	3	3	3	3	3	4
	Bank4 (Bottom Edge)	0	0	0	0	0	0
	Bank5 (Bottom Edge)	0	0	0	0	0	0
	Bank6 (Left Edge)	2	7	2	6	7	8
	Bank7 (Left Edge)	5	5	5	5	5	5
	Bank8 (Right Edge)	0	0	0	0	0	0

LatticeECP2M Pin Information Summary, LFE2M20 and LFE2M35

Pin Type		LFE2M20		LFE2M35		
		256 fpBGA	484 fpBGA	256 fpBGA	484 fpBGA	672 fpBGA
Single Ended User I/O		140	304	140	303	410
Differential Pair User I/O		70	152	70	151	199
Configuration	TAP Pins	5	5	5	5	5
	Muxed Pins	14	14	14	14	14
	Dedicated Pins (Non TAP)	7	7	7	7	7
Non Configuration	Muxed Pins	64	84	60	84	89
	Dedicated Pins	3	3	3	3	3
VCC		6	16	6	16	29
VCCAUX		4	8	4	8	17
VCCPLL		1	4	1	4	8
VCCIO	Bank0	1	4	1	4	5
	Bank1	1	3	1	3	4
	Bank2	2	4	2	4	5
	Bank3	2	4	2	4	5
	Bank4	2	4	2	4	4
	Bank5	2	4	2	4	5
	Bank6	2	4	2	4	5
	Bank7	2	4	2	4	5
	Bank8	1	2	1	2	2
GND, GND0 to GND7		22	57	22	57	80
NC		17	11	17	12	37
Single Ended/ Differential I/O Pairs per Bank (including emulated with resistors)	Bank0	0/0	36/18	0/0	36/18	63/31
	Bank1	0/0	18/9	0/0	18/9	18/9
	Bank2	14/7	30/15	14/7	30/15	50/25
	Bank3	16/8	36/18	16/8	36/18	43/21
	Bank4	32/16	62/31	32/16	62/31	50/21
	Bank5	20/10	28/14	20/10	28/14	60/30
	Bank6	16/8	40/20	16/8	39/19	52/25
	Bank7	28/14	40/20	28/14	40/20	60/30
	Bank8	14/7	14/7	14/7	14/7	14/7
True LVDS I/O Pairs per Bank	Bank0 (Top Edge)	0	0	0	0	0
	Bank1 (Top Edge)	0	0	0	0	0
	Bank2 (Right Edge)	3	7	3	7	12
	Bank3 (Right Edge)	4	9	4	9	11
	Bank4 (Bottom Edge)	0	0	0	0	0
	Bank5 (Bottom Edge)	0	0	0	0	0
	Bank6 (Left Edge)	4	10	4	10	14
	Bank7 (Left Edge)	7	10	7	10	15
	Bank8 (Right Edge)	0	0	0	0	0

LatticeECP2M Pin Information Summary, LFE2M50, LFE2M70 and LFE2M100

Pin Type		LFE2M50			LFE2M70		LFE2M100	
		484 fpBGA	672 fpBGA	900 fpBGA	900 fpBGA	1152 fpBGA	900 fpBGA	1152 fpBGA
Single Ended User I/O		270	372	410	416	436	416	520
Differential Pair User I/O		135	185	205	208	218	207	260
Configuration	TAP Pins	5	5	5	5	5	5	5
	Muxed Pins	14	14	14	14	14	14	14
	Dedicated Pins (Non TAP)	7	7	7	7	7	7	7
Non Configuration	Muxed Pins	69	72	72	75	76	74	78
	Dedicated Pins	3	3	3	3	3	3	3
VCC		16	20	62	44	44	44	44
VCCAUX		8	26	18	16	12	16	12
VCCPLL		4	8	4	4	4	4	4
VCCIO	Bank0	4	5	6	6	7	6	7
	Bank1	3	4	6	6	7	6	7
	Bank2	4	5	9	9	9	9	9
	Bank3	4	5	9	9	9	9	9
	Bank4	4	4	6	6	7	6	7
	Bank5	4	5	6	6	7	6	7
	Bank6	4	5	9	9	9	9	9
	Bank7	4	5	9	9	9	9	9
	Bank8	2	2	2	2	2	2	2
GND, GND0 to GND7		57	80	122	122	134	122	134
NC		31	35	121	63	283	63	199
Single Ended/ Differential I/O Pairs per Bank (including emulated with resistors)	Bank0	36/18	63/31	56/28	34/17	46/23	34/17	54/27
	Bank1	18/9	18/9	36/18	42/21	34/17	42/21	44/22
	Bank2	30/15	50/25	54/27	70/35	72/36	70/35	80/40
	Bank3	36/18	43/21	44/22	60/30	64/32	60/30	80/40
	Bank4	42/21	24/12	38/19	38/19	40/20	38/19	44/22
	Bank5	28/14	60/30	58/29	40/20	40/20	40/20	46/23
	Bank6	40/20	54/27	60/30	62/31	66/33	62/31	82/41
	Bank7	40/20	60/30	64/32	70/35	74/37	70/35	90/45
	Bank8	0/0	0/0	0/0	0/0	0/0	0/0	0/0
True LVDS I/O Pairs per Bank	Bank0 (Top Edge)	0	0	0	0	0	0	0
	Bank1 (Top Edge)	0	0	0	0	0	0	0
	Bank2 (Right Edge)	7	12	13	17	18	17	20
	Bank3 (Right Edge)	9	11	11	15	16	15	20
	Bank4 (Bottom Edge)	0	0	0	0	0	0	0
	Bank5 (Bottom Edge)	0	0	0	0	0	0	0
	Bank6 (Left Edge)	10	14	15	15	16	15	20
	Bank7 (Left Edge)	10	15	17	17	18	17	22
	Bank8 (Right Edge)	0	0	0	0	0	0	0

LFE2-6E/SE and LFE2-12E/SE Logic Signal Connections: 144 TQFP

LFE2-6E/SE					LFE2-12E/12SE				
Pin Number	Pin/Pad Function	Bank	Dual Function	Differential	Pin/Pad Function	Bank	Dual Function	Differential	
1	PL2A	7	VREF2_7	T (LVDS)*	PL2A	7	VREF2_7	T (LVDS)*	
2	PL2B	7	VREF1_7	C (LVDS)*	PL2B	7	VREF1_7	C (LVDS)*	
3	PL4A	7		T (LVDS)*	PL4A	7		T (LVDS)*	
4	PL4B	7		C (LVDS)*	PL4B	7		C (LVDS)*	
5	PL6A	7	LDQ10	T (LVDS)*	PL6A	7	LDQ10	T (LVDS)*	
6	VCCAUX	-			VCCAUX	-			
7	PL6B	7	LDQ10	C (LVDS)*	PL6B	7	LDQ10	C (LVDS)*	
8	PL8A	7	LDQ10	T (LVDS)*	PL8A	7	LDQ10	T (LVDS)*	
9	VCCIO7	7			VCCIO7	7			
10	PL8B	7	LDQ10	C (LVDS)*	PL8B	7	LDQ10	C (LVDS)*	
11	GND	-			GND	-			
12	PL12A	7	LDQ10	T (LVDS)*	PL12A	7	LDQ10	T (LVDS)*	
13	PL12B	7	LDQ10	C (LVDS)*	PL12B	7	LDQ10	C (LVDS)*	
14	PL13A	7	PCLKT7_0/LDQ10	T	PL13A	7	PCLKT7_0/LDQ10	T	
15	PL13B	7	PCLKC7_0/LDQ10	C	PL13B	7	PCLKC7_0/LDQ10	C	
16	VCC	-			VCC	-			
17	PL15A	6	PCLKT6_0	T (LVDS)*	PL15A	6	PCLKT6_0	T (LVDS)*	
18	PL15B	6	PCLKC6_0	C (LVDS)*	PL15B	6	PCLKC6_0	C (LVDS)*	
19	PL16A	6	VREF2_6	T	PL16A	6	VREF2_6	T	
20	PL16B	6	VREF1_6	C	PL16B	6	VREF1_6	C	
21	GND	-			GND	-			
22	VCC	-			VCC	-			
23	PL18A	6	LLM0_GDLLT_FB_A	T	PL18A	6	LLM0_GDLLT_FB_A	T	
24	PL18B	6	LLM0_GDLLC_FB_A	C	PL18B	6	LLM0_GDLLC_FB_A	C	
25	LLM0_PLLCAP	6			LLM0_PLLCAP	6			
26	PL20A	6	LLM0_GPLLT_IN_A**	T (LVDS)*	PL20A	6	LLM0_GPLLT_IN_A**	T (LVDS)*	
27	PL20B	6	LLM0_GPLLC_IN_A**	C (LVDS)*	PL20B	6	LLM0_GPLLC_IN_A**	C (LVDS)*	
28	PL22A	6			PL22A	6			
29	VCC	-			VCC	-			
30	GND	-			GND	-			
31	VCCIO6	6			VCCIO6	6			
32	TCK	-			TCK	-			
33	TDI	-			TDI	-			
34	TDO	-			TDO	-			
35	VCCJ	-			VCCJ	-			
36	TMS	-			TMS	-			
37	PB2A	5	VREF2_5/BDQ6	T	PB2A	5	VREF2_5/BDQ6	T	
38	PB2B	5	VREF1_5/BDQ6	C	PB2B	5	VREF1_5/BDQ6	C	
39	VCCAUX	-			VCCAUX	-			
40	PB4A	5	BDQ6	T	PB6A	5	BDQS6	T	
41	PB4B	5	BDQ6	C	PB6B	5	BDQ6	C	
42	VCCIO5	5			VCCIO5	5			
43	PB6A	5	BDQS6	T	PB12A	5	BDQ15	T	
44	PB6B	5	BDQ6	C	PB12B	5	BDQ15	C	
45	NC	5			PB16A	5	BDQ15	T	

LFE2-6E/SE and LFE2-12E/SE Logic Signal Connections: 144 TQFP (Cont.)

LFE2-6E/SE					LFE2-12E/12SE				
Pin Number	Pin/Pad Function	Bank	Dual Function	Differential	Pin/Pad Function	Bank	Dual Function	Differential	
91	PR20B	3	RLM0_GPLL_C_IN_A**	C (LVDS)*	PR20B	3	RLM0_GPLL_C_IN_A**	C (LVDS)*	
92	PR20A	3	RLM0_GPLL_T_IN_A**	T (LVDS)*	PR20A	3	RLM0_GPLL_T_IN_A**	T (LVDS)*	
93	RLM0_PLLCAP	3			RLM0_PLLCAP	3			
94	VCC	-			VCC	-			
95	GND	-			GND	-			
96	PR17B	3	RLM0_GDLL_C_IN_A**	C (LVDS)*	PR17B	3	RLM0_GDLL_C_IN_A**	C (LVDS)*	
97	PR17A	3	RLM0_GDLL_T_IN_A**	T (LVDS)*	PR17A	3	RLM0_GDLL_T_IN_A**	T (LVDS)*	
98	PR16B	3	VREF2_3	C	PR16B	3	VREF2_3	C	
99	PR16A	3	VREF1_3	T	PR16A	3	VREF1_3	T	
100	PR15B	3	PCLKC3_0	C (LVDS)*	PR15B	3	PCLKC3_0	C (LVDS)*	
101	PR15A	3	PCLKT3_0	T (LVDS)*	PR15A	3	PCLKT3_0	T (LVDS)*	
102	VCC	-			VCC	-			
103	PR13B	2	PCLKC2_0/RDQ10	C	PR13B	2	PCLKC2_0/RDQ10	C	
104	PR13A	2	PCLKT2_0/RDQ10	T	PR13A	2	PCLKT2_0/RDQ10	T	
105	GND	-			GND	-			
106	VCCIO2	2			VCCIO2	2			
107	PR2B	2	VREF2_2	C (LVDS)*	PR2B	2	VREF2_2	C (LVDS)*	
108	PR2A	2	VREF1_2	T (LVDS)*	PR2A	2	VREF1_2	T (LVDS)*	
109	PT28B	1	VREF2_1	C	PT55B	1	VREF2_1	C	
110	PT28A	1	VREF1_1	T	PT55A	1	VREF1_1	T	
111	PT26B	1		C	PT54B	1		C	
112	PT26A	1		T	PT54A	1		T	
113	PT24B	1		C	PT52B	1		C	
114	PT24A	1		T	PT52A	1		T	
115	PT22B	1		C	PT50B	1		C	
116	PT22A	1		T	PT50A	1		T	
117	VCCIO1	1			VCCIO1	1			
118	PT20B	1		C	PT48B	1		C	
119	PT20A	1		T	PT48A	1		T	
120	GND	-			GND	-			
121	PT18B	1		C	PT44B	1		C	
122	PT18A	1		T	PT44A	1		T	
123	PT16A	1			PT40B	1		C	
124	NC	1			PT40A	1		T	
125	PT14B	1		C	PT34B	1		C	
126	PT14A	1		T	PT34A	1		T	
127	NC	1			NC	1			
128	VCC	-			VCC	-			
129	PT12B	1	PCLKC1_0	C	PT30B	1	PCLKC1_0	C	
130	PT12A	1	PCLKT1_0	T	PT30A	1	PCLKT1_0	T	
131	PT10B	0	PCLKC0_0	C	PT28B	0	PCLKC0_0	C	
132	XRES	0			XRES	0			
133	GND	-			GND	-			
134	PT10A	0	PCLKT0_0	T	PT28A	0	PCLKT0_0	T	
135	VCC	-			VCC	-			

LFE2-35E/SE and LFE2-50E/SE Logic Signal Connections: 484 fpBGA (Cont.)

LFE2-35E/SE					LFE2-50E/SE			
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential
K1	PL23B	7	LDQ22	C	PL42B	7	LDQ41	C
L4	PL24A	7	LDQ22	T (LVDS)*	PL43A	7	LDQ41	T (LVDS)*
L3	PL24B	7	LDQ22	C (LVDS)*	PL43B	7	LDQ41	C (LVDS)*
L2	PL25A	7	PCLKT7_0/LDQ22	T	PL44A	7	PCLKT7_0/LDQ41	T
GNDIO	GNDIO7	-			GNDIO7	-		
L1	PL25B	7	PCLKC7_0/LDQ22	C	PL44B	7	PCLKC7_0/LDQ41	C
M5	PL27A	6	PCLKT6_0/LDQ31	T (LVDS)*	PL46A	6	PCLKT6_0/LDQ50	T (LVDS)*
M6	PL27B	6	PCLKC6_0/LDQ31	C (LVDS)*	PL46B	6	PCLKC6_0/LDQ50	C (LVDS)*
M3	PL28A	6	VREF2_6/LDQ31	T	PL47A	6	VREF2_6/LDQ50	T
M4	PL28B	6	VREF1_6/LDQ31	C	PL47B	6	VREF1_6/LDQ50	C
M2	PL29A	6	LDQ31	T (LVDS)*	PL48A	6	LDQ50	T (LVDS)*
VCCIO	VCCIO6	6			VCCIO	6		
M1	PL29B	6	LDQ31	C (LVDS)*	PL48B	6	LDQ50	C (LVDS)*
N1	PL30A	6	LDQ31	T	PL49A	6	LDQ50	T
N2	PL30B	6	LDQ31	C	PL49B	6	LDQ50	C
GNDIO	GNDIO6	-			GNDIO6	-		
VCCIO	VCCIO6	6			VCCIO	6		
N3	PL39A	6	LDQS39***	T (LVDS)*	PL58A	6	LDQS58***	T (LVDS)*
N4	PL39B	6	LDQ39	C (LVDS)*	PL58B	6	LDQ58	C (LVDS)*
N5	PL40A	6	LDQ39	T	PL59A	6	LDQ58	T
VCCIO	VCCIO6	6			VCCIO	6		
P5	PL40B	6	LDQ39	C	PL59B	6	LDQ58	C
P1	PL41A	6	LLM0_GDLLT_IN_A**/LDQ39	T (LVDS)*	PL60A	6	LLM0_GDLLT_IN_A**/LDQ58	T (LVDS)*
P2	PL41B	6	LLM0_GDLLC_IN_A**/LDQ39	C (LVDS)*	PL60B	6	LLM0_GDLLC_IN_A**/LDQ58	C (LVDS)*
P4	PL42A	6	LLM0_GDLLT_FB_A/LDQ39	T	PL61A	6	LLM0_GDLLT_FB_A/LDQ58	T
GNDIO	GNDIO6	-			GNDIO6	-		
R4	PL42B	6	LLM0_GDLLC_FB_A/LDQ39	C	PL61B	6	LLM0_GDLLC_FB_D/LDQ58	C
P6	LLM0_PLLCAP	6			LLM0_PLLCAP	6		
R1	PL44A	6	LLM0_GPLLT_IN_A**/LDQ48	T (LVDS)*	PL63A	6	LLM0_GPLLT_IN_A**/LDQ67	T (LVDS)*
R2	PL44B	6	LLM0_GPLLC_IN_A**/LDQ48	C (LVDS)*	PL63B	6	LLM0_GPLLC_IN_A**/LDQ67	C (LVDS)*
R3	PL45A	6	LLM0_GPLLT_FB_A/LDQ48	T	PL64A	6	LLM0_GPLLT_FB_A/LDQ67	T
T4	PL45B	6	LLM0_GPLLC_FB_A/LDQ48	C	PL64B	6	LLM0_GPLLC_FB_A/LDQ67	C
T1	PL46A	6	LDQ48	T (LVDS)*	PL65A	6	LDQ67	T (LVDS)*
VCCIO	VCCIO6	6			VCCIO	6		
T2	PL46B	6	LDQ48	C (LVDS)*	PL65B	6	LDQ67	C (LVDS)*
T5	PL47A	6	LDQ48	T	PL66A	6	LDQ67	T
T3	PL47B	6	LDQ48	C	PL66B	6	LDQ67	C
GNDIO	GNDIO6	-			VCCIO	6		
VCCIO	VCCIO6	-			GNDIO6	-		
U1	PL52A	6	LDQ56	T (LVDS)*	PL71A	6	LDQ75	T (LVDS)*
U2	PL52B	6	LDQ56	C (LVDS)*	PL71B	6	LDQ75	C (LVDS)*
V1	PL53A	6	LDQ56	T	PL72A	6	LDQ75	T
V2	PL53B	6	LDQ56	C	PL72B	6	LDQ75	C
VCCIO	VCCIO6	6			VCCIO	6		
R6	PL54A	6	LDQ56	T (LVDS)*	PL73A	6	LDQ75	T (LVDS)*
T6	PL54B	6	LDQ56	C (LVDS)*	PL73B	6	LDQ75	C (LVDS)*

LFE2-35E/SE and LFE2-50E/SE Logic Signal Connections: 484 fpBGA (Cont.)

LFE2-35E/SE					LFE2-50E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential	Ball/Pad Function	Bank	Dual Function	Differential	
W13	PB46A	4	BDQ42	T	PB55A	4	BDQ51	T	
GNDIO	GNDIO4	-			GNDIO4	-			
W14	PB46B	4	BDQ42	C	PB55B	4	BDQ51	C	
AB18	PB48A	4	BDQ51	T	PB57A	4	BDQ60	T	
AB19	PB48B	4	BDQ51	C	PB57B	4	BDQ60	C	
V14	PB49A	4	BDQ51	T	PB58A	4	BDQ60	T	
W15	PB49B	4	BDQ51	C	PB58B	4	BDQ60	C	
VCCIO	VCCIO4	4			VCCIO	4			
Y15	PB50A	4	BDQ51	T	PB59A	4	BDQ60	T	
AA15	PB50B	4	BDQ51	C	PB59B	4	BDQ60	C	
GNDIO	GNDIO4	-			GNDIO4	-			
AA16	PB51A	4	BDQS51	T	PB60A	4	BDQS60	T	
AA17	PB51B	4	BDQ51	C	PB60B	4	BDQ60	C	
AB20	PB52A	4	BDQ51	T	PB61A	4	BDQ60	T	
AB21	PB52B	4	BDQ51	C	PB61B	4	BDQ60	C	
U15	PB53A	4	BDQ51	T	PB62A	4	BDQ60	T	
U16	PB53B	4	BDQ51	C	PB62B	4	BDQ60	C	
VCCIO	VCCIO4	4			VCCIO	4			
Y16	PB54A	4	BDQ51	T	PB63A	4	BDQ60	T	
W16	PB54B	4	BDQ51	C	PB63B	4	BDQ60	C	
AA18	PB55A	4	BDQ51	T	PB64A	4	BDQ60	T	
AA20	PB55B	4	BDQ51	C	PB64B	4	BDQ60	C	
GNDIO	GNDIO4	-			GNDIO4	-			
VCCIO	VCCIO4	4			VCCIO	4			
AA21	PB66A	4	BDQ69	T	PB75A	4	BDQ78	T	
AA22	PB66B	4	BDQ69	C	PB75B	4	BDQ78	C	
V16	PB67A	4	BDQ69	T	PB76A	4	BDQ78	T	
V17	PB67B	4	BDQ69	C	PB76B	4	BDQ78	C	
VCCIO	VCCIO4	4			VCCIO	4			
Y18	PB68A	4	BDQ69	T	PB77A	4	BDQ78	T	
Y17	PB68B	4	BDQ69	C	PB77B	4	BDQ78	C	
GNDIO	GNDIO4	-			GNDIO4	-			
Y19	PB69A	4	BDQS69	T	PB78A	4	BDQS78	T	
Y20	PB69B	4	BDQ69	C	PB78B	4	BDQ78	C	
W17	PB70A	4	BDQ69	T	PB79A	4	BDQ78	T	
W18	PB70B	4	BDQ69	C	PB79B	4	BDQ78	C	
Y21	PB71A	4	BDQ69	T	PB80A	4	BDQ78	T	
Y22	PB71B	4	BDQ69	C	PB80B	4	BDQ78	C	
VCCIO	VCCIO4	4			VCCIO	4			
U18	PB72A	4	BDQ69	T	PB81A	4	BDQ78	T	
V18	PB72B	4	BDQ69	C	PB81B	4	BDQ78	C	
T15	PB73A	4	VREF2_4/BDQ69	T	PB82A	4	VREF2_4/BDQ78	T	
T16	PB73B	4	VREF1_4/BDQ69	C	PB82B	4	VREF1_4/BDQ78	C	
GNDIO	GNDIO4	-			GNDIO4	-			
W19	CFG2	8			CFG2	8			
V19	CFG1	8			CFG1	8			

LFE2-70E/SE Logic Signal Connections: 900 fpBGA (Cont.)

LFE2-70E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential
P3	PL54B	7	LDQ54	C (LVDS)*
R6	PL55A	7	LDQ54	T
VCCIO	VCCIO7	7		
R8	PL55B	7	LDQ54	C
P2	PL56A	7	LDQ54	T (LVDS)*
P1	PL56B	7	LDQ54	C (LVDS)*
R5	PL57A	7	PCLKT7_0/LDQ54	T
GND	GNDIO7	-		
R7	PL57B	7	PCLKC7_0/LDQ54	C
R4	PL59A	6	PCLKT6_0/LDQ63	T (LVDS)*
R3	PL59B	6	PCLKC6_0/LDQ63	C (LVDS)*
T5	PL60A	6	VREF2_6/LDQ63	T
T7	PL60B	6	VREF1_6/LDQ63	C
T3	PL61A	6	LDQ63	T (LVDS)*
VCCIO	VCCIO6	6		
T4	PL61B	6	LDQ63	C (LVDS)*
T6	PL62A	6	LDQ63	T
T8	PL62B	6	LDQ63	C
T2	PL63A	6	LDQS63	T (LVDS)*
GND	GNDIO6	-		
T1	PL63B	6	LDQ63	C (LVDS)*
U7	PL64A	6	LDQ63	T
U5	PL64B	6	LDQ63	C
VCCIO	VCCIO6	6		
U4	PL65A	6	LDQ63	T (LVDS)*
U3	PL65B	6	LDQ63	C (LVDS)*
U8	PL66A	6	LDQ63	T
U6	PL66B	6	LDQ63	C
GND	GNDIO6	-		
U2	PL67A	6	LDQ71	T (LVDS)*
U1	PL67B	6	LDQ71	C (LVDS)*
V7	PL68A	6	LDQ71	T
V5	PL68B	6	LDQ71	C
VCCIO	VCCIO6	6		
V2	PL69A	6	LDQ71	T (LVDS)*
V1	PL69B	6	LDQ71	C (LVDS)*
V8	PL70A	6	LDQ71	T
V6	PL70B	6	LDQ71	C
GND	GNDIO6	-		
W1	PL71A	6	LDQS71	T (LVDS)*
W2	PL71B	6	LDQ71	C (LVDS)*
W5	PL72A	6	LDQ71	T
VCCIO	VCCIO6	6		

LFE2-70E/SE Logic Signal Connections: 900 fpBGA (Cont.)

LFE2-70E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential
AH12	PB45A	5	BDQ42	T
AF14	PB45B	5	BDQ42	C
AJ13	PB46A	5	BDQ42	T
GND	GNDIO5	-		
AK13	PB46B	5	BDQ42	C
AB15	PB47A	5	BDQ51	T
AD15	PB47B	5	BDQ51	C
AE15	PB48A	5	BDQ51	T
AF15	PB48B	5	BDQ51	C
AG15	PB49A	5	BDQ51	T
AG14	PB49B	5	BDQ51	C
VCCIO	VCCIO5	5		
AH15	PB50A	5	BDQ51	T
AH14	PB50B	5	BDQ51	C
GND	GNDIO5	-		
AJ14	PB51A	5	BDQS51	T
AK14	PB51B	5	BDQ51	C
AD16	PB52A	5	BDQ51	T
AF16	PB52B	5	BDQ51	C
AJ15	PB53A	5	PCLKT5_0/BDQ51	T
AK15	PB53B	5	PCLKC5_0/BDQ51	C
VCCIO	VCCIO5	5		
GND	GNDIO5	-		
AE16	PB58A	4	PCLKT4_0/BDQ60	T
VCCIO	VCCIO4	4		
AC15	PB58B	4	PCLKC4_0/BDQ60	C
AJ16	PB59A	4	BDQ60	T
AK16	PB59B	4	BDQ60	C
AC16	PB60A	4	BDQS60	T
GND	GNDIO4	-		
AB16	PB60B	4	BDQ60	C
AH17	PB61A	4	BDQ60	T
AG17	PB61B	4	BDQ60	C
AF17	PB62A	4	BDQ60	T
VCCIO	VCCIO4	4		
AD17	PB62B	4	BDQ60	C
AE17	PB63A	4	BDQ60	T
AC17	PB63B	4	BDQ60	C
AJ17	PB64A	4	BDQ60	T
GND	GNDIO4	-		
AK17	PB64B	4	BDQ60	C
AK18	PB65A	4	BDQ69	T
AJ18	PB65B	4	BDQ69	C

LFE2-70E/SE Logic Signal Connections: 900 fpBGA (Cont.)

LFE2-70E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential
D25	PT99A	1		T
J22	PT98B	1		C
J21	PT98A	1		T
VCCIO	VCCIO1	1		
B25	PT97B	1		C
A25	PT97A	1		T
E24	PT96B	1		C
F24	PT96A	1		T
GND	GNDIO1	-		
F23	PT95B	1		C
H22	PT95A	1		T
D24	PT94B	1		C
C24	PT94A	1		T
VCCIO	VCCIO1	1		
E23	PT93B	1		C
G23	PT93A	1		T
B24	PT92B	1		C
A24	PT92A	1		T
C27	PT91B	1		C
GND	GNDIO1	-		
D27	PT91A	1		T
C26	PT90B	1		C
D26	PT90A	1		T
A27	PT89B	1		C
VCCIO	VCCIO1	1		
B27	PT89A	1		T
A28	PT88B	1		C
B28	PT88A	1		T
A29	PT87B	1		C
B29	PT87A	1		T
GND	GNDIO1	-		
VCCIO	VCCIO1	1		
H21	PT80B	1		C
F22	PT80A	1		T
VCCIO	VCCIO1	1		
B23	PT79B	1		C
A23	PT79A	1		T
G24	PT78B	1		C
E22	PT78A	1		T
GND	GNDIO1	-		
D22	PT77B	1		C
C22	PT77A	1		T
G22	PT76B	1		C

LFE2M50E/SE Logic Signal Connections: 484 fpBGA (Cont.)

LFE2M50E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential
Y6	PB8A	5	BDQ6	T
Y5	PB8B	5	BDQ6	C
VCCIO	VCCIO5	5		
AB3	PB9A	5	BDQ6	T
AB4	PB9B	5	BDQ6	C
AB5	PB10A	5	BDQ6	T
AA6	PB10B	5	BDQ6	C
GNDIO	GNDIO5	-		
VCCIO	VCCIO5	5		
V9	PB40A	5	BDQ42	T
U9	PB40B	5	BDQ42	C
VCCIO	VCCIO5	5		
U10	PB41A	5	BDQ42	T
T10	PB41B	5	BDQ42	C
GNDIO	GNDIO5	-		
W9	PB42A	5	BDQS42****	T
Y8	PB42B	5	BDQ42	C
AA7	PB43A	5	VREF2_5/BDQ42	T
Y7	PB43B	5	VREF1_5/BDQ42	C
AB6	PB44A	5	PCLKT5_0/BDQ42	T
AB7	PB44B	5	PCLKC5_0/BDQ42	C
VCCIO	VCCIO5	5		
GNDIO	GNDIO5	-		
AA8	PB49A	4	PCLKT4_0/BDQ51	T
VCCIO	VCCIO4	4		
AB8	PB49B	4	PCLKC4_0/BDQ51	C
AA9	PB50A	4	VREF2_4/BDQ51	T
Y9	PB50B	4	VREF1_4/BDQ51	C
AB9	PB51A	4	BDQS51****	T
GNDIO	GNDIO4	-		
AB10	PB51B	4	BDQ51	C
AA10	PB52A	4	BDQ51	T
Y11	PB52B	4	BDQ51	C
VCCIO	VCCIO4	4		
GNDIO	GNDIO4	-		
V10	PB56A	4	BDQ60	T
U11	PB56B	4	BDQ60	C
V11	PB57A	4	BDQ60	T
W11	PB57B	4	BDQ60	C
AA11	PB58A	4	BDQ60	T
AB11	PB58B	4	BDQ60	C
VCCIO	VCCIO4	4		
T11	PB59A	4	BDQ60	T

LFE2M100E/SE Logic Signal Connections: 900 fpBGA (Cont.)

LFE2M100E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential
VCCIO	VCCIO3	3		
T22	PR69A	3	RDQ72	T
T29	PR68B	3	RDQ72	C (LVDS)*
T28	PR68A	3	RDQ72	T (LVDS)*
R23	PR66B	3	RLM4_SPLLC_FB_A/RDQ63	C
GNDIO	GNDIO3	-		
-	-	-		
R22	PR66A	3	RLM4_SPLLT_FB_A/RDQ63	T
P30	PR65B	3	RLM4_SPLLC_IN_A/RDQ63	C (LVDS)*
R29	PR65A	3	RLM4_SPLLT_IN_A/RDQ63	T (LVDS)*
T27	PR64B	3	RDQ63	C
VCCIO	VCCIO3	3		
T26	PR64A	3	RDQ63	T
GNDIO	GNDIO3	-		
N30	PR61B	3	RDQ63	C (LVDS)*
N29	PR61A	3	RDQ63	T (LVDS)*
VCCIO	VCCIO3	3		
R27	PR60B	3	VREF2_3/RDQ63	C
R28	PR60A	3	VREF1_3/RDQ63	T
P29	PR59B	3	PCLKC3_0/RDQ63	C (LVDS)*
P28	PR59A	3	PCLKT3_0/RDQ63	T (LVDS)*
M30	PR57B	2	PCLKC2_0/RDQ54	C
M29	PR57A	2	PCLKT2_0/RDQ54	T
GNDIO	GNDIO2	-		
P23	PR56B	2	RDQ54	C (LVDS)*
P24	PR56A	2	RDQ54	T (LVDS)*
R26	PR55B	2	RDQ54	C
P27	PR55A	2	RDQ54	T
VCCIO	VCCIO2	2		
P25	PR54B	2	RDQ54	C (LVDS)*
P26	PR54A	2	RDQS54	T (LVDS)*
K30	PR53B	2	RDQ54	C
GNDIO	GNDIO2	-		
K29	PR53A	2	RDQ54	T
N22	PR52B	2	RDQ54	C (LVDS)*
P22	PR52A	2	RDQ54	T (LVDS)*
J30	PR51B	2	RUM3_SPLLC_FB_A/RDQ54	C
VCCIO	VCCIO2	2		
J29	PR51A	2	RUM3_SPLLT_FB_A/RDQ54	T
N24	PR50B	2	RUM3_SPLLC_IN_A/RDQ54	C (LVDS)*
N23	PR50A	2	RUM3_SPLLT_IN_A/RDQ54	T (LVDS)*
N25	PR48B	2	RDQ45	C
N26	PR48A	2	RDQ45	T

LFE2M100E/SE Logic Signal Connections: 900 fpBGA (Cont.)

LFE2M100E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential
M19	VCC	-		
M20	VCC	-		
N11	VCC	-		
N12	VCC	-		
N19	VCC	-		
N20	VCC	-		
P12	VCC	-		
P19	VCC	-		
R12	VCC	-		
R19	VCC	-		
T12	VCC	-		
T19	VCC	-		
U12	VCC	-		
U19	VCC	-		
V11	VCC	-		
V12	VCC	-		
V19	VCC	-		
V20	VCC	-		
W11	VCC	-		
W12	VCC	-		
W13	VCC	-		
W14	VCC	-		
W15	VCC	-		
W16	VCC	-		
W17	VCC	-		
W18	VCC	-		
W19	VCC	-		
W20	VCC	-		
Y12	VCC	-		
Y13	VCC	-		
Y18	VCC	-		
Y19	VCC	-		
D14	VCCIO0	0		
E6	VCCIO0	0		
E9	VCCIO0	0		
F12	VCCIO0	0		
K12	VCCIO0	0		
K13	VCCIO0	0		
D17	VCCIO1	1		
E22	VCCIO1	1		
E25	VCCIO1	1		
F19	VCCIO1	1		
K18	VCCIO1	1		

LFE2M100E/SE Logic Signal Connections: 900 fpBGA (Cont.)

LFE2M100E/SE				
Ball Number	Ball/Pad Function	Bank	Dual Function	Differential
AE27	GND	-		
AE4	GND	-		
AE9	GND	-		
AF14	GND	-		
AF17	GND	-		
AF25	GND	-		
AF6	GND	-		
AJ10	GND	-		
AJ21	GND	-		
AJ27	GND	-		
AJ4	GND	-		
AK1	GND	-		
AK13	GND	-		
AK18	GND	-		
AK24	GND	-		
AK30	GND	-		
AK7	GND	-		
B10	GND	-		
B21	GND	-		
B27	GND	-		
B4	GND	-		
D25	GND	-		
D6	GND	-		
E14	GND	-		
E17	GND	-		
F22	GND	-		
F27	GND	-		
F4	GND	-		
F9	GND	-		
G12	GND	-		
G19	GND	-		
J24	GND	-		
J7	GND	-		
K14	GND	-		
K15	GND	-		
K16	GND	-		
K17	GND	-		
K27	GND	-		
K4	GND	-		
L14	GND	-		
L15	GND	-		
L16	GND	-		
L17	GND	-		