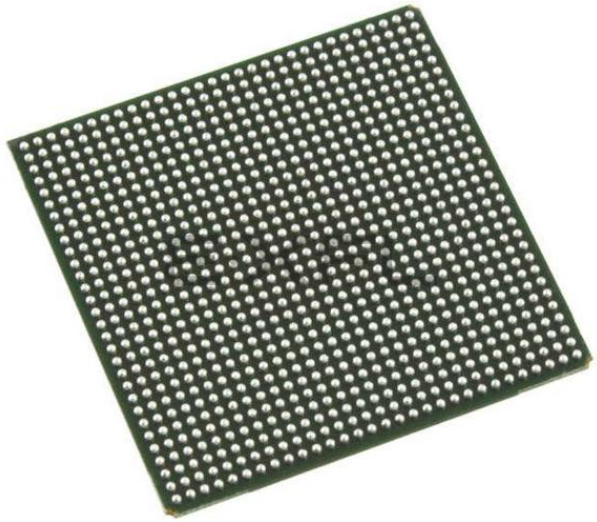
# Lattice Semiconductor Corporation - LFE2M70SE-7F900C Datasheet



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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

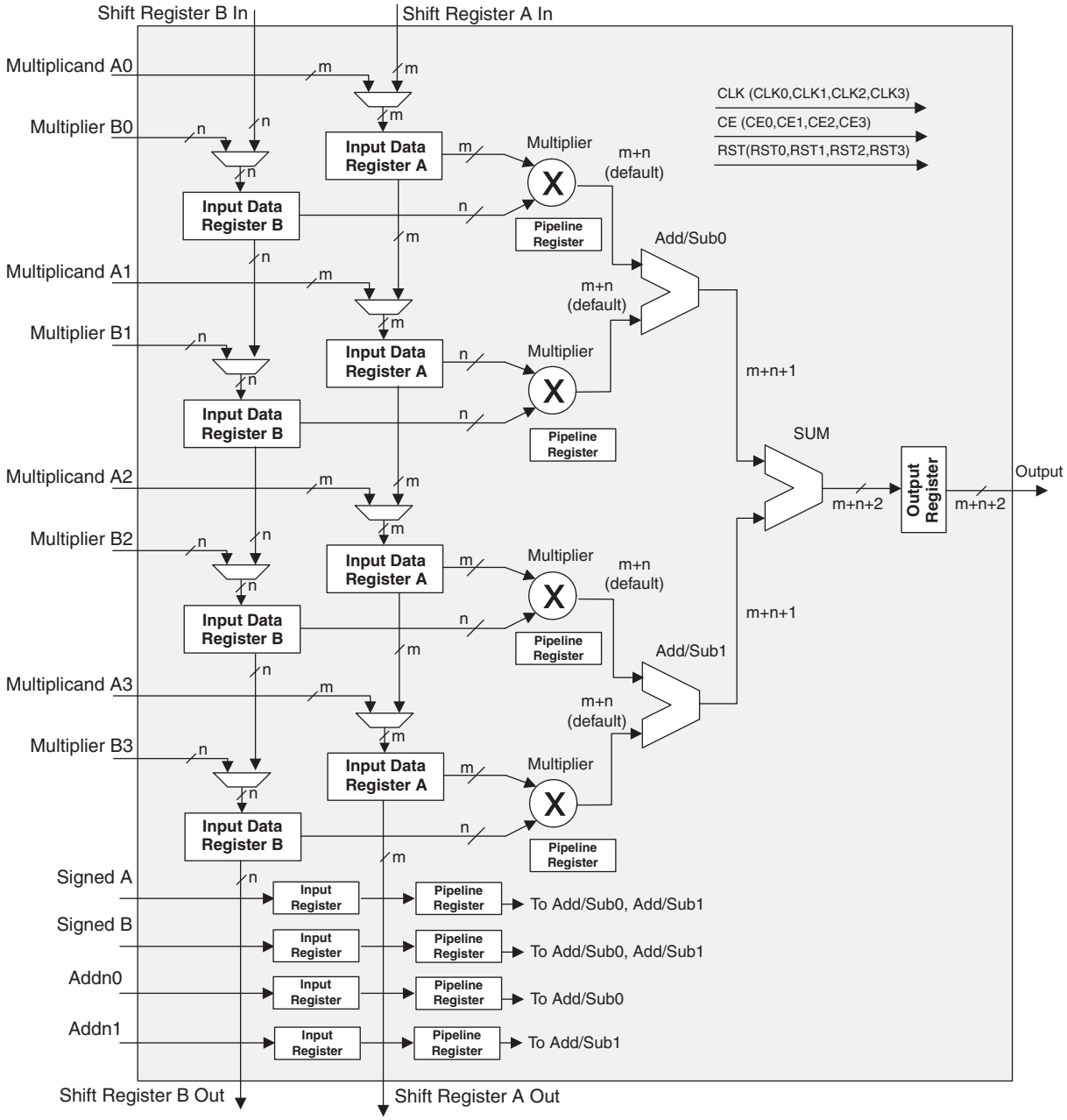
The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Obsolete |
| Number of LABs/CLBs | 8375 |
| Number of Logic Elements/Cells | 67000 |
| Total RAM Bits | 4642816 |
| Number of I/O | 416 |
| Number of Gates | - |
| Voltage - Supply | 1.14V ~ 1.26V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 85°C (TJ) |
| Package / Case | 900-BBGA |
| Supplier Device Package | 900-FPBGA (31x31) |
| Purchase URL | https://www.e-xfl.com/product-detail/lattice-semiconductor/lfe2m70se-7f900c |

## MULTADDSUBSUM sysDSP Element

In this case, the operands A0 and B0 are multiplied and the result is added/subtracted with the result of the multiplier operation of operands A1 and B1. Additionally the operands A2 and B2 are multiplied and the result is added/subtracted with the result of the multiplier operation of operands A3 and B3. The result of both addition/subtraction are added in a summation block. The user can enable the input, output and pipeline registers. Figure 2-26 shows the MULTADDSUBSUM sysDSP element.

***Figure 2-26. MULTADDSUBSUM***




## Clock, Clock Enable and Reset Resources

Global Clock, Clock Enable and Reset signals from routing are available to every DSP block. Four Clock, Reset and Clock Enable signals are selected for the sysDSP block. From four clock sources (CLK0, CLK1, CLK2, CLK3)

*Figure 3-7. DDR and DDR2 Parameters*

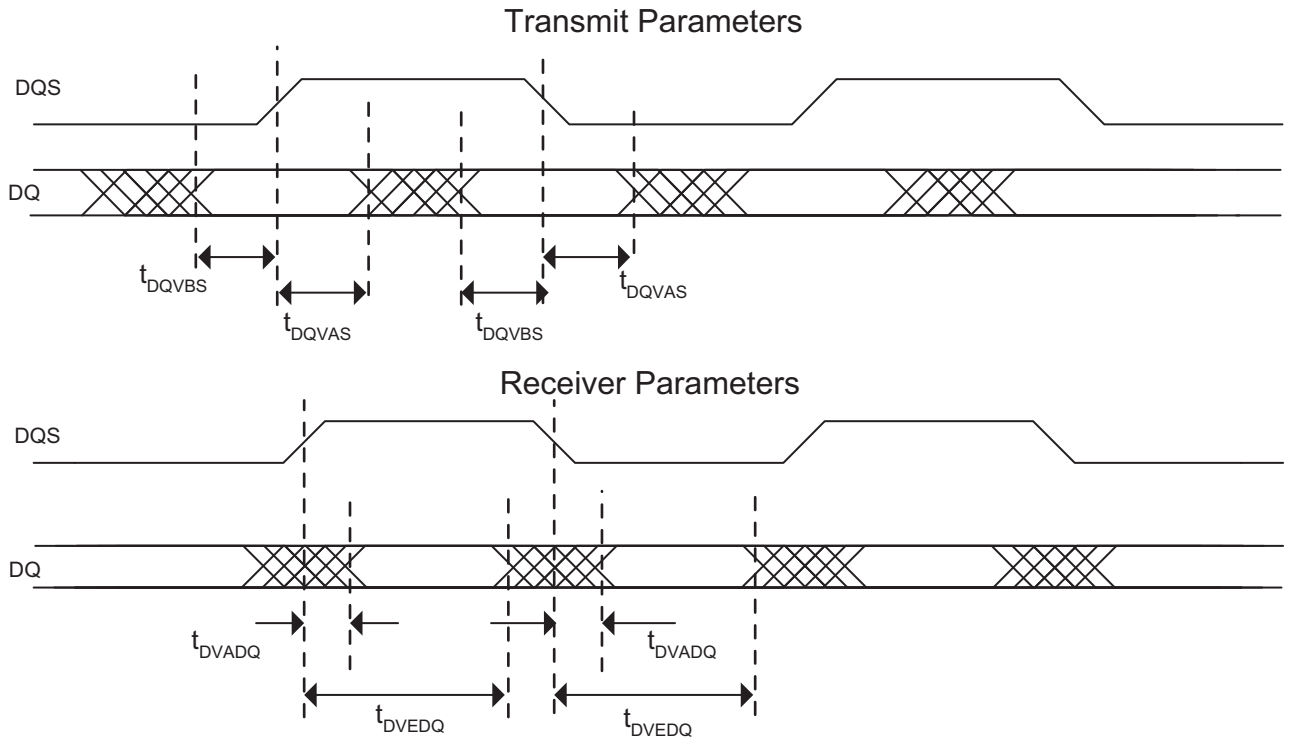
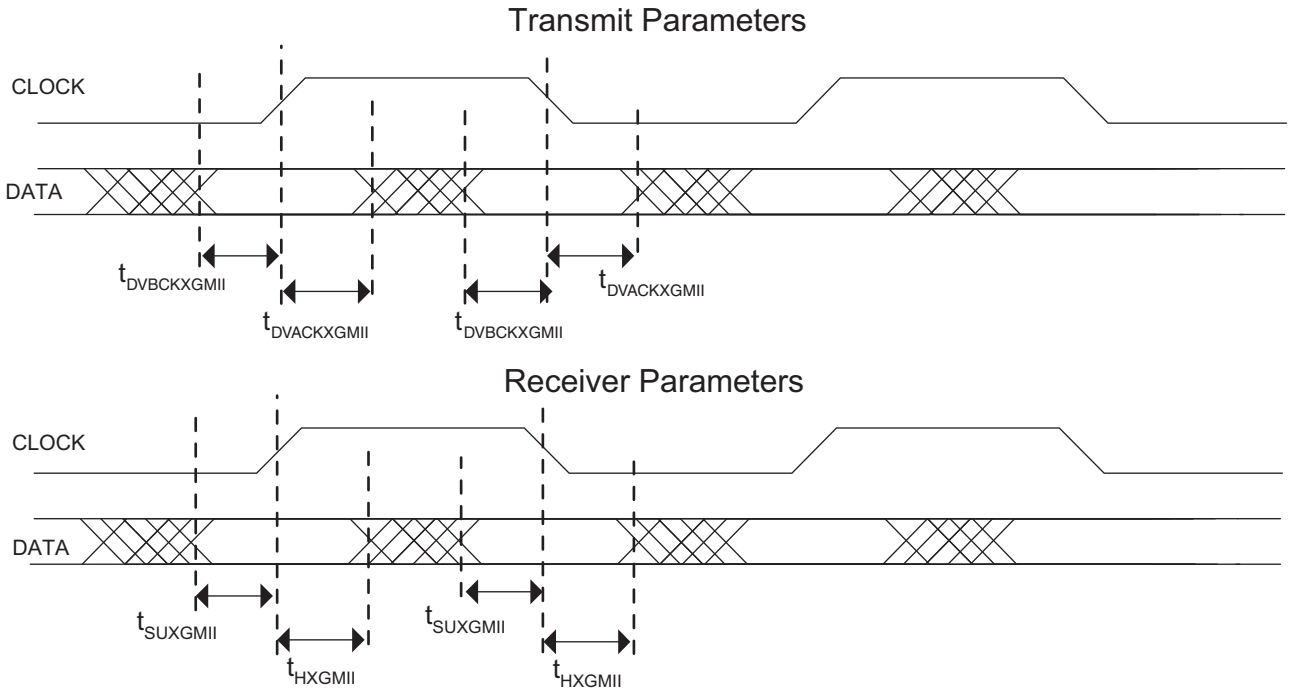



*Figure 3-8. XGMII Parameters*



# SERDES High Speed Data Receiver (LatticeECP2M Family Only)

***Table 3-11. Serial Input Data Specifications***

| Symbol | Description | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| $RX\text{-}CID_S$ | Stream of nontransitions[1] (CID = Consecutive Identical Digits) @ $10^{-12}$ BER | | 7 @ 3.125 Gbps<br>20 @ 1.25 Gbps | | Bits |
| $V_{RX\text{-}DIFF\text{-}S}$ | Differential input sensitivity | 100 | — | — | mV, p-p |
| $V_{RX\text{-}IN}$ | Input levels | 0 | — | $V_{CCRX}$ + 0.8 | V |
| $V_{RX\text{-}CM\text{-}DC}$ | Input common mode range (DC coupled) | 0.5 | — | 1.2 | V |
| $V_{RX\text{-}CM\text{-}AC}$ | Input common mode range (AC coupled)[3] | 0 | — | 1.5 | V |
| $T_{RX\text{-}RELOCK}$ | CDR re-lock time[2] | — | — | 3000 | Bits |
| $Z_{RX\text{-}TERM}$ | Input termination 50/75 Ohm/High Z | — | 50 | | Ohms |
| $RL_{RX\text{-}RL}$ | Return loss (without package) | — | 9 | — | dB |

1. This is the number of bits allowed without a transition on the incoming data stream when using DC coupling.
2. This is the typical number of bit times to re-lock to a new phase of frequency within +/- 300 ppm, assuming 8b10b encoded data and the CDR is in lock state. When CDR is in un-lock state, or reset is applied, the total re-lock settling time will be approximately 4ms including analog settle time, calibration time, and acquisition time.
3. AC coupling is used to interface to LVPECL and LVDS.

## Input Data Jitter Tolerance

A receiver's ability to tolerate incoming signal jitter is very dependent on jitter type. High speed serial interface standards have recognized the dependency on jitter type and have recently modified specifications to indicate tolerance levels for different jitter types as they relate to specific protocols (e.g. FC, etc.). Sinusoidal jitter is considered to be a worst case jitter type.

***Table 3-12. Receiver Total Jitter Tolerance Specification[1]***

| Description | Frequency | Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| Deterministic | 3.125 Gbps | 600 mV differential eye | — | — | 0.54 | UI, p-p |
| Random | | 600 mV differential eye | — | — | 0.26 | UI, p-p |
| Total | | 600 mV differential eye | — | — | 0.80 | UI, p-p |
| Deterministic | 2.5 Gbps | 600 mV differential eye | — | — | 0.61 | UI, p-p |
| Random | | 600 mV differential eye | — | — | 0.22 | UI, p-p |
| Total | | 600 mV differential eye | — | — | 0.81 | UI, p-p |
| Deterministic | 1.25 Gbps | 600 mV differential eye | — | — | 0.53 | UI, p-p |
| Random | | 600 mV differential eye | — | — | 0.22 | UI, p-p |
| Total | | 600 mV differential eye | — | — | 0.80 | UI, p-p |
| Deterministic | 250 Mbps[2] | 600 mV differential eye | — | — | 0.42 | UI, p-p |
| Random | | 600 mV differential eye | — | — | 0.10 | UI, p-p |
| Total | | 600 mV differential eye | — | — | 0.60 | UI, p-p |

1. Values are measured with PRBS $2^7$-1, all channels operating, FPGA Logic active, I/Os around SERDES pins quiet, voltages are nominal, room temperature.
2. Jitter specification is limited by measurement equipment capability.

# LFE2-12E/SE and LFE2-20E/SE Logic Signal Connections: 484 fpBGA (Cont.)

| LFE2-12E/12SE | | | | | LFE2-20E/20SE | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| AB7 | PB13B | 5 | BDQ15 | C | PB22B | 5 | BDQ24 | C |
| Y8 | PB16A | 5 | BDQ15 | T | PB25A | 5 | BDQ24 | T |
| GNDIO | GNDIO5 | - | | | GNDIO | - | | |
| W9 | PB15A | 5 | BDQS15 | T | PB24A | 5 | BDQS24 | T |
| AA8 | PB16B | 5 | BDQ15 | C | PB25B | 5 | BDQ24 | C |
| V9 | PB15B | 5 | BDQ15 | C | PB24B | 5 | BDQ24 | C |
| AB8 | PB18A | 5 | BDQ15 | T | PB27A | 5 | BDQ24 | T |
| VCCIO | VCCIO5 | 5 | | | VCCIO5 | 5 | | |
| W10 | PB17A | 5 | BDQ15 | T | PB26A | 5 | BDQ24 | T |
| AA9 | PB18B | 5 | BDQ15 | C | PB27B | 5 | BDQ24 | C |
| V10 | PB17B | 5 | BDQ15 | C | PB26B | 5 | BDQ24 | C |
| GNDIO | GNDIO5 | - | | | GNDIO | - | | |
| Y10 | PB21A | 5 | BDQ24 | T | PB30A | 5 | BDQ33 | T |
| AB9 | PB20A | 5 | BDQ24 | T | PB29A | 5 | BDQ33 | T |
| AA10 | PB21B | 5 | BDQ24 | C | PB30B | 5 | BDQ33 | C |
| AB10 | PB20B | 5 | BDQ24 | C | PB29B | 5 | BDQ33 | C |
| AB11 | PB23A | 5 | BDQ24 | T | PB32A | 5 | BDQ33 | T |
| U10 | PB22A | 5 | BDQ24 | T | PB31A | 5 | BDQ33 | T |
| VCCIO | VCCIO5 | 5 | | | VCCIO5 | 5 | | |
| AA11 | PB23B | 5 | BDQ24 | C | PB32B | 5 | BDQ33 | C |
| U11 | PB22B | 5 | BDQ24 | C | PB31B | 5 | BDQ33 | C |
| GNDIO | GNDIO5 | - | | | GNDIO5 | - | | |
| AB12 | PB25A | 5 | BDQ24 | T | PB34A | 5 | BDQ33 | T |
| Y11 | PB24A | 5 | BDQS24 | T | PB33A | 5 | BDQS33 | T |
| AA12 | PB25B | 5 | BDQ24 | C | PB34B | 5 | BDQ33 | C |
| W11 | PB24B | 5 | BDQ24 | C | PB33B | 5 | BDQ33 | C |
| AB13 | PB26A | 5 | PCLKT5_0/BDQ24 | T | PB35A | 5 | PCLKT5_0/BDQ33 | T |
| VCCIO | VCCIO5 | 5 | | | VCCIO5 | 5 | | |
| AB14 | PB26B | 5 | PCLKC5_0/BDQ24 | C | PB35B | 5 | PCLKC5_0/BDQ33 | C |
| GNDIO | GNDIO5 | - | | | GNDIO5 | - | | |
| Y12 | PB32A | 4 | BDQ33 | T | PB41A | 4 | BDQ42 | T |
| W12 | PB32B | 4 | BDQ33 | C | PB41B | 4 | BDQ42 | C |
| VCCIO | VCCIO4 | 4 | | | VCCIO4 | 4 | | |
| U12 | PB31A | 4 | PCLKT4_0/BDQ33 | T | PB40A | 4 | PCLKT4_0/BDQ42 | T |
| V12 | PB31B | 4 | PCLKC4_0/BDQ33 | C | PB40B | 4 | PCLKC4_0/BDQ42 | C |
| U13 | PB34A | 4 | BDQ33 | T | PB43A | 4 | BDQ42 | T |
| GNDIO | GNDIO4 | - | | | GNDIO4 | - | | |
| AA13 | PB33A | 4 | BDQS33 | T | PB42A | 4 | BDQS42 | T |
| U14 | PB34B | 4 | BDQ33 | C | PB43B | 4 | BDQ42 | C |
| Y13 | PB33B | 4 | BDQ33 | C | PB42B | 4 | BDQ42 | C |
| AB16 | PB36A | 4 | BDQ33 | T | PB45A | 4 | BDQ42 | T |
| VCCIO | VCCIO4 | 4 | | | VCCIO4 | 4 | | |
| AB15 | PB35A | 4 | BDQ33 | T | PB44A | 4 | BDQ42 | T |
| AB17 | PB36B | 4 | BDQ33 | C | PB45B | 4 | BDQ42 | C |

# LFE2-12E/SE and LFE2-20E/SE Logic Signal Connections: 484 fpBGA (Cont.)

| LFE2-12E/12SE | | | | | LFE2-20E/20SE | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| J9 | GND | - | | | GND | - | | |
| K10 | GND | - | | | GND | - | | |
| K11 | GND | - | | | GND | - | | |
| K12 | GND | - | | | GND | - | | |
| K13 | GND | - | | | GND | - | | |
| K15 | GND | - | | | GND | - | | |
| K8 | GND | - | | | GND | - | | |
| L10 | GND | - | | | GND | - | | |
| L11 | GND | - | | | GND | - | | |
| L12 | GND | - | | | GND | - | | |
| L13 | GND | - | | | GND | - | | |
| L15 | GND | - | | | GND | - | | |
| L8 | GND | - | | | GND | - | | |
| M10 | GND | - | | | GND | - | | |
| M11 | GND | - | | | GND | - | | |
| M12 | GND | - | | | GND | - | | |
| M13 | GND | - | | | GND | - | | |
| M15 | GND | - | | | GND | - | | |
| M8 | GND | - | | | GND | - | | |
| N10 | GND | - | | | GND | - | | |
| N11 | GND | - | | | GND | - | | |
| N12 | GND | - | | | GND | - | | |
| N13 | GND | - | | | GND | - | | |
| N15 | GND | - | | | GND | - | | |
| N8 | GND | - | | | GND | - | | |
| P14 | GND | - | | | GND | - | | |
| P20 | GND | - | | | GND | - | | |
| P3 | GND | - | | | GND | - | | |
| P9 | GND | - | | | GND | - | | |
| R10 | GND | - | | | GND | - | | |
| R11 | GND | - | | | GND | - | | |
| R12 | GND | - | | | GND | - | | |
| R13 | GND | - | | | GND | - | | |
| U17 | GND | - | | | GND | - | | |
| U6 | GND | - | | | GND | - | | |
| W2 | GND | - | | | GND | - | | |
| W21 | GND | - | | | GND | - | | |
| Y14 | GND | - | | | GND | - | | |
| Y9 | GND | - | | | GND | - | | |
| H6 | NC | - | | | NC | - | | |
| J6 | NC | - | | | NC | - | | |
| H3 | NC | - | | | NC | - | | |
| H2 | NC | - | | | NC | - | | |
| H17 | NC | - | | | NC | - | | |

# LFE2-35E/SE and LFE2-50E/SE Logic Signal Connections: 484 fpBGA (Cont.)

| LFE2-35E/SE | | | | | LFE2-50E/SE | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| W20 | CFG0 | 8 | | | CFG0 | 8 | | |
| V20 | PROGRAMN | 8 | | | PROGRAMN | 8 | | |
| W22 | CCLK | 8 | | | CCLK | 8 | | |
| V22 | INITN | 8 | | | INITN | 8 | | |
| V21 | DONE | 8 | | | DONE | 8 | | |
| GNDIO | GNDIO8 | - | | | GNDIO8 | - | | |
| R16 | PR58B | 8 | WRITEN | C | PR77B | 8 | WRITEN | C |
| R17 | PR58A | 8 | CS1N | T | PR77A | 8 | CS1N | T |
| U19 | PR57B | 8 | CSN | C | PR76B | 8 | CSN | C |
| U20 | PR57A | 8 | D0/SPIFASTN | T | PR76A | 8 | D0/SPIFASTN | T |
| VCCIO | VCCIO8 | 8 | | | VCCIO | 8 | | |
| U22 | PR56B | 8 | D1 | C | PR75B | 8 | D1 | C |
| U21 | PR56A | 8 | D2 | T | PR75A | 8 | D2 | T |
| T20 | PR55B | 8 | D3 | C | PR74B | 8 | D3 | C |
| GNDIO | GNDIO8 | - | | | GNDIO8 | - | | |
| T19 | PR55A | 8 | D4 | T | PR74A | 8 | D4 | T |
| T17 | PR54B | 8 | D5 | C | PR73B | 8 | D5 | C |
| T18 | PR54A | 8 | D6 | T | PR73A | 8 | D6 | T |
| T21 | PR53B | 8 | D7/SPID0 | C | PR72B | 8 | D7/SPID0 | C |
| VCCIO | VCCIO8 | 8 | | | VCCIO | 8 | | |
| T22 | PR53A | 8 | DI/CSSPI0N | T | PR72A | 8 | DI/CSSPI0N | T |
| R18 | PR52B | 8 | DOUT/CSON | C | PR71B | 8 | DOUT/CSON | C |
| R19 | PR52A | 8 | BUSY/SISPI | T | PR71A | 8 | BUSY/SISPI | T |
| GNDIO | GNDIO3 | - | | | GNDIO3 | - | | |
| VCCIO | VCCIO3 | 3 | | | VCCIO | 3 | | |
| R22 | PR47B | 3 | RDQ48 | C | PR66B | 3 | RDQ67 | C |
| R21 | PR47A | 3 | RDQ48 | T | PR66A | 3 | RDQ67 | T |
| P18 | PR46B | 3 | RDQ48 | C (LVDS)* | PR65B | 3 | RDQ67 | C (LVDS)* |
| P19 | PR46A | 3 | RDQ48 | T (LVDS)* | PR65A | 3 | RDQ67 | T (LVDS)* |
| VCCIO | VCCIO3 | 3 | | | VCCIO | 3 | | |
| R20 | PR45B | 3 | RLM0_GPLLC_FB_A/RDQ48 | C | PR64B | 3 | RLM0_GPLLC_FB_A/RDQ67 | C |
| P22 | PR45A | 3 | RLM0_GPLLT_FB_A/RDQ48 | T | PR64A | 3 | RLM0_GPLLT_FB_A/RDQ67 | T |
| P21 | PR44B | 3 | RLM0_GPLLC_IN_A**/RDQ48 | C (LVDS)* | PR63B | 3 | RLM0_GPLLC_IN_A**/RDQ67 | C (LVDS)* |
| N21 | PR44A | 3 | RLM0_GPLLT_IN_A**/RDQ48 | T (LVDS)* | PR63A | 3 | RLM0_GPLLT_IN_A**/RDQ67 | T (LVDS)* |
| N17 | RLM0_PLLCAP | 3 | | | RLM0_PLLCAP | 3 | | |
| N22 | PR42B | 3 | RLM0_GDLLC_FB_A/RDQ39 | C | PR61B | 3 | RLM0_GDLLC_FB_A/RDQ58 | C |
| N20 | PR42A | 3 | RLM0_GDLLT_FB_A/RDQ39 | T | PR61A | 3 | RLM0_GDLLT_FB_A/RDQ58 | T |
| GNDIO | GNDIO3 | - | | | GNDIO3 | - | | |
| M22 | PR41B | 3 | RLM0_GDLLC_IN_A**/RDQ39 | C (LVDS)* | PR60B | 3 | RLM0_GDLLC_IN_A**/RDQ58 | C (LVDS)* |
| M21 | PR41A | 3 | RLM0_GDLLT_IN_A**/RDQ39 | T (LVDS)* | PR60A | 3 | RLM0_GDLLT_IN_A**/RDQ58 | T (LVDS)* |
| N19 | PR40B | 3 | RDQ39 | C | PR59B | 3 | RDQ58 | C |
| M19 | PR40A | 3 | RDQ39 | T | PR59A | 3 | RDQ58 | T |
| VCCIO | VCCIO3 | 3 | | | VCCIO | 3 | | |
| GNDIO | GNDIO3 | - | | | GNDIO3 | - | | |
| L22 | PR30B | 3 | RDQ31 | C | PR49B | 3 | RDQ50 | C |
| K22 | PR30A | 3 | RDQ31 | T | PR49A | 3 | RDQ50 | T |

# LFE2-35E/SE and LFE2-50E/SE Logic Signal Connections: 484 fpBGA (Cont.)

| LFE2-35E/SE | | | | | LFE2-50E/SE | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| J10 | VCC | - | | | VCC | - | | |
| J11 | VCC | - | | | VCC | - | | |
| J12 | VCC | - | | | VCC | - | | |
| J13 | VCC | - | | | VCC | - | | |
| K14 | VCC | - | | | VCC | - | | |
| K9 | VCC | - | | | VCC | - | | |
| L14 | VCC | - | | | VCC | - | | |
| L9 | VCC | - | | | VCC | - | | |
| M14 | VCC | - | | | VCC | - | | |
| M9 | VCC | - | | | VCC | - | | |
| N14 | VCC | - | | | VCC | - | | |
| N9 | VCC | - | | | VCC | - | | |
| P10 | VCC | - | | | VCC | - | | |
| P11 | VCC | - | | | VCC | - | | |
| P12 | VCC | - | | | VCC | - | | |
| P13 | VCC | - | | | VCC | - | | |
| G5 | VCCAUX | - | | | VCCAUX | 0 | | |
| K5 | VCCAUX | - | | | VCCAUX | 0 | | |
| R5 | VCCAUX | - | | | VCCAUX | 1 | | |
| V7 | VCCAUX | - | | | VCCAUX | 1 | | |
| V11 | VCCAUX | - | | | VCCAUX | 2 | | |
| V8 | VCCAUX | - | | | VCCAUX | 2 | | |
| V13 | VCCAUX | - | | | VCCAUX | 3 | | |
| V15 | VCCAUX | - | | | VCCAUX | 3 | | |
| M17 | VCCAUX | - | | | VCCAUX | 4 | | |
| P17 | VCCAUX | - | | | VCCAUX | 4 | | |
| E17 | VCCAUX | - | | | VCCAUX | 5 | | |
| G18 | VCCAUX | - | | | VCCAUX | 5 | | |
| D11 | VCCAUX | - | | | VCCAUX | 6 | | |
| F13 | VCCAUX | - | | | VCCAUX | 6 | | |
| C5 | VCCAUX | - | | | VCCAUX | 7 | | |
| E6 | VCCAUX | - | | | VCCAUX | 7 | | |
| G10 | VCCIO0 | 0 | | | VCCIO0 | 0 | | |
| G9 | VCCIO0 | 0 | | | VCCIO0 | 0 | | |
| H8 | VCCIO0 | 0 | | | VCCIO0 | 0 | | |
| H9 | VCCIO0 | 0 | | | VCCIO0 | 0 | | |
| G11 | VCCIO1 | 1 | | | VCCIO1 | 1 | | |
| G12 | VCCIO1 | 1 | | | VCCIO1 | 1 | | |
| G13 | VCCIO1 | 1 | | | VCCIO1 | 1 | | |
| G14 | VCCIO1 | 1 | | | VCCIO1 | 1 | | |
| H14 | VCCIO2 | 2 | | | VCCIO2 | 2 | | |
| H15 | VCCIO2 | 2 | | | VCCIO2 | 2 | | |
| J15 | VCCIO2 | 2 | | | VCCIO2 | 2 | | |
| K16 | VCCIO2 | 2 | | | VCCIO2 | 2 | | |
| L16 | VCCIO3 | 3 | | | VCCIO3 | 3 | | |
| M16 | VCCIO3 | 3 | | | VCCIO3 | 3 | | |

# LFE2-20E/SE and LFE2-35E/SE Logic Signal Connections: 672 fpBGA (Cont.)

| LFE2-20E/20SE | | | | | LFE2-35E/35SE | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| N15 | GND | - | | | GND | - | | |
| N17 | GND | - | | | GND | - | | |
| P10 | GND | - | | | GND | - | | |
| P12 | GND | - | | | GND | - | | |
| P13 | GND | - | | | GND | - | | |
| P14 | GND | - | | | GND | - | | |
| P15 | GND | - | | | GND | - | | |
| P17 | GND | - | | | GND | - | | |
| R13 | GND | - | | | GND | - | | |
| R14 | GND | - | | | GND | - | | |
| T10 | GND | - | | | GND | - | | |
| T11 | GND | - | | | GND | - | | |
| T16 | GND | - | | | GND | - | | |
| T17 | GND | - | | | GND | - | | |
| T24 | GND | - | | | GND | - | | |
| T3 | GND | - | | | GND | - | | |
| U10 | GND | - | | | GND | - | | |
| U11 | GND | - | | | GND | - | | |
| U13 | GND | - | | | GND | - | | |
| U14 | GND | - | | | GND | - | | |
| U16 | GND | - | | | GND | - | | |
| U17 | GND | - | | | GND | - | | |
| V13 | GND | - | | | GND | - | | |
| V14 | GND | - | | | GND | - | | |
| V21 | GND | - | | | GND | - | | |
| V6 | GND | - | | | GND | - | | |
| M3 | NC | - | | | NC | - | | |
| N6 | NC | - | | | NC | - | | |
| P24 | NC | - | | | NC | - | | |

* Supports true LVDS. Other differential signals must be emulated with external resistors.
** These dedicated input pins can be used for GPLLs or GDLLs within the respective quadrant.
***Due to packaging bond out option, this DQS does not have all the necessary DQ pins bonded out for a full 8-bit data width.

Note: VCCIO and GND pads are used to determine the average DC current drawn by I/Os between GND/VCCIO connections, or between the last GND/VCCIO in an I/O bank and the end of an I/O bank. The substrate pads listed in the Pin Table do not necessarily have a one to one connection with a package ball or pin.

# LFE2-50E/SE and LFE2-70E/SE Logic Signal Connections: 672 fpBGA

| LFE2-50E/SE | | | | | LFE2-70E/SE | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| D2 | PL2A | 7 | VREF2_7 | T (LVDS)* | PL2A | 7 | VREF2_7 | T (LVDS)* |
| D1 | PL2B | 7 | VREF1_7 | C (LVDS)* | PL2B | 7 | VREF1_7 | C (LVDS)* |
| GND | GNDIO7 | - | | | GNDIO7 | - | | |
| F6 | PL5A | 7 | LDQ8 | T | PL18A | 7 | LDQ21 | T |
| F5 | PL5B | 7 | LDQ8 | C | PL18B | 7 | LDQ21 | C |
| VCCIO | VCCIO7 | 7 | | | VCCIO7 | 7 | | |
| E4 | PL6A | 7 | LDQ8 | T (LVDS)* | PL19A | 7 | LDQ21 | T (LVDS)* |
| E3 | PL6B | 7 | LDQ8 | C (LVDS)* | PL19B | 7 | LDQ21 | C (LVDS)* |
| E2 | PL7A | 7 | LDQ8 | T | PL20A | 7 | LDQ21 | T |
| E1 | PL7B | 7 | LDQ8 | C | PL20B | 7 | LDQ21 | C |
| GND | GNDIO7 | - | | | GNDIO7 | - | | |
| H6 | PL8A | 7 | LDQS8 | T (LVDS)* | PL21A | 7 | LDQS21 | T (LVDS)* |
| H5 | PL8B | 7 | LDQ8 | C (LVDS)* | PL21B | 7 | LDQ21 | C (LVDS)* |
| F2 | PL9A | 7 | LDQ8 | T | PL22A | 7 | LDQ21 | T |
| VCCIO | VCCIO7 | 7 | | | VCCIO7 | 7 | | |
| F1 | PL9B | 7 | LDQ8 | C | PL22B | 7 | LDQ21 | C |
| H8 | PL10A | 7 | LDQ8 | T (LVDS)* | PL23A | 7 | LDQ21 | T (LVDS)* |
| J9 | PL10B | 7 | LDQ8 | C (LVDS)* | PL23B | 7 | LDQ21 | C (LVDS)* |
| G4 | PL11A | 7 | LDQ8 | T | PL24A | 7 | LDQ21 | T |
| GND | GNDIO7 | - | | | GNDIO7 | - | | |
| G3 | PL11B | 7 | LDQ8 | C | PL24B | 7 | LDQ21 | C |
| H7 | PL12A | 7 | LDQ16 | T (LVDS)* | PL25A | 7 | LDQ29 | T (LVDS)* |
| J8 | PL12B | 7 | LDQ16 | C (LVDS)* | PL25B | 7 | LDQ29 | C (LVDS)* |
| G2 | PL13A | 7 | LDQ16 | T | PL26A | 7 | LDQ29 | T |
| G1 | PL13B | 7 | LDQ16 | C | PL26B | 7 | LDQ29 | C |
| H3 | PL14A | 7 | LDQ16 | T (LVDS)* | PL27A | 7 | LDQ29 | T (LVDS)* |
| VCCIO | VCCIO7 | 7 | | | VCCIO7 | 7 | | |
| H4 | PL14B | 7 | LDQ16 | C (LVDS)* | PL27B | 7 | LDQ29 | C (LVDS)* |
| J5 | PL15A | 7 | LDQ16 | T | PL28A | 7 | LDQ29 | T |
| J4 | PL15B | 7 | LDQ16 | C | PL28B | 7 | LDQ29 | C |
| J3 | PL16A | 7 | LDQS16 | T (LVDS)* | PL29A | 7 | LDQS29 | T (LVDS)* |
| GND | GNDIO7 | - | | | GNDIO7 | - | | |
| K4 | PL16B | 7 | LDQ16 | C (LVDS)* | PL29B | 7 | LDQ29 | C (LVDS)* |
| H1 | PL17A | 7 | LDQ16 | T | PL30A | 7 | LDQ29 | T |
| H2 | PL17B | 7 | LDQ16 | C | PL30B | 7 | LDQ29 | C |
| VCCIO | VCCIO7 | 7 | | | VCCIO7 | 7 | | |
| K6 | PL18A | 7 | LDQ16 | T (LVDS)* | PL31A | 7 | LDQ29 | T (LVDS)* |
| K7 | PL18B | 7 | LDQ16 | C (LVDS)* | PL31B | 7 | LDQ29 | C (LVDS)* |
| J1 | PL19A | 7 | LDQ16 | T | PL32A | 7 | LDQ29 | T |
| J2 | PL19B | 7 | LDQ16 | C | PL32B | 7 | LDQ29 | C |
| GND | GNDIO7 | - | | | GNDIO7 | - | | |
| VCCIO | VCCIO7 | 7 | | | VCCIO7 | 7 | | |
| K3 | PL23A | 7 | LDQ24 | T | PL36A | 7 | LDQ37 | T |
| K2 | PL23B | 7 | LDQ24 | C | PL36B | 7 | LDQ37 | C |
| GND | GNDIO7 | - | | | GNDIO7 | - | | |
| K1 | PL24A | 7 | LDQS24*** | T (LVDS)* | PL37A | 7 | LDQS37*** | T (LVDS)* |

# LFE2-50E/SE and LFE2-70E/SE Logic Signal Connections: 672 fpBGA (Cont.)

| LFE2-50E/SE | | | | | LFE2-70E/SE | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| GND | GNDIO1 | - | | | GNDIO1 | - | | |
| C15 | PT54B | 1 | | C | PT63B | 1 | | C |
| A15 | PT54A | 1 | | T | PT63A | 1 | | T |
| A13 | PT53B | 1 | | C | PT62B | 1 | | C |
| B13 | PT53A | 1 | | T | PT62A | 1 | | T |
| VCCIO | VCCIO1 | 1 | | | VCCIO1 | 1 | | |
| H17 | PT52B | 1 | | C | PT61B | 1 | | C |
| H15 | PT52A | 1 | | T | PT61A | 1 | | T |
| D13 | PT51B | 1 | | C | PT60B | 1 | | C |
| C14 | PT51A | 1 | | T | PT60A | 1 | | T |
| GND | GNDIO1 | - | | | GNDIO1 | - | | |
| G14 | PT50B | 1 | | C | PT59B | 1 | | C |
| E14 | PT50A | 1 | | T | PT59A | 1 | | T |
| A12 | PT49B | 1 | | C | PT58B | 1 | | C |
| B12 | PT49A | 1 | | T | PT58A | 1 | | T |
| VCCIO | VCCIO1 | 1 | | | VCCIO1 | 1 | | |
| F14 | PT48B | 1 | PCLKC1_0 | C | PT57B | 1 | PCLKC1_0 | C |
| D14 | PT48A | 1 | PCLKT1_0 | T | PT57A | 1 | PCLKT1_0 | T |
| H16 | XRES | 1 | | | XRES | 1 | | |
| H14 | PT46B | 0 | PCLKC0_0 | C | PT55B | 0 | PCLKC0_0 | C |
| GND | GNDIO0 | - | | | GNDIO0 | - | | |
| H13 | PT46A | 0 | PCLKT0_0 | T | PT55A | 0 | PCLKT0_0 | T |
| A11 | PT45B | 0 | | C | PT54B | 0 | | C |
| B11 | PT45A | 0 | | T | PT54A | 0 | | T |
| C13 | PT44B | 0 | | C | PT53B | 0 | | C |
| VCCIO | VCCIO0 | 0 | | | VCCIO0 | 0 | | |
| E13 | PT44A | 0 | | T | PT53A | 0 | | T |
| D12 | PT43B | 0 | | C | PT52B | 0 | | C |
| F13 | PT43A | 0 | | T | PT52A | 0 | | T |
| A10 | PT42B | 0 | | C | PT51B | 0 | | C |
| B10 | PT42A | 0 | | T | PT51A | 0 | | T |
| C12 | PT41B | 0 | | C | PT50B | 0 | | C |
| GND | GNDIO0 | - | | | GNDIO0 | - | | |
| C10 | PT41A | 0 | | T | PT50A | 0 | | T |
| G13 | PT40B | 0 | | C | PT49B | 0 | | C |
| VCCIO | VCCIO0 | 0 | | | VCCIO0 | 0 | | |
| H12 | PT40A | 0 | | T | PT49A | 0 | | T |
| A9 | PT39B | 0 | | C | PT48B | 0 | | C |
| B9 | PT39A | 0 | | T | PT48A | 0 | | T |
| E12 | PT38B | 0 | | C | PT47B | 0 | | C |
| G12 | PT38A | 0 | | T | PT47A | 0 | | T |
| A8 | PT37B | 0 | | C | PT46B | 0 | | C |
| B8 | PT37A | 0 | | T | PT46A | 0 | | T |
| GND | GNDIO0 | - | | | GNDIO0 | - | | |
| E11 | PT36B | 0 | | C | PT45B | 0 | | C |
| C9 | PT36A | 0 | | T | PT45A | 0 | | T |

# LFE2-50E/SE and LFE2-70E/SE Logic Signal Connections: 672 fpBGA (Cont.)

| LFE2-50E/SE | | | | | LFE2-70E/SE | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| N15 | GND | - | | | GND | - | | |
| N17 | GND | - | | | GND | - | | |
| P10 | GND | - | | | GND | - | | |
| P12 | GND | - | | | GND | - | | |
| P13 | GND | - | | | GND | - | | |
| P14 | GND | - | | | GND | - | | |
| P15 | GND | - | | | GND | - | | |
| P17 | GND | - | | | GND | - | | |
| R13 | GND | - | | | GND | - | | |
| R14 | GND | - | | | GND | - | | |
| T10 | GND | - | | | GND | - | | |
| T11 | GND | - | | | GND | - | | |
| T16 | GND | - | | | GND | - | | |
| T17 | GND | - | | | GND | - | | |
| T24 | GND | - | | | GND | - | | |
| T3 | GND | - | | | GND | - | | |
| U10 | GND | - | | | GND | - | | |
| U11 | GND | - | | | GND | - | | |
| U13 | GND | - | | | GND | - | | |
| U14 | GND | - | | | GND | - | | |
| U16 | GND | - | | | GND | - | | |
| U17 | GND | - | | | GND | - | | |
| V13 | GND | - | | | GND | - | | |
| V14 | GND | - | | | GND | - | | |
| V21 | GND | - | | | GND | - | | |
| V6 | GND | - | | | GND | - | | |
| M3 | NC | - | | | NC | - | | |
| N6 | NC | - | | | NC | - | | |
| P24 | NC | - | | | NC | - | | |

* Supports true LVDS. Other differential signals must be emulated with external resistors.
** These dedicated input pins can be used for GPLLs or GDLLs within the respective quadrant.
***Due to packaging bond out option, this DQS does not have all the necessary DQ pins bonded out for a full 8-bit data width.

Note: VCCIO and GND pads are used to determine the average DC current drawn by I/Os between GND/VCCIO connections, or between the last GND/VCCIO in an I/O bank and the end of an I/O bank. The substrate pads listed in the Pin Table do not necessarily have a one to one connection with a package ball or pin.

## LFE2-70E/SE Logic Signal Connections: 900 fpBGA (Cont.)

| LFE2-70E/SE | | | | |
|---|---|---|---|---|
| **Ball Number** | **Ball/Pad Function** | **Bank** | **Dual Function** | **Differential** |
| AH24 | PB89A | 4 | BDQ87 | T |
| AH25 | PB89B | 4 | BDQ87 | C |
| VCCIO | VCCIO4 | 4 | | |
| AJ26 | PB90A | 4 | BDQ87 | T |
| AK26 | PB90B | 4 | BDQ87 | C |
| AF25 | PB91A | 4 | BDQ87 | T |
| AG25 | PB91B | 4 | BDQ87 | C |
| GND | GNDIO4 | - | | |
| AK22 | PB92A | 4 | BDQ96 | T |
| AJ22 | PB92B | 4 | BDQ96 | C |
| AE22 | PB93A | 4 | BDQ96 | T |
| AF22 | PB93B | 4 | BDQ96 | C |
| AG22 | PB94A | 4 | BDQ96 | T |
| VCCIO | VCCIO4 | 4 | | |
| AH22 | PB94B | 4 | BDQ96 | C |
| AG24 | PB95A | 4 | BDQ96 | T |
| AG23 | PB95B | 4 | BDQ96 | C |
| AE23 | PB96A | 4 | BDQS96 | |
| GND | GNDIO4 | - | | |
| AC22 | PB97A | 4 | BDQ96 | |
| AJ23 | PB98A | 4 | BDQ96 | T |
| VCCIO | VCCIO4 | 4 | | |
| AK23 | PB98B | 4 | BDQ96 | C |
| AD24 | PB99A | 4 | BDQ96 | T |
| AF24 | PB99B | 4 | BDQ96 | C |
| AC23 | PB100A | 4 | VREF2_4/BDQ96 | T |
| GND | GNDIO4 | - | | |
| AE24 | PB100B | 4 | VREF1_4/BDQ96 | C |
| AE25 | CFG2 | 8 | | |
| AB22 | CFG1 | 8 | | |
| AE26 | CFG0 | 8 | | |
| AA22 | PROGRAMN | 8 | | |
| AD25 | CCLK | 8 | | |
| AD26 | INITN | 8 | | |
| AC24 | DONE | 8 | | |
| GND | GNDIO4 | - | | |
| AC25 | PR90B | 8 | WRITEN | C |
| AE27 | PR90A | 8 | CS1N | T |
| AC26 | PR89B | 8 | CSN | C |
| AE28 | PR89A | 8 | D0/SPIFASTN | T |
| VCCIO | VCCIO8 | 8 | | |
| AD27 | PR88B | 8 | D1 | C |
| AD28 | PR88A | 8 | D2 | T |

# LFE2M-20E/SE and LFE2M-35E/SE Logic Signal Connections: 256 fpBGA (Cont.)

| LFE2M20E/SE | | | | | LFE2M35E/SE | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| F14 | PR24B | 2 | RDQ22 | C (LVDS)* | PR34B | 2 | RDQ32 | C(LVDS)* |
| F13 | PR24A | 2 | RDQ22 | T (LVDS)* | PR34A | 2 | RDQ32 | T (LVDS)* |
| VCCIO | VCCIO2 | 2 | | | VCCIO2 | 2 | | |
| GNDIO | GNDIO2 | - | | | GNDIO2 | - | | |
| H11 | PR14B | 2 | | C | PR14B | 2 | RDQ15 | C |
| G11 | PR14A | 2 | | T | PR14A | 2 | RDQ15 | T |
| E13 | PR13B | 2 | | C (LVDS)* | PR13B | 2 | RDQ15 | C(LVDS)* |
| F12 | PR13A | 2 | | T (LVDS)* | PR13A | 2 | RDQ15 | T (LVDS)* |
| VCCIO | VCCIO2 | 2 | | | VCCIO2 | 2 | | |
| F11 | PR12B | 2 | RUM0_SPLLC_FB_A | C | PR12B | 2 | RUM0_SPLLC_FB_A/RDQ15 | C |
| E12 | PR12A | 2 | RUM0_SPLLT_FB_A | T | PR12A | 2 | RUM0_SPLLT_FB_A/RDQ15 | T |
| D16 | PR11B | 2 | RUM0_SPLLC_IN_A | C (LVDS)* | PR11B | 2 | RUM0_SPLLC_IN_A/RDQ15 | C(LVDS)* |
| D15 | PR11A | 2 | RUM0_SPLLT_IN_A | T (LVDS)* | PR11A | 2 | RUM0_SPLLT_IN_A/RDQ15 | T (LVDS)* |
| C16 | PR9B | 2 | VREF2_2 | C | PR9B | 2 | VREF2_2 | C |
| GNDIO | GNDIO2 | - | | | GNDIO2 | - | | |
| B16 | PR9A | 2 | VREF1_2 | T | PR9A | 2 | VREF1_2 | T |
| VCCIO | VCCIO2 | 2 | | | VCCIO2 | 2 | | |
| F4 | XRES | - | | | XRES | - | | |
| C15 | URC_SQ_VCCRX0 | 12 | | | URC_SQ_VCCRX0 | 12 | | |
| A14 | URC_SQ_HDINP0 | 12 | | T | URC_SQ_HDINP0 | 12 | | T |
| B15 | URC_SQ_VCCIB0 | 12 | | | URC_SQ_VCCIB0 | 12 | | |
| B14 | URC_SQ_HDINN0 | 12 | | C | URC_SQ_HDINN0 | 12 | | C |
| C12 | URC_SQ_VCCTX0 | 12 | | | URC_SQ_VCCTX0 | 12 | | |
| A11 | URC_SQ_HDOUTP0 | 12 | | T | URC_SQ_HDOUTP0 | 12 | | T |
| A12 | URC_SQ_VCCOB0 | 12 | | | URC_SQ_VCCOB0 | 12 | | |
| B11 | URC_SQ_HDOUTN0 | 12 | | C | URC_SQ_HDOUTN0 | 12 | | C |
| C11 | URC_SQ_VCCTX1 | 12 | | | URC_SQ_VCCTX1 | 12 | | |
| B10 | URC_SQ_HDOUTN1 | 12 | | C | URC_SQ_HDOUTN1 | 12 | | C |
| C10 | URC_SQ_VCCOB1 | 12 | | | URC_SQ_VCCOB1 | 12 | | |
| A10 | URC_SQ_HDOUTP1 | 12 | | T | URC_SQ_HDOUTP1 | 12 | | T |
| C14 | URC_SQ_VCCRX1 | 12 | | | URC_SQ_VCCRX1 | 12 | | |
| B13 | URC_SQ_HDINN1 | 12 | | C | URC_SQ_HDINN1 | 12 | | C |
| C13 | URC_SQ_VCCIB1 | 12 | | | URC_SQ_VCCIB1 | 12 | | |
| A13 | URC_SQ_HDINP1 | 12 | | T | URC_SQ_HDINP1 | 12 | | T |
| B9 | URC_SQ_VCCAUX33 | 12 | | | URC_SQ_VCCAUX33 | 12 | | |
| D8 | URC_SQ_REFCLKN | 12 | | C | URC_SQ_REFCLKN | 12 | | C |
| D9 | URC_SQ_REFCLKP | 12 | | T | URC_SQ_REFCLKP | 12 | | T |
| C9 | URC_SQ_VCCP | 12 | | | URC_SQ_VCCP | 12 | | |
| A5 | URC_SQ_HDINP2 | 12 | | T | URC_SQ_HDINP2 | 12 | | T |
| C5 | URC_SQ_VCCIB2 | 12 | | | URC_SQ_VCCIB2 | 12 | | |
| B5 | URC_SQ_HDINN2 | 12 | | C | URC_SQ_HDINN2 | 12 | | C |
| C4 | URC_SQ_VCCRX2 | 12 | | | URC_SQ_VCCRX2 | 12 | | |
| A8 | URC_SQ_HDOUTP2 | 12 | | T | URC_SQ_HDOUTP2 | 12 | | T |
| C8 | URC_SQ_VCCOB2 | 12 | | | URC_SQ_VCCOB2 | 12 | | |
| B8 | URC_SQ_HDOUTN2 | 12 | | C | URC_SQ_HDOUTN2 | 12 | | C |
| C7 | URC_SQ_VCCTX2 | 12 | | | URC_SQ_VCCTX2 | 12 | | |
| B7 | URC_SQ_HDOUTN3 | 12 | | C | URC_SQ_HDOUTN3 | 12 | | C |
| A6 | URC_SQ_VCCOB3 | 12 | | | URC_SQ_VCCOB3 | 12 | | |

# LFE2M20E/SE and LFE2M35E/SE Logic Signal Connections: 484 fpBGA

| LFE2M20E/SE | | | | | LFE2M35E/SE | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| D1 | PL2A | 7 | LDQ6 | T (LVDS)* | PL2A | 7 | LDQ6 | T (LVDS)* |
| E1 | PL2B | 7 | LDQ6 | C (LVDS)* | PL2B | 7 | LDQ6 | C (LVDS)* |
| F1 | PL3A | 7 | LDQ6 | T | PL3A | 7 | LDQ6 | T |
| F2 | PL3B | 7 | LDQ6 | C | PL3B | 7 | LDQ6 | C |
| F5 | PL4A | 7 | LDQ6 | T (LVDS)* | PL4A | 7 | LDQ6 | T (LVDS)* |
| VCCIO | VCCIO7 | 7 | | | VCCIO7 | 7 | | |
| G6 | PL4B | 7 | LDQ6 | C (LVDS)* | PL4B | 7 | LDQ6 | C (LVDS)* |
| F4 | PL5A | 7 | LDQ6 | T | PL5A | 7 | LDQ6 | T |
| F3 | PL5B | 7 | LDQ6 | C | PL5B | 7 | LDQ6 | C |
| G1 | PL6A | 7 | LDQS6 | T (LVDS)* | PL6A | 7 | LDQS6 | T (LVDS)* |
| GNDIO | GNDIO7 | - | | | GNDIO7 | - | | |
| G2 | PL6B | 7 | LDQ6 | C (LVDS)* | PL6B | 7 | LDQ6 | C (LVDS)* |
| H1 | PL7A | 7 | LDQ6 | T | PL7A | 7 | LDQ6 | T |
| H2 | PL7B | 7 | LDQ6 | C | PL7B | 7 | LDQ6 | C |
| VCCIO | VCCIO7 | 7 | | | VCCIO7 | 7 | | |
| H7 | PL8A | 7 | LDQ6 | T (LVDS)* | PL8A | 7 | LDQ6 | T (LVDS)* |
| H6 | PL8B | 7 | LDQ6 | C (LVDS)* | PL8B | 7 | LDQ6 | C (LVDS)* |
| G3 | PL9A | 7 | VREF2_7/LDQ6 | T | PL9A | 7 | VREF2_7/LDQ6 | T |
| H3 | PL9B | 7 | VREF1_7/LDQ6 | C | PL9B | 7 | VREF1_7/LDQ6 | C |
| GNDIO | GNDIO7 | - | | | GNDIO7 | - | | |
| H5 | PL11A | 7 | LUM0_SPLLT_IN_A | T (LVDS)* | PL11A | 7 | LUM0_SPLLT_IN_A/LDQ15 | T (LVDS)* |
| H4 | PL11B | 7 | LUM0_SPLLC_IN_A | C (LVDS)* | PL11B | 7 | LUM0_SPLLC_IN_A/LDQ15 | C (LVDS)* |
| J1 | PL12A | 7 | LUM0_SPLLT_FB_A | T | PL12A | 7 | LUM0_SPLLT_FB_A/LDQ15 | T |
| J2 | PL12B | 7 | LUM0_SPLLC_FB_A | C | PL12B | 7 | LUM0_SPLLC_FB_A/LDQ15 | C |
| J3 | PL13A | 7 | | T (LVDS)* | PL13A | 7 | LDQ15 | T (LVDS)* |
| VCCIO | VCCIO7 | 7 | | | VCCIO7 | 7 | | |
| J4 | PL13B | 7 | | C (LVDS)* | PL13B | 7 | LDQ15 | C (LVDS)* |
| J7 | PL14A | 7 | | T | PL14A | 7 | LDQ15 | T |
| J6 | PL14B | 7 | | C | PL14B | 7 | LDQ15 | C |
| GNDIO | GNDIO7 | - | | | GNDIO7 | - | | |
| VCCIO | VCCIO7 | 7 | | | VCCIO7 | 7 | | |
| K1 | PL18A | 7 | LUM1_SPLLT_IN_A/LDQ22 | T (LVDS)* | PL28A | 7 | LUM1_SPLLT_IN_A/LDQ32 | T (LVDS)* |
| K2 | PL18B | 7 | LUM1_SPLLC_IN_A/LDQ22 | C (LVDS)* | PL28B | 7 | LUM1_SPLLC_IN_A/LDQ32 | C (LVDS)* |
| J5 | PL19A | 7 | LUM1_SPLLT_FB_A/LDQ22 | T | PL29A | 7 | LUM1_SPLLT_FB_A/LDQ32 | T |
| K5 | PL19B | 7 | LUM1_SPLLC_FB_A/LDQ22 | C | PL29B | 7 | LUM1_SPLLC_FB_A/LDQ32 | C |
| VCCIO | VCCIO7 | 7 | | | VCCIO7 | 7 | | |
| K7 | PL20A | 7 | LDQ22 | T (LVDS)* | PL30A | 7 | LDQ32 | T (LVDS)* |
| K6 | PL20B | 7 | LDQ22 | C (LVDS)* | PL30B | 7 | LDQ32 | C (LVDS)* |
| L6 | PL21A | 7 | LDQ22 | T | PL31A | 7 | LDQ32 | T |
| L7 | PL21B | 7 | LDQ22 | C | PL31B | 7 | LDQ32 | C |
| GNDIO | GNDIO7 | - | | | GNDIO7 | - | | |
| L1 | PL22A | 7 | LDQS22 | T (LVDS)* | PL32A | 7 | LDQS32 | T (LVDS)* |
| L2 | PL22B | 7 | LDQ22 | C (LVDS)* | PL32B | 7 | LDQ32 | C (LVDS)* |
| M7 | PL23A | 7 | LDQ22 | T | PL33A | 7 | LDQ32 | T |
| VCCIO | VCCIO7 | 7 | | | VCCIO7 | 7 | | |
| L5 | PL23B | 7 | LDQ22 | C | PL33B | 7 | LDQ32 | C |
| L3 | PL24A | 7 | LDQ22 | T (LVDS)* | PL34A | 7 | LDQ32 | T (LVDS)* |

## LFE2M50E/SE Logic Signal Connections: 484 fpBGA (Cont.)

| LFE2M50E/SE | | | | |
|---|---|---|---|---|
| **Ball Number** | **Ball/Pad Function** | **Bank** | **Dual Function** | **Differential** |
| M19 | PR50A | 3 | RDQ52 | T (LVDS)* |
| M18 | PR49B | 3 | RDQ52 | C |
| VCCIO | VCCIO3 | 3 | | |
| L16 | PR49A | 3 | RDQ52 | T |
| L22 | PR48B | 3 | RDQ52 | C (LVDS)* |
| L21 | PR48A | 3 | RDQ52 | T (LVDS)* |
| GNDIO | GNDIO3 | - | | |
| K22 | PR46B | 3 | RLM3_SPLLC_FB_A | C |
| VCCIO | VCCIO3 | 3 | | |
| K21 | PR46A | 3 | RLM3_SPLLT_FB_A | T |
| L17 | PR45B | 3 | RLM3_SPLLC_IN_A | C (LVDS)* |
| L18 | PR45A | 3 | RLM3_SPLLT_IN_A | T (LVDS)* |
| GNDIO | GNDIO3 | - | | |
| L20 | PR44B | 3 | | C |
| L19 | PR44A | 3 | | T |
| K16 | PR43B | 3 | | C (LVDS)* |
| K17 | PR43A | 3 | | T (LVDS)* |
| VCCIO | VCCIO3 | 3 | | |
| J16 | PR42B | 3 | VREF2_3 | C |
| K18 | PR42A | 3 | VREF1_3 | T |
| J22 | PR41B | 3 | PCLKC3_0 | C (LVDS)* |
| J21 | PR41A | 3 | PCLKT3_0 | T (LVDS)* |
| H22 | PR39B | 2 | PCLKC2_0/RDQ36 | C |
| H21 | PR39A | 2 | PCLKT2_0/RDQ36 | T |
| GNDIO | GNDIO2 | - | | |
| J17 | PR38B | 2 | RDQ36 | C (LVDS)* |
| J18 | PR38A | 2 | RDQ36 | T (LVDS)* |
| J20 | PR37B | 2 | RDQ36 | C |
| J19 | PR37A | 2 | RDQ36 | T |
| VCCIO | VCCIO2 | 2 | | |
| H16 | PR36B | 2 | RDQ36 | C (LVDS)* |
| H17 | PR36A | 2 | RDQS36 | T (LVDS)* |
| G22 | PR35B | 2 | RDQ36 | C |
| GNDIO | GNDIO2 | - | | |
| G21 | PR35A | 2 | RDQ36 | T |
| H20 | PR34B | 2 | RDQ36 | C (LVDS)* |
| H19 | PR34A | 2 | RDQ36 | T (LVDS)* |
| G16 | PR33B | 2 | RUM3_SPLLC_FB_A/RDQ36 | C |
| VCCIO | VCCIO2 | 2 | | |
| H18 | PR33A | 2 | RUM3_SPLLT_FB_A/RDQ36 | T |
| F22 | PR32B | 2 | RUM3_SPLLC_IN_A/RDQ36 | C (LVDS)* |
| F21 | PR32A | 2 | RUM3_SPLLT_IN_A/RDQ36 | T (LVDS)* |
| G20 | PR30B | 2 | RDQ27 | C |

# LFE2M35E/SE and LFE2M50E/SE Logic Signal Connections: 672 fpBGA (Cont.)

| LFE2M35E/SE | | | | | LFE2M50E/SE | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| D23 | NC | - | | | NC | - | | |
| D24 | NC | - | | | NC | - | | |
| D25 | NC | - | | | NC | - | | |
| D26 | NC | - | | | NC | - | | |
| E20 | NC | - | | | NC | - | | |
| E21 | NC | - | | | NC | - | | |
| E25 | NC | - | | | NC | - | | |
| E26 | NC | - | | | NC | - | | |
| F20 | NC | - | | | NC | - | | |
| G20 | NC | - | | | NC | - | | |
| K10 | NC | - | | | NC | - | | |
| K17 | NC | - | | | NC | - | | |
| R4 | NC | - | | | NC | - | | |
| U10 | NC | - | | | NC | - | | |
| U23 | NC | - | | | NC | - | | |
| V10 | NC | - | | | NC | - | | |
| W7 | NC | - | | | NC | - | | |
| AB21 | PB69B | 4 | BDQ69 | C | NC | - | | |
| AC20 | PB58A | 4 | BDQ60 | T | NC | - | | |
| AC21 | PB63A | 4 | BDQ60 | T | NC | - | | |
| AC22 | PB69A | 4 | BDQS69**** | T | NC | - | | |
| AC23 | PB71A | 4 | BDQ69 | T | NC | - | | |
| AC25 | PB71B | 4 | BDQ69 | C | NC | - | | |
| AD26 | PB70B | 4 | BDQ69 | C | NC | - | | |
| W20 | PB72B | 4 | BDQ69 | C | NC | - | | |
| H7 | L_VCCPLL | - | | | L_VCCPLL | - | | |
| K6 | L_VCCPLL | - | | | L_VCCPLL | - | | |
| P7 | L_VCCPLL | - | | | L_VCCPLL | - | | |
| R8 | L_VCCPLL | - | | | L_VCCPLL | - | | |
| V18 | R_VCCPLL | - | | | R_VCCPLL | - | | |
| P20 | R_VCCPLL | - | | | R_VCCPLL | - | | |
| J17 | R_VCCPLL | - | | | R_VCCPLL | - | | |
| G19 | R_VCCPLL | - | | | R_VCCPLL | - | | |

* Supports true LVDS. Other differential signals must be emulated with external resistors.
** These dedicated input pins can be used for GPLLs or GDLLs within the respective quadrant.
*** For density migration, board design must take into account that these sysCONFIG pins are dual function for the lower density devices (ECP2M20 and ECP2M35). They can be either sysCONFIG pins or general purpose I/Os. These pins are dedicated pins for the higher density devices (ECP2M50, ECP2M70 and ECP2M100).
****Due to packaging bond out option, this DQS does not have all the necessary DQ pins bonded out for a full 8-bit data width.

Note: VCCIO and GND pads are used to determine the average DC current drawn by I/Os between GND/VCCIO connections, or between the last GND/VCCIO in an I/O bank and the end of an I/O bank. The substrate pads listed in the Pin Table do not necessarily have a one to one connection with a package ball or pin.

# LFE2M50E/SE and LFE2M70E/SE Logic Signal Connections: 900 fpBGA (Cont.)

| LFE2M50E/SE | | | | | LFE2M70E/SE | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| T2 | PL45B | 6 | LLM3_SPLLC_IN_A | C (LVDS)* | PL57B | 6 | LLM3_SPLLC_IN_A/LDQ55 | C (LVDS)* |
| U9 | PL46A | 6 | LLM3_SPLLT_FB_A | T | PL58A | 6 | LLM3_SPLLT_FB_A/LDQ55 | T |
| U8 | PL46B | 6 | LLM3_SPLLC_FB_A | C | PL58B | 6 | LLM3_SPLLC_FB_A/LDQ55 | C |
| VCCIO | VCCIO6 | 6 | | | GNDIO6 | - | | |
| U5 | PL48A | 6 | LDQ52 | T (LVDS)* | PL60A | 6 | LDQ64 | T (LVDS)* |
| U4 | PL48B | 6 | LDQ52 | C (LVDS)* | PL60B | 6 | LDQ64 | C (LVDS)* |
| V9 | PL49A | 6 | LDQ52 | T | PL61A | 6 | LDQ64 | T |
| V7 | PL49B | 6 | LDQ52 | C | PL61B | 6 | LDQ64 | C |
| VCCIO | VCCIO6 | 6 | | | VCCIO6 | 6 | | |
| U3 | PL50A | 6 | LDQ52 | T (LVDS)* | PL62A | 6 | LDQ64 | T (LVDS)* |
| U2 | PL50B | 6 | LDQ52 | C (LVDS)* | PL62B | 6 | LDQ64 | C (LVDS)* |
| V8 | PL51A | 6 | LDQ52 | T | PL63A | 6 | LDQ64 | T |
| U6 | PL51B | 6 | LDQ52 | C | PL63B | 6 | LDQ64 | C |
| GNDIO | GNDIO6 | - | | | GNDIO6 | - | | |
| U1 | PL52A | 6 | LDQS52 | T (LVDS)* | PL64A | 6 | LDQS64 | T (LVDS)* |
| V2 | PL52B | 6 | LDQ52 | C (LVDS)* | PL64B | 6 | LDQ64 | C (LVDS)* |
| V5 | PL53A | 6 | LDQ52 | T | PL65A | 6 | LDQ64 | T |
| VCCIO | VCCIO6 | 6 | | | VCCIO6 | 6 | | |
| V6 | PL53B | 6 | LDQ52 | C | PL65B | 6 | LDQ64 | C |
| V1 | PL54A | 6 | LDQ52 | T (LVDS)* | PL66A | 6 | LDQ64 | T (LVDS)* |
| W1 | PL54B | 6 | LDQ52 | C (LVDS)* | PL66B | 6 | LDQ64 | C (LVDS)* |
| W5 | PL55A | 6 | LDQ52 | T | PL67A | 6 | LDQ64 | T |
| GNDIO | GNDIO6 | - | | | GNDIO6 | - | | |
| W6 | PL55B | 6 | LDQ52 | C | PL67B | 6 | LDQ64 | C |
| W3 | PL57A | 6 | | T (LVDS)* | PL69A | 6 | LDQ73 | T (LVDS)* |
| W4 | PL57B | 6 | | C (LVDS)* | PL69B | 6 | LDQ73 | C (LVDS)* |
| W2 | PL58A | 6 | | T | PL70A | 6 | LDQ73 | T |
| Y4 | PL58B | 6 | | C | PL70B | 6 | LDQ73 | C |
| Y1 | PL59A | 6 | | T (LVDS)* | PL71A | 6 | LDQ73 | T (LVDS)* |
| VCCIO | VCCIO6 | 6 | | | VCCIO6 | 6 | | |
| Y2 | PL59B | 6 | | C (LVDS)* | PL71B | 6 | LDQ73 | C (LVDS)* |
| Y5 | PL60A | 6 | | T | PL72A | 6 | LDQ73 | T |
| Y6 | PL60B | 6 | | C | PL72B | 6 | LDQ73 | C |
| AA1 | NC | - | | | PL73A | 6 | LDQS73 | T (LVDS)* |
| GNDIO | GNDIO6 | - | | | GNDIO6 | - | | |
| AA2 | NC | - | | | PL73B | 6 | LDQ73 | C (LVDS)* |
| Y3 | NC | - | | | PL74A | 6 | LDQ73 | T |
| AB1 | NC | - | | | PL74B | 6 | LDQ73 | C |
| - | - | - | | | VCCIO6 | 6 | | |
| Y9 | NC | - | | | PL75A | 6 | LDQ73 | T (LVDS)* |
| Y8 | NC | - | | | PL75B | 6 | LDQ73 | C (LVDS)* |
| Y7 | NC | - | | | PL76A | 6 | LDQ73 | T |
| AA7 | NC | - | | | PL76B | 6 | LDQ73 | C |
| - | - | - | | | GNDIO6 | - | | |
| - | - | - | | | - | - | | |
| AB2 | NC | - | | | PL78A | 6 | LDQ82 | T (LVDS)* |
| AB3 | NC | - | | | PL78B | 6 | LDQ82 | C (LVDS)* |
| AA5 | NC | - | | | PL79A | 6 | LDQ82 | T |

# LFE2M70E/SE and LFE2M100E/SE Logic Signal Connections: 1152 fpBGA (Cont.)

| LFE2M70E/SE | | | | LFE2M100E/SE | | | | |
|---|---|---|---|---|---|---|---|---|
| Ball Number | Ball/Pad Function | Bank | Dual Function | Differential | Ball/Pad Function | Bank | Dual Function | Differential |
| U8 | PL43B | 7 | LUM3_SPLLC_FB_A/LDQ46 | C | PL51B | 7 | LUM3_SPLLC_FB_A/LDQ54 | C |
| VCCIO | VCCIO7 | 7 | | | VCCIO7 | 7 | | |
| T6 | PL44A | 7 | LDQ46 | T (LVDS)* | PL52A | 7 | LDQ54 | T (LVDS)* |
| R6 | PL44B | 7 | LDQ46 | C (LVDS)* | PL52B | 7 | LDQ54 | C (LVDS)* |
| U9 | PL45A | 7 | LDQ46 | T | PL53A | 7 | LDQ54 | T |
| T7 | PL45B | 7 | LDQ46 | C | PL53B | 7 | LDQ54 | C |
| GNDIO | GNDIO7 | - | | | GNDIO7 | - | | |
| U5 | PL46A | 7 | LDQS46 | T (LVDS)* | PL54A | 7 | LDQS54 | T (LVDS)* |
| U6 | PL46B | 7 | LDQ46 | C (LVDS)* | PL54B | 7 | LDQ54 | C (LVDS)* |
| U7 | PL47A | 7 | LDQ46 | T | PL55A | 7 | LDQ54 | T |
| VCCIO | VCCIO7 | 7 | | | VCCIO7 | 7 | | |
| V9 | PL47B | 7 | LDQ46 | C | PL55B | 7 | LDQ54 | C |
| V11 | PL48A | 7 | LDQ46 | T (LVDS)* | PL56A | 7 | LDQ54 | T (LVDS)* |
| V10 | PL48B | 7 | LDQ46 | C (LVDS)* | PL56B | 7 | LDQ54 | C (LVDS)* |
| U4 | PL49A | 7 | PCLKT7_0/LDQ46 | T | PL57A | 7 | PCLKT7_0/LDQ54 | T |
| GNDIO | GNDIO7 | - | | | GNDIO7 | - | | |
| U3 | PL49B | 7 | PCLKC7_0/LDQ46 | C | PL57B | 7 | PCLKC7_0/LDQ54 | C |
| U2 | PL51A | 6 | PCLKT6_0/LDQ55 | T (LVDS)* | PL59A | 6 | PCLKT6_0/LDQ63 | T (LVDS)* |
| U1 | PL51B | 6 | PCLKC6_0/LDQ55 | C (LVDS)* | PL59B | 6 | PCLKC6_0/LDQ63 | C (LVDS)* |
| V5 | PL52A | 6 | VREF2_6/LDQ55 | T | PL60A | 6 | VREF2_6/LDQ63 | T |
| V6 | PL52B | 6 | VREF1_6/LDQ55 | C | PL60B | 6 | VREF1_6/LDQ63 | C |
| V7 | PL53A | 6 | LDQ55 | T (LVDS)* | PL61A | 6 | LDQ63 | T (LVDS)* |
| VCCIO | VCCIO6 | 6 | | | VCCIO6 | 6 | | |
| V8 | PL53B | 6 | LDQ55 | C (LVDS)* | PL61B | 6 | LDQ63 | C (LVDS)* |
| V4 | PL54A | 6 | LDQ55 | T | PL62A | 6 | LDQ63 | T |
| V3 | PL54B | 6 | LDQ55 | C | PL62B | 6 | LDQ63 | C |
| V2 | PL55A | 6 | LDQS55 | T (LVDS)* | PL63A | 6 | LDQS63 | T (LVDS)* |
| GNDIO | GNDIO6 | - | | | GNDIO6 | - | | |
| V1 | PL55B | 6 | LDQ55 | C (LVDS)* | PL63B | 6 | LDQ63 | C (LVDS)* |
| W7 | PL56A | 6 | LDQ55 | T | PL64A | 6 | LDQ63 | T |
| W5 | PL56B | 6 | LDQ55 | C | PL64B | 6 | LDQ63 | C |
| VCCIO | VCCIO6 | 6 | | | VCCIO6 | 6 | | |
| W2 | PL57A | 6 | LLM3_SPLLT_IN_A/LDQ55 | T (LVDS)* | PL65A | 6 | LLM4_SPLLT_IN_A/LDQ63 | T (LVDS)* |
| W1 | PL57B | 6 | LLM3_SPLLC_IN_A/LDQ55 | C (LVDS)* | PL65B | 6 | LLM4_SPLLC_IN_A/LDQ63 | C (LVDS)* |
| Y6 | PL58A | 6 | LLM3_SPLLT_FB_A/LDQ55 | T | PL66A | 6 | LLM4_SPLLT_FB_A/LDQ63 | T |
| W6 | PL58B | 6 | LLM3_SPLLC_FB_A/LDQ55 | C | PL66B | 6 | LLM4_SPLLC_FB_A/LDQ63 | C |
| GNDIO | GNDIO6 | - | | | GNDIO6 | - | | |
| Y1 | PL60A | 6 | LDQ64 | T (LVDS)* | PL68A | 6 | LDQ72 | T (LVDS)* |
| Y2 | PL60B | 6 | LDQ64 | C (LVDS)* | PL68B | 6 | LDQ72 | C (LVDS)* |
| Y7 | PL61A | 6 | LDQ64 | T | PL69A | 6 | LDQ72 | T |
| Y5 | PL61B | 6 | LDQ64 | C | PL69B | 6 | LDQ72 | C |
| VCCIO | VCCIO6 | 6 | | | VCCIO6 | 6 | | |
| W10 | PL62A | 6 | LDQ64 | T (LVDS)* | PL70A | 6 | LDQ72 | T (LVDS)* |
| Y8 | PL62B | 6 | LDQ64 | C (LVDS)* | PL70B | 6 | LDQ72 | C (LVDS)* |
| Y4 | PL63A | 6 | LDQ64 | T | PL71A | 6 | LDQ72 | T |
| Y3 | PL63B | 6 | LDQ64 | C | PL71B | 6 | LDQ72 | C |
| GNDIO | GNDIO6 | - | | | GNDIO6 | - | | |
| AA1 | PL64A | 6 | LDQS64 | T (LVDS)* | PL72A | 6 | LDQS72 | T (LVDS)* |
| AA2 | PL64B | 6 | LDQ64 | C (LVDS)* | PL72B | 6 | LDQ72 | C (LVDS)* |

## LatticeECP2 Standard Series Devices, Lead-Free Packaging

**Commercial**

| Part Number | I/Os | Voltage | Grade | Package | Pins | Temp. | LUTs (K) |
|---|---|---|---|---|---|---|---|
| LFE2-6E-5TN144C | 90 | 1.2V | -5 | Lead-Free TQFP | 144 | COM | 6 |
| LFE2-6E-6TN144C | 90 | 1.2V | -6 | Lead-Free TQFP | 144 | COM | 6 |
| LFE2-6E-7TN144C | 90 | 1.2V | -7 | Lead-Free TQFP | 144 | COM | 6 |
| LFE2-6E-5FN256C | 190 | 1.2V | -5 | Lead-Free fpBGA | 256 | COM | 6 |
| LFE2-6E-6FN256C | 190 | 1.2V | -6 | Lead-Free fpBGA | 256 | COM | 6 |
| LFE2-6E-7FN256C | 190 | 1.2V | -7 | Lead-Free fpBGA | 256 | COM | 6 |

| Part Number | I/Os | Voltage | Grade | Package | Pins | Temp. | LUTs (K) |
|---|---|---|---|---|---|---|---|
| LFE2-12E-5TN144C | 93 | 1.2V | -5 | Lead-Free TQFP | 144 | COM | 12 |
| LFE2-12E-6TN144C | 93 | 1.2V | -6 | Lead-Free TQFP | 144 | COM | 12 |
| LFE2-12E-7TN144C | 93 | 1.2V | -7 | Lead-Free TQFP | 144 | COM | 12 |
| LFE2-12E-5QN208C | 131 | 1.2V | -5 | Lead-Free PQFP | 208 | COM | 12 |
| LFE2-12E-6QN208C | 131 | 1.2V | -6 | Lead-Free PQFP | 208 | COM | 12 |
| LFE2-12E-7QN208C | 131 | 1.2V | -7 | Lead-Free PQFP | 208 | COM | 12 |
| LFE2-12E-5FN256C | 193 | 1.2V | -5 | Lead-Free fpBGA | 256 | COM | 12 |
| LFE2-12E-6FN256C | 193 | 1.2V | -6 | Lead-Free fpBGA | 256 | COM | 12 |
| LFE2-12E-7FN256C | 193 | 1.2V | -7 | Lead-Free fpBGA | 256 | COM | 12 |
| LFE2-12E-5FN484C | 297 | 1.2V | -5 | Lead-Free fpBGA | 484 | COM | 12 |
| LFE2-12E-6FN484C | 297 | 1.2V | -6 | Lead-Free fpBGA | 484 | COM | 12 |
| LFE2-12E-7FN484C | 297 | 1.2V | -7 | Lead-Free fpBGA | 484 | COM | 12 |

| Part Number | I/Os | Voltage | Grade | Package | Pins | Temp. | LUTs (K) |
|---|---|---|---|---|---|---|---|
| LFE2-20E-5QN208C | 131 | 1.2V | -5 | Lead-Free PQFP | 208 | COM | 20 |
| LFE2-20E-6QN208C | 131 | 1.2V | -6 | Lead-Free PQFP | 208 | COM | 20 |
| LFE2-20E-7QN208C | 131 | 1.2V | -7 | Lead-Free PQFP | 208 | COM | 20 |
| LFE2-20E-5FN256C | 193 | 1.2V | -5 | Lead-Free fpBGA | 256 | COM | 20 |
| LFE2-20E-6FN256C | 193 | 1.2V | -6 | Lead-Free fpBGA | 256 | COM | 20 |
| LFE2-20E-7FN256C | 193 | 1.2V | -7 | Lead-Free fpBGA | 256 | COM | 20 |
| LFE2-20E-5FN484C | 331 | 1.2V | -5 | Lead-Free fpBGA | 484 | COM | 20 |
| LFE2-20E-6FN484C | 331 | 1.2V | -6 | Lead-Free fpBGA | 484 | COM | 20 |
| LFE2-20E-7FN484C | 331 | 1.2V | -7 | Lead-Free fpBGA | 484 | COM | 20 |
| LFE2-20E-5FN672C | 402 | 1.2V | -5 | Lead-Free fpBGA | 672 | COM | 20 |
| LFE2-20E-6FN672C | 402 | 1.2V | -6 | Lead-Free fpBGA | 672 | COM | 20 |
| LFE2-20E-7FN672C | 402 | 1.2V | -7 | Lead-Free fpBGA | 672 | COM | 20 |

| Date | Version | Section | Change Summary |
|---|---|---|---|
| August 2006 (cont.) | 01.1 (cont.) | Pinout Information (cont.) | Added Information on: Available Device Resources per Packaged Device table. |
| | | Ordering Information | Updated ordering part number table to include ECP2-12. |
| | | | Updated topside mark drawing. |
| September 2006 | 02.0 | Multiple | Added information regarding LatticeECP2M support throughout. |
| September 2006 | 02.1 | DC and Switching Characteristics | Added Receiver Total Jitter Tolerance Specification table. |
| | | | Removed power-up requirements for proper configuration footnote in Recommended Operating Conditions table. |
| December 2006 | 02.2 | Introduction | LatticeECP2M Selection Guide table has been updated. |
| | | Architecture | Figure 2-16. Per Region Secondary Clock Selection has been updated. |
| | | | Figure 2-39. Simplified Channel Block Diagram for SERDES and PCS has been updated. |
| | | DC and Switching | Footnotes have been added to Recommended Operating Conditions. |
| | | | DC Electrical Characteristics table has been updated. |
| | | | Supply Current (Standby) tables have been updated. |
| | | | Initialization Supply Current table have been updated. |
| | | | Updated timing numbers to include LFE2-12E (rev A 0.08). |
| | | Pinout Information | Updated to include the entire ECP2 device information as well as 256-fpBGA and 484-fpBGA pin information for the ECP2M35E. |
| | | Ordering Information | Updated to include the entire ECP2 and ECP2M device ordering information. |
| February 2007 | 02.3 | Architecture | Updated EBR Asynchronous Reset section. |
| March 2007 | 02.4 | DC and Switching Characteristics | Power-sequencing footnotes have been added to the Recommended Operating Conditions. DDR2 performance has been updated to 266MHz. |
| March 2007 | 02.5 | Introduction | Added “Security Series” to the LatticeECP2 and LatticeECP2M families. |
| | | Architecture | Enhanced Configuration Option section updated. |
| | | DC and Switching | Recommended Operating Conditions table - footnote 4 updated. |
| | | Ordering Information | “Security Series” ordering part numbers added. |
| April 2007 | 02.6 | Introduction | LatticeECP2M family table has been updated for user I/O counts. |
| | | Ordering Information | LatticeECP2M family ordering part number section has been updated to add 1152-fpBGA package for the ECP2M70 and ECP2M100. |
| July 2007 | 02.7 | Architecture | Updated text in Ripple Mode section. |
| | | DC and Switching | ECP2/M Supply Current information has been updated.<br>Typical Building Block Function Performance, External Switching Characteristics, Internal Switching Characteristics, Family Timing Adders, sysCLOCK GPLL Timing, sysCLOCK SPLL Timing, DLL Timing and sysCONFIG Port Timing Specifications have been updated (timing rev. A 0.10).<br>SERDES timing information has been updated.<br>PCI Express timing information has been updated. |
| | | Pinout Information | Added LatticeECP2M20 pinout information. |
| August 2007 | 02.8 | Introduction | 1156-fpBGA package option has been removed from the LatticeECP2M family. |
| | | Architecture | Table 2-16. Selectable Master Clock (CCLK) Frequencies During Configuration table has been updated. |
| | | DC and Switching | Supply Current (Standby) table has been updated. |
| | | | DSP Function timing has been updated. |