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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	4MHz
Connectivity	UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	16
Program Memory Size	1.75KB (1K x 14)
Program Memory Type	FLASH
EEPROM Size	128 x 8
RAM Size	224 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SSOP (0.209", 5.30mm Width)
Supplier Device Package	20-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16f627-04e-ss

NOTES:

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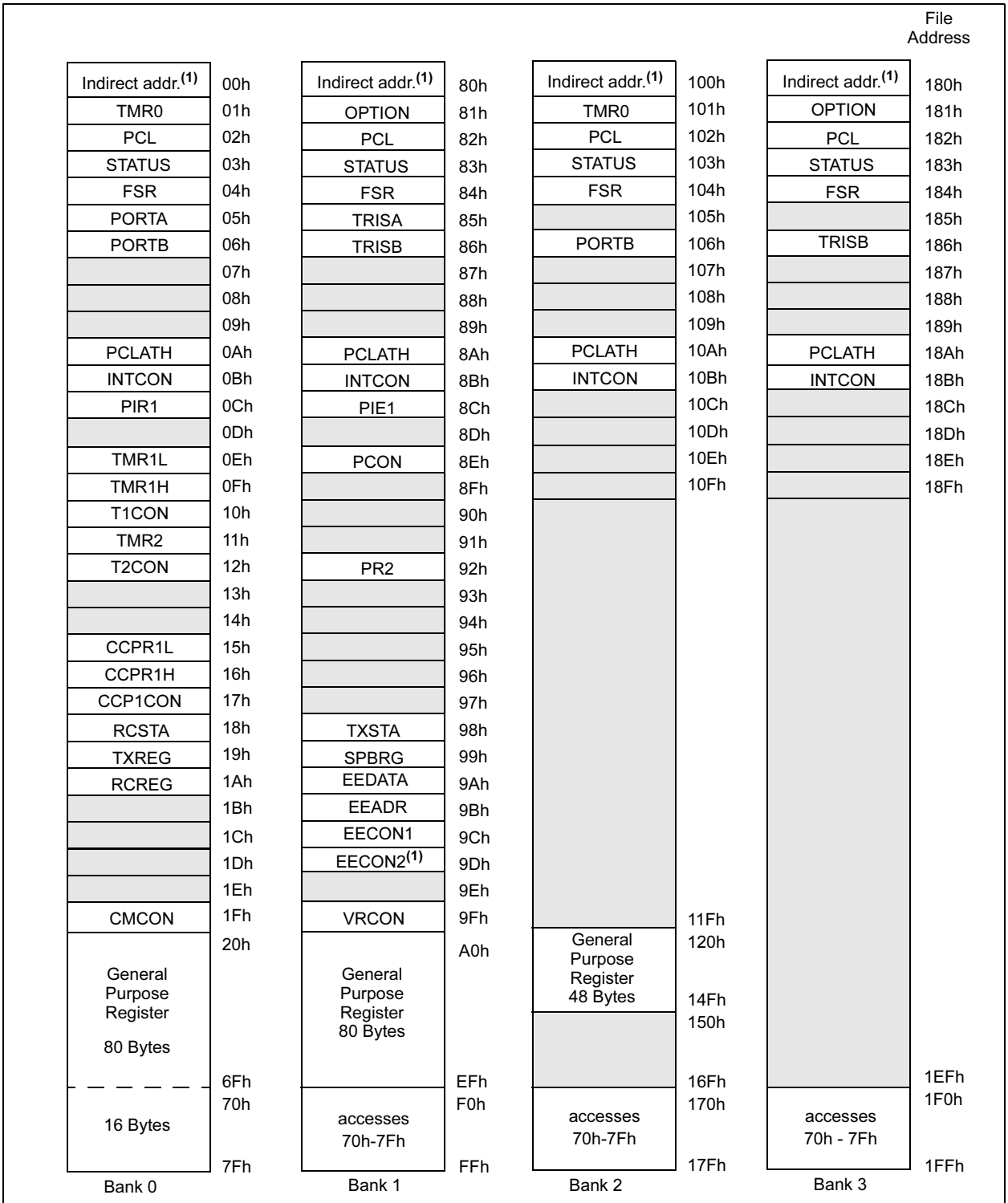
FIGURE 3-2: DATA MEMORY MAP OF THE PIC16F627 AND PIC16F628



Unimplemented data memory locations, read as '0'.

Note 1: Not a physical register.

TABLE 3-4: SPECIAL FUNCTION REGISTERS SUMMARY BANK 3

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR Reset(1)	Details on Page
Bank 3											
180h	INDF	Addressing this location uses contents of FSR to address data memory (not a physical register)								xxxx xxxx	25
181h	OPTION	$\overline{RBPU}$	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	20
182h	PCL	Program Counter's (PC) Least Significant Byte								0000 0000	25
183h	STATUS	IRP	RP1	RP0	$\overline{TO}$	$\overline{PD}$	Z	DC	C	0001 1xxx	19
184h	FSR	Indirect data memory address pointer								xxxx xxxx	25
185h	—	Unimplemented								—	—
186h	TRISB	TRISB7	TRISB6	TRISB5	TRISB4	TRISB3	TRISB2	TRISB1	TRISB0	1111 1111	34
187h	—	Unimplemented								—	—
188h	—	Unimplemented								—	—
189h	—	Unimplemented								—	—
18Ah	PCLATH	—	—	—	Write buffer for upper 5 bits of program counter					---0 0000	25
18Bh	INTCON	GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	21
18Ch	—	Unimplemented								—	—
18Dh	—	Unimplemented								—	—
18Eh	—	Unimplemented								—	—
18Fh	—	Unimplemented								—	—
190h	—	Unimplemented								—	—
191h	—	Unimplemented								—	—
192h	—	Unimplemented								—	—
193h	—	Unimplemented								—	—
194h	—	Unimplemented								—	—
195h	—	Unimplemented								—	—
196h	—	Unimplemented								—	—
197h	—	Unimplemented								—	—
198h	—	Unimplemented								—	—
199h	—	Unimplemented								—	—
19Ah	—	Unimplemented								—	—
19Bh	—	Unimplemented								—	—
19Ch	—	Unimplemented								—	—
19Dh	—	Unimplemented								—	—
19Eh	—	Unimplemented								—	—
19Fh	—	Unimplemented								—	—

Legend: — = Unimplemented locations read as '0', u = unchanged, x = unknown, q = value depends on condition, shaded = unimplemented

Note 1: For the Initialization Condition for Registers Tables, refer to Table 14-7 and Table 14-8 on page 98.

NOTES:

FIGURE 5-15: BLOCK DIAGRAM OF THE RB7/T1OSI PIN

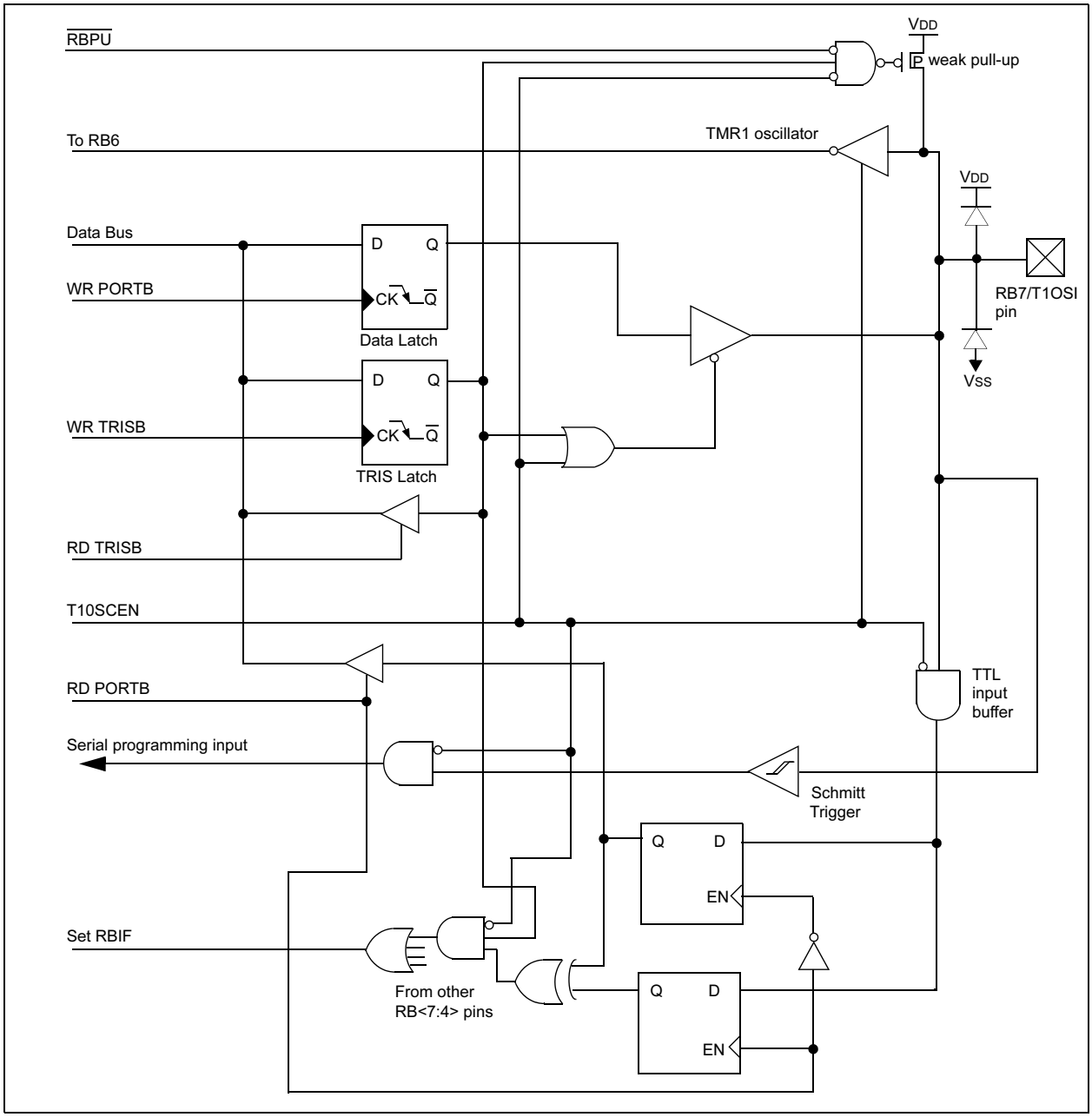
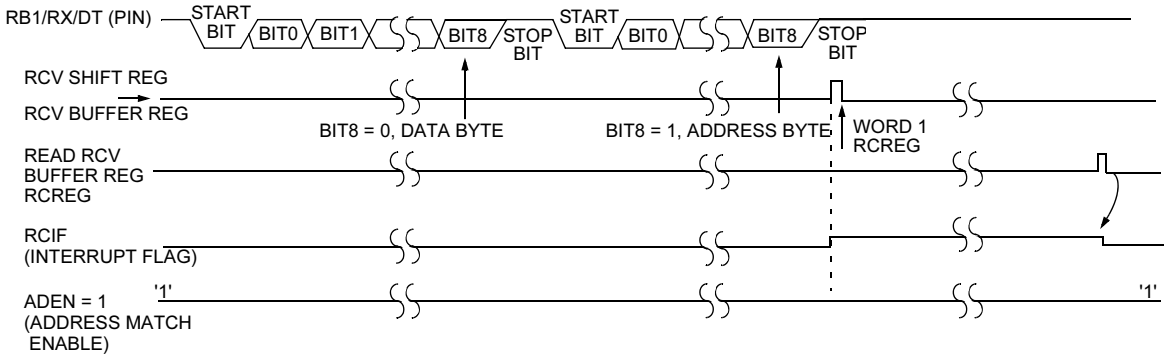
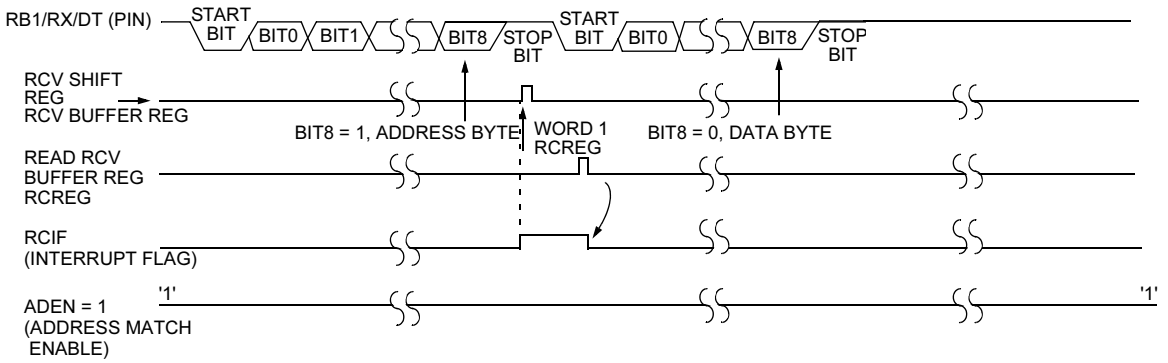


FIGURE 12-9: ASYNCHRONOUS RECEPTION WITH ADDRESS DETECT



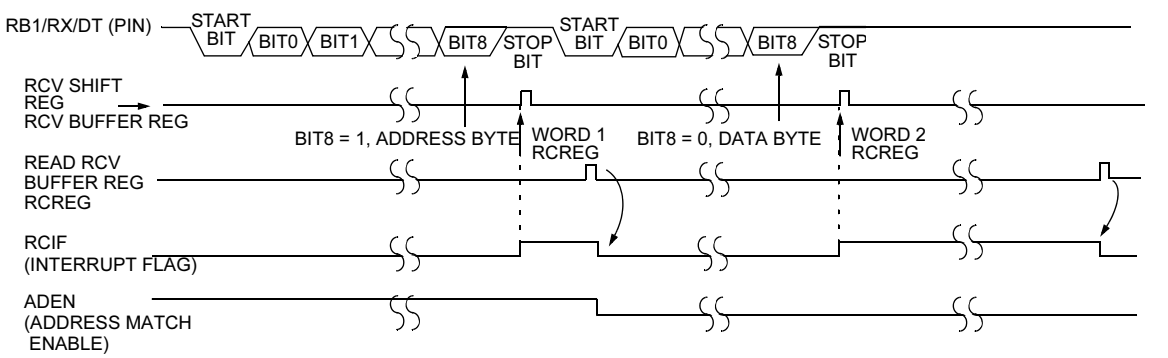
Note 1: This timing diagram shows a data byte followed by an address byte. The data byte is not read into the RCREG (Receive Buffer) because ADEN = 1 and Bit 8 = 0.

FIGURE 12-10: ASYNCHRONOUS RECEPTION WITH ADDRESS BYTE FIRST



Note 1: This timing diagram shows an address byte followed by an data byte. The data byte is not read into the RCREG (receive buffer) because ADEN was not updated (still = 1) and Bit 8 = 0.

FIGURE 12-11: ASYNCHRONOUS RECEPTION WITH ADDRESS BYTE FIRST FOLLOWED BY VALID DATA BYTE



Note 1: This timing diagram shows an address byte followed by an data byte. The data byte is read into the RCREG (Receive Buffer) because ADEN was updated after an address match, and was cleared to a '0', so the contents of the Receive Shift Register (RSR) are read into the Receive Buffer regardless of the value of Bit 8.

13.0 DATA EEPROM MEMORY

The EEPROM data memory is readable and writable during normal operation (full V_{DD} range). This memory is not directly mapped in the register file space. Instead it is indirectly addressed through the Special Function Registers (SFRs). There are four SFRs used to read and write this memory. These registers are:

- EECON1
- EECON2 (Not a physically implemented register)
- EEDATA
- EEADR

EEDATA holds the 8-bit data for read/write, and EEADR holds the address of the EEPROM location being accessed. PIC16F62X devices have 128 bytes of data EEPROM with an address range from 0h to 7Fh.

The EEPROM data memory allows byte read and write. A byte write automatically erases the location and writes the new data (erase before write). The EEPROM data memory is rated for high erase/write cycles. The write time is controlled by an on-chip timer. The write-time will vary with voltage and temperature as well as from chip to chip. Please refer to AC specifications for exact limits.

When the device is code protected, the CPU may continue to read and write the data EEPROM memory. The device programmer can no longer access this memory.

Additional information on the Data EEPROM is available in the PICmicro™ Mid-Range Reference Manual, (DS33023).

REGISTER 13-1: EEADR REGISTER (ADDRESS: 9Bh)

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reserved	EADR6	EADR5	EADR4	EADR3	EADR2	EADR1	EADR0
bit 7							bit 0

bit 7 **Unimplemented Address**: Must be set to ‘0’

bit 6-0 **EEADR**: Specifies one of 128 locations of EEPROM Read/Write Operation

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	’1’ = Bit is set	’0’ = Bit is cleared	x = Bit is unknown

13.1 EEADR

The EEADR register can address up to a maximum of 256 bytes of data EEPROM. Only the first 128 bytes of data EEPROM are implemented and only seven of the eight bits in the register (EEADR<6:0>) are required.

The upper bit is address decoded. This means that this bit should always be '0' to ensure that the address is in the 128 byte memory space.

13.2 EECON1 AND EECON2 REGISTERS

EECON1 is the control register with five low order bits physically implemented. The upper-three bits are non-existent and read as '0's.

Control bits RD and WR initiate read and write, respectively. These bits cannot be cleared, only set, in software. They are cleared in hardware at completion of the read or write operation. The inability to clear the WR bit in software prevents the accidental, premature termination of a write operation.

The WREN bit, when set, will allow a write operation. On power-up, the WREN bit is clear. The WRERR bit is set when a write operation is interrupted by a $\overline{\text{MCLR}}$ Reset or a WDT Timeout Reset during normal operation. In these situations, following RESET, the user can check the WRERR bit and rewrite the location. The data and address will be unchanged in the EEDATA and EEADR registers.

Interrupt flag bit EEIF in the PIR1 register is set when write is complete. This bit must be cleared in software.

EECON2 is not a physical register. Reading EECON2 will read all '0's. The EECON2 register is used exclusively in the Data EEPROM write sequence.

FIGURE 14-2: EXTERNAL PARALLEL RESONANT CRYSTAL OSCILLATOR CIRCUIT

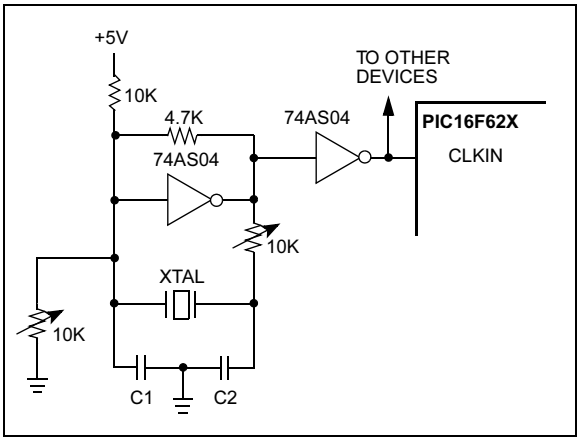
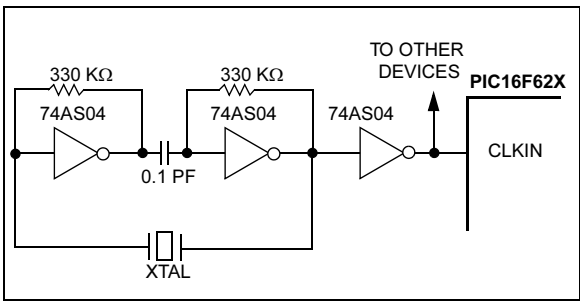


Figure 14-3 shows a series resonant oscillator circuit. This circuit is also designed to use the fundamental frequency of the crystal. The inverter performs a 180° phase shift in a series resonant oscillator circuit. The 330 kΩ resistors provide the negative feedback to bias the inverters in their linear region.

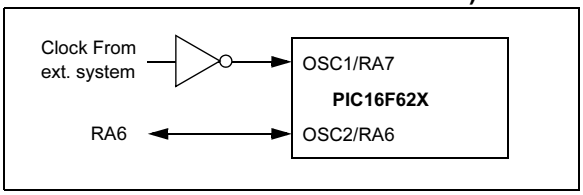
FIGURE 14-3: EXTERNAL SERIES RESONANT CRYSTAL OSCILLATOR CIRCUIT



14.2.4 EXTERNAL CLOCK IN

For applications, where a clock is already available elsewhere, users may directly drive the PIC16F62X provided that this external clock source meets the AC/DC timing requirements listed in Section 17.4. Figure 14-4 shows how an external clock circuit should be configured.

FIGURE 14-4: EXTERNAL CLOCK INPUT OPERATION (EC, HS, XT OR LP OSC CONFIGURATION)



14.2.5 ER OSCILLATOR

For timing insensitive applications, the ER (External Resistor) Clock mode offers additional cost savings. Only one external component, a resistor to VSS, is needed to set the operating frequency of the internal oscillator. The resistor draws a DC bias current which controls the oscillation frequency. In addition to the resistance value, the oscillator frequency will vary from unit to unit, and as a function of supply voltage and temperature. Since the controlling parameter is a DC current and not a capacitance, the particular package type and lead frame will not have a significant effect on the resultant frequency.

Figure 14-5 shows how the controlling resistor is connected to the PIC16F62X. For REXT values below 10k, the oscillator operation becomes sensitive to temperature. For very high REXT values (e.g., 1M), the oscillator becomes sensitive to leakage and may stop completely. Thus, we recommend keeping REXT between 10k and 1M.

FIGURE 14-5: EXTERNAL RESISTOR

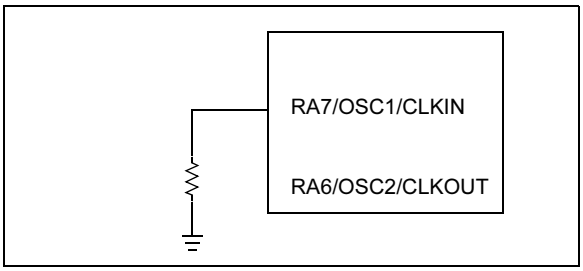


Table 14-3 shows the relationship between the resistance value and the operating frequency.

TABLE 14-3: RESISTANCE AND FREQUENCY RELATIONSHIP

Resistance	Frequency
0	10.4 MHz
1K	10 MHz
10K	7.4 MHz
20K	5.3 MHz
47K	3 MHz
100K	1.6 MHz
220K	800 kHz
470K	300 kHz
1M	200 kHz

The ER Oscillator mode has two options that control the unused OSC2 pin. The first allows it to be used as a general purpose I/O port. The other configures the pin as an output providing the FOSC signal (internal clock divided by 4) for test or external synchronization purposes.

14.5.5 TIMEOUT SEQUENCE

On power-up the timeout sequence is as follows: First PWRT timeout is invoked after POR has expired. Then OST is activated. The total timeout will vary based on oscillator configuration and PWRTE bit status. For example, in ER mode with PWRTE bit erased (PWRT disabled), there will be no timeout at all. Figure 14-8, Figure 14-9 and Figure 14-10 depict timeout sequences.

Since the timeouts occur from the POR pulse, if MCLR is kept low long enough, the timeouts will expire. Then bringing MCLR high will begin execution immediately (see Figure 14-9). This is useful for testing purposes or to synchronize more than one PIC16F62X device operating in parallel.

Table 14-7 shows the RESET conditions for some special registers, while Table 14-8 shows the RESET conditions for all the registers.

14.5.6 POWER CONTROL (PCON) STATUS REGISTER

The Power Control/STATUS register, PCON (address 8Eh) has two bits.

Bit0 is BOD (Brown-out). BOD is unknown on Power-on Reset. It must then be set by the user and checked on subsequent RESETS to see if BOD = 0 indicating that a brown-out has occurred. The BOD STATUS bit is a don't care and is not necessarily predictable if the brown-out circuit is disabled (by setting BODEN bit = 0 in the Configuration word).

Bit1 is POR (Power-on Reset). It is a '0' on Power-on Reset and unaffected otherwise. The user must write a '1' to this bit following a Power-on Reset. On a subsequent RESET if POR is '0', it will indicate that a Power-on Reset must have occurred (V_{DD} may have gone too low).

TABLE 14-4: TIMEOUT IN VARIOUS SITUATIONS

Oscillator Configuration	Power-up		Brown-out Detect Reset	Wake-up from SLEEP
	PWRTE = 0	PWRTE = 1		
XT, HS, LP	72 ms + 1024 TOSC	1024 TOSC	72 ms + 1024 TOSC	1024 TOSC
ER, INTRC, EC	72 ms	—	72 ms	—

TABLE 14-5: STATUS/PCON BITS AND THEIR SIGNIFICANCE

POR	BOD	TO	PD	
0	X	1	1	Power-on Reset
0	X	0	X	Illegal, TO is set on POR
0	X	X	0	Illegal, PD is set on POR
1	0	X	X	Brown-out Detect Reset
1	1	0	u	WDT Reset
1	1	0	0	WDT Wake-up
1	1	u	u	MCLR Reset during normal operation
1	1	1	0	MCLR Reset during SLEEP

Legend: u = unchanged, x = unknown.

TABLE 14-6: SUMMARY OF REGISTERS ASSOCIATED WITH BROWN-OUT

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR Reset	Value on all other RESETS(1)
03h	STATUS	IRP	RP1	RPO	TO	PD	Z	DC	C	0001 1xxx	000q quuu
8Eh	PCON	—	—	—	—	OSCF	Reset	POR	BOD	---- 1-0x	---- u-uq

Note 1: Other (non Power-up) Resets include MCLR Reset, Brown-out Detect Reset and Watchdog Timer Reset during normal operation.

TABLE 14-7: INITIALIZATION CONDITION FOR SPECIAL REGISTERS

Condition	Program Counter	STATUS Register	PCON Register
Power-on Reset	000h	0001 1xxx	---- 1-0x
$\overline{MCLR}$ Reset during normal operation	000h	000u uuuu	---- 1-uu
$\overline{MCLR}$ Reset during SLEEP	000h	0001 0uuu	---- 1-uu
WDT Reset	000h	0000 uuuu	---- 1-uu
WDT Wake-up	PC + 1	uuu0 0uuu	---- u-uu
Brown-out Detect Reset	000h	000x xuuu	---- 1-u0
Interrupt Wake-up from SLEEP	PC + 1(1)	uuu1 0uuu	---- u-uu

Legend: u = unchanged, x = unknown, - = unimplemented bit, reads as '0'.

Note 1: When the wake-up is due to an interrupt and global enable bit, GIE is set, the PC is loaded with the interrupt vector (0004h) after execution of PC+1.

TABLE 14-8: INITIALIZATION CONDITION FOR REGISTERS

Register	Address	Power-on Reset	• $\overline{MCLR}$ Reset during normal operation • $\overline{MCLR}$ Reset during SLEEP • WDT Reset • Brown-out Detect Reset (1)	• Wake-up from SLEEP through interrupt • Wake-up from SLEEP through WDT timeout
W	—	xxxx xxxx	uuuu uuuu	uuuu uuuu
INDF	00h	—	—	—
TMR0	01h	xxxx xxxx	uuuu uuuu	uuuu uuuu
PCL	02h	0000 0000	0000 0000	PC + 1(3)
STATUS	03h	0001 1xxx	000q quuu(4)	uuuq quuu(4)
FSR	04h	xxxx xxxx	uuuu uuuu	uuuu uuuu
PORTA	05h	xxxx 0000	xxxx u000	xxxx 0000
PORTB	06h	xxxx xxxx	uuuu uuuu	uuuu uuuu
T1CON	10h	--00 0000	--uu uuuu	--uu uuuu
T2CON	12h	-000 0000	-000 0000	-uuu uuuu
CCP1CON	17h	--00 0000	--00 0000	--uu uuuu
RCSTA	18h	0000 -00x	0000 -00x	uuuu -uuu
CMCON	1Fh	0000 0000	0000 0000	uu-- uuuu
PCLATH	0Ah	---0 0000	---0 0000	---u uuuu
INTCON	0Bh	0000 000x	0000 000u	uuuu uqqq(2)
PIR1	0Ch	0000 -000	0000 -000	-q-- ----(2,5)
OPTION	81h	1111 1111	1111 1111	uuuu uuuu
TRISA	85h	11-1 1111	11-- 1111	uu-u uuuu
TRISB	86h	1111 1111	1111 1111	uuuu uuuu
PIE1	8Ch	0000 -000	0000 -000	uuuu -uuu
PCON	8Eh	---- 1-0x	---- 1-uq(1,6)	---- --uu
TXSTA	98h	0000 -010	0000 -010	uuuu -uuu
EECON1	9Ch	---- x000	---- q000	---- uuuu
VRCON	9Fh	000- 0000	000- 0000	uuu- uuuu

Legend: u = unchanged, x = unknown, - = unimplemented bit, reads as '0', q = value depends on condition.

Note 1: If VDD goes too low, Power-on Reset will be activated and registers will be affected differently.
2: One or more bits in INTCON, PIR1 and/or PIR2 will be affected (to cause wake-up).
3: When the wake-up is due to an interrupt and the GIE bit is set, the PC is loaded with the interrupt vector (0004h).
4: See Table 14-7 for RESET value for specific condition.
5: If wake-up was due to comparator input changing, then Bit 6 = 1. All other interrupts generating a wake-up will cause Bit 6 = u.
6: If RESET was due to brown-out, then Bit 0 = 0. All other RESETS will cause Bit 0 = u.

CLRW **Clear W**

Syntax: [*label*] CLRW

Operands: None

Operation: 00h → (W)
1 → Z

Status Affected: Z

Encoding:

00	0001	0000	0011

Description: W register is cleared. Zero bit (Z) is set.

Words: 1

Cycles: 1

Example
```
CLRW
```
Before Instruction
W = 0x5A
After Instruction
W = 0x00
Z = 1

CLRWDT **Clear Watchdog Timer**

Syntax: [*label*] CLRWDT

Operands: None

Operation: 00h → WDT
0 → WDT prescaler,
1 → $\overline{TO}$
1 → $\overline{PD}$

Status Affected: $\overline{TO}$, $\overline{PD}$

Encoding:

00	0000	0110	0100

Description: CLRWDT instruction resets the Watchdog Timer. It also resets the prescaler of the WDT. STATUS bits $\overline{TO}$ and $\overline{PD}$ are set.

Words: 1

Cycles: 1

Example
```
CLRWDT
```
Before Instruction
WDT counter = ?
After Instruction
WDT counter = 0x00
WDT prescaler = 0
$\overline{TO}$ = 1
$\overline{PD}$ = 1

COMF **Complement f**

Syntax: [*label*] COMF f,d

Operands: 0 ≤ f ≤ 127
d ∈ [0,1]

Operation: ($\bar{f}$) → (dest)

Status Affected: Z

Encoding:

00	1001	dfff	ffff

Description: The contents of register 'f' are complemented. If 'd' is 0 the result is stored in W. If 'd' is 1 the result is stored back in register 'f'.

Words: 1

Cycles: 1

Example
```
COMF    REG1, 0
```
Before Instruction
REG1 = 0x13
After Instruction
REG1 = 0x13
W = 0xEC

DECF **Decrement f**

Syntax: [*label*] DECF f,d

Operands: 0 ≤ f ≤ 127
d ∈ [0,1]

Operation: (f) - 1 → (dest)

Status Affected: Z

Encoding:

00	0011	dfff	ffff

Description: Decrement register 'f'. If 'd' is 0 the result is stored in the W register. If 'd' is 1 the result is stored back in register 'f'.

Words: 1

Cycles: 1

Example
```
DECF    CNT, 1
```
Before Instruction
CNT = 0x01
Z = 0
After Instruction
CNT = 0x00
Z = 1

IORLW **Inclusive OR Literal with W**

Syntax: [*label*] IORLW k

Operands: $0 \le k \le 255$

Operation: (W) .OR. k → (W)

Status Affected: Z

Encoding:

11	1000	kkkk	kkkk

Description: The contents of the W register is OR'ed with the eight bit literal 'k'. The result is placed in the W register.

Words: 1

Cycles: 1

Example
```
IORLW   0x35
```
Before Instruction
W = 0x9A
After Instruction
W = 0xBF
Z = 0

IORWF **Inclusive OR W with f**

Syntax: [*label*] IORWF f,d

Operands: $0 \le f \le 127$
$d \in [0,1]$

Operation: (W) .OR. (f) → (dest)

Status Affected: Z

Encoding:

00	0100	dfff	ffff

Description: Inclusive OR the W register with register 'f'. If 'd' is 0 the result is placed in the W register. If 'd' is 1 the result is placed back in register 'f'.

Words: 1

Cycles: 1

Example
```
IORWF   REG1, 0
```
Before Instruction
REG1 = 0x13
W = 0x91
After Instruction
REG1 = 0x13
W = 0x93
Z = 1

MOVLW **Move Literal to W**

Syntax: [*label*] MOVLW k

Operands: $0 \le k \le 255$

Operation: k → (W)

Status Affected: None

Encoding:

11	00xx	kkkk	kkkk

Description: The eight bit literal 'k' is loaded into W register. The don't cares will assemble as 0's.

Words: 1

Cycles: 1

Example
```
MOVLW   0x5A
```
After Instruction
W = 0x5A

MOVF **Move f**

Syntax: [*label*] MOVF f,d

Operands: $0 \le f \le 127$
$d \in [0,1]$

Operation: (f) → (dest)

Status Affected: Z

Encoding:

00	1000	dfff	ffff

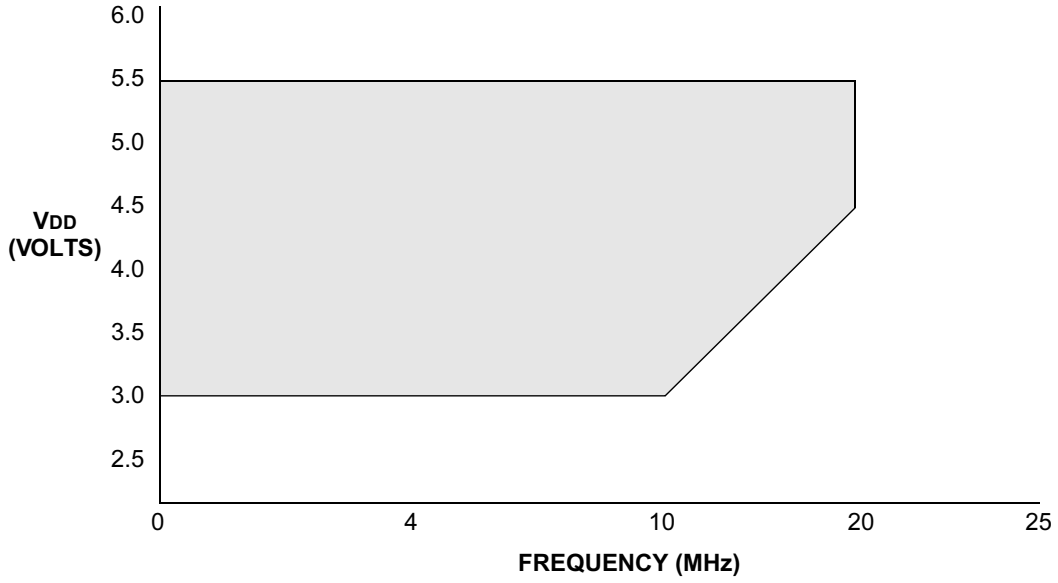
Description: The contents of register f is moved to a destination dependent upon the status of d. If d = 0, destination is W register. If d = 1, the destination is file register f itself. d = 1 is useful to test a file register since status flag Z is affected.

Words: 1

Cycles: 1

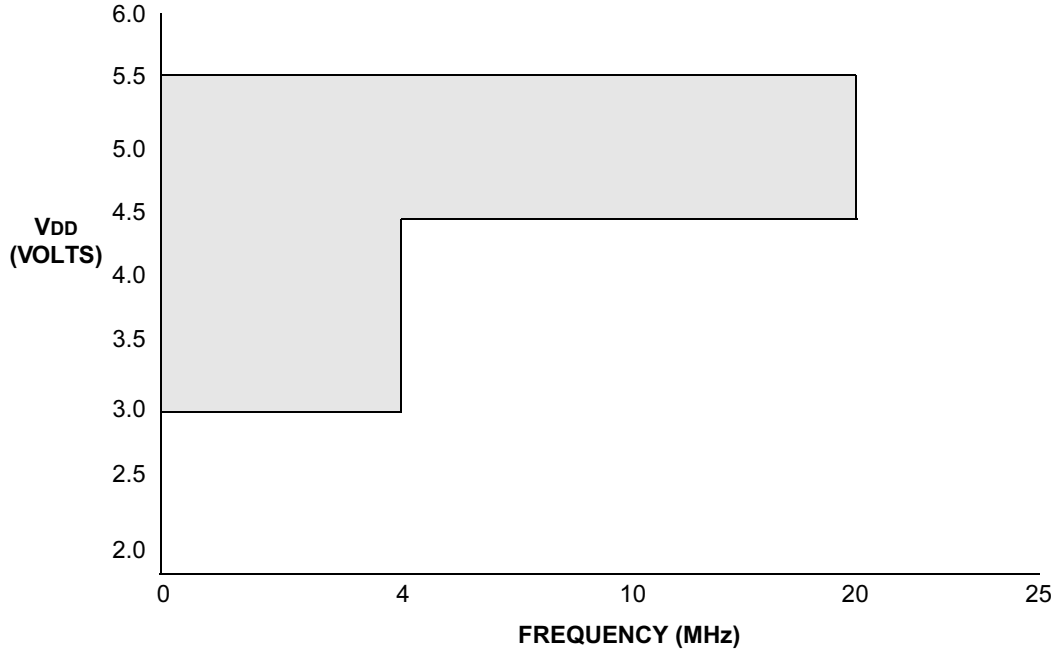
Example
```
MOVF    REG1, 0
```
After Instruction
W = value in REG1 register
Z = 1

FIGURE 17-1: PIC16F62X VOLTAGE-FREQUENCY GRAPH, 0°C ≤ TA ≤ +70°C



Note 1: The shaded region indicates the permissible combinations of voltage and frequency.

FIGURE 17-2: PIC16F62X VOLTAGE-FREQUENCY GRAPH, -40°C ≤ TA < 0°C, +70°C < TA ≤ 85°C



Note 1: The shaded region indicates the permissible combinations of voltage and frequency.

TABLE 17-1: COMPARATOR SPECIFICATIONS

	Operating Conditions: 3.0V < VDD <5.5V, -40°C < TA < +125°C, unless otherwise stated.						
Param No.	**Characteristics**	**Sym**	**Min**	**Typ**	**Max**	**Units**	**Comments**
D300	Input offset voltage	VIOFF	—	±5.0	±10	mV	
D301*	Input Common mode voltage	VICM	0	—	VDD - 1.5	V	
D302*	Common Mode Rejection Ratio	CMRR	55	—	—	db	
300* 300A	Response Time(1)	TRESP	—	150	400 600	ns ns	16F62X 16LF62X
301	Comparator Mode Change to Output Valid*	TMC2OV	—	—	10	µs	

* These parameters are characterized but not tested.

Note 1: Response time measured with one comparator input at (VDD - 1.5)/2 while the other input transitions from VSS to VDD.

TABLE 17-2: VOLTAGE REFERENCE SPECIFICATIONS

	Operating Conditions: 3.0V < VDD < 5.5V, -40°C < TA < +125°C, unless otherwise stated.						
Spec No.	**Characteristics**	**Sym**	**Min**	**Typ**	**Max**	**Units**	**Comments**
D310	Resolution	VRES	VDD/24	—	VDD/32	LSb	
D311	Absolute Accuracy	VRaa	— —	— —	1/4 1/2	LSb LSb	Low Range (VRR = 1) High Range (VRR = 0)
D312*	Unit Resistor Value (R)	VRur	—	2k	—	Ω	
310*	Settling Time(1)	Tset	—	—	10	µs	

* These parameters are characterized but not tested.

Note 1: Settling time measured while VRR = 1 and VR<3:0> transitions from `0000` to `1111`.

TABLE 17-8: CAPTURE/COMPARE/PWM REQUIREMENTS

Param No.	Sym	Characteristic			Min	Typ†	Max	Units	Conditions
50*	TccL	CCP input low time	No Prescaler		0.5TCY + 20	—	—	ns	
			With Prescaler	16F62X	10	—	—	ns	
				16LF62X	20	—	—	ns	
51*	TccH	CCP input high time	No Prescaler		0.5TCY + 20	—	—	ns	
			With Prescaler	16F62X	10	—	—	ns	
				16LF62X	20	—	—	ns	
52*	TccP	CCP input period			$\frac{3T_{CY} + 40}{N}$	—	—	ns	N = prescale value (1,4 or 16)
53*	TccR	CCP output rise time		16F62X		10	25	ns	
				16LF62X		25	45	ns	
54*	TccF	CCP output fall time		16F62X		10	25	ns	
				16LF62X		25	45	ns	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

FIGURE 17-12: TIMER0 CLOCK TIMING

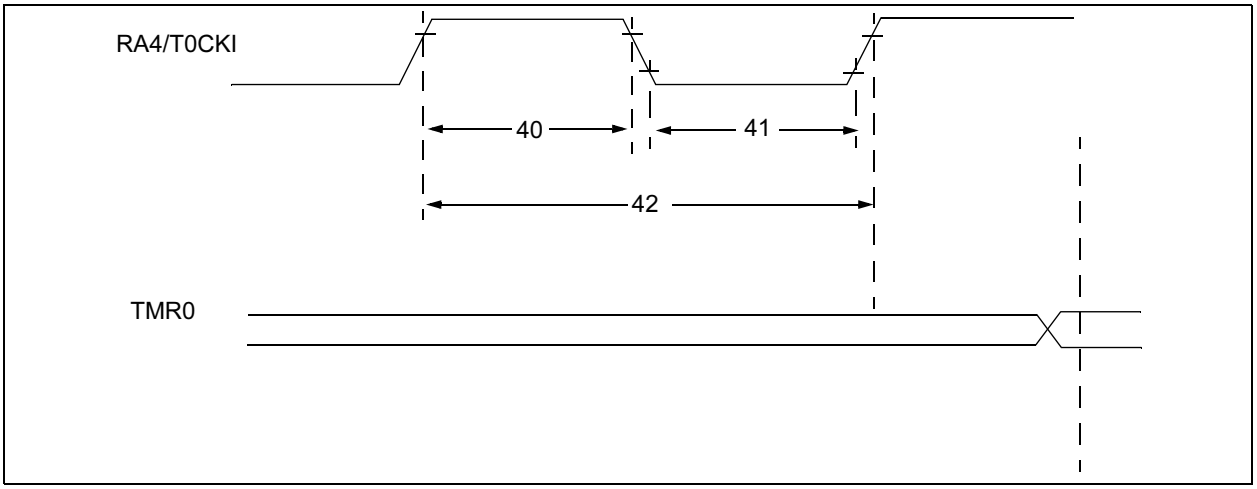


TABLE 17-9: TIMER0 CLOCK REQUIREMENTS

Param No.	Sym	Characteristic		Min	Typ†	Max	Units	Conditions
40	Tt0H	T0CKI High Pulse Width	No Prescaler	0.5 TCY + 20*	—	—	ns	
			With Prescaler	10*	—	—	ns	
41	Tt0L	T0CKI Low Pulse Width	No Prescaler	0.5 TCY + 20*	—	—	ns	
			With Prescaler	10*	—	—	ns	
42	Tt0P	T0CKI Period		$\frac{T_{CY} + 40}{N}$*	—	—	ns	N = prescale value (1, 2, 4, ..., 256)

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note: The graphs and tables provided in this section are for design guidance and are not tested.

FIGURE 18-12: ΔITMR1OSC VS VDD OVER TEMP (0C to +70°C) SLEEP MODE, TIMER1 OSCILLATOR, 32 kHz XTAL

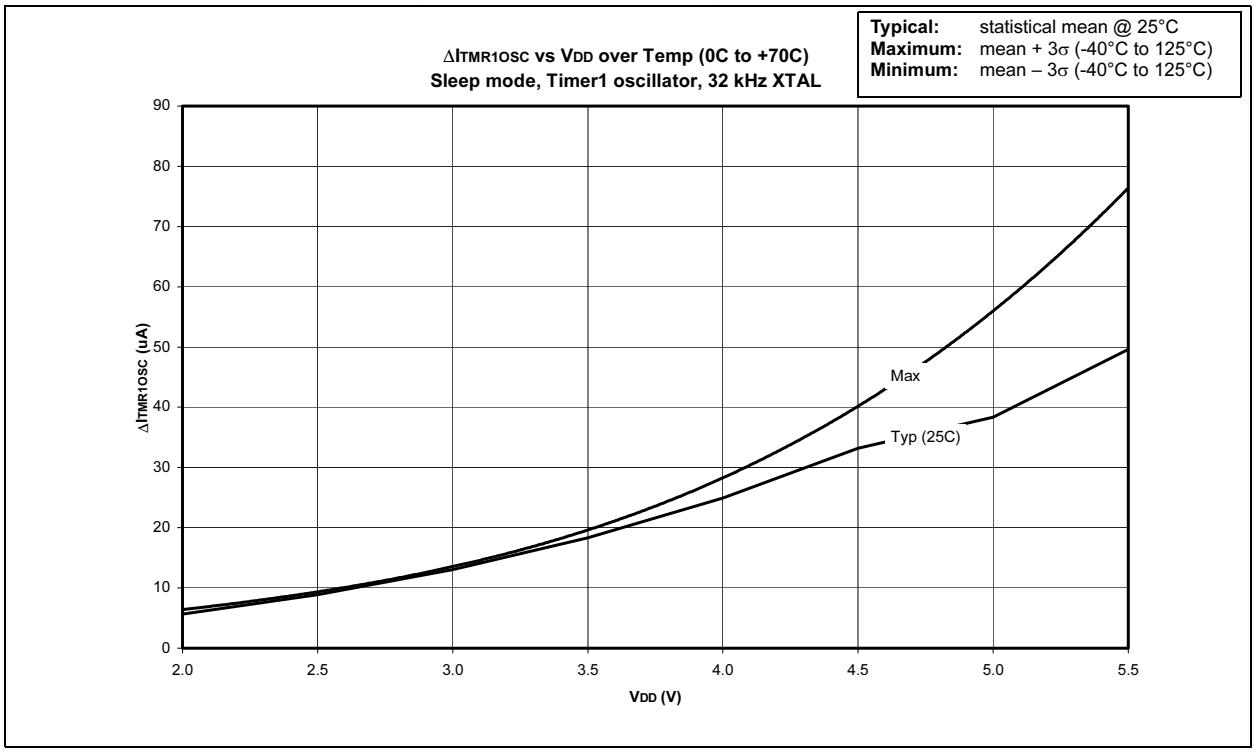
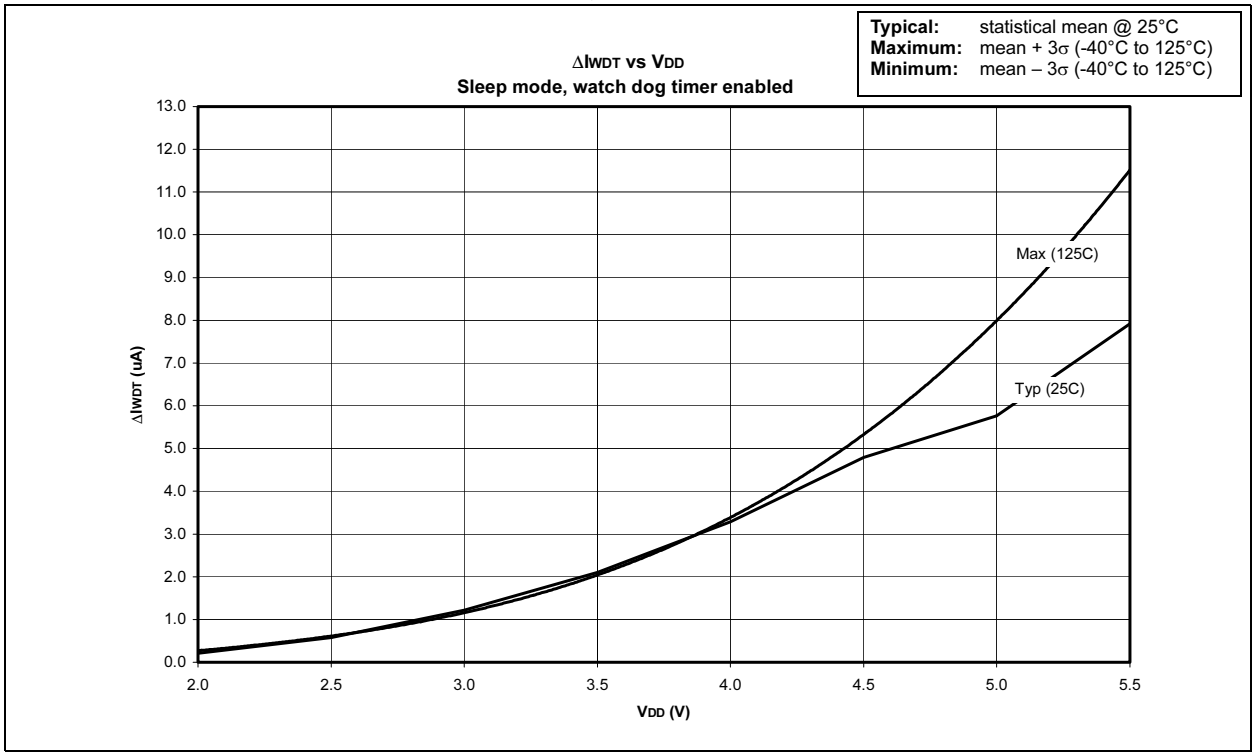


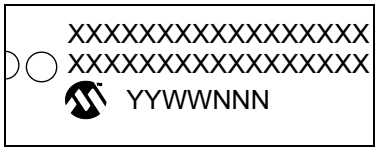
FIGURE 18-13: ΔIWDT VS VDD SLEEP MODE, WATCH DOG TIMER ENABLED



19.0 PACKAGING INFORMATION

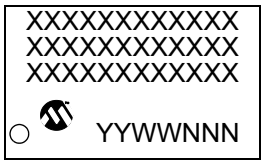
19.1 Package Marking Information

18-LEAD PDIP

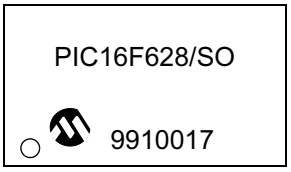


EXAMPLE

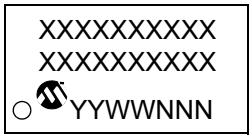
18-LEAD SOIC (.300")



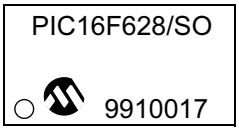
EXAMPLE



20-LEAD SSOP



EXAMPLE

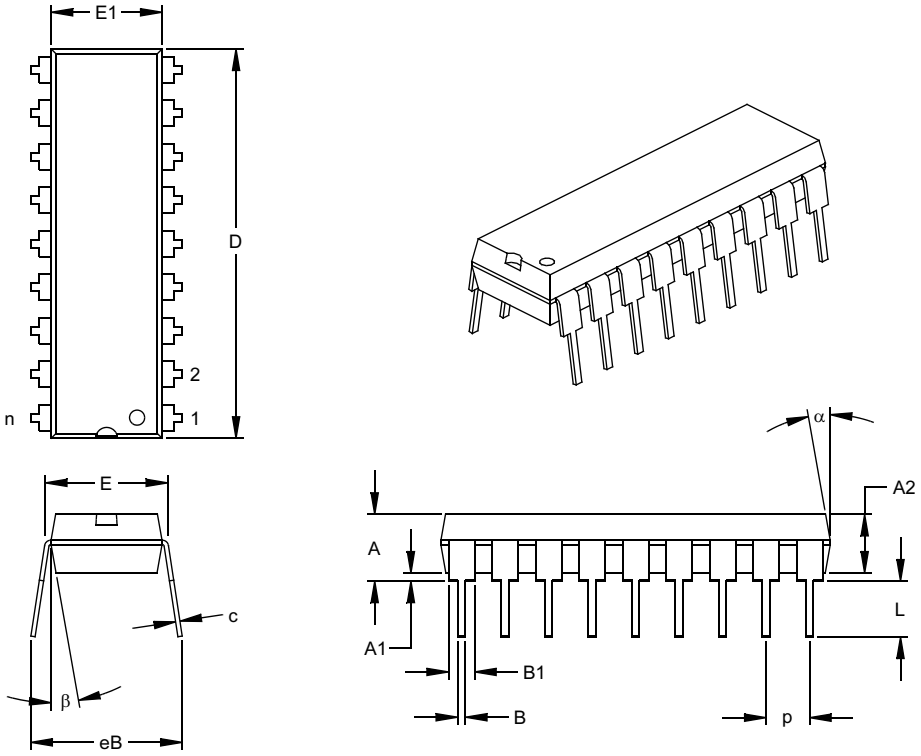


Legend:	MM...M	Microchip part number information
	XX...X	Customer specific information(1)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line thus limiting the number of available characters for customer specific information.

* Standard OTP marking consists of Microchip part number, year code, week code, facility code, mask rev#, and assembly code. For OTP marking beyond this, certain price adders apply. Please check with your Microchip Sales Office. For QTP devices, any special marking adders are included in QTP price.

K04-007 18-Lead Plastic Dual In-line (P) – 300 mil



Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		18			18	
Pitch	p		.100			2.54	
Top to Seating Plane	A	.140	.155	.170	3.56	3.94	4.32
Molded Package Thickness	A2	.115	.130	.145	2.92	3.30	3.68
Base to Seating Plane	A1	.015			0.38		
Shoulder to Shoulder Width	E	.300	.313	.325	7.62	7.94	8.26
Molded Package Width	E1	.240	.250	.260	6.10	6.35	6.60
Overall Length	D	.890	.898	.905	22.61	22.80	22.99
Tip to Seating Plane	L	.125	.130	.135	3.18	3.30	3.43
Lead Thickness	c	.008	.012	.015	0.20	0.29	0.38
Upper Lead Width	B1	.045	.058	.070	1.14	1.46	1.78
Lower Lead Width	B	.014	.018	.022	0.36	0.46	0.56
Overall Row Spacing §	eB	.310	.370	.430	7.87	9.40	10.92
Mold Draft Angle Top	α	5	10	15	5	10	15
Mold Draft Angle Bottom	β	5	10	15	5	10	15

* Controlling Parameter
§ Significant Characteristic

Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010” (0.254mm) per side.
JEDEC Equivalent: MS-001
Drawing No. C04-007

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