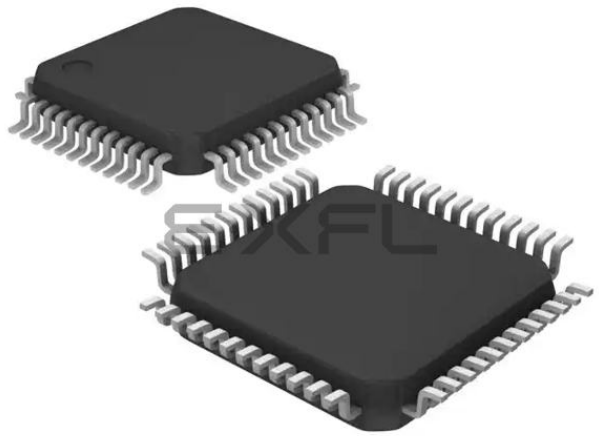

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What is "Embedded - Microcontrollers"?

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	I²C, IrDA, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	34
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.62V ~ 3.6V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atsam3n0aa-aur

1. SAM3N Description

Atmel's SAM3N series is a member of a family of Flash microcontrollers based on the high performance 32-bit ARM Cortex-M3 RISC processor. It operates at a maximum speed of 48 MHz and features up to 256 Kbytes of Flash and up to 24 Kbytes of SRAM. The peripheral set includes 2x USARTs, 2x UARTs, 2x TWIs, 3x SPI, as well as 1 PWM timer, 6x general purpose 16-bit timers, an RTC, a 10-bit ADC and a 10-bit DAC.

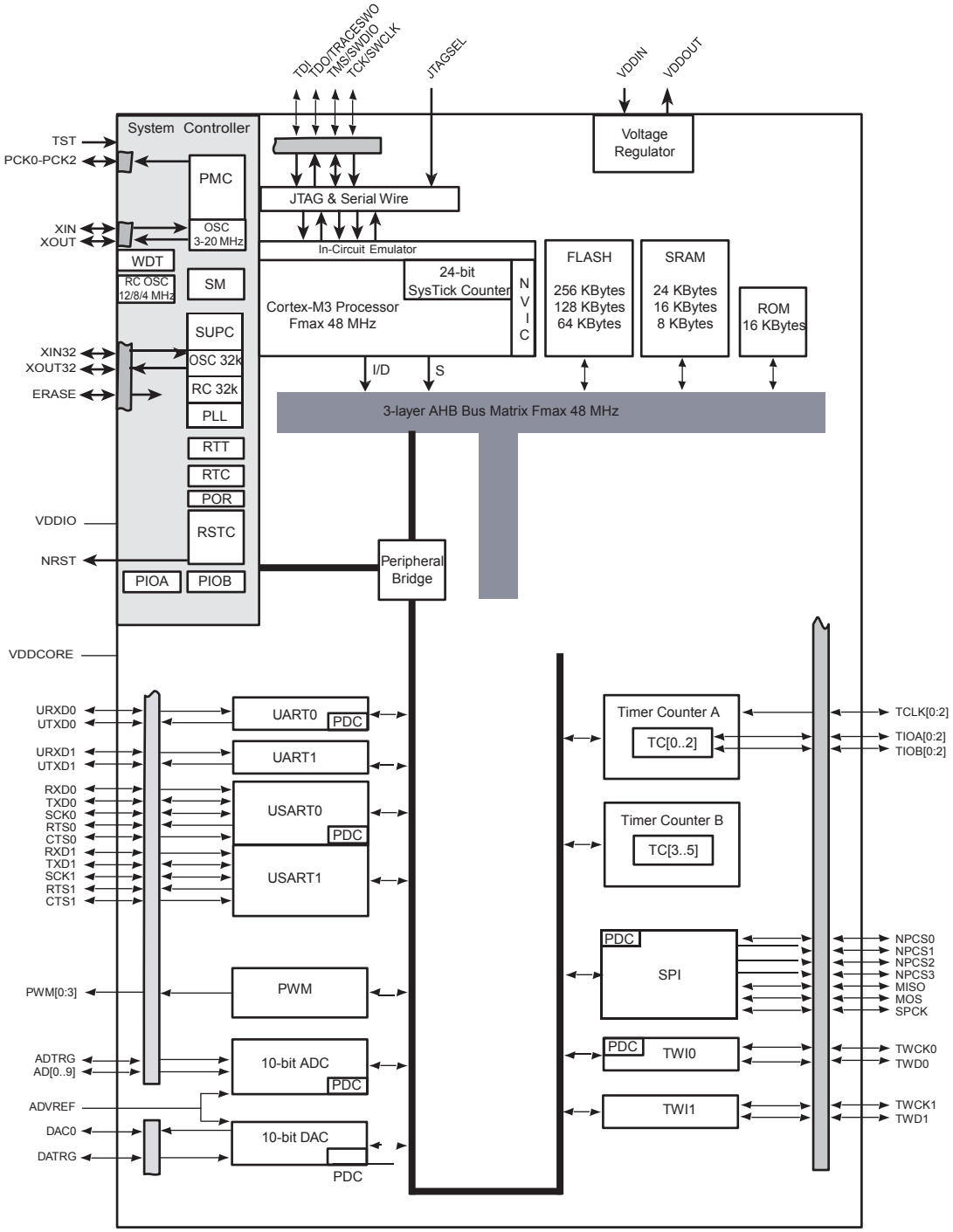
The SAM3N series is ready for capacitive touch thanks to the QTouch library, offering an easy way to implement buttons, wheels and sliders.

The SAM3N device is an entry-level general purpose microcontroller. That makes the SAM3N the ideal starting point to move from 8- /16-bit to 32-bit microcontrollers.

It operates from 1.62V to 3.6V and is available in 48-pin, 64-pin and 100-pin QFP, 48-pin and 64-pin QFN, and 100-pin BGA packages.

The SAM3N series is the ideal migration path from the SAM3S for applications that require a reduced BOM cost. The SAM3N series is pin-to-pin compatible with the SAM3S series. Its aggressive price point and high level of integration pushes its scope of use far into cost-sensitive, high-volume applications.

Figure 2-2. SAM3N 64-pin version Block Diagram



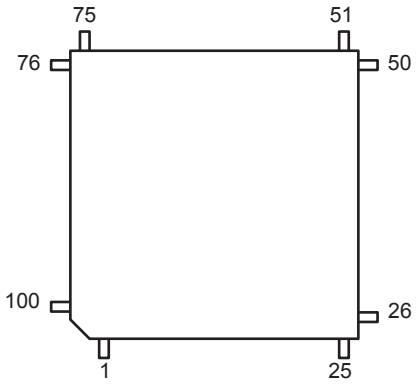
4. Package and Pinout

SAM3N4/2/1/0/00 series is pin-to-pin compatible with SAM3S products. Furthermore SAM3N4/2/1/0/00 devices have new functionalities referenced in italic inTable 4-1, Table 4-3 and Table 4-4.

4.1 SAM3N4/2/1/0/00C Package and Pinout

4.1.1 100-lead LQFP Package Outline

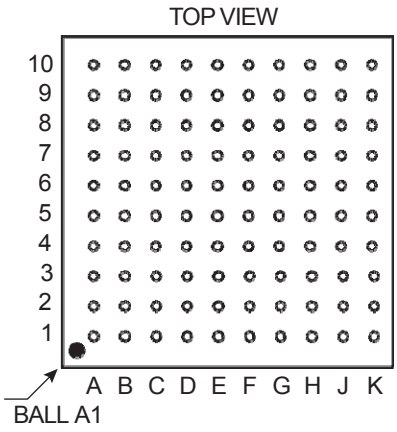
Figure 4-1. Orientation of the 100-lead LQFP Package



4.1.2 100-ball TFBGA Package Outline

The 100-Ball TFBGA package has a 0.8 mm ball pitch and respects Green Standards. Its dimensions are 9 x 9 x 1.1 mm.

Figure 4-2. Orientation of the 100-ball TFBGA Package



4.1.3 100-Lead LQFP Pinout

Table 4-1. 100-lead LQFP SAM3N4/2/1/0/00C Pinout

1	ADVREF	26	GND	51	TDI/PB4	76	TDO/TRACESWO/PB5
2	GND	27	VDDIO	52	PA6/PGMNOE	77	JTAGSEL
3	PB0/AD4	28	PA16/PGMD4	53	PA5/PGMRDY	78	PC18
4	PC29/AD13	29	PC7	54	PC28	79	TMS/SWDIO/PB6
5	PB1/AD5	30	PA15/PGMD3	55	PA4/PGMNCMD	80	PC19
6	PC30/AD14	31	PA14/PGMD2	56	VDDCORE	81	PA31
7	PB2/AD6	32	PC6	57	PA27	82	PC20
8	PC31/AD15	33	PA13/PGMD1	58	PC8	83	TCK/SWCLK/PB7
9	PB3/AD7	34	PA24	59	PA28	84	PC21
10	VDDIN	35	PC5	60	NRST	85	VDDCORE
11	VDDOUT	36	VDDCORE	61	TST	86	PC22
12	PA17/PGMD5/AD0	37	PC4	62	PC9	87	ERASE/PB12
13	PC26	38	PA25	63	PA29	88	PB10
14	PA18/PGMD6/AD1	39	PA26	64	PA30	89	PB11
15	PA21/AD8	40	PC3	65	PC10	90	PC23
16	VDDCORE	41	PA12/PGMD0	66	PA3	91	VDDIO
17	PC27	42	PA11/PGMM3	67	PA2/PGMEN2	92	PC24
18	PA19/PGMD7/AD2	43	PC2	68	PC11	93	PB13/DAC0
19	PC15/AD11	44	PA10/PGMM2	69	VDDIO	94	PC25
20	PA22/AD9	45	GND	70	GND	95	GND
21	PC13/AD10	46	PA9/PGMM1	71	PC14	96	PB8/XOUT
22	PA23	47	PC1	72	PA1/PGMEN1	97	PB9/*PGMCK/XIN*
23	PC12/AD12	48	PA8/XOUT32/ PGMM0	73	PC16	98	VDDIO
24	PA20/AD3	49	PA7/XIN32/ PGMNVALID	74	PA0/PGMEN0	99	PB14
25	PC0	50	VDDIO	75	PC17	100	VDDPLL

4.1.4 100-ball TFBGA Pinout

Table 4-2. 100-ball TFBGA SAM3N4/2/1/0/00C Pinout

A1	PB1	C6	PB7	F1	PA18	H6	PC4
A2	PC29	C7	PC16	F2	PC26	H7	PA11
A3	VDDIO	C8	PA1	F3	VDDOUT	H8	PC1
A4	PB9	C9	PC17	F4	GND	H9	PA6
A5	PB8	C10	PA0	F5	VDDIO	H10	PB4
A6	PB13	D1	PB3	F6	PA27	J1	PC15
A7	PB11	D2	PB0	F7	PC8	J2	PC0
A8	PB10	D3	PC24	F8	PA28	J3	PA16
A9	PB6	D4	PC22	F9	TST	J4	PC6
A10	JTAGSEL	D5	GND	F10	PC9	J5	PA24
B1	PC30	D6	GND	G1	PA21	J6	PA25
B2	ADVREF	D7	VDDCORE	G2	PC27	J7	PA10
B3	GNDANA	D8	PA2	G3	PA15	J8	GND
B4	PB14	D9	PC11	G4	VDDCORE	J9	VDDCORE
B5	PC21	D10	PC14	G5	VDDCORE	J10	VDDIO
B6	PC20	E1	PA17	G6	PA26	K1	PA22
B7	PA31	E2	PC31	G7	PA12	K2	PC13
B8	PC19	E3	VDDIN	G8	PC28	K3	PC12
B9	PC18	E4	GND	G9	PA4	K4	PA20
B10	PB5	E5	GND	G10	PA5	K5	PC5
C1	PB2	E6	NRST	H1	PA19	K6	PC3
C2	VDDPLL	E7	PA29	H2	PA23	K7	PC2
C3	PC25	E8	PA30	H3	PC7	K8	PA9
C4	PC23	E9	PC10	H4	PA14	K9	PA8
C5	PB12	E10	PA3	H5	PA13	K10	PA7

- Supply Monitor alarm
- RTC alarm
- RTT alarm

5.5.2 Wait Mode

The purpose of the wait mode is to achieve very low power consumption while maintaining the whole device in a powered state for a startup time of less than 10 µs. Current Consumption in Wait mode is typically 15 µA (total current consumption) if the internal voltage regulator is used or 8 µA if an external regulator is used.

In this mode, the clocks of the core, peripherals and memories are stopped. However, the core, peripherals and memories power supplies are still powered. From this mode, a fast start up is available.

This mode is entered via Wait for Event (WFE) instructions with LPM = 1 (Low Power Mode bit in PMC_FSMR). The Cortex-M3 is able to handle external or internal events in order to wake up the core (WFE). By configuring the WUP0-15 external lines as fast startup wake-up pins (refer to Section 5.7 “Fast Start-Up”). RTC or RTT Alarm wake-up events can be used to wake up the CPU (exit from WFE).

Entering Wait Mode:

- Select the 4/8/12 MHz fast RC oscillator as Main Clock
- Set the LPM bit in the PMC Fast Startup Mode Register (PMC_FSMR)
- Execute the Wait-For-Event (WFE) instruction of the processor

Note: Internal Main clock resynchronization cycles are necessary between the writing of MOSCRCEN bit and the effective entry in Wait mode. Depending on the user application, Waiting for MOSCRCEN bit to be cleared is recommended to ensure that the core will not execute undesired instructions.

5.5.3 Sleep Mode

The purpose of sleep mode is to optimize power consumption of the device versus response time. In this mode, only the core clock is stopped. The peripheral clocks can be enabled. The current consumption in this mode is application dependent.

This mode is entered via Wait for Interrupt (WFI) or Wait for Event (WFE) instructions with LPM = 0 in PMC_FSMR.

The processor can be woke up from an interrupt if WFI instruction of the Cortex M3 is used, or from an event if the WFE instruction is used to enter this mode.

5.5.4 Low Power Mode Summary Table

The modes detailed above are the main low power modes. Each part can be set to on or off separately and wake up sources can be individually configured. Table 5-1 below shows a summary of the configurations of the low power modes.

Table 5-1. Low Power Mode Configuration Summary

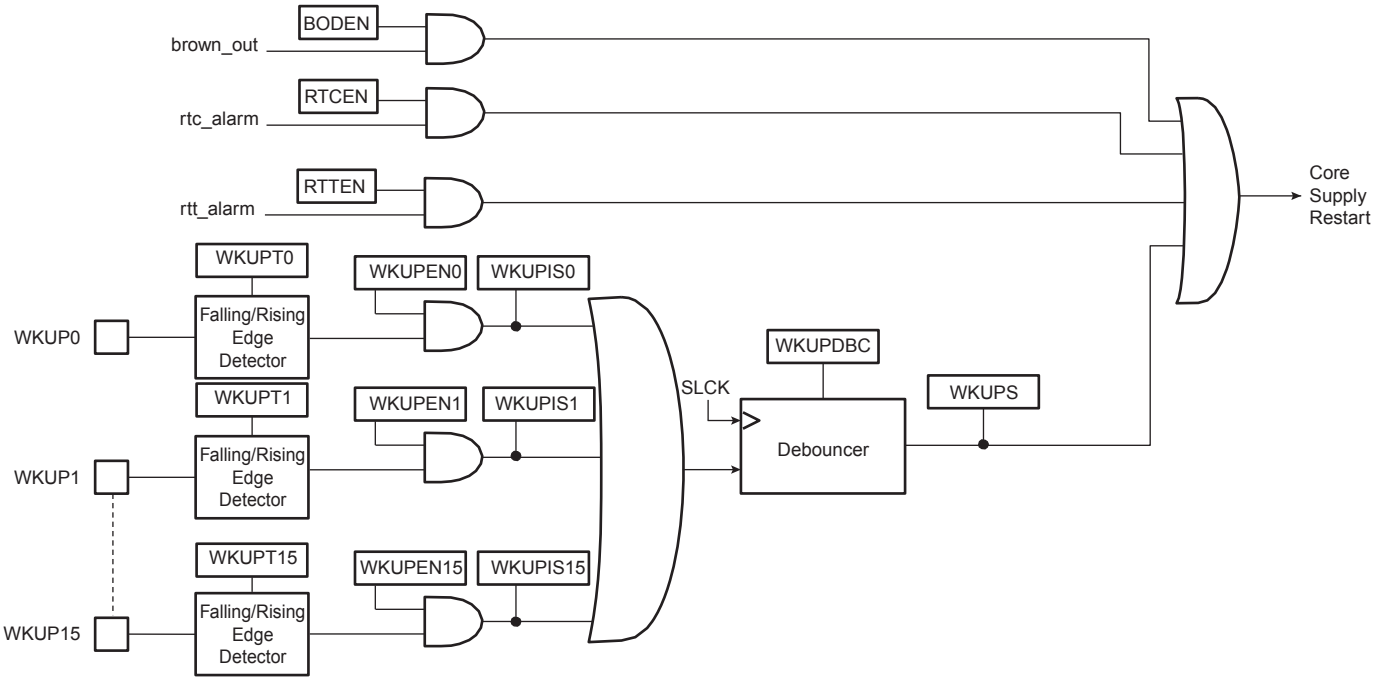
Mode	SUPC, 32 kHz Oscillator RTC RTT Backup Registers, POR (Backup Region)	Regulator	Core Memory Peripherals	Mode Entry	Potential Wake Up Sources	Core at Wake Up	PIO State while in Low Power Mode	PIO State at Wake Up	Consumption (2) (3)	Wake Up Time(1)
Backup Mode	ON	OFF	OFF (Not powered)	WFE +SLEEPDEEP bit = 1	WUP0-15 pins BOD alarm RTC alarm RTT alarm	Reset	Previous state saved	PIOA & PIOB & PIOC Inputs with pull ups	3 µA typ(4)	< 0.1 ms
Wait Mode	ON	ON	Powered (Not clocked)	WFE +SLEEPDEEP bit = 0 +LPM bit = 1	Any Event from: Fast startup through WUP0-15 pins RTC alarm RTT alarm	Clocked back	Previous state saved	Unchanged	5 µA/15 µA (5)	< 10 µs
Sleep Mode	ON	ON	Powered(7) (Not clocked)	WFE or WFI +SLEEPDEEP bit = 0 +LPM bit = 0	Entry mode = WFI Interrupt Only; Entry mode = WFE Any Enabled Interrupt and/or Any Event from: Fast start-up through WUP0-15 pins RTC alarm RTT alarm	Clocked back	Previous state saved	Unchanged	(6)	(6)

Notes:
1. When considering wake-up time, the time required to start the PLL is not taken into account. Once started, the device works with the 4/8/12 MHz Fast RC oscillator. The user has to add the PLL start-up time if it is needed in the system. The wake-up time is defined as the time taken for wake up until the first instruction is fetched.
2. The external loads on PIOs are not taken into account in the calculation.
3. Supply Monitor current consumption is not included.
4. Total Current consumption.
5. 5 µA on VDDCORE, 15 µA for total current consumption (using internal voltage regulator), 8 µA for total current consumption (without using internal voltage regulator).
6. Depends on MCK frequency.
7. In this mode the core is supplied and not clocked but some peripherals can be clocked.

5.6 Wake-up Sources

The wake-up events allow the device to exit backup mode. When a wake-up event is detected, the Supply Controller performs a sequence which automatically reenables the core power supply and the SRAM power supply, if they are not already enabled.

Figure 5-4. Wake-up Source

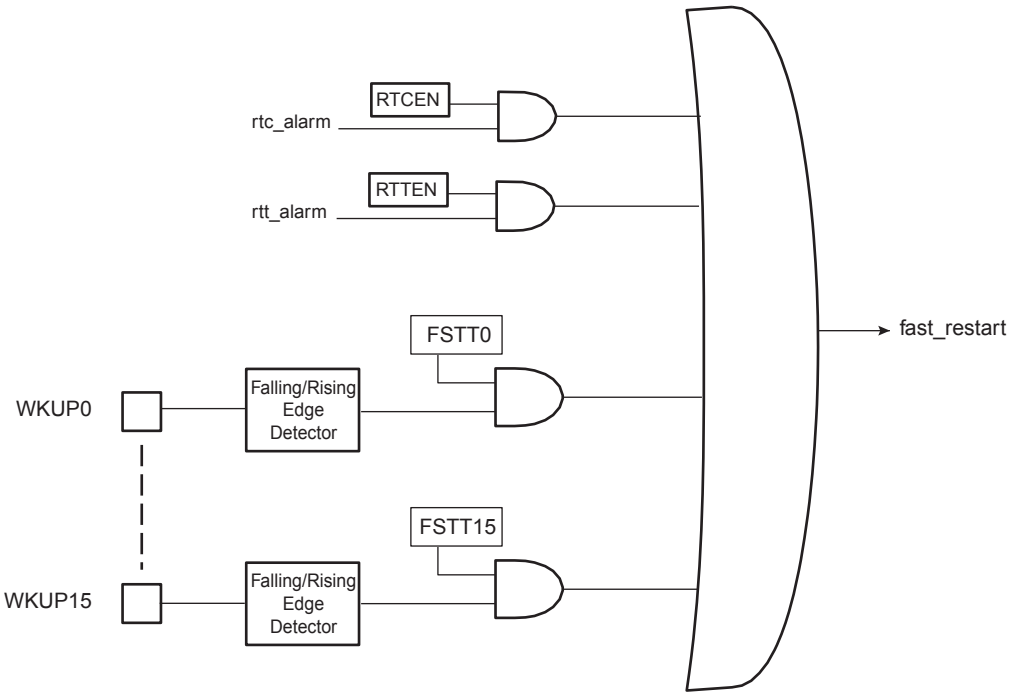


5.7 Fast Start-Up

The SAM3N allows the processor to restart in a few microseconds while the processor is in wait mode. A fast start up can occur upon detection of a low level on one of the 19 wake-up inputs (WKUP0 to 15 + SM + RTC + RTT).

The fast restart circuitry, as shown in Figure 5-5, is fully asynchronous and provides a fast start-up signal to the Power Management Controller. As soon as the fast start-up signal is asserted, the PMC automatically restarts the embedded 4 MHz fast RC oscillator, switches the master clock on this 4 MHz clock and reenables the processor clock.

Figure 5-5. Fast Start-Up Sources



6. Input/Output Lines

The SAM3N has several kinds of input/output (I/O) lines such as general purpose I/Os (GPIO) and system I/Os. GPIOs can have alternate functionality due to multiplexing capabilities of the PIO controllers. The same PIO line can be used whether in IO mode or by the multiplexed peripheral. System I/Os include pins such as test pins, oscillators, erase or analog inputs.

6.1 General Purpose I/O Lines

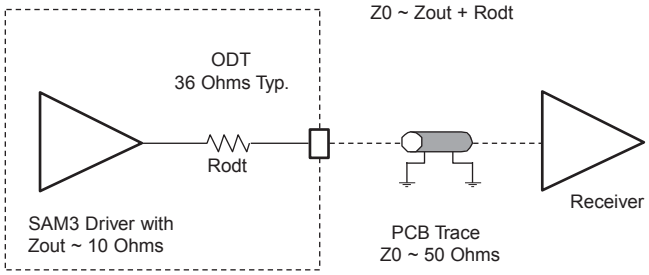
GPIO Lines are managed by PIO Controllers. All I/Os have several input or output modes such as pull-up or pull-down, input Schmitt triggers, multi-drive (open-drain), glitch filters, debouncing or input change interrupt. Programming of these modes is performed independently for each I/O line through the PIO controller user interface. For more details, refer to the product PIO controller section.

The input output buffers of the PIO lines are supplied through VDDIO power supply rail.

The SAM3N embeds high speed pads able to handle up to 45 MHz for SPI clock lines and 35 MHz on other lines. See AC Characteristics Section in the Electrical Characteristics Section of the datasheet for more details. Typical pull-up and pull-down value is 100 kΩ for all I/Os.

Each I/O line also embeds an ODT (On-Die Termination), (see Figure 6-1). It consists of an internal series resistor termination scheme for impedance matching between the driver output (SAM3N) and the PCB trace impedance preventing signal reflection. The series resistor helps to reduce I/O switching current (di/dt) thereby reducing in turn, EMI. It also decreases overshoot and undershoot (ringing) due to inductance of interconnect between devices or between boards. In conclusion ODT helps diminish signal integrity issues.

Figure 6-1. On-Die Termination



6.2 System I/O Lines

System I/O lines are pins used by oscillators, test mode, reset and JTAG to name but a few. Described below are the SAM3N system I/O lines shared with PIO lines:

These pins are software configurable as general purpose I/O or system pins. At startup the default function of these pins is always used.

7. Processor and Architecture

7.1 ARM Cortex-M3 Processor

- Version 2.0
- Thumb-2 (ISA) subset consisting of all base Thumb-2 instructions, 16-bit and 32-bit.
- Harvard processor architecture enabling simultaneous instruction fetch with data load/store.
- Three-stage pipeline.
- Single cycle 32-bit multiply.
- Hardware divide.
- Thumb and Debug states.
- Handler and Thread modes.
- Low latency ISR entry and exit.

7.2 APB/AHB Bridge

The SAM3N4/2/1/0/00 product embeds one peripheral bridge:

The peripherals of the bridge are clocked by MCK.

7.3 Matrix Masters

The Bus Matrix of the SAM3N product manages 3 masters, which means that each master can perform an access concurrently with others, to an available slave.

Each master has its own decoder, which is defined specifically for each master. In order to simplify the addressing, all the masters have the same decodings.

Table 7-1. List of Bus Matrix Masters

Master 0	Cortex-M3 Instruction/Data
Master 1	Cortex-M3 System
Master 2	Peripheral DMA Controller (PDC)

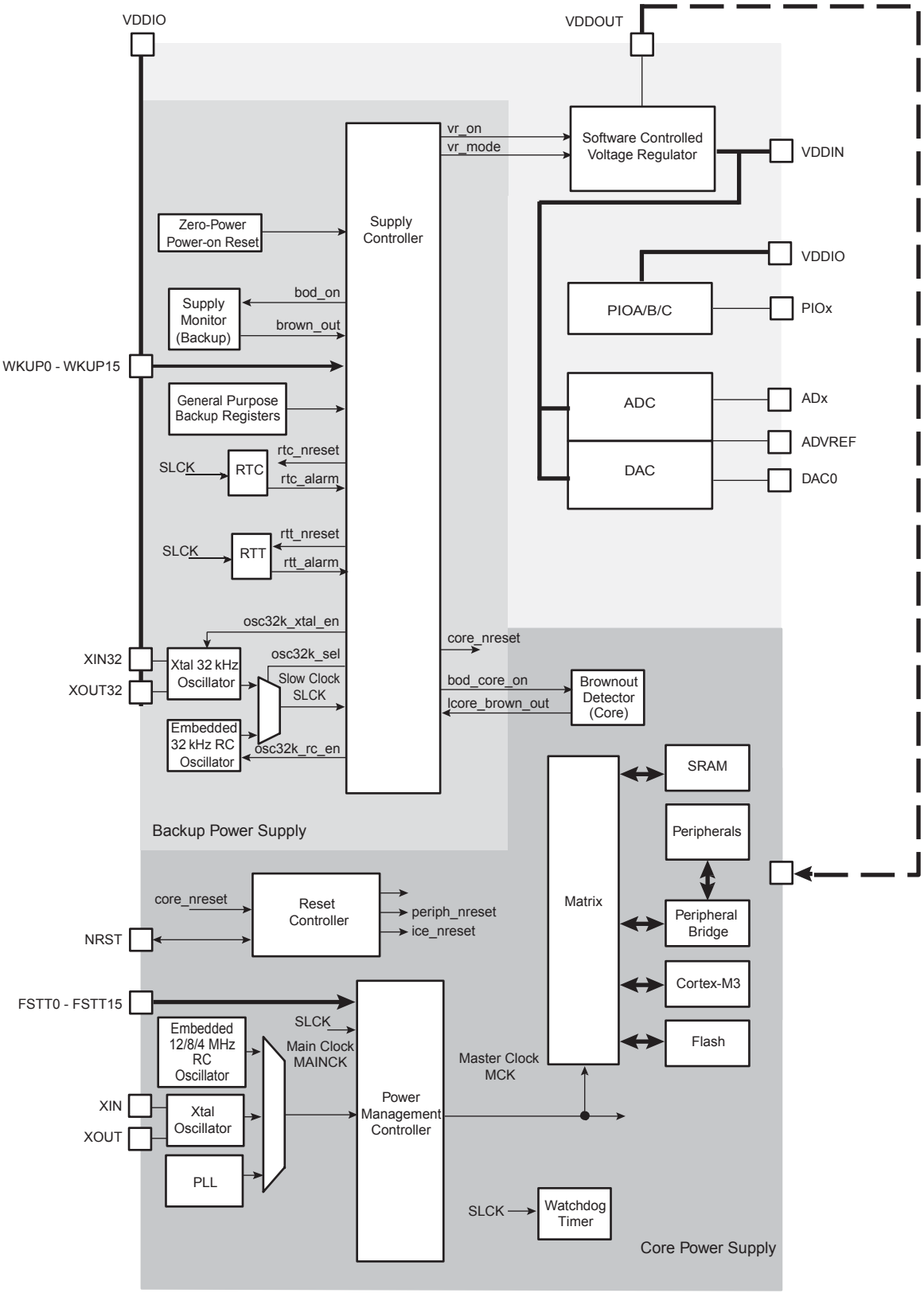
7.4 Matrix Slaves

The Bus Matrix of the SAM3N product manages 4 slaves. Each slave has its own arbiter, allowing a different arbitration per slave.

Table 7-2. List of Bus Matrix Slaves

Slave 0	Internal SRAM
Slave 1	Internal ROM
Slave 2	Internal Flash
Slave 3	Peripheral Bridge

Figure 10-1. System Controller Block Diagram



FSTT0 - FSTT15 are possible Fast Startup Sources, generated by WKUP0-WKUP15 Pins, but are not physical pins.

Table 11-1. Peripheral Identifiers (Continued)

Instance ID	Instance Name	NVIC Interrupt	PMC Clock Control	Instance Description
25	TC2	**X**	**X**	Timer/Counter 2
26	TC3	**X**	**X**	Timer/Counter 3
27	TC4	**X**	**X**	Timer/Counter 4
28	TC5	**X**	**X**	Timer/Counter 5
29	ADC	**X**	**X**	Analog-to-Digital Converter
30	DACC	**X**	**X**	Digital-to-Analog Converter
31	PWM	**X**	**X**	Pulse Width Modulation

11.2 Peripheral Signals Multiplexing on I/O Lines

The SAM3N product features 2 PIO controllers (48-pin and 64-pin version) or 3 PIO controllers (100-pin version), PIOA, PIOB and PIOC, that multiplex the I/O lines of the peripheral set.

The SAM3N 64-pin and 100-pin PIO Controller controls up to 32 lines (see Table 10-2, “PIO available according to pin count,” on page 40). Each line can be assigned to one of three peripheral functions: A, B or C. The multiplexing tables in the following paragraphs define how the I/O lines of the peripherals A, B and C are multiplexed on the PIO Controllers. The column “Comments” has been inserted in this table for the user’s own comments; it may be used to track how pins are defined in an application.

Note that some peripheral functions which are output only, might be duplicated within the tables.

11.2.2 PIO Controller B Multiplexing

Table 11-3. Multiplexing on PIO Controller B (PIOB)

I/O Line	Peripheral A	Peripheral B	Peripheral C	Extra Function	System Function	Comments
PB0	PWM0			AD4		
PB1	PWM1			AD5		
PB2	URXD1	NPCS2		AD6/WKUP12		
PB3	UTXD1	PCK2		AD7		
PB4	TWD1	PWM2			TDI	
PB5	TWCK1			WKUP13	TDO/ TRACESWO	
PB6					TMS/SWDIO	
PB7					TCK/SWCLK	
PB8					XOUT	
PB9					XIN	
PB10						
PB11						
PB12					ERASE	
PB13		PCK0		DAC0		64/100-pin versions
PB14	NPCS1	PWM3				64/100-pin versions

12. Embedded Peripherals Overview

12.1 Serial Peripheral Interface (SPI)

- Supports communication with serial external devices
  - Four chip selects with external decoder support allow communication with up to 15 peripherals
  - Serial memories, such as DataFlash and 3-wire EEPROMs
  - Serial peripherals, such as ADCs, DACs, LCD Controllers, CAN Controllers and Sensors
  - External co-processors
- Master or slave serial peripheral bus interface
  - 8- to 16-bit programmable data length per chip select
  - Programmable phase and polarity per chip select
  - Programmable transfer delays between consecutive transfers and between clock and data per chip select
  - Programmable delay between consecutive transfers
  - Selectable mode fault detection
- Very fast transfers supported
  - Transfers with baud rates up to MCK
  - The chip select line may be left active to speed up transfers on the same device

12.2 Two Wire Interface (TWI)

- Master, Multi-Master and Slave Mode Operation
- Compatibility with Atmel two-wire interface, serial memory and I^2C compatible devices
- One, two or three bytes for slave address
- Sequential read/write operations
- Bit Rate: Up to 400 kbit/s
- General Call Supported in Slave Mode
- Connecting to PDC channel capabilities optimizes data transfers in Master Mode only (for TWI0 only)
  - One channel for the receiver, one channel for the transmitter
  - Next buffer support

12.3 Universal Asynchronous Receiver Transceiver (UART)

- Two-pin UART
  - Implemented features are 100% compatible with the standard Atmel USART
  - Independent receiver and transmitter with a common programmable Baud Rate Generator
  - Even, Odd, Mark or Space Parity Generation
  - Parity, Framing and Overrun Error Detection
  - Automatic Echo, Local Loopback and Remote Loopback Channel Modes

  - Two multi-purpose input/output signals
- Two global registers that act on all three TC Channels
- Quadrature decoder
  - Advanced line filtering
  - Position/revolution/speed
- 2-bit Gray Up/Down Counter for Stepper Motor

12.6 Pulse Width Modulation Controller (PWM)

- Four channels, one 16-bit counter per channel
- Common clock generator, providing thirteen different clocks
  - One Modulo n counter providing eleven clocks
  - Two independent linear dividers working on modulo n counter outputs
- Independent channel programming
  - Independent enable/disable commands
  - Independent clock selection
  - Independent period and duty cycle, with double buffering
  - Programmable selection of the output waveform polarity

12.7 10-bit Analog-to-Digital Converter

- Up to 16-channel ADC
- 10-bit 384 Ksamples/sec. or 8-bit 583 Ksamples/sec. Successive Approximation Register ADC
- ±2 LSB Integral Non Linearity, ±1 LSB Differential Non Linearity
- Integrated 8-to-1 multiplexer, offering eight independent 3.3V analog inputs
- External voltage reference for better accuracy on low voltage inputs
- Individual enable and disable of each channel
- Multiple trigger source
  - Hardware or software trigger
  - External trigger pin
  - Timer Counter 0 to 2 outputs TIOA0 to TIOA2 trigger
- Sleep Mode and conversion sequencer
  - Automatic wakeup on trigger and back to sleep mode after conversions of all enabled channels

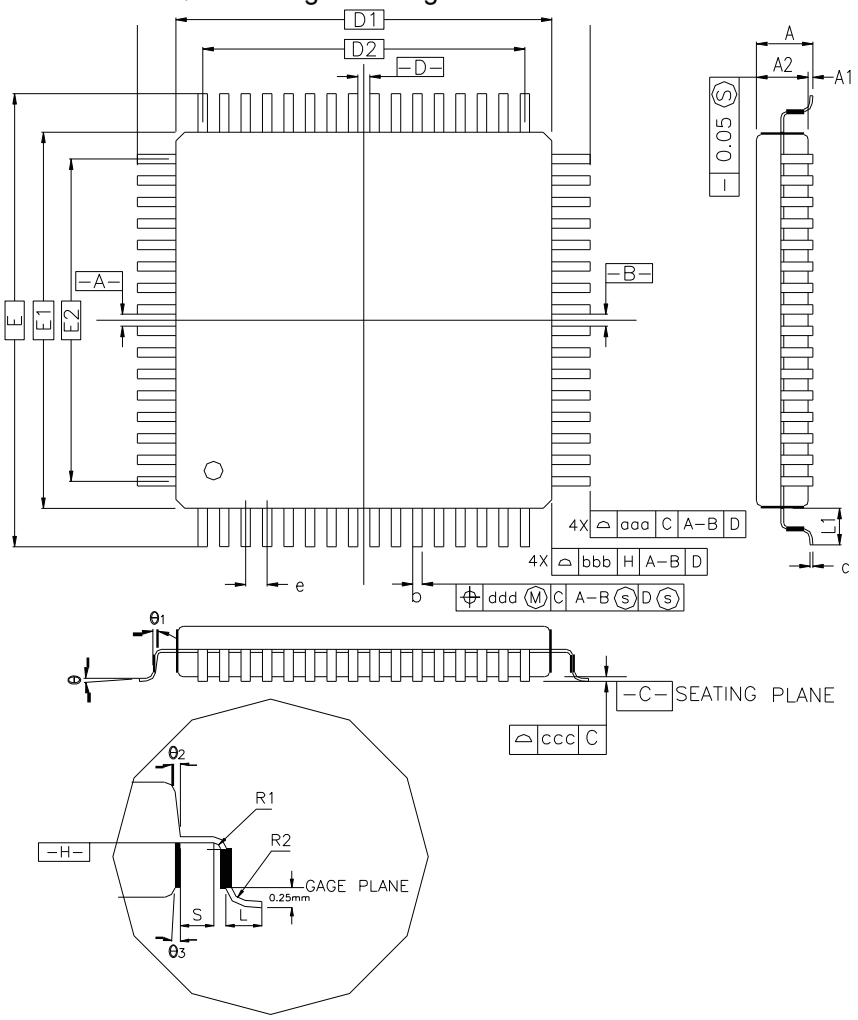
12.8 Digital-to-Analog Converter (DAC)

- 1 channel 10-bit DAC
- Up to 500 ksamples/s conversion rate
- Flexible conversion range
- Multiple trigger sources
- One PDC channel

13. Package Drawings

The SAM3N series devices are available in LQFP, QFN and TFBGA packages.

Figure 13-1. 100-lead LQFP Package Drawing



COTROL DIMENSIONS ARE IN MILLIMETERS.

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	
A	—	—	1.60	—	—	0
A_1	0.05	—	0.15	0.002	—	0
A_2	1.35	1.40	1.45	0.053	0.055	0
D	16.00 BSC.			0.630 BSC		
D_1	14.00 BSC.			0.551 BSC		
E	16.00 BSC.			0.630 BSC		
E_1	14.00 BSC.			0.551 BSC		
R_2	0.08	—	0.20	0.003	—	0
R_1	0.08	—	—	0.003	—	
θ	0°	3.5°	7°	0°	3.5°	
θ_1	0°	—	—	0°	—	
θ_2	11°	12°	13°	11°	12°	
θ_3	11°	12°	13°	11°	12°	
c	0.09	—	0.20	0.004	—	0
L	0.45	0.60	0.75	0.018	0.024	0
L_1	1.00 REF			0.039 REF		
S	0.20	—	—	0.008	—	

Note : 1. This drawing is for general information only. Refer to JEDEC Drawing MS-026 for additional information.

Figure 13-3. 64and4B·leadLQFP Package Drawing

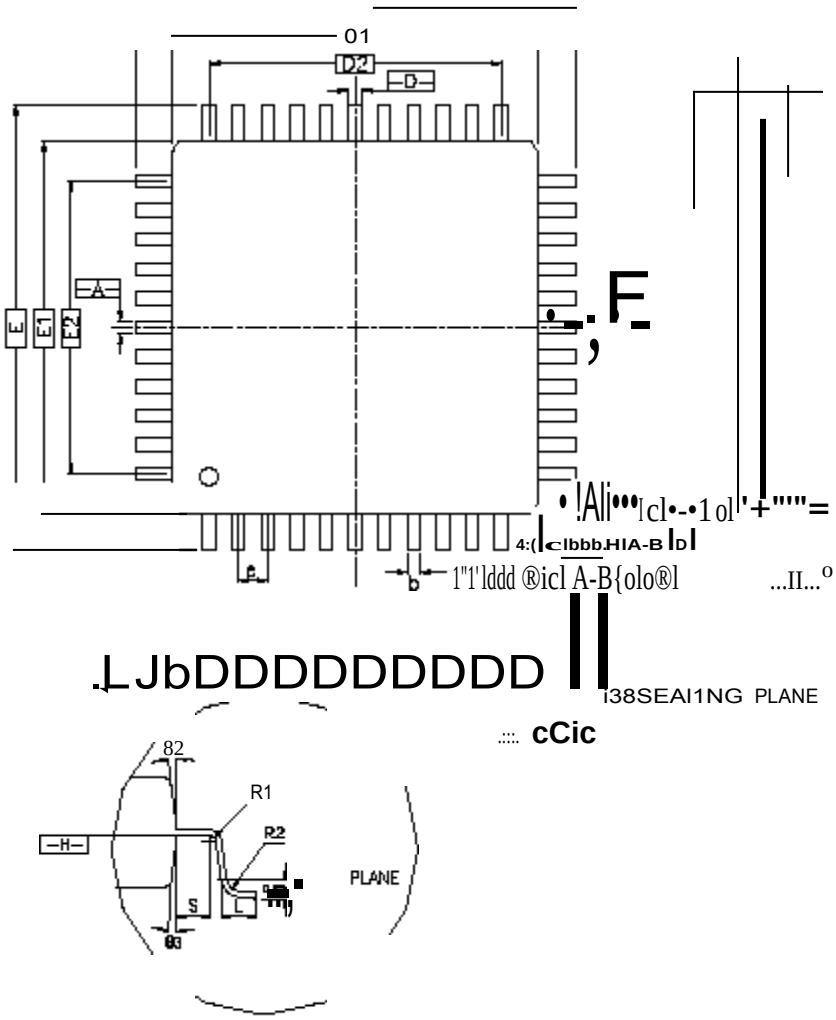


Table 13-2. 64-lead LQFP Package Dimensions (in mm)

Symbol	Millimeter			Inch		
	Min	**Nom**	**Max**	**Min**	**Nom**	**Max**
A	–	–	1.60	–	–	0.063
A1	0.05	–	0.15	0.002	–	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
D	12.00 BSC			0.472 BSC		
D1	10.00 BSC			0.383 BSC		
E	12.00 BSC			0.472 BSC		
E1	10.00 BSC			0.383 BSC		
R2	0.08	–	0.20	0.003	–	0.008
R1	0.08	–	–	0.003	–	–
q	0°	3.5°	7°	0°	3.5°	7°
θ_1	0°	–	–	0°	–	–
θ_2	11°	12°	13°	11°	12°	13°
θ_3	11°	12°	13°	11°	12°	13°
c	0.09	–	0.20	0.004	–	0.008
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF			0.039 REF		
S	0.20	–	–	0.008	–	–
b	0.17	0.20	0.27	0.007	0.008	0.011
e	0.50 BSC.			0.020 BSC.		
D2	7.50			0.285		
E2	7.50			0.285		
Tolerances of Form and Position						
aaa	0.20			0.008		
bbb	0.20			0.008		
ccc	0.08			0.003		
ddd	0.08			0.003		

Table 13-3. 48-pad QFN Package Dimensions (in mm)

Symbol	Millimeter			Inch		
	Min	**Nom**	**Max**	**Min**	**Nom**	**Max**
A	–	–	090	–	–	0.035
A1	–	–	0.050	–	–	0.002
A2	–	0.65	0.70	–	0.026	0.028
A3	0.20 REF			0.008 REF		
b	0.18	0.20	0.23	0.007	0.008	0.009
D	7.00 bsc			0.276 bsc		
D2	5.45	5.60	5.75	0.215	0.220	0.226
E	7.00 bsc			0.276 bsc		
E2	5.45	5.60	5.75	0.215	0.220	0.226
L	0.35	0.40	0.45	0.014	0.016	0.018
e	0.50 bsc			0.020 bsc		
R	0.09	–	–	0.004	–	–
Tolerances of Form and Position						
aaa	0.10			0.004		
bbb	0.10			0.004		
ccc	0.05			0.002		