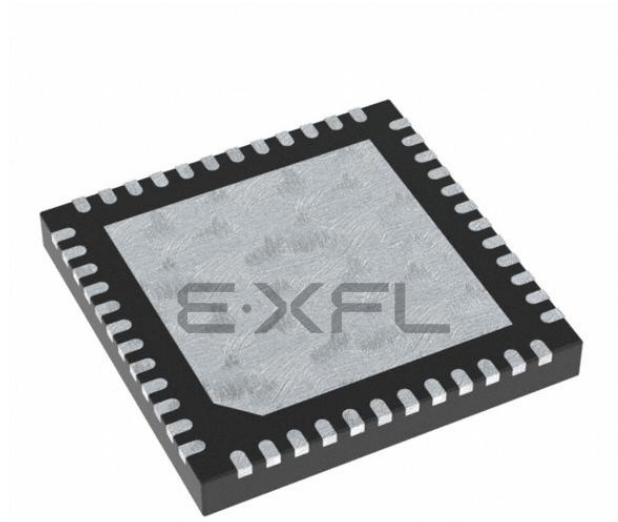

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	I²C, IrDA, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	34
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.62V ~ 3.6V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-VFQFN Exposed Pad
Supplier Device Package	48-QFN (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atsam3n0aa-mur

1. SAM3N Description

Atmel's SAM3N series is a member of a family of Flash microcontrollers based on the high performance 32-bit ARM Cortex-M3 RISC processor. It operates at a maximum speed of 48 MHz and features up to 256 Kbytes of Flash and up to 24 Kbytes of SRAM. The peripheral set includes 2x USARTs, 2x UARTs, 2x TWIs, 3x SPI, as well as 1 PWM timer, 6x general purpose 16-bit timers, an RTC, a 10-bit ADC and a 10-bit DAC.

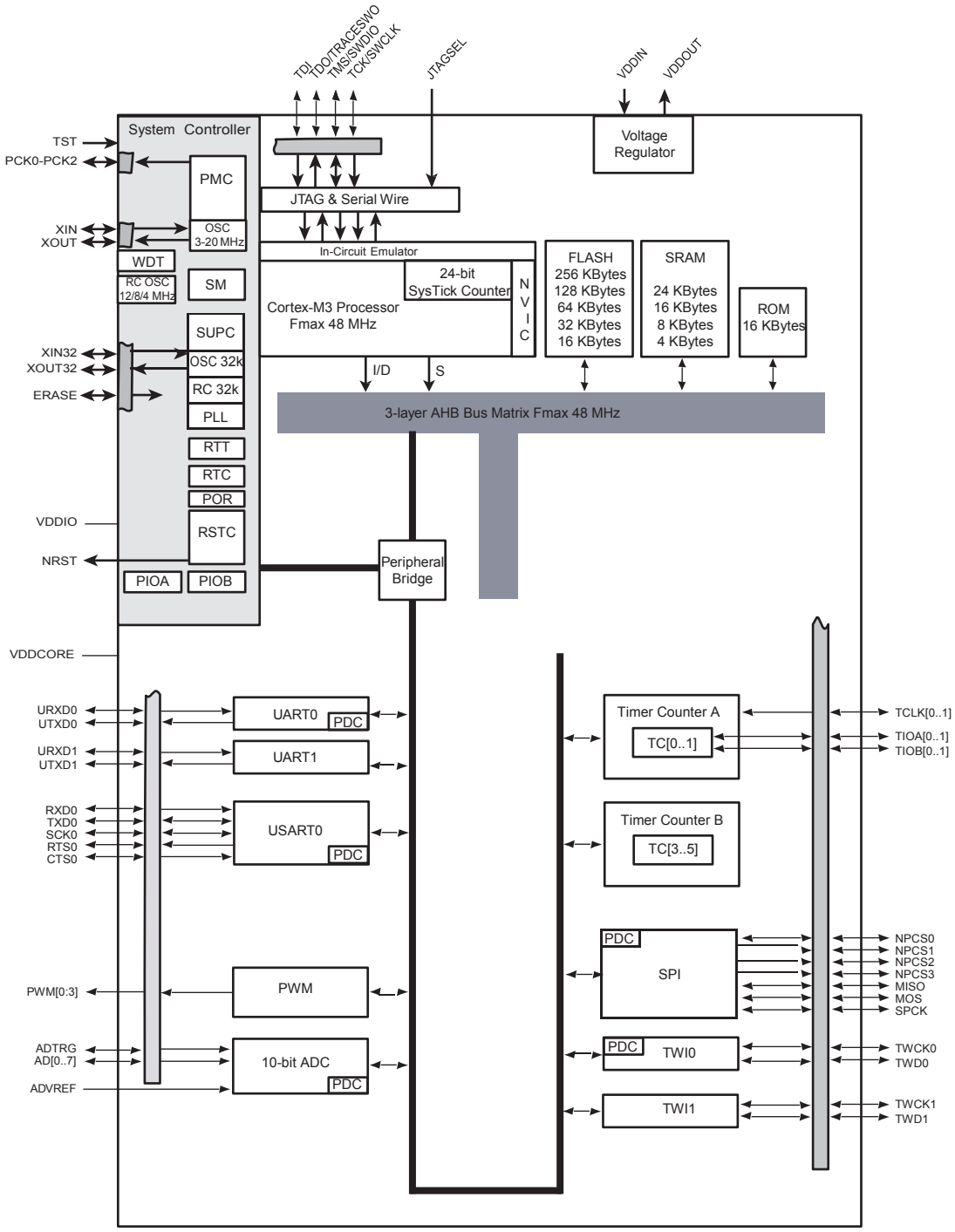
The SAM3N series is ready for capacitive touch thanks to the QTouch library, offering an easy way to implement buttons, wheels and sliders.

The SAM3N device is an entry-level general purpose microcontroller. That makes the SAM3N the ideal starting point to move from 8- /16-bit to 32-bit microcontrollers.

It operates from 1.62V to 3.6V and is available in 48-pin, 64-pin and 100-pin QFP, 48-pin and 64-pin QFN, and 100-pin BGA packages.

The SAM3N series is the ideal migration path from the SAM3S for applications that require a reduced BOM cost. The SAM3N series is pin-to-pin compatible with the SAM3S series. Its aggressive price point and high level of integration pushes its scope of use far into cost-sensitive, high-volume applications.

Figure 2-3. SAM3N 48-pin version Block Diagramz



4.2 SAM3N4/2/1/0/00B Package and Pinout

Figure 4-3. Orientation of the 64-pad QFN Package

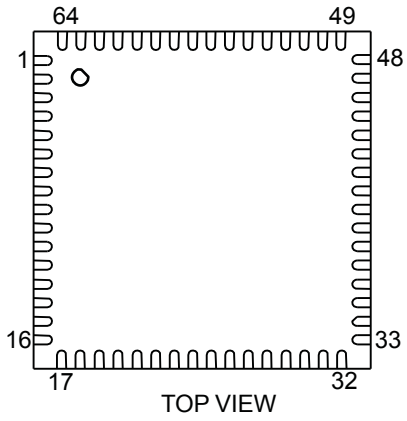
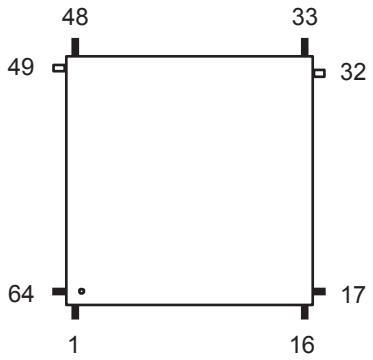


Figure 4-4. Orientation of the 64-lead LQFP Package



4.2.1 64-Lead LQFP and QFN Pinout

64-pin version SAM3N devices are pin-to-pin compatible with SAM3S products. Furthermore, SAM3N products have new functionalities shown in italic in Table 4-3.

Table 4-3. 64-pin SAM3N4/2/1/0/00B Pinout

1	ADVREF	17	GND	33	*TDI/PB4*	49	*TDO/TRACESWO/PB5*
2	GND	18	VDDIO	34	PA6/PGMNOE	50	JTAGSEL
3	*PB0/AD4*	19	PA16/PGMD4	35	PA5/PGMRDY	51	*TMS/SWDIO/PB6*
4	*PB1AD5*	20	PA15/PGMD3	36	PA4/PGMNCMD	52	PA31
5	*PB2/AD6*	21	PA14/PGMD2	37	PA27/PGMD15	53	*TCK/SWCLK/PB7*
6	*PB3/AD7*	22	PA13/PGMD1	38	PA28	54	VDDCORE
7	VDDIN	23	PA24/PGMD12	39	NRST	55	*ERASE/PB12*
8	VDDOUT	24	VDDCORE	40	TST	56	*PB10*
9	PA17/PGMD5/AD0	25	PA25/PGMD13	41	PA29	57	*PB11*
10	PA18/PGMD6/AD1	26	PA26/PGMD14	42	PA30	58	VDDIO
11	PA21/PGMD9/AD8	27	PA12/PGMD0	43	PA3	59	*PB13/DAC0*
12	VDDCORE	28	PA11/PGMM3	44	PA2/PGMEN2	60	GND
13	PA19/PGMD7/AD2	29	PA10/PGMM2	45	VDDIO	61	*XOUT/PB8*
14	PA22/PGMD10/AD9	30	PA9/PGMM1	46	GND	62	*XIN/PGMCK/PB9*
15	PA23/PGMD11	31	PA8/XOUT32/PGMM0	47	PA1/PGMEN1	63	*PB14*
16	PA20/PGMD8/AD3	32	PA7/XIN32/XOUT32/PGMNVALID	48	PA0/PGMEN0	64	VDDPLL

Note: The bottom pad of the QFN package must be connected to ground.

4.3.1 48-Lead LQFP and QFN Pinout

Table 4-4. 48-pin SAM3N4/2/1/0/00A Pinout

1	ADVREF	13	VDDIO	25	*TDI/PB4*	37	*TDO/TRACESWO/ PB5*
2	GND	14	PA16/PGMD4	26	PA6/PGMNOE	38	JTAGSEL
3	*PB0/AD4*	15	PA15/PGMD3	27	PA5/PGMRDY	39	*TMS/SWDIO/PB6*
4	*PB1/AD5*	16	PA14/PGMD2	28	PA4/PGMNCMD	40	*TCK/SWCLK/PB7*
5	*PB2/AD6*	17	PA13/PGMD1	29	NRST	41	VDDCORE
6	*PB3/AD7*	18	VDDCORE	30	TST	42	*ERASE/PB12*
7	VDDIN	19	PA12/PGMD0	31	PA3	43	*PB10*
8	VDDOUT	20	PA11/PGMM3	32	PA2/PGMEN2	44	*PB11*
9	PA17/PGMD5/AD0	21	PA10/PGMM2	33	VDDIO	45	*XOUT/PB8*
10	PA18/PGMD6/AD1	22	PA9/PGMM1	34	GND	46	*XIN/P/PB9/GMCK*
11	PA19/PGMD7/AD2	23	PA8/XOUT32/PG MM0	35	PA1/PGMEN1	47	VDDIO
12	PA20/AD3	24	PA7/XIN32/PGMN VALID	36	PA0/PGMEN0	48	VDDPLL

Note: The bottom pad of the QFN package must be connected to ground.

Figure 5-1. Single Supply

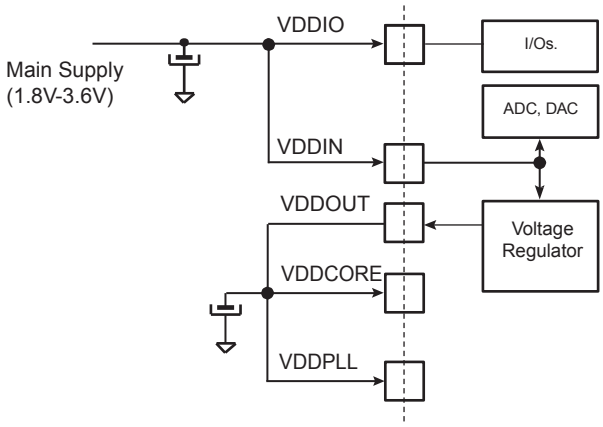
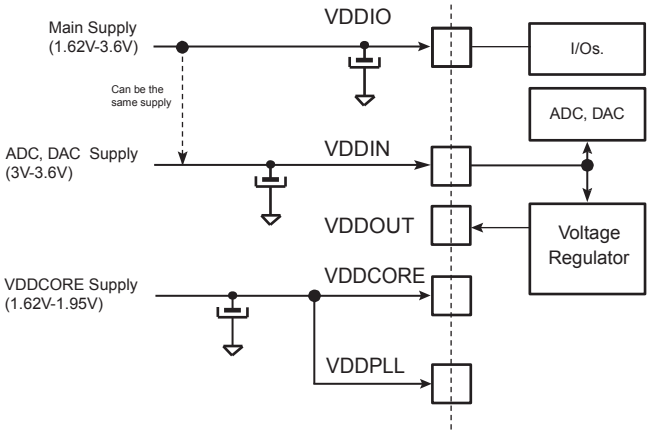


Figure 5-2. Core Externally Supplied



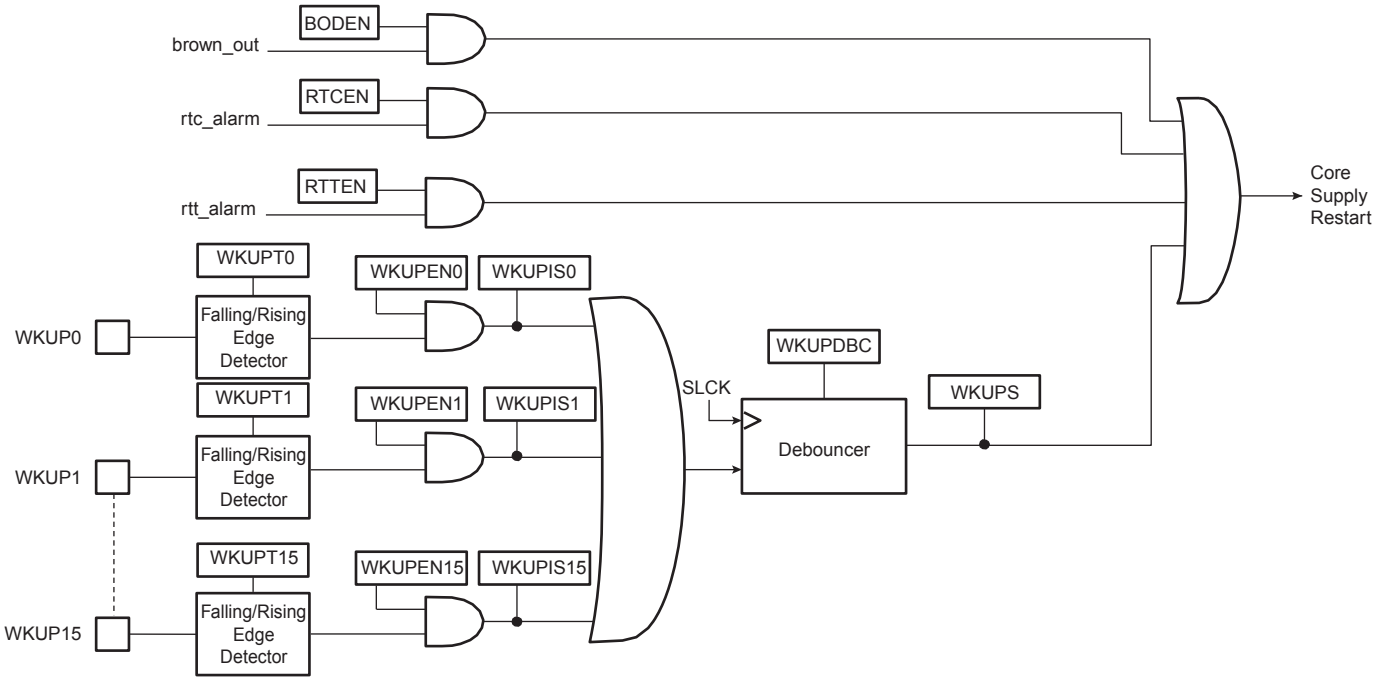
Note: Restrictions
With Main Supply < 3V, ADC and DAC are not usable.
With Main Supply >= 3V, all peripherals are usable.

Figure 5-3 below provides an example of the powering scheme when using a backup battery. Since the PIO state is preserved when in backup mode, any free PIO line can be used to switch off the external regulator by driving the PIO line at low level (PIO is input, pull-up enabled after backup reset). External wake-up of the system can be from a push button or any signal. See Section 5.6 “Wake-up Sources” for further details.TFBGA

5.6 Wake-up Sources

The wake-up events allow the device to exit backup mode. When a wake-up event is detected, the Supply Controller performs a sequence which automatically reenables the core power supply and the SRAM power supply, if they are not already enabled.

Figure 5-4. Wake-up Source



6.3 Test Pin

The TST pin is used for JTAG Boundary Scan Manufacturing Test or Fast Flash programming mode of the SAM3N series. The TST pin integrates a permanent pull-down resistor of about 15 kΩ to GND, so that it can be left unconnected for normal operations. To enter fast programming mode, see the Fast Flash Programming Interface (FFPI) section. For more on the manufacturing and test mode, refer to the “Debug and Test” section of the product datasheet.

6.4 NRST Pin

The NRST pin is bidirectional. It is handled by the on-chip reset controller and can be driven low to provide a reset signal to the external components or asserted low externally to reset the microcontroller. It will reset the Core and the peripherals except the Backup region (RTC, RTT and Supply Controller). There is no constraint on the length of the reset pulse and the reset controller can guarantee a minimum pulse length. The NRST pin integrates a permanent pull-up resistor to VDDIO of about 100 kΩ . By default, the NRST pin is configured as an input.

6.5 ERASE Pin

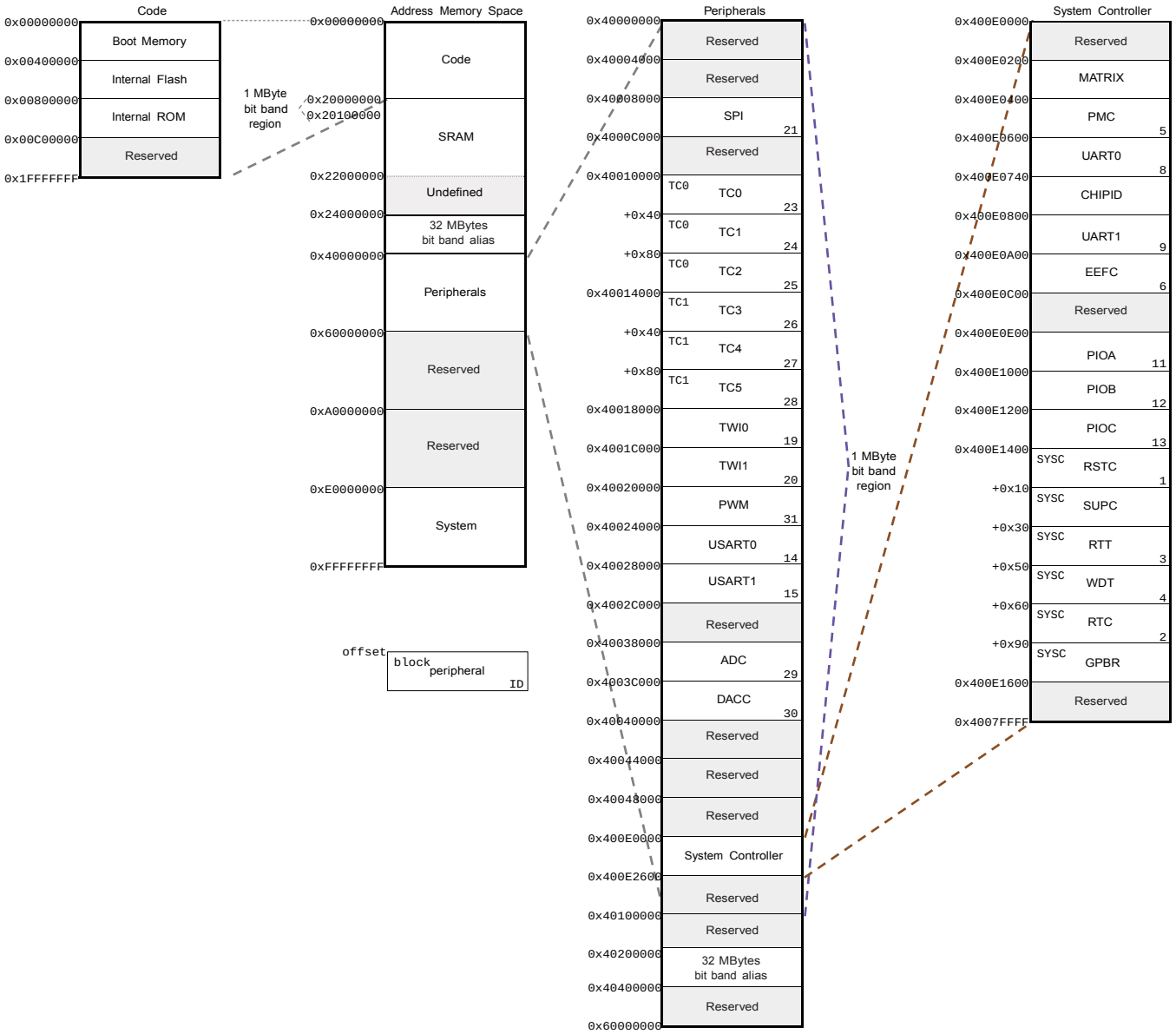
The ERASE pin is used to reinitialize the Flash content (and some of its NVM bits) to an erased state (all bits read as logic level 1). It integrates a pull-down resistor of about 100 kΩ to GND, so that it can be left unconnected for normal operations.

This pin is debounced by SCLK to improve the glitch tolerance. When the ERASE pin is tied high during less than 100 ms, it is not taken into account. The pin must be tied high during more than 220 ms to perform a Flash erase operation.

The ERASE pin is a system I/O pin and can be used as a standard I/O. At startup, the ERASE pin is not configured as a PIO pin. If the ERASE pin is used as a standard I/O, startup level of this pin must be low to prevent unwanted erasing. Please refer to Section 11.2 “Peripheral Signals Multiplexing on I/O Lines” on page 42. Also, if the ERASE pin is used as a standard I/O output, asserting the pin to low does not erase the Flash.

8. Product Mapping

Figure 8-1. SAM3N4/2/1/0/00 Product Mapping



9.1.3.9 *Fast Flash Programming Interface*

The Fast Flash Programming Interface allows programming the device through either a serial JTAG interface or through a multiplexed fully-handshaked parallel port. It allows gang programming with market-standard industrial programmers.

The FFPI supports read, page program, page erase, full erase, lock, unlock and protect commands.

The Fast Flash Programming Interface is enabled and the Fast Programming Mode is entered when TST and PA0 and PA1are tied low.

9.1.3.10 *SAM-BA Boot*

The SAM-BA Boot is a default Boot Program which provides an easy way to program in-situ the on-chip Flash memory.

The SAM-BA Boot Assistant supports serial communication via the UART0.

The SAM-BA Boot provides an interface with SAM-BA Graphic User Interface (GUI).

The SAM-BA Boot is in ROM and is mapped in Flash at address 0x0 when GPNVM bit 1 is set to 0.

9.1.3.11 *GPNVM Bits*

The SAM3N features three GPNVM bits that can be cleared or set respectively through the commands “Clear GPNVM Bit” and “Set GPNVM Bit” of the EEFC User Interface.

.

Table 9-2. General-purpose Non volatile Memory Bits

GPNVMBit[#]	Function
0	Security bit
1	Boot mode selection

9.1.4 Boot Strategies

The system always boots at address 0x0. To ensure a maximum boot possibilities the memory layout can be changed via GPNVM.

A general purpose NVM (GPNVM) bit is used to boot either on the ROM (default) or from the Flash.

The GPNVM bit can be cleared or set respectively through the commands “Clear General-purpose NVM Bit” and “Set General-purpose NVM Bit” of the EEFC User Interface.

Setting the GPNVM Bit 1 selects the boot from the Flash, clearing it selects the boot from the ROM. Asserting ERASE clears the GPNVM Bit 1 and thus selects the boot from the ROM by default.

10. System Controller

The System Controller is a set of peripherals, which allow handling of key elements of the system, such as power, resets, clocks, time, interrupts, watchdog, etc...

See the System Controller block diagram in Figure 10-1 on page 35.

10.13 Chip Identification

- Chip Identifier (CHIPID) registers permit recognition of the device and its revision.

Table 10-1. SAM3N Chip ID Register

Chip Name	CHIPID_CIDR	CHIPID_EXID
ATSAM3N4C (Rev A)	0x29540960	0x0
ATSAM3N2C (Rev A)	0x29590760	0x0
ATSAM3N1C (Rev A)	0x29580560	0x0
ATSAM3N4B (Rev A)	0x29440960	0x0
ATSAM3N2B (Rev A)	0x29490760	0x0
ATSAM3N1B (Rev A)	0x29480560	0x0
ATSAM3N4A (Rev A)	0x29340960	0x0
ATSAM3N2A (Rev A)	0x29390760	0x0
ATSAM3N1A (Rev A)	0x29380560	0x0

- JTAG ID: 0x05B2E03F

10.14 UART

- Two-pin UART
  - Implemented features are 100% compatible with the standard Atmel USART
  - Independent receiver and transmitter with a common programmable Baud Rate Generator
  - Even, Odd, Mark or Space Parity Generation
  - Parity, Framing and Overrun Error Detection
  - Automatic Echo, Local Loopback and Remote Loopback Channel Modes
  - Support for two PDC channels with connection to receiver and transmitter

10.15 PIO Controllers

- 3 PIO Controllers, PIOA, PIOB and PIOC (100-pin version only) controlling a maximum of 79 I/O Lines
- Each PIO Controller controls up to 32 programmable I/O Lines
- Fully programmable through Set/Clear Registers

Table 10-2. PIO available according to pin count

Version	48 pin	64 pin	100 pin
PIOA	21	32	32
PIOB	13	15	15
PIOC	-	-	32

- Multiplexing of four peripheral functions per I/O Line
- For each I/O Line (whether assigned to a peripheral or used as general purpose I/O)
  - Input change, rising edge, falling edge, low level and level interrupt
  - Debouncing and Glitch filter

  - Multi-drive option enables driving in open drain
  - Programmable pull up on each I/O line
  - Pin data status register, supplies visibility of the level on the pin at any time
- Selection of the drive level
- Synchronous output, provides Set and Clear of several I/O lines in a single write

11. Peripherals

11.1 Peripheral Identifiers

Table 11-1 defines the Peripheral Identifiers of the SAM3N4/2/1/0/00. A peripheral identifier is required for the control of the peripheral interrupt with the Nested Vectored Interrupt Controller and for the control of the peripheral clock with the Power Management Controller.

Table 11-1. Peripheral Identifiers

Instance ID	Instance Name	NVIC Interrupt	PMC Clock Control	Instance Description
0	SUPC	**X**		**Supply Controller**
1	RSTC	**X**		Reset Controller
2	RTC	**X**		Real Time Clock
3	RTT	**X**		Real Time Timer
4	WDT	**X**		Watchdog Timer
5	PMC	**X**		Power Management Controller
6	EEFC	**X**		Enhanced Flash Controller
7	-	**-**		Reserved
8	UART0	**X**	**X**	UART 0
9	UART1	**X**	**X**	UART 1
10	-	**-**	**-**	Reserved
11	PIOA	**X**	**X**	Parallel I/O Controller A
12	PIOB	**X**	**X**	Parallel I/O Controller B
13	PIOC	**X**	**X**	Parallel I/O Controller C
14	USART0	**X**	**X**	USART 0
15	USART1	**X**	**X**	USART 1
16	-	**-**	**-**	Reserved
17	-	**-**	**-**	Reserved
18	-	**-**	**-**	Reserved
19	TWI0	**X**	**X**	Two Wire Interface 0
20	TWI1	**X**	**X**	Two Wire Interface 1
21	SPI	**X**	**X**	Serial Peripheral Interface
22	-	**-**	**-**	Reserved
23	TC0	**X**	**X**	Timer/Counter 0
24	TC1	**X**	**X**	Timer/Counter 1

Table 11-1. Peripheral Identifiers (Continued)

Instance ID	Instance Name	NVIC Interrupt	PMC Clock Control	Instance Description
25	TC2	**X**	**X**	Timer/Counter 2
26	TC3	**X**	**X**	Timer/Counter 3
27	TC4	**X**	**X**	Timer/Counter 4
28	TC5	**X**	**X**	Timer/Counter 5
29	ADC	**X**	**X**	Analog-to-Digital Converter
30	DACC	**X**	**X**	Digital-to-Analog Converter
31	PWM	**X**	**X**	Pulse Width Modulation

11.2 Peripheral Signals Multiplexing on I/O Lines

The SAM3N product features 2 PIO controllers (48-pin and 64-pin version) or 3 PIO controllers (100-pin version), PIOA, PIOB and PIOC, that multiplex the I/O lines of the peripheral set.

The SAM3N 64-pin and 100-pin PIO Controller controls up to 32 lines (see Table 10-2, “PIO available according to pin count,” on page 40). Each line can be assigned to one of three peripheral functions: A, B or C. The multiplexing tables in the following paragraphs define how the I/O lines of the peripherals A, B and C are multiplexed on the PIO Controllers. The column “Comments” has been inserted in this table for the user’s own comments; it may be used to track how pins are defined in an application.

Note that some peripheral functions which are output only, might be duplicated within the tables.

11.2.3 PIO Controller C Multiplexing

I/O Line	Peripheral A	Peripheral B	Peripheral C	Extra Function	System Function	Comments
PC0						100-pin version
PC1						100-pin version
PC2						100-pin version
PC3						100-pin version
PC4		NPCS1				100-pin version
PC5						100-pin version
PC6						100-pin version
PC7		NPCS2				100-pin version
PC8		PWM0				100-pin version
PC9		PWM1				100-pin version
PC10		PWM2				100-pin version
PC11		PWM3				100-pin version
PC12				AD12		100-pin version
PC13				AD10		100-pin version
PC14		PCK2				100-pin version
PC15				AD11		100-pin version
PC16		PCK0				100-pin version
PC17		PCK1				100-pin version
PC18		PWM0				100-pin version
PC19		PWM1				100-pin version
PC20		PWM2				100-pin version
PC21		PWM3				100-pin version
PC22		PWM0				100-pin version
PC23		TIOA3				100-pin version
PC24		TIOB3				100-pin version
PC25		TCLK3				100-pin version
PC26		TIOA4				100-pin version
PC27		TIOB4				100-pin version
PC28		TCLK4				100-pin version
PC29		TIOA5		AD13		100-pin version
PC30		TIOB5		AD14		100-pin version
PC31		TCLK5		AD15		100-pin version

Figure 13-3. 64and4B·leadLQFP Package Drawing

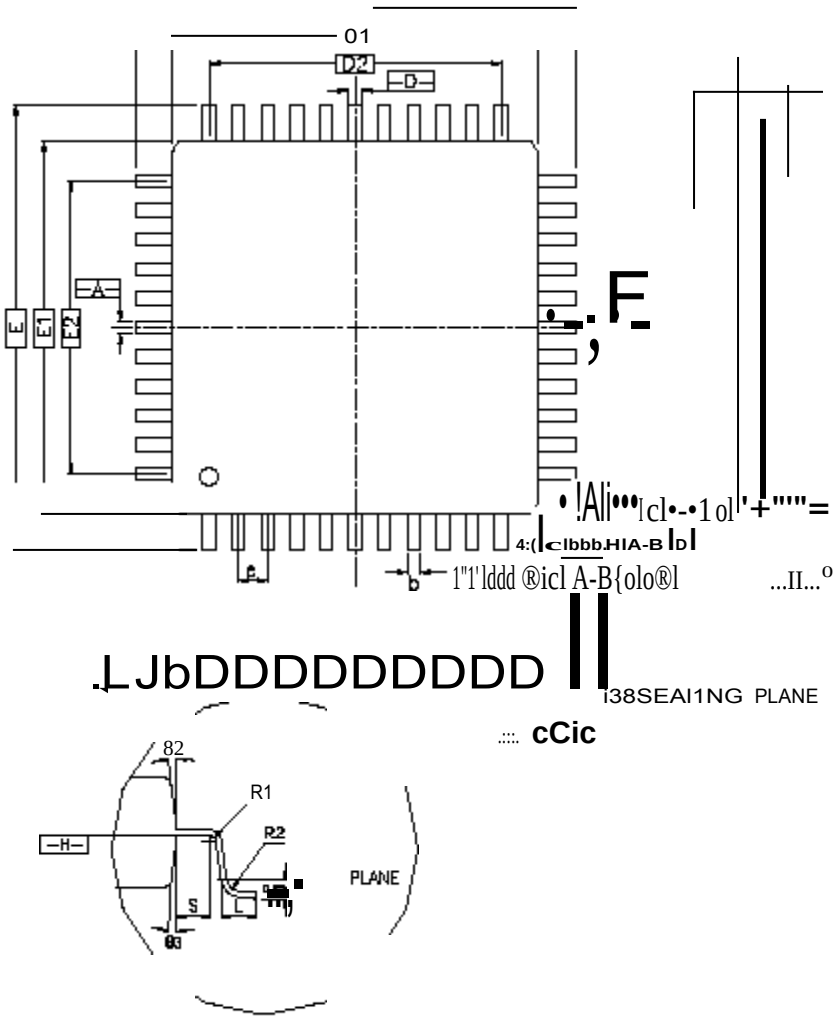
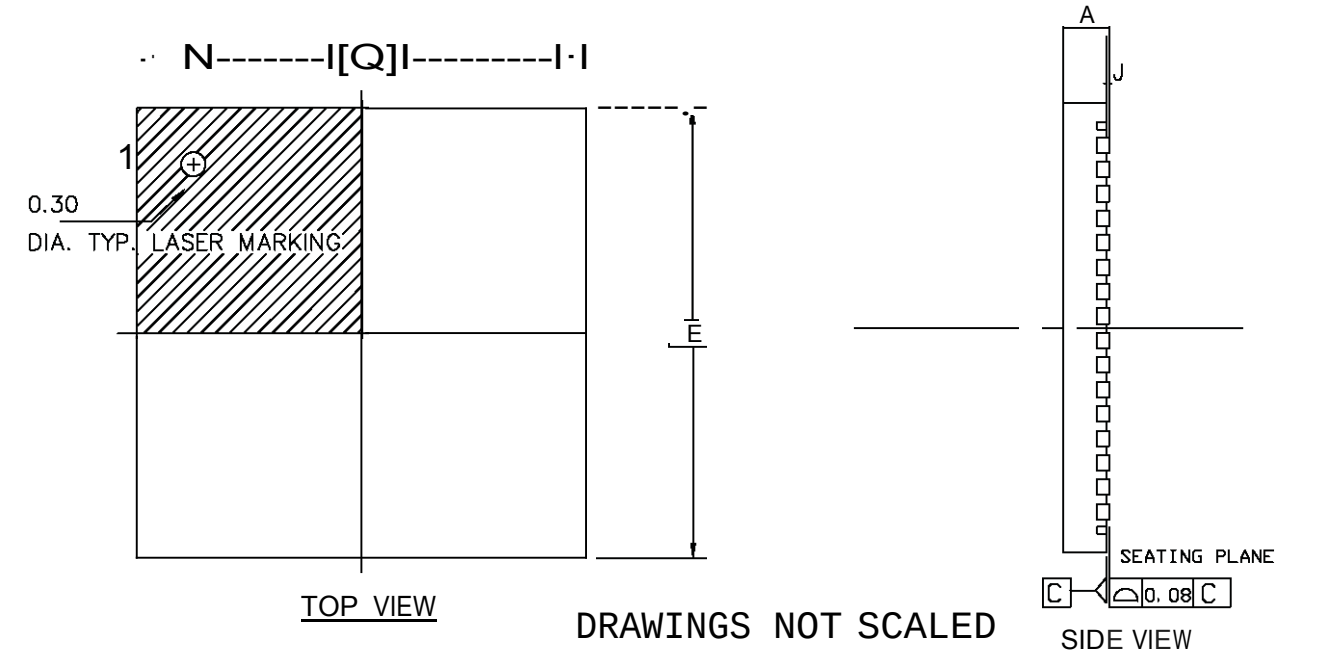
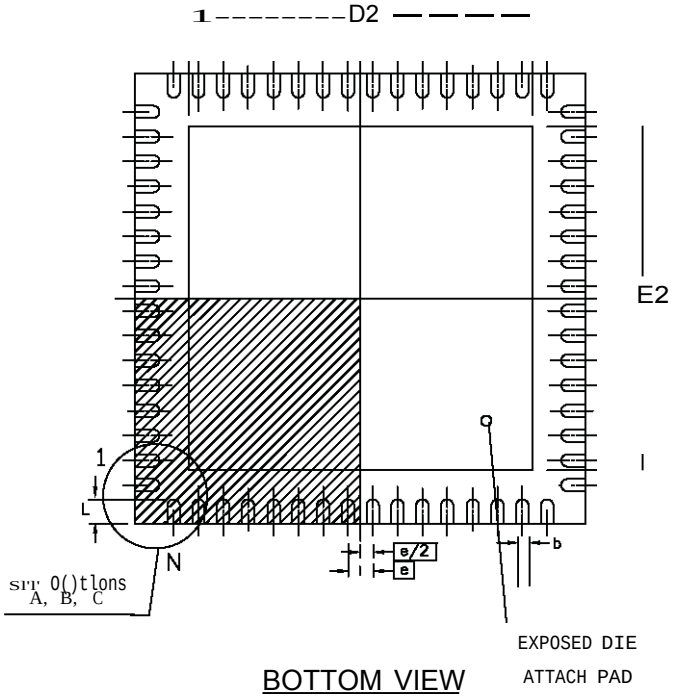


Table 13-1. 48-lead LQFP Package Dimensions (in mm)

Symbol	Millimeter			Inch		
	Min	**Nom**	**Max**	**Min**	**Nom**	**Max**
A	–	–	1.60	–	–	0.063
A1	0.05	–	0.15	0.002	–	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
D	9.00 BSC			0.354 BSC		
D1	7.00 BSC			0.276 BSC		
E	9.00 BSC			0.354 BSC		
E1	7.00 BSC			0.276 BSC		
R2	0.08	–	0.20	0.003	–	0.008
R1	0.08	–	–	0.003	–	–
q	0°	3.5°	7°	0°	3.5°	7°
θ_1	0°	–	–	0°	–	–
θ_2	11°	12°	13°	11°	12°	13°
θ_3	11°	12°	13°	11°	12°	13°
c	0.09	–	0.20	0.004	–	0.008
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF			0.039 REF		
S	0.20	–	–	0.008	–	–
b	0.17	0.20	0.27	0.007	0.008	0.011
e	0.50 BSC.			0.020 BSC.		
D2	5.50			0.217		
E2	5.50			0.217		
Tolerances of Form and Position						
aaa	0.20			0.008		
bbb	0.20			0.008		
ccc	0.08			0.003		
ddd	0.08			0.003		

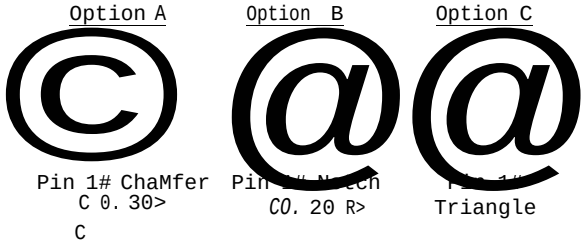
Figure 13-5. 64-pad QFN Package Drawing





COMMON DIMENSIONS IN MM

SYMBOL	MIN.	NOM.	MAX.	NOTES
A	0.80	----	1.00	
j	0.00	----	0.05	
D/E	9.00 BSC			
D2/E2	3.25	----	7.50	
N	64			
e	0.50 BSC			
L	0.30	0.40	0.55	
lo	0.18	0.25	0.30	



14. Ordering Information

Table 14-1.

Ordering Code	MRL	Flash (Kbytes)	Package	Package Type	Temperature Operating Range
ATSAM3N4CA-AU	A	256	LQFP100	Green	Industrial -40°C to 85°C
ATSAM3N4CA-CU	A	256	TFBGA100	Green	Industrial -40°C to 85°C
ATSAM3N4BA-AU	A	256	LQFP64	Green	Industrial -40°C to 85°C
ATSAM3N4BA-MU	A	256	QFN64	Green	Industrial -40°C to 85°C
ATSAM3N4AA-AU	A	256	LQFP48	Green	Industrial -40°C to 85°C
ATSAM3N4AA-MU	A	256	QFN48	Green	Industrial -40°C to 85°C
ATSAM3N2CA-AU	A	128	LQFP100	Green	Industrial -40°C to 85°C
ATSAM3N2CA-CU	A	128	TFBGA100	Green	Industrial -40°C to 85°C
ATSAM3N2BA-AU	A	128	LQFP64	Green	Industrial -40°C to 85°C
ATSAM3N2BA-MU	A	128	QFN64	Green	Industrial -40°C to 85°C
ATSAM3N2AA-AU	A	128	LQFP48	Green	Industrial -40°C to 85°C
ATSAM3N2AA-MU	A	128	QFN48	Green	Industrial -40°C to 85°C
ATSAM3N1CA-AU	A	64	LQFP100	Green	Industrial -40°C to 85°C
ATSAM3N1CB-AU	B	64	LQFP100	Green	Industrial -40°C to 85°C
ATSAM3N1CA-CU	A	64	TFBGA100	Green	Industrial -40°C to 85°C
ATSAM3N1CB-CU	B	64	TFBGA100	Green	Industrial -40°C to 85°C
ATSAM3N1BA-AU	A	64	LQFP64	Green	Industrial -40°C to 85°C
ATSAM3N1BB-AU	B	64	LQFP64	Green	Industrial -40°C to 85°C
ATSAM3N1BA-MU	A	64	QFN 64	Green	Industrial -40°C to 85°C
ATSAM3N1BB-MU	B	64	QFN 64	Green	Industrial -40°C to 85°C

58 SAM3N Summary