Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	I²C, IrDA, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	47
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.62V ~ 3.6V
Data Converters	A/D 10x10b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atsam3n0ba-au

1.1 Configuration Summary

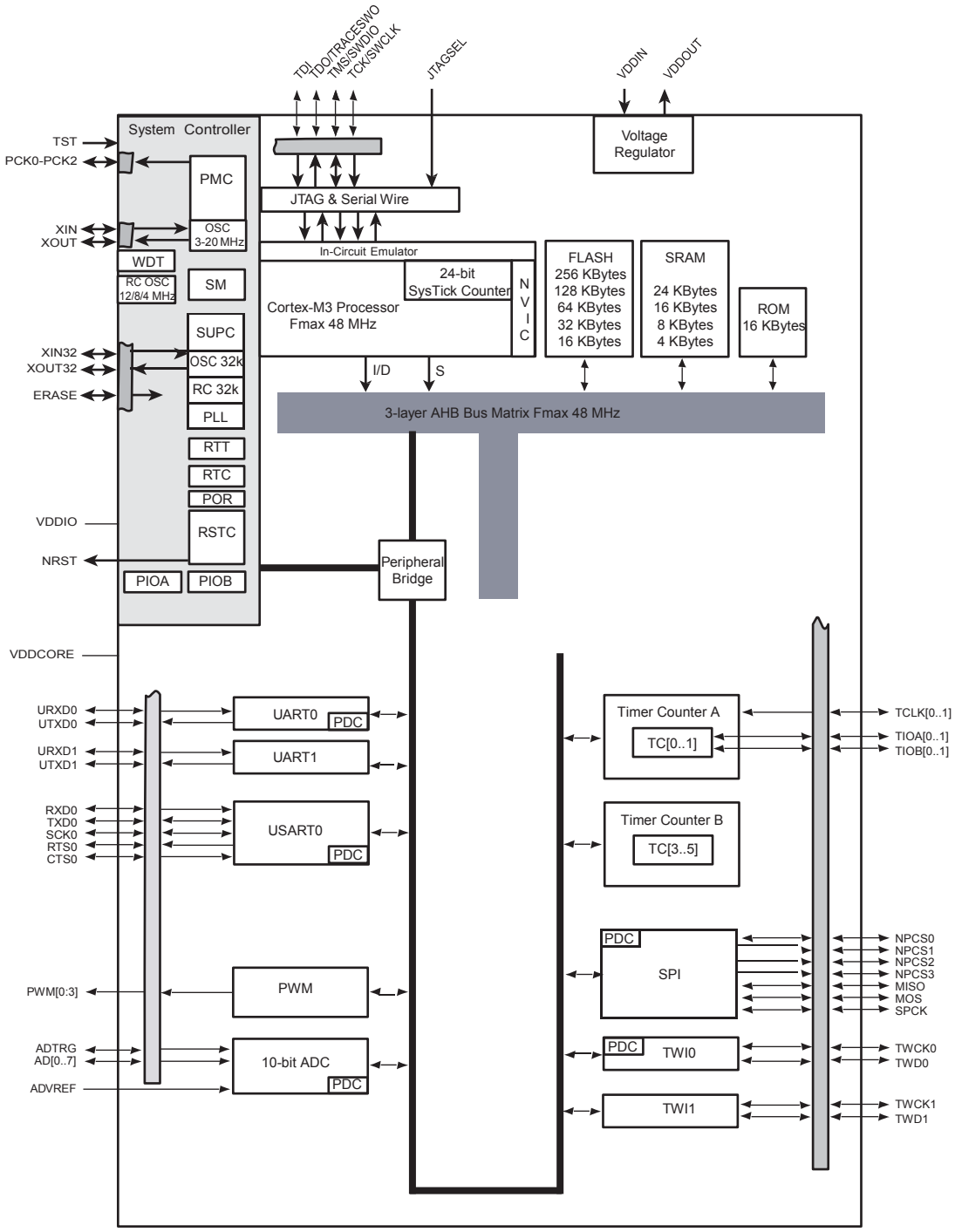
The SAM3N4/2/1/0/00 differ in memory size, package and features list. Table 1-1 summarizes the configurations of the 9 devices.

Table 1-1. Configuration Summary

Device	Flash	SRAM	Package	Number of PIOs	ADC	Timer	PDC Channels	USART	DAC
SAM3N4A	256 Kbytes	24 Kbytes	LQFP48 QFN48	34	8 channels	6(1)	8	1	_
SAM3N4B	256 Kbytes	24 Kbytes	LQFP64 QFN64	47	10 channels	6(2)	10	2	1
SAM3N4C	256 Kbytes	24 Kbytes	LQFP100 BGA100	79	16 channels	6	10	2	1
SAM3N2A	128 Kbytes	16 Kbytes	LQFP48 QFN48	34	8 channels	6(1)	8	1	_
SAM3N2B	128 Kbytes	16 Kbytes	LQFP64 QFN64	47	10 channels	6((2)	10	2	1
SAM3N2C	128 Kbytes	16 Kbytes	LQFP100 BGA100	79	16 channels	6	10	2	1
SAM3N1A	64 Kbytes	8 Kbytes	LQFP48 QFN48	34	8 channels	6(1)	8	1	_
SAM3N1B	64 Kbytes	8 Kbytes	LQFP64 QFN64	47	10 channels	6(2)	10	2	1
SAM3N1C	64 Kbytes	8 Kbytes	LQFP100 BGA100	79	16 channels	6	10	2	1
SAM3N0A	32 Kbytes	8 Kbytes	LQFP48 QFN48	34	8 channels	6(1)	8	1	_
SAM3N0B	32 Kbytes	8 Kbytes	LQFP64 QFN64	47	10 channels	6(2)	10	2	1
SAM3N0C	32 Kbytes	8 Kbytes	LQFP100 BGA100	79	16 channels	6	10	2	1
SAM3N00A	16 Kbytes	4 KBytes	LQFP48 QFN48	34	8 channels	6(1)	8	1	_
SAM3N00B	16 Kbytes	4 KBytes	LQFP64 QFN64	47	10 channels	6(2)	10	2	1

Notes: 1. Only two TC channels are accessible through the PIO.
2. Only three TC channels are accessible through the PIO.

Figure 2-3. SAM3N 48-pin version Block Diagramz



3. Signal Description

Table 3-1 gives details on the signal name classified by peripheral.

Table 3-1. Signal Description List

Signal Name	Function	Type	Active Level	Voltage Reference	Comments
Power Supplies					
VDDIO	Peripherals I/O Lines Power Supply	Power			1.62V to 3.6V
VDDIN	Voltage Regulator, ADC and DAC Power Supply	Power			1.8V to 3.6V(3)
VDDOUT	Voltage Regulator Output	Power			1.8V Output
VDDPLL	Oscillator and PLL Power Supply	Power			1.65 V to 1.95V
VDDCORE	Power the core, the embedded memories and the peripherals	Power			1.65V to 1.95V Connected externally to VDDOUT
GND	Ground	Ground			
Clocks, Oscillators and PLLs					
XIN	Main Oscillator Input	Input		VDDIO	Reset State: - PIO Input - Internal Pull-up disabled - Schmitt Trigger enabled(1)
XOUT	Main Oscillator Output	Output			
XIN32	Slow Clock Oscillator Input	Input			
XOUT32	Slow Clock Oscillator Output	Output			
PCK0 - PCK2	Programmable Clock Output	Output			Reset State: - PIO Input - Internal Pull-up enabled - Schmitt Trigger enabled(1)
ICE and JTAG					
TCK/SWCLK	Test Clock/Serial Wire Clock	Input		VDDIO	Reset State: - SWJ-DP Mode - Internal pull-up disabled - Schmitt Trigger enabled(1)
TDI	Test Data In	Input			
TDO/TRACESWO	Test Data Out/Trace Asynchronous Data Out	Output			
TMS/SWDIO	Test Mode Select /Serial Wire Input/Output	Input / I/O			
JTAGSEL	JTAG Selection	Input	High		Permanent Internal pull-down

4.2 SAM3N4/2/1/0/00B Package and Pinout

Figure 4-3. Orientation of the 64-pad QFN Package

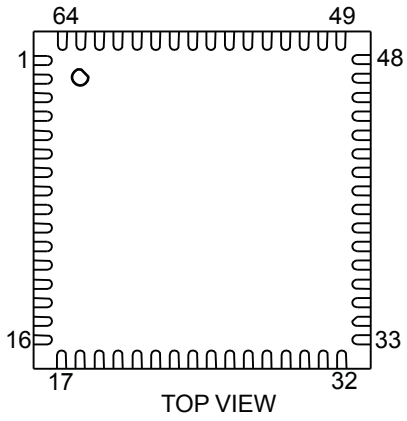
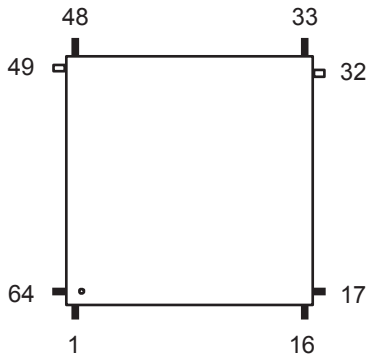


Figure 4-4. Orientation of the 64-lead LQFP Package



4.2.1 64-Lead LQFP and QFN Pinout

64-pin version SAM3N devices are pin-to-pin compatible with SAM3S products. Furthermore, SAM3N products have new functionalities shown in italic in Table 4-3.

Table 4-3. 64-pin SAM3N4/2/1/0/00B Pinout

1	ADVREF	17	GND	33	*TDI/PB4*	49	*TDO/TRACESWO/PB5*
2	GND	18	VDDIO	34	PA6/PGMNOE	50	JTAGSEL
3	*PB0/AD4*	19	PA16/PGMD4	35	PA5/PGMRDY	51	*TMS/SWDIO/PB6*
4	*PB1AD5*	20	PA15/PGMD3	36	PA4/PGMNCMD	52	PA31
5	*PB2/AD6*	21	PA14/PGMD2	37	PA27/PGMD15	53	*TCK/SWCLK/PB7*
6	*PB3/AD7*	22	PA13/PGMD1	38	PA28	54	VDDCORE
7	VDDIN	23	PA24/PGMD12	39	NRST	55	*ERASE/PB12*
8	VDDOUT	24	VDDCORE	40	TST	56	*PB10*
9	PA17/PGMD5/AD0	25	PA25/PGMD13	41	PA29	57	*PB11*
10	PA18/PGMD6/AD1	26	PA26/PGMD14	42	PA30	58	VDDIO
11	PA21/PGMD9/AD8	27	PA12/PGMD0	43	PA3	59	*PB13/DAC0*
12	VDDCORE	28	PA11/PGMM3	44	PA2/PGMEN2	60	GND
13	PA19/PGMD7/AD2	29	PA10/PGMM2	45	VDDIO	61	*XOUT/PB8*
14	PA22/PGMD10/AD9	30	PA9/PGMM1	46	GND	62	*XIN/PGMCK/PB9*
15	PA23/PGMD11	31	PA8/XOUT32/PGMM0	47	PA1/PGMEN1	63	*PB14*
16	PA20/PGMD8/AD3	32	PA7/XIN32/XOUT32/PGMNVALID	48	PA0/PGMEN0	64	VDDPLL

Note: The bottom pad of the QFN package must be connected to ground.

- Supply Monitor alarm
- RTC alarm
- RTT alarm

5.5.2 Wait Mode

The purpose of the wait mode is to achieve very low power consumption while maintaining the whole device in a powered state for a startup time of less than 10 µs. Current Consumption in Wait mode is typically 15 µA (total current consumption) if the internal voltage regulator is used or 8 µA if an external regulator is used.

In this mode, the clocks of the core, peripherals and memories are stopped. However, the core, peripherals and memories power supplies are still powered. From this mode, a fast start up is available.

This mode is entered via Wait for Event (WFE) instructions with LPM = 1 (Low Power Mode bit in PMC_FSMR). The Cortex-M3 is able to handle external or internal events in order to wake up the core (WFE). By configuring the WUP0-15 external lines as fast startup wake-up pins (refer to Section 5.7 “Fast Start-Up”). RTC or RTT Alarm wake-up events can be used to wake up the CPU (exit from WFE).

Entering Wait Mode:

- Select the 4/8/12 MHz fast RC oscillator as Main Clock
- Set the LPM bit in the PMC Fast Startup Mode Register (PMC_FSMR)
- Execute the Wait-For-Event (WFE) instruction of the processor

Note: Internal Main clock resynchronization cycles are necessary between the writing of MOSCRCEN bit and the effective entry in Wait mode. Depending on the user application, Waiting for MOSCRCEN bit to be cleared is recommended to ensure that the core will not execute undesired instructions.

5.5.3 Sleep Mode

The purpose of sleep mode is to optimize power consumption of the device versus response time. In this mode, only the core clock is stopped. The peripheral clocks can be enabled. The current consumption in this mode is application dependent.

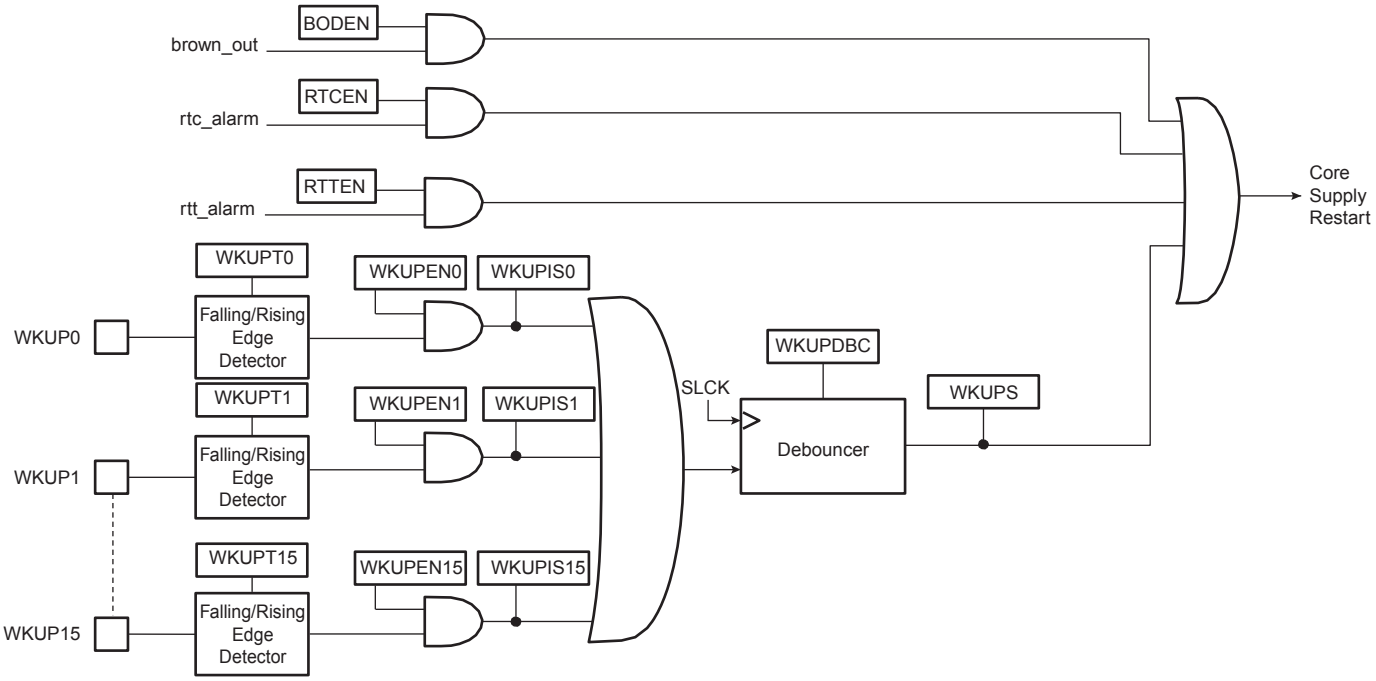
This mode is entered via Wait for Interrupt (WFI) or Wait for Event (WFE) instructions with LPM = 0 in PMC_FSMR.

The processor can be woke up from an interrupt if WFI instruction of the Cortex M3 is used, or from an event if the WFE instruction is used to enter this mode.

5.6 Wake-up Sources

The wake-up events allow the device to exit backup mode. When a wake-up event is detected, the Supply Controller performs a sequence which automatically reenables the core power supply and the SRAM power supply, if they are not already enabled.

Figure 5-4. Wake-up Source



7.5 Master to Slave Access

All the Masters can normally access all the Slaves. However, some paths do not make sense, for example allowing access from the Cortex-M3 S Bus to the Internal ROM. Thus, these paths are forbidden or simply not wired, and shown as "-" in Table 7-3.

Table 7-3. SAM3N Master to Slave Access

Masters		0	1	2
Slaves		Cortex-M3 I/D Bus	Cortex-M3 S Bus	PDC
0	Internal SRAM	-	X	X
1	Internal ROM	X	-	X
2	Internal Flash	X	-	-
3	Peripheral Bridge	-	X	X

7.6 Peripheral DMA Controller

- Handles data transfer between peripherals and memories
- Low bus arbitration overhead
  - One Master Clock cycle needed for a transfer from memory to peripheral
  - Two Master Clock cycles needed for a transfer from peripheral to memory
- Next Pointer management for reducing interrupt latency requirement

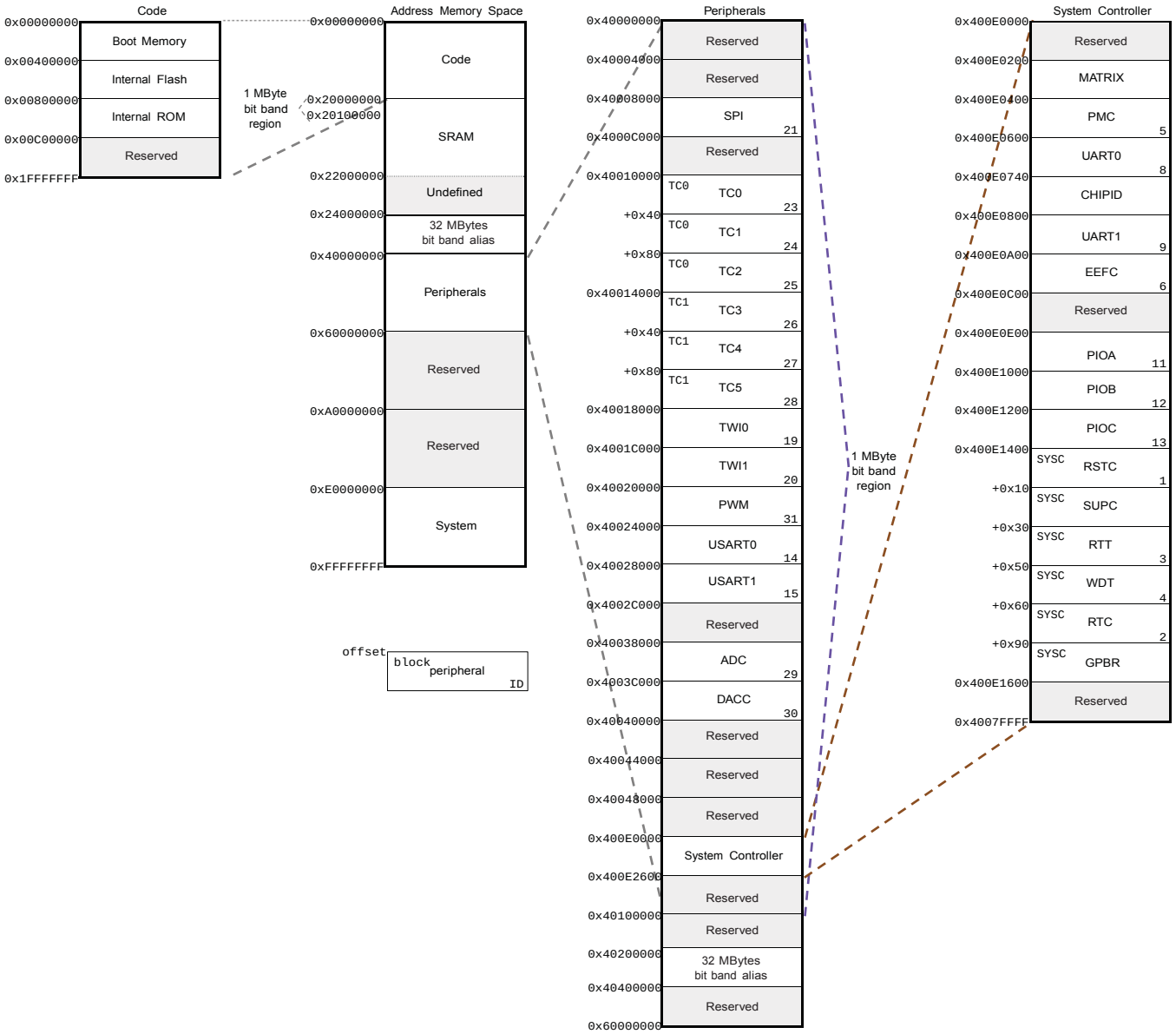
The Peripheral DMA Controller handles transfer requests from the channel according to the following priorities (Low to High priorities):

Table 7-4. Peripheral DMA Controller

Instance name	Channel T/R	100 & 64 Pins	48 Pins
TWI0	Transmit	x	x
UART0	Transmit	x	x
USART0	Transmit	x	x
DAC	Transmit	x	N/A
SPI	Transmit	x	x
TWI0	Receive	x	x
UART0	Receive	x	x
USART0	Receive	x	x
ADC	Receive	x	x
SPI	Receive	x	x

8. Product Mapping

Figure 8-1. SAM3N4/2/1/0/00 Product Mapping

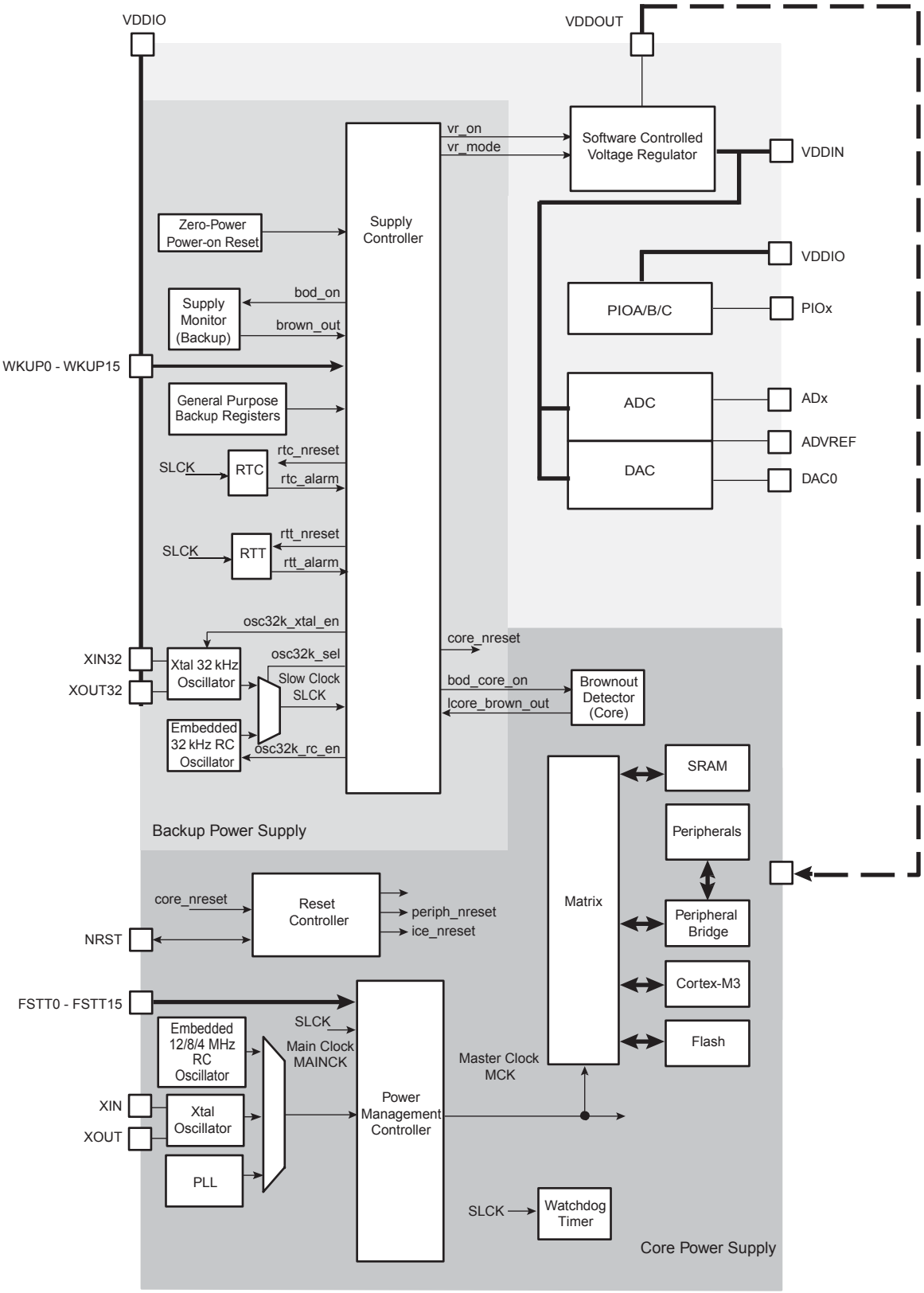


10. System Controller

The System Controller is a set of peripherals, which allow handling of key elements of the system, such as power, resets, clocks, time, interrupts, watchdog, etc...

See the System Controller block diagram in Figure 10-1 on page 35.

Figure 10-1. System Controller Block Diagram



FSTT0 - FSTT15 are possible Fast Startup Sources, generated by WKUP0-WKUP15 Pins, but are not physical pins.

The reset circuitry is based on a zero-power power-on reset cell and a brownout detector cell. The zero-power power-on reset allows the Supply Controller to start properly, while the software-programmable brownout detector allows detection of either a battery discharge or main voltage loss.

The Slow Clock generator is based on a 32 kHz crystal oscillator and an embedded 32 kHz RC oscillator. The Slow Clock defaults to the RC oscillator, but the software can enable the crystal oscillator and select it as the Slow Clock source.

The Supply Controller starts up the device by sequentially enabling the internal power switches and the Voltage Regulator, then it generates the proper reset signals to the core power supply.

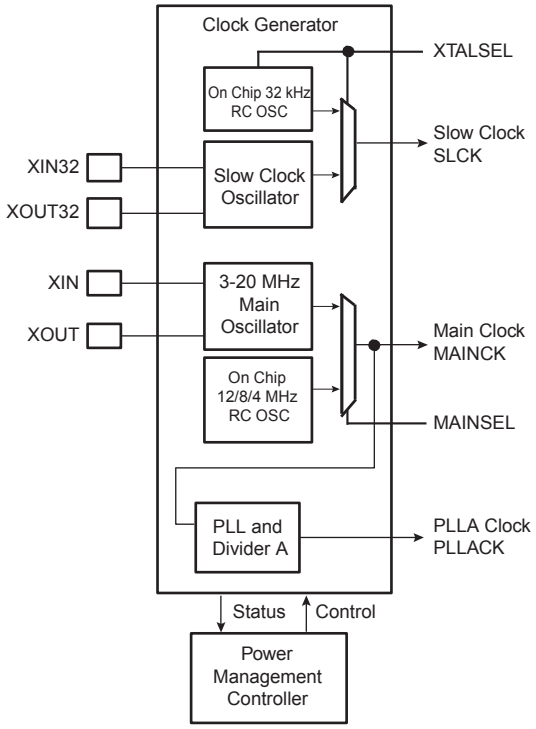
It also enables to set the system in different low power modes and to wake it up from a wide range of events.

10.5 Clock Generator

The Clock Generator is made up of:

- One Low Power 32768Hz Slow Clock Oscillator with bypass mode
- One Low-Power RC Oscillator
- One 3-20 MHz Crystal or Ceramic resonator Oscillator, which can be bypassed
- One Fast RC Oscillator factory programmed, 3 output frequencies can be selected: 4, 8 or 12 MHz. By default 4 MHz is selected.
- One 60 to 130 MHz programmable PLL, capable to provide the clock MCK to the processor and to the peripherals. The input frequency of PLL is from 3.5 to 20 MHz.

Figure 10-2. Clock Generator Block Diagram



10.6 Power Management Controller

The Power Management Controller provides all the clock signals to the system. It provides:

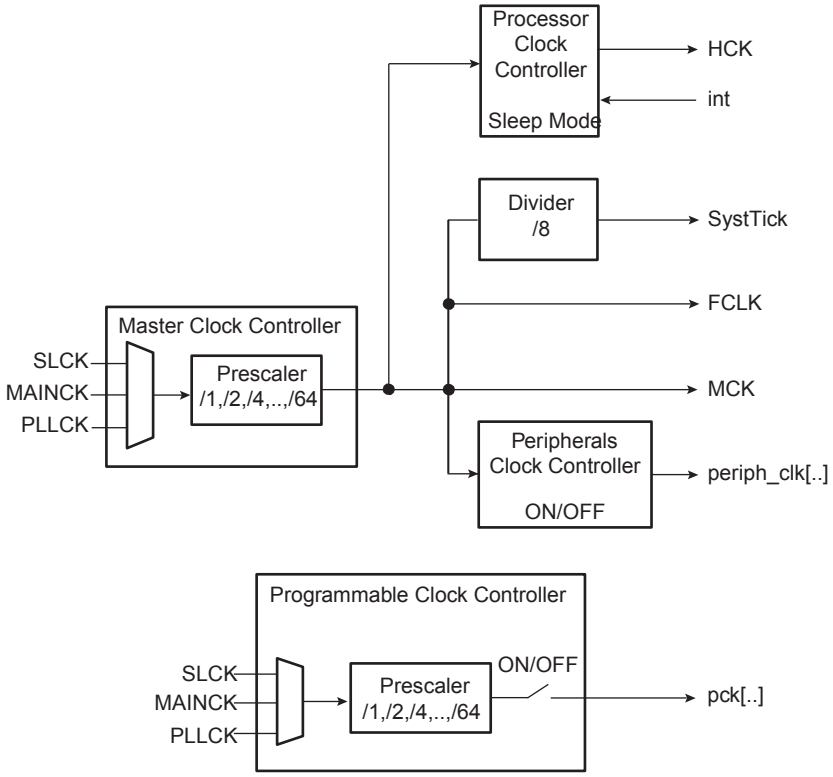
- the Processor Clock HCLK
- the Free running processor clock FCLK
- the Cortex SysTick external clock
- the Master Clock MCK, in particular to the Matrix and the memory interfaces
- independent peripheral clocks, typically at the frequency of MCK
- three programmable clock outputs: PCK0, PCK1 and PCK2

The Supply Controller selects between the 32 kHz RC oscillator or the crystal oscillator. The unused oscillator is disabled automatically so that power consumption is optimized.

By default, at startup the chip runs out of the Master Clock using the Fast RC Oscillator running at 4 MHz.

The user can trim by software the 8 and 12 MHz RC Oscillator frequency.

Figure 10-3. SAM3N4/2/1/0/00 Power Management Controller Block Diagram



The SysTick calibration value is fixed at 6000 which allows the generation of a time base of 1 ms with SysTick clock at 6 MHz (48 MHz/8)

10.7 Watchdog Timer

- 16-bit key-protected only-once-Programmable Counter
- Windowed, prevents the processor to be in a dead-lock on the watchdog access

11.2.2 PIO Controller B Multiplexing

Table 11-3. Multiplexing on PIO Controller B (PIOB)

I/O Line	Peripheral A	Peripheral B	Peripheral C	Extra Function	System Function	Comments
PB0	PWM0			AD4		
PB1	PWM1			AD5		
PB2	URXD1	NPCS2		AD6/WKUP12		
PB3	UTXD1	PCK2		AD7		
PB4	TWD1	PWM2			TDI	
PB5	TWCK1			WKUP13	TDO/ TRACESWO	
PB6					TMS/SWDIO	
PB7					TCK/SWCLK	
PB8					XOUT	
PB9					XIN	
PB10						
PB11						
PB12					ERASE	
PB13		PCK0		DAC0		64/100-pin versions
PB14	NPCS1	PWM3				64/100-pin versions

12. Embedded Peripherals Overview

12.1 Serial Peripheral Interface (SPI)

- Supports communication with serial external devices
  - Four chip selects with external decoder support allow communication with up to 15 peripherals
  - Serial memories, such as DataFlash and 3-wire EEPROMs
  - Serial peripherals, such as ADCs, DACs, LCD Controllers, CAN Controllers and Sensors
  - External co-processors
- Master or slave serial peripheral bus interface
  - 8- to 16-bit programmable data length per chip select
  - Programmable phase and polarity per chip select
  - Programmable transfer delays between consecutive transfers and between clock and data per chip select
  - Programmable delay between consecutive transfers
  - Selectable mode fault detection
- Very fast transfers supported
  - Transfers with baud rates up to MCK
  - The chip select line may be left active to speed up transfers on the same device

12.2 Two Wire Interface (TWI)

- Master, Multi-Master and Slave Mode Operation
- Compatibility with Atmel two-wire interface, serial memory and I^2C compatible devices
- One, two or three bytes for slave address
- Sequential read/write operations
- Bit Rate: Up to 400 kbit/s
- General Call Supported in Slave Mode
- Connecting to PDC channel capabilities optimizes data transfers in Master Mode only (for TWI0 only)
  - One channel for the receiver, one channel for the transmitter
  - Next buffer support

12.3 Universal Asynchronous Receiver Transceiver (UART)

- Two-pin UART
  - Implemented features are 100% compatible with the standard Atmel USART
  - Independent receiver and transmitter with a common programmable Baud Rate Generator
  - Even, Odd, Mark or Space Parity Generation
  - Parity, Framing and Overrun Error Detection
  - Automatic Echo, Local Loopback and Remote Loopback Channel Modes

  - Two multi-purpose input/output signals
- Two global registers that act on all three TC Channels
- Quadrature decoder
  - Advanced line filtering
  - Position/revolution/speed
- 2-bit Gray Up/Down Counter for Stepper Motor

12.6 Pulse Width Modulation Controller (PWM)

- Four channels, one 16-bit counter per channel
- Common clock generator, providing thirteen different clocks
  - One Modulo n counter providing eleven clocks
  - Two independent linear dividers working on modulo n counter outputs
- Independent channel programming
  - Independent enable/disable commands
  - Independent clock selection
  - Independent period and duty cycle, with double buffering
  - Programmable selection of the output waveform polarity

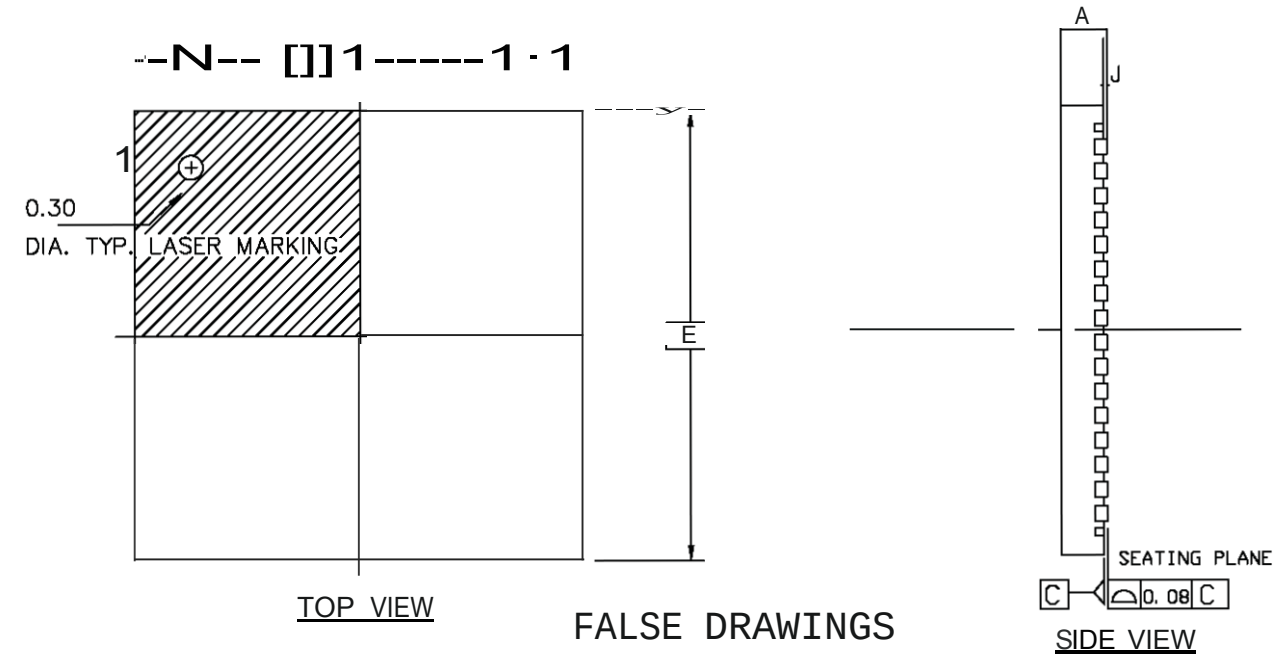
12.7 10-bit Analog-to-Digital Converter

- Up to 16-channel ADC
- 10-bit 384 Ksamples/sec. or 8-bit 583 Ksamples/sec. Successive Approximation Register ADC
- ±2 LSB Integral Non Linearity, ±1 LSB Differential Non Linearity
- Integrated 8-to-1 multiplexer, offering eight independent 3.3V analog inputs
- External voltage reference for better accuracy on low voltage inputs
- Individual enable and disable of each channel
- Multiple trigger source
  - Hardware or software trigger
  - External trigger pin
  - Timer Counter 0 to 2 outputs TIOA0 to TIOA2 trigger
- Sleep Mode and conversion sequencer
  - Automatic wakeup on trigger and back to sleep mode after conversions of all enabled channels

12.8 Digital-to-Analog Converter (DAC)

- 1 channel 10-bit DAC
- Up to 500 ksamples/s conversion rate
- Flexible conversion range
- Multiple trigger sources
- One PDC channel

Figure 13-4. 48-pad QFN Package Drawing



COMMON DIMENSIONS IN MM

SYMBOL	MIN.	NOM.	MAX.	NOTES
A	0.80	0.85	0.90	
J	0.00	----	0.05	
D/E		7.00 BSC		
D2/E2	5.00	5.10	5.20	
N		48		
e		0.50 BSC		
L	0.30	0.40	0.50	
b	0.18	0.25	0.30	

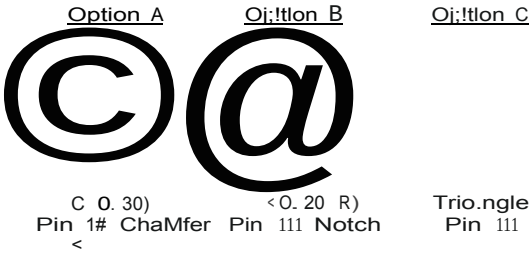
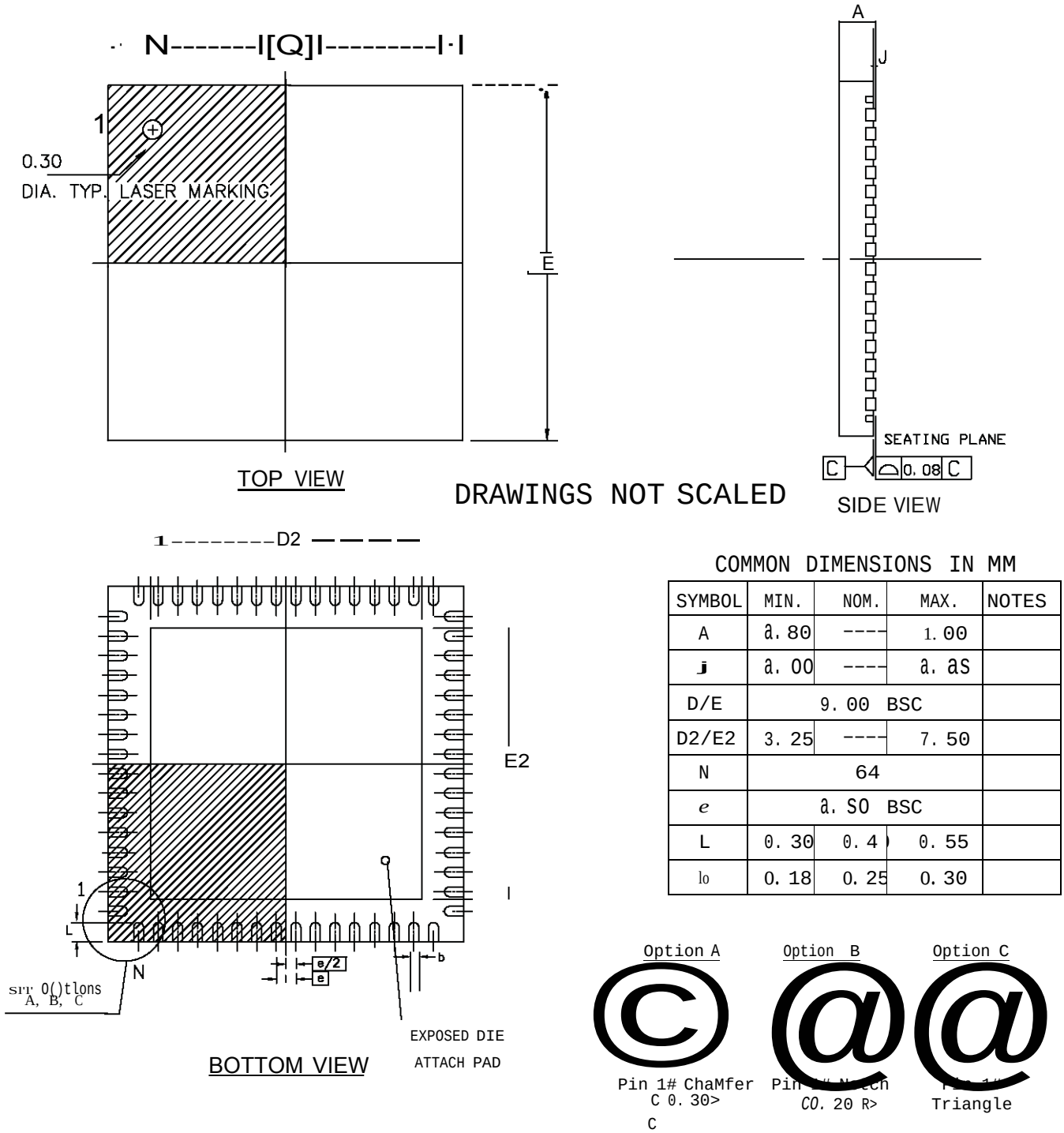


Figure 13-5. 64-pad QFN Package Drawing



COMMON DIMENSIONS IN MM

SYMBOL	MIN.	NOM.	MAX.	NOTES
A	0.80	----	1.00	
j	0.00	----	0.05	
D/E		9.00 BSC		
D2/E2	3.25	----	7.50	
N		64		
e		0.50 BSC		
L	0.30	0.40	0.55	
lo	0.18	0.25	0.30	

14. Ordering Information

Table 14-1.

Ordering Code	MRL	Flash (Kbytes)	Package	Package Type	Temperature Operating Range
ATSAM3N4CA-AU	A	256	LQFP100	Green	Industrial -40°C to 85°C
ATSAM3N4CA-CU	A	256	TFBGA100	Green	Industrial -40°C to 85°C
ATSAM3N4BA-AU	A	256	LQFP64	Green	Industrial -40°C to 85°C
ATSAM3N4BA-MU	A	256	QFN64	Green	Industrial -40°C to 85°C
ATSAM3N4AA-AU	A	256	LQFP48	Green	Industrial -40°C to 85°C
ATSAM3N4AA-MU	A	256	QFN48	Green	Industrial -40°C to 85°C
ATSAM3N2CA-AU	A	128	LQFP100	Green	Industrial -40°C to 85°C
ATSAM3N2CA-CU	A	128	TFBGA100	Green	Industrial -40°C to 85°C
ATSAM3N2BA-AU	A	128	LQFP64	Green	Industrial -40°C to 85°C
ATSAM3N2BA-MU	A	128	QFN64	Green	Industrial -40°C to 85°C
ATSAM3N2AA-AU	A	128	LQFP48	Green	Industrial -40°C to 85°C
ATSAM3N2AA-MU	A	128	QFN48	Green	Industrial -40°C to 85°C
ATSAM3N1CA-AU	A	64	LQFP100	Green	Industrial -40°C to 85°C
ATSAM3N1CB-AU	B	64	LQFP100	Green	Industrial -40°C to 85°C
ATSAM3N1CA-CU	A	64	TFBGA100	Green	Industrial -40°C to 85°C
ATSAM3N1CB-CU	B	64	TFBGA100	Green	Industrial -40°C to 85°C
ATSAM3N1BA-AU	A	64	LQFP64	Green	Industrial -40°C to 85°C
ATSAM3N1BB-AU	B	64	LQFP64	Green	Industrial -40°C to 85°C
ATSAM3N1BA-MU	A	64	QFN 64	Green	Industrial -40°C to 85°C
ATSAM3N1BB-MU	B	64	QFN 64	Green	Industrial -40°C to 85°C

Table 14-1.

Ordering Code	MRL	Flash (Kbytes)	Package	Package Type	Temperature Operating Range
ATSAM3N1AA-AU	A	64	LQFP48	Green	Industrial -40°C to 85°C
ATSAM3N1AB-AU	B	64	LQFP48	Green	Industrial -40°C to 85°C
ATSAM3N1AA-MU	A	64	QFN48	Green	Industrial -40°C to 85°C
ATSAM3N1AB-MU	B	64	QFN48	Green	Industrial -40°C to 85°C
ATSAM3N0CA-AU	A	32	LQFP100	Green	Industrial -40°C to 85°C
ATSAM3N0CA-CU	A	32	TFBGA100	Green	Industrial -40°C to 85°C
ATSAM3N0BA-AU	A	32	LQFP64	Green	Industrial -40°C to 85°C
ATSAM3N0BA-MU	A	32	QFN64	Green	Industrial -40°C to 85°C
ATSAM3N0AA-AU	A	32	LQFP48	Green	Industrial -40°C to 85°C
ATSAM3N0AA-MU	A	32	QFN48	Green	Industrial -40°C to 85°C
ATSAM3N00BA-AU	A	16	LQFP64	Green	Industrial -40°C to 85°C
ATSAM3N00BA-MU	A	16	QFN64	Green	Industrial -40°C to 85°C
ATSAM3N00AA-AU	A	16	LQFP48	Green	Industrial -40°C to 85°C
ATSAM3N00AA-MU	A	16	QFN48	Green	Industrial -40°C to 85°C