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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	I²C, IrDA, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	79
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.62V ~ 3.6V
Data Converters	A/D 16x10b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atsam3n0ca-aur

Table 3-1. Signal Description List (Continued)

Signal Name	Function	Type	Active Level	Voltage Reference	Comments
Serial Peripheral Interface - SPI					
MISO	Master In Slave Out	I/O			
MOSI	Master Out Slave In	I/O			
SPCK	SPI Serial Clock	I/O			
SPI_NPCS0	SPI Peripheral Chip Select 0	I/O	Low		
SPI_NPCS1 - SPI_NPCS3	SPI Peripheral Chip Select	Output	Low		
Two-Wire Interface- TWIx					
TWDx	TWIx Two-wire Serial Data	I/O			
TWCKx	TWIx Two-wire Serial Clock	I/O			
Analog					
ADVREF	ADC and DAC Reference	Analog			
10-bit Analog-to-Digital Converter - ADC					
AD0 - AD15	Analog Inputs	Analog			
ADTRG	ADC Trigger	Input		VDDIO	
Digital-to-Analog Converter Controller- DACC					
DAC0	DACC channel analog output	Analog			
DATRG	DACC Trigger	Input		VDDIO	
Fast Flash Programming Interface					
PGMEN0-PGMEN2	Programming Enabling	Input		VDDIO	
PGMM0-PGMM3	Programming Mode	Input			
PGMD0-PGMD15	Programming Data	I/O			
PGMRDY	Programming Ready	Output	High		
PGMNVALID	Data Direction	Output	Low		
PGMNOE	Programming Read	Input	Low		
PGMCK	Programming Clock	Input			
PGMNCMD	Programming Command	Input	Low		

Notes: 1. Schmitt Triggers can be disabled through PIO registers.
2. Some PIO lines are shared with System IOs.
3. See Section 5.3 “Typical Powering Schematics” for restriction on voltage range of Analog Cells.

4.1.3 100-Lead LQFP Pinout

Table 4-1. 100-lead LQFP SAM3N4/2/1/0/00C Pinout

1	ADVREF	26	GND	51	TDI/PB4	76	TDO/TRACESWO/PB5
2	GND	27	VDDIO	52	PA6/PGMNOE	77	JTAGSEL
3	PB0/AD4	28	PA16/PGMD4	53	PA5/PGMRDY	78	PC18
4	PC29/AD13	29	PC7	54	PC28	79	TMS/SWDIO/PB6
5	PB1/AD5	30	PA15/PGMD3	55	PA4/PGMNCMD	80	PC19
6	PC30/AD14	31	PA14/PGMD2	56	VDDCORE	81	PA31
7	PB2/AD6	32	PC6	57	PA27	82	PC20
8	PC31/AD15	33	PA13/PGMD1	58	PC8	83	TCK/SWCLK/PB7
9	PB3/AD7	34	PA24	59	PA28	84	PC21
10	VDDIN	35	PC5	60	NRST	85	VDDCORE
11	VDDOUT	36	VDDCORE	61	TST	86	PC22
12	PA17/PGMD5/AD0	37	PC4	62	PC9	87	ERASE/PB12
13	PC26	38	PA25	63	PA29	88	PB10
14	PA18/PGMD6/AD1	39	PA26	64	PA30	89	PB11
15	PA21/AD8	40	PC3	65	PC10	90	PC23
16	VDDCORE	41	PA12/PGMD0	66	PA3	91	VDDIO
17	PC27	42	PA11/PGMM3	67	PA2/PGMEN2	92	PC24
18	PA19/PGMD7/AD2	43	PC2	68	PC11	93	PB13/DAC0
19	PC15/AD11	44	PA10/PGMM2	69	VDDIO	94	PC25
20	PA22/AD9	45	GND	70	GND	95	GND
21	PC13/AD10	46	PA9/PGMM1	71	PC14	96	PB8/XOUT
22	PA23	47	PC1	72	PA1/PGMEN1	97	PB9/*PGMCK/XIN*
23	PC12/AD12	48	PA8/XOUT32/ PGMM0	73	PC16	98	VDDIO
24	PA20/AD3	49	PA7/XIN32/ PGMNVALID	74	PA0/PGMEN0	99	PB14
25	PC0	50	VDDIO	75	PC17	100	VDDPLL

4.1.4 100-ball TFBGA Pinout

Table 4-2. 100-ball TFBGA SAM3N4/2/1/0/00C Pinout

A1	PB1	C6	PB7	F1	PA18	H6	PC4
A2	PC29	C7	PC16	F2	PC26	H7	PA11
A3	VDDIO	C8	PA1	F3	VDDOUT	H8	PC1
A4	PB9	C9	PC17	F4	GND	H9	PA6
A5	PB8	C10	PA0	F5	VDDIO	H10	PB4
A6	PB13	D1	PB3	F6	PA27	J1	PC15
A7	PB11	D2	PB0	F7	PC8	J2	PC0
A8	PB10	D3	PC24	F8	PA28	J3	PA16
A9	PB6	D4	PC22	F9	TST	J4	PC6
A10	JTAGSEL	D5	GND	F10	PC9	J5	PA24
B1	PC30	D6	GND	G1	PA21	J6	PA25
B2	ADVREF	D7	VDDCORE	G2	PC27	J7	PA10
B3	GNDANA	D8	PA2	G3	PA15	J8	GND
B4	PB14	D9	PC11	G4	VDDCORE	J9	VDDCORE
B5	PC21	D10	PC14	G5	VDDCORE	J10	VDDIO
B6	PC20	E1	PA17	G6	PA26	K1	PA22
B7	PA31	E2	PC31	G7	PA12	K2	PC13
B8	PC19	E3	VDDIN	G8	PC28	K3	PC12
B9	PC18	E4	GND	G9	PA4	K4	PA20
B10	PB5	E5	GND	G10	PA5	K5	PC5
C1	PB2	E6	NRST	H1	PA19	K6	PC3
C2	VDDPLL	E7	PA29	H2	PA23	K7	PC2
C3	PC25	E8	PA30	H3	PC7	K8	PA9
C4	PC23	E9	PC10	H4	PA14	K9	PA8
C5	PB12	E10	PA3	H5	PA13	K10	PA7

4.2 SAM3N4/2/1/0/00B Package and Pinout

Figure 4-3. Orientation of the 64-pad QFN Package

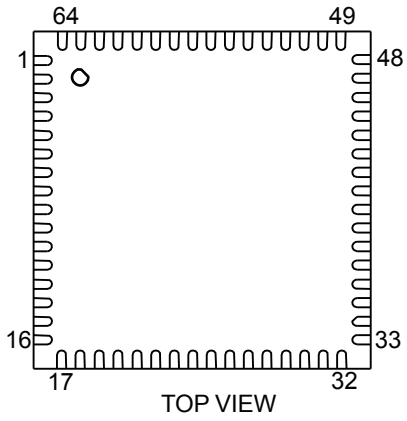
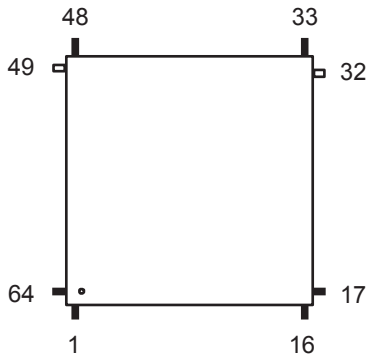


Figure 4-4. Orientation of the 64-lead LQFP Package



4.3.1 48-Lead LQFP and QFN Pinout

Table 4-4. 48-pin SAM3N4/2/1/0/00A Pinout

1	ADVREF	13	VDDIO	25	*TDI/PB4*	37	*TDO/TRACESWO/ PB5*
2	GND	14	PA16/PGMD4	26	PA6/PGMNOE	38	JTAGSEL
3	*PB0/AD4*	15	PA15/PGMD3	27	PA5/PGMRDY	39	*TMS/SWDIO/PB6*
4	*PB1/AD5*	16	PA14/PGMD2	28	PA4/PGMNCMD	40	*TCK/SWCLK/PB7*
5	*PB2/AD6*	17	PA13/PGMD1	29	NRST	41	VDDCORE
6	*PB3/AD7*	18	VDDCORE	30	TST	42	*ERASE/PB12*
7	VDDIN	19	PA12/PGMD0	31	PA3	43	*PB10*
8	VDDOUT	20	PA11/PGMM3	32	PA2/PGMEN2	44	*PB11*
9	PA17/PGMD5/AD0	21	PA10/PGMM2	33	VDDIO	45	*XOUT/PB8*
10	PA18/PGMD6/AD1	22	PA9/PGMM1	34	GND	46	*XIN/P/PB9/GMCK*
11	PA19/PGMD7/AD2	23	PA8/XOUT32/PG MM0	35	PA1/PGMEN1	47	VDDIO
12	PA20/AD3	24	PA7/XIN32/PGMN VALID	36	PA0/PGMEN0	48	VDDPLL

Note: The bottom pad of the QFN package must be connected to ground.

5. Power Considerations

5.1 Power Supplies

The SAM3N product has several types of power supply pins:

- VDDCORE pins: Power the core, including the processor, the embedded memories and the peripherals. Voltage ranges from 1.62V and 1.95V.
- VDDIO pins: Power the Peripherals I/O lines, Backup part, 32 kHz crystal oscillator and oscillator pads. Voltage ranges from 1.62V and 3.6V
- VDDIN pin: Voltage Regulator, ADC and DAC Power Supply. Voltage ranges from 1.8V to 3.6V for the Voltage Regulator
- VDDPLL pin: Powers the PLL, the Fast RC and the 3 to 20 MHz oscillators. Voltage ranges from 1.62V and 1.95V.

5.2 Voltage Regulator

The SAM3N embeds a voltage regulator that is managed by the Supply Controller.

This internal regulator is intended to supply the internal core of SAM3N. It features two different operating modes:

- In Normal mode, the voltage regulator consumes less than 700 µA static current and draws 60 mA of output current. Internal adaptive biasing adjusts the regulator quiescent current depending on the required load current. In Wait Mode quiescent current is only 7 µA.
- In Backup mode, the voltage regulator consumes less than 1 µA while its output (VDDOUT) is driven internally to GND. The default output voltage is 1.80V and the start-up time to reach Normal mode is less than100 µs.

For adequate input and output power supply decoupling/bypassing, refer to the Voltage Regulator section in the Electrical Characteristics section of the datasheet.

5.3 Typical Powering Schematics

The SAM3N supports a 1.62V-3.6V single supply mode. The internal regulator input connected to the source and its output feeds VDDCORE. Figure 5-1 shows the power schematics.

As VDDIN powers the voltage regulator and the ADC/DAC, when the user does not want to use the embedded voltage regulator, it can be disabled by software via the SUPC (note that it is different from Backup mode).

Table 6-1. System I/O Configuration Pin List.

SYSTEM_IO bit number	Default function after reset	Other function	Constraints for normal start	Configuration
12	ERASE	PB12	Low Level at startup(1)	In Matrix User Interface Registers (Refer to the System I/O Configuration Register in the Bus Matrix section of the product datasheet.)
7	TCK/SWCLK	PB7	-	
6	TMS/SWDIO	PB6	-	
5	TDO/TRACESWO	PB5	-	
4	TDI	PB4	-	
-	PA7	XIN32	-	See footnote (2) below
-	PA8	XOUT32	-	
-	PB9	XIN	-	See footnote (3) below
-	PB8	XOUT	-	

Notes:
1. If PB12 is used as PIO input in user applications, a low level must be ensured at startup to prevent Flash erase before the user application sets PB12 into PIO mode.
2. In the product Datasheet Refer to: Slow Clock Generator of the Supply Controller section.
3. In the product Datasheet Refer to: 3 to 20 MHZ Crystal Oscillator information in the PMC section.

6.2.1 Serial Wire JTAG Debug Port (SWJ-DP) Pins

The SWJ-DP pins are TCK/SWCLK, TMS/SWDIO, TDO/SWO, TDI and commonly provided on a standard 20-pin JTAG connector defined by ARM. For more details about voltage reference and reset state, refer to Table 3-1 on page 7.

At startup, SWJ-DP pins are configured in SWJ-DP mode to allow connection with debugging probe. Please refer to the Debug and Test Section of the product datasheet.

SWJ-DP pins can be used as standard I/Os to provide users more general input/output pins when the debug port is not needed in the end application. Mode selection between SWJ-DP mode (System IO mode) and general IO mode is performed through the AHB Matrix Special Function Registers (MATRIX_SFR). Configuration of the pad for pull-up, triggers, debouncing and glitch filters is possible regardless of the mode.

The JTAGSEL pin is used to select the JTAG boundary scan when asserted at a high level. It integrates a permanent pull-down resistor of about 15 kΩ to GND, so that it can be left unconnected for normal operations.

By default, the JTAG Debug Port is active. If the debugger host wants to switch to the Serial Wire Debug Port, it must provide a dedicated JTAG sequence on TMS/SWDIO and TCK/SWCLK which disables the JTAG-DP and enables the SW-DP. When the Serial Wire Debug Port is active, TDO/TRACESWO can be used for trace.

The asynchronous TRACE output (TRACESWO) is multiplexed with TDO. So the asynchronous trace can only be used with SW-DP, not JTAG-DP. For more information about SW-DP and JTAG-DP switching, please refer to the Debug and Test Section.

7. Processor and Architecture

7.1 ARM Cortex-M3 Processor

- Version 2.0
- Thumb-2 (ISA) subset consisting of all base Thumb-2 instructions, 16-bit and 32-bit.
- Harvard processor architecture enabling simultaneous instruction fetch with data load/store.
- Three-stage pipeline.
- Single cycle 32-bit multiply.
- Hardware divide.
- Thumb and Debug states.
- Handler and Thread modes.
- Low latency ISR entry and exit.

7.2 APB/AHB Bridge

The SAM3N4/2/1/0/00 product embeds one peripheral bridge:

The peripherals of the bridge are clocked by MCK.

7.3 Matrix Masters

The Bus Matrix of the SAM3N product manages 3 masters, which means that each master can perform an access concurrently with others, to an available slave.

Each master has its own decoder, which is defined specifically for each master. In order to simplify the addressing, all the masters have the same decodings.

Table 7-1. List of Bus Matrix Masters

Master 0	Cortex-M3 Instruction/Data
Master 1	Cortex-M3 System
Master 2	Peripheral DMA Controller (PDC)

7.4 Matrix Slaves

The Bus Matrix of the SAM3N product manages 4 slaves. Each slave has its own arbiter, allowing a different arbitration per slave.

Table 7-2. List of Bus Matrix Slaves

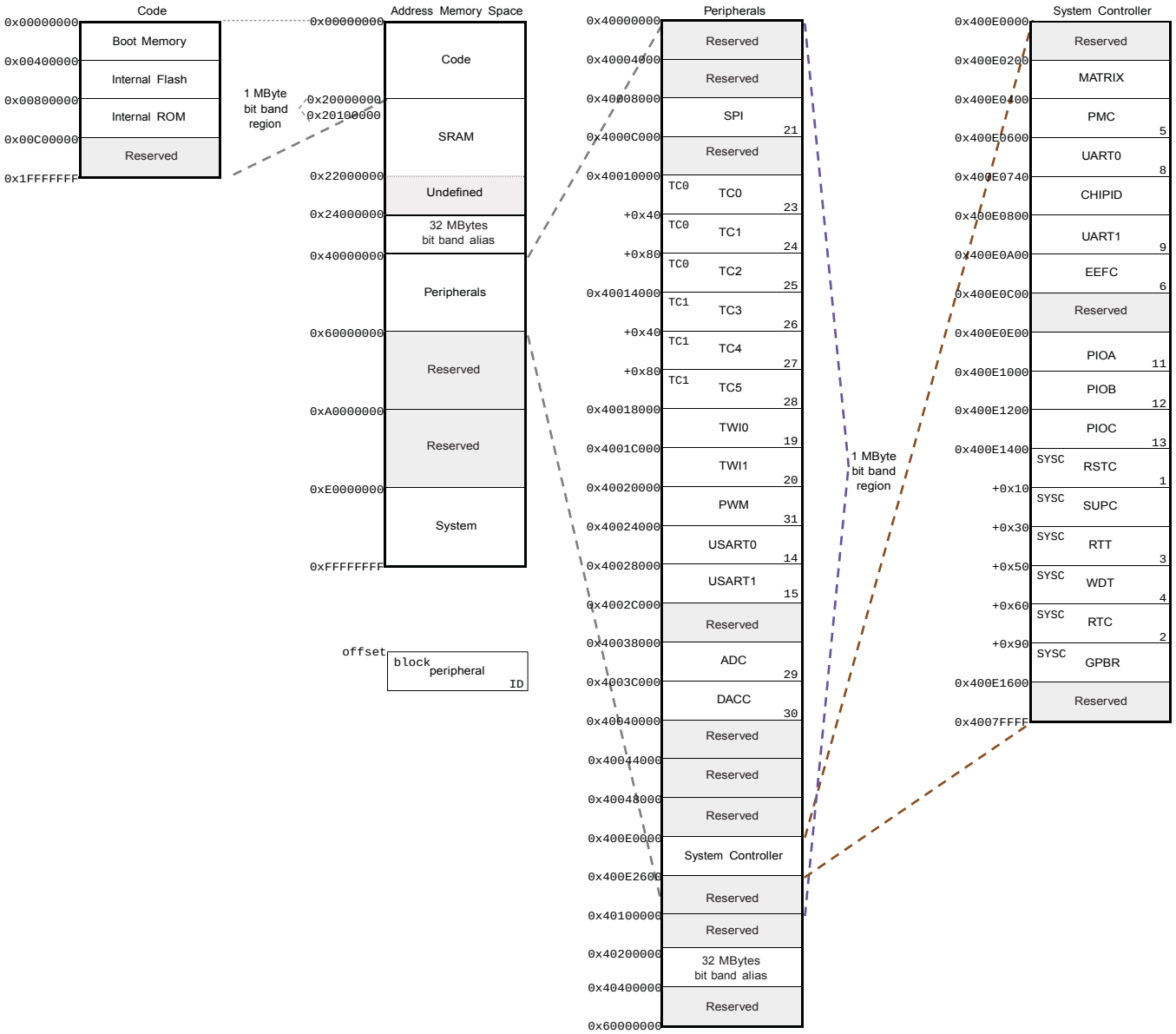
Slave 0	Internal SRAM
Slave 1	Internal ROM
Slave 2	Internal Flash
Slave 3	Peripheral Bridge

7.7 Debug and Test Features

- Debug access to all memory and registers in the system, including Cortex-M3 register bank when the core is running, halted, or held in reset.
- Serial Wire Debug Port (SW-DP) and Serial Wire JTAG Debug Port (SWJ-DP) debug access
- Flash Patch and Breakpoint (FPB) unit for implementing breakpoints and code patches
- Data Watchpoint and Trace (DWT) unit for implementing watchpoints, data tracing, and system profiling
- Instrumentation Trace Macrocell (ITM) for support of printf style debugging
- IEEE1149.1 JTAG Boundary-can on All Digital Pins

8. Product Mapping

Figure 8-1. SAM3N4/2/1/0/00 Product Mapping



9.1.3.4 Flash Speed

The user needs to set the number of wait states depending on the frequency used.

For more details, refer to the AC Characteristics sub section in the product Electrical Characteristics Section.

9.1.3.5 Lock Regions

Several lock bits used to protect write and erase operations on lock regions. A lock region is composed of several consecutive pages, and each lock region has its associated lock bit.

Table 9-1. Lock bit number

Product	Number of lock bits	Lock region size
SAM3N4	16	16 kbytes (64 pages)
SAM3N2	8	16 kbytes (64 pages)
SAM3N1	4	16 kbytes (64 pages)

If a locked-region's erase or program command occurs, the command is aborted and the EEFC triggers an interrupt.

The lock bits are software programmable through the EEFC User Interface. The command "Set Lock Bit" enables the protection. The command "Clear Lock Bit" unlocks the lock region.

Asserting the ERASE pin clears the lock bits, thus unlocking the entire Flash.

9.1.3.6 Security Bit Feature

The SAM3N features a security bit, based on a specific General Purpose NVM bit (GPNVM bit 0). When the security is enabled, any access to the Flash, either through the ICE interface or through the Fast Flash Programming Interface, is forbidden. This ensures the confidentiality of the code programmed in the Flash.

This security bit can only be enabled, through the command "Set General Purpose NVM Bit 0" of the EEFC User Interface. Disabling the security bit can only be achieved by asserting the ERASE pin at 1, after a full Flash erase is performed. When the security bit is deactivated, all accesses to the Flash are permitted.

It is important to note that the assertion of the ERASE pin should always be longer than 200 ms.

As the ERASE pin integrates a permanent pull-down, it can be left unconnected during normal operation. However, it is safer to connect it directly to GND for the final application.

9.1.3.7 Calibration Bits

NVM bits are used to calibrate the brownout detector and the voltage regulator. These bits are factory configured and cannot be changed by the user. The ERASE pin has no effect on the calibration bits.

9.1.3.8 Unique Identifier

Each device integrates its own 128-bit unique identifier. These bits are factory configured and cannot be changed by the user. The ERASE pin has no effect on the unique identifier.

10. System Controller

The System Controller is a set of peripherals, which allow handling of key elements of the system, such as power, resets, clocks, time, interrupts, watchdog, etc...

See the System Controller block diagram in Figure 10-1 on page 35.

10.6 Power Management Controller

The Power Management Controller provides all the clock signals to the system. It provides:

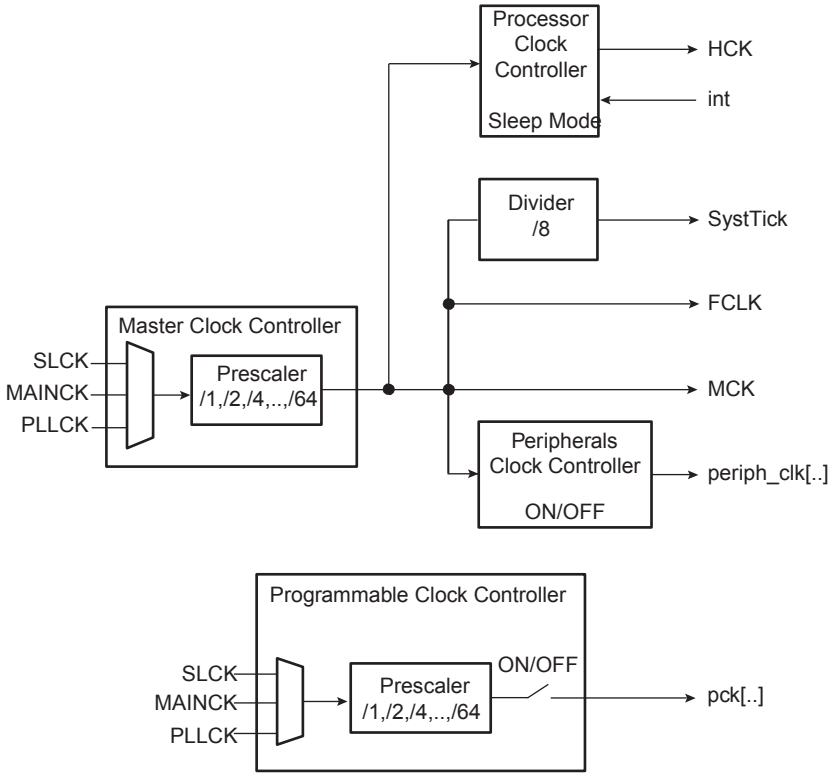
- the Processor Clock HCLK
- the Free running processor clock FCLK
- the Cortex SysTick external clock
- the Master Clock MCK, in particular to the Matrix and the memory interfaces
- independent peripheral clocks, typically at the frequency of MCK
- three programmable clock outputs: PCK0, PCK1 and PCK2

The Supply Controller selects between the 32 kHz RC oscillator or the crystal oscillator. The unused oscillator is disabled automatically so that power consumption is optimized.

By default, at startup the chip runs out of the Master Clock using the Fast RC Oscillator running at 4 MHz.

The user can trim by software the 8 and 12 MHz RC Oscillator frequency.

Figure 10-3. SAM3N4/2/1/0/00 Power Management Controller Block Diagram



The SysTick calibration value is fixed at 6000 which allows the generation of a time base of 1 ms with SysTick clock at 6 MHz (48 MHz/8)

10.7 Watchdog Timer

- 16-bit key-protected only-once-Programmable Counter
- Windowed, prevents the processor to be in a dead-lock on the watchdog access

  - Multi-drive option enables driving in open drain
  - Programmable pull up on each I/O line
  - Pin data status register, supplies visibility of the level on the pin at any time
- Selection of the drive level
- Synchronous output, provides Set and Clear of several I/O lines in a single write

11. Peripherals

11.1 Peripheral Identifiers

Table 11-1 defines the Peripheral Identifiers of the SAM3N4/2/1/0/00. A peripheral identifier is required for the control of the peripheral interrupt with the Nested Vectored Interrupt Controller and for the control of the peripheral clock with the Power Management Controller.

Table 11-1. Peripheral Identifiers

Instance ID	Instance Name	NVIC Interrupt	PMC Clock Control	Instance Description
0	SUPC	**X**		**Supply Controller**
1	RSTC	**X**		Reset Controller
2	RTC	**X**		Real Time Clock
3	RTT	**X**		Real Time Timer
4	WDT	**X**		Watchdog Timer
5	PMC	**X**		Power Management Controller
6	EEFC	**X**		Enhanced Flash Controller
7	-	**-**		Reserved
8	UART0	**X**	**X**	UART 0
9	UART1	**X**	**X**	UART 1
10	-	**-**	**-**	Reserved
11	PIOA	**X**	**X**	Parallel I/O Controller A
12	PIOB	**X**	**X**	Parallel I/O Controller B
13	PIOC	**X**	**X**	Parallel I/O Controller C
14	USART0	**X**	**X**	USART 0
15	USART1	**X**	**X**	USART 1
16	-	**-**	**-**	Reserved
17	-	**-**	**-**	Reserved
18	-	**-**	**-**	Reserved
19	TWI0	**X**	**X**	Two Wire Interface 0
20	TWI1	**X**	**X**	Two Wire Interface 1
21	SPI	**X**	**X**	Serial Peripheral Interface
22	-	**-**	**-**	Reserved
23	TC0	**X**	**X**	Timer/Counter 0
24	TC1	**X**	**X**	Timer/Counter 1

  - Support for two PDC channels with connection to receiver and transmitter (for UART0 only)

12.4 USART

- Programmable Baud Rate Generator
- 5- to 9-bit full-duplex synchronous or asynchronous serial communications
  - 1, 1.5 or 2 stop bits in Asynchronous Mode or 1 or 2 stop bits in Synchronous Mode
  - Parity generation and error detection
  - Framing error detection, overrun error detection
  - MSB- or LSB-first
  - Optional break generation and detection
  - By 8 or by-16 over-sampling receiver frequency
  - Hardware handshaking RTS-CTS
  - Receiver time-out and transmitter timeguard
  - Optional Multi-drop Mode with address generation and detection
- RS485 with driver control signal
- ISO7816, T = 0 or T = 1 Protocols for interfacing with smart cards (Only on USART0)
  - NACK handling, error counter with repetition and iteration limit
- SPI Mode
  - Master or Slave
  - Serial Clock programmable Phase and Polarity
  - SPI Serial Clock (SCK) Frequency up to MCK/4
- IrDA modulation and demodulation (Only on USART0)
  - Communication at up to 115.2 Kbps
- Test Modes
  - Remote Loopback, Local Loopback, Automatic Echo
- PDC support (for USART0 only)

12.5 Timer Counter (TC)

- Six 16-bit Timer Counter Channels
- Wide range of functions including:
  - Frequency Measurement
  - Event Counting
  - Interval Measurement
  - Pulse Generation
  - Delay Timing
  - Pulse Width Modulation
  - Up/down Capabilities
- Each channel is user-configurable and contains:
  - Three external clock inputs
  - Five internal clock inputs

  - Two multi-purpose input/output signals
- Two global registers that act on all three TC Channels
- Quadrature decoder
  - Advanced line filtering
  - Position/revolution/speed
- 2-bit Gray Up/Down Counter for Stepper Motor

12.6 Pulse Width Modulation Controller (PWM)

- Four channels, one 16-bit counter per channel
- Common clock generator, providing thirteen different clocks
  - One Modulo n counter providing eleven clocks
  - Two independent linear dividers working on modulo n counter outputs
- Independent channel programming
  - Independent enable/disable commands
  - Independent clock selection
  - Independent period and duty cycle, with double buffering
  - Programmable selection of the output waveform polarity

12.7 10-bit Analog-to-Digital Converter

- Up to 16-channel ADC
- 10-bit 384 Ksamples/sec. or 8-bit 583 Ksamples/sec. Successive Approximation Register ADC
- ±2 LSB Integral Non Linearity, ±1 LSB Differential Non Linearity
- Integrated 8-to-1 multiplexer, offering eight independent 3.3V analog inputs
- External voltage reference for better accuracy on low voltage inputs
- Individual enable and disable of each channel
- Multiple trigger source
  - Hardware or software trigger
  - External trigger pin
  - Timer Counter 0 to 2 outputs TIOA0 to TIOA2 trigger
- Sleep Mode and conversion sequencer
  - Automatic wakeup on trigger and back to sleep mode after conversions of all enabled channels

12.8 Digital-to-Analog Converter (DAC)

- 1 channel 10-bit DAC
- Up to 500 ksamples/s conversion rate
- Flexible conversion range
- Multiple trigger sources
- One PDC channel

Figure 13-3. 64and4B·leadLQFP Package Drawing

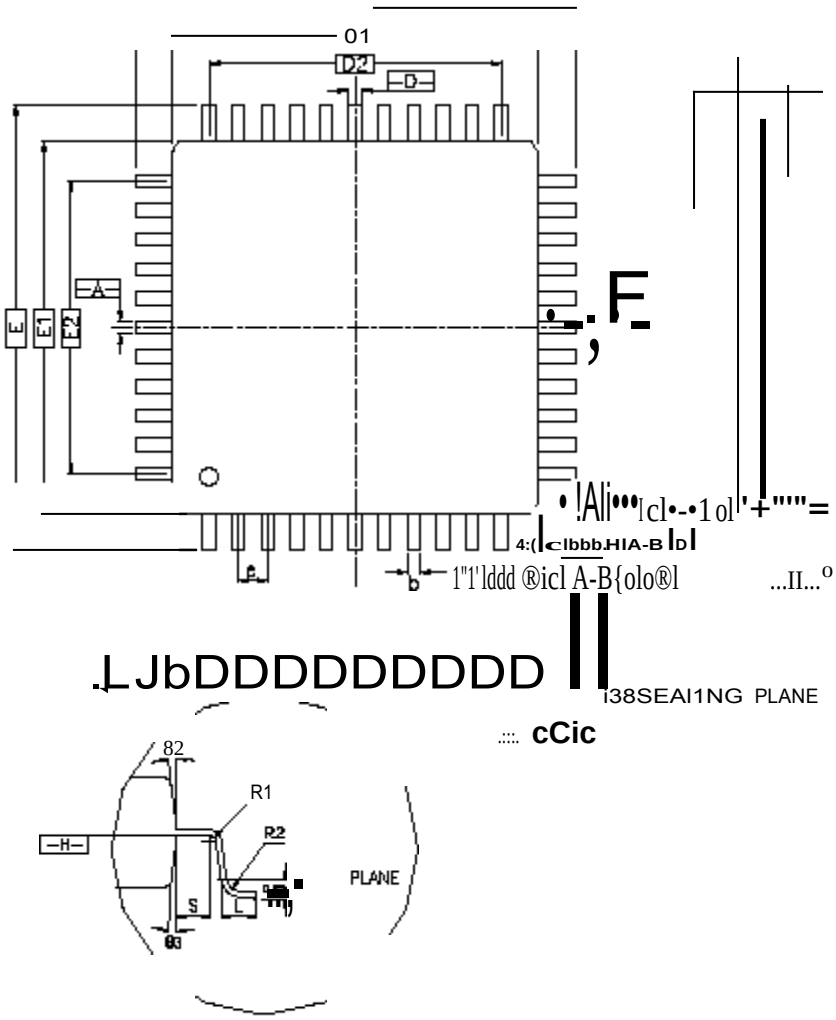
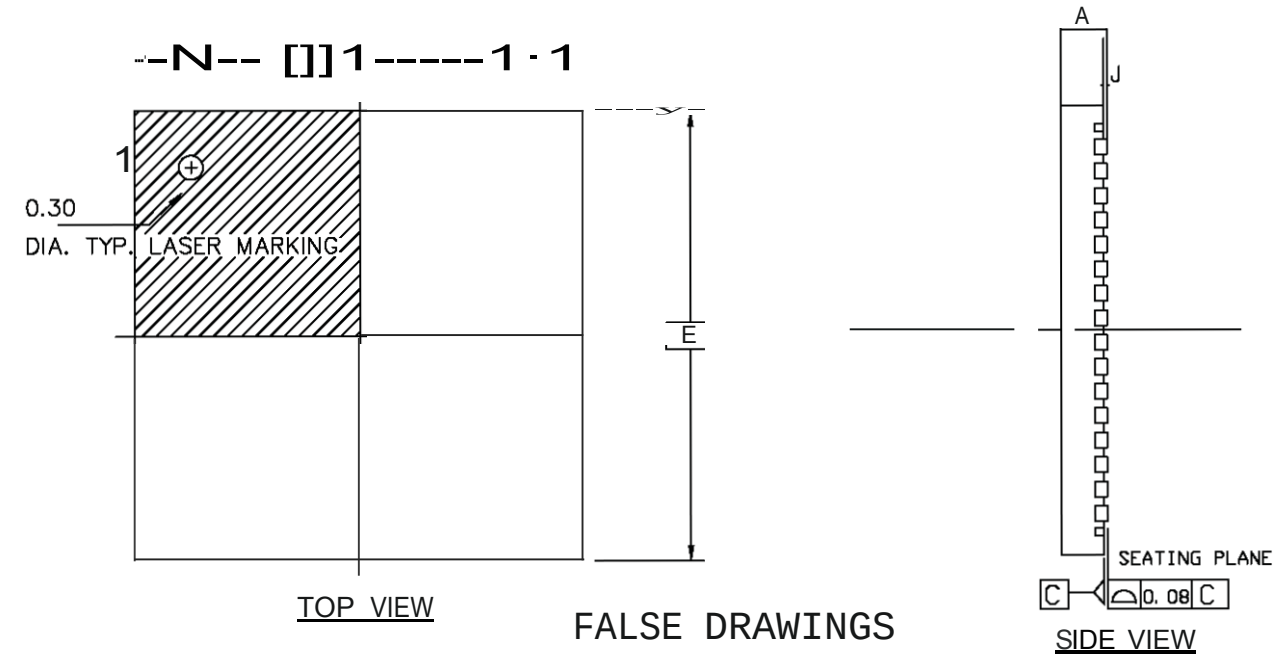


Figure 13-4. 48-pad QFN Package Drawing



COMMON DIMENSIONS IN MM

SYMBOL	MIN.	NOM.	MAX.	NOTES
A	0.80	0.85	0.90	
J	0.00	----	0.05	
D/E		7.00 BSC		
D2/E2	5.00	5.10	5.20	
N		48		
e		0.50 BSC		
L	0.30	0.40	0.50	
b	0.18	0.25	0.30	

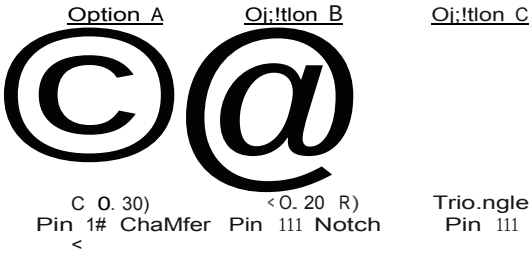
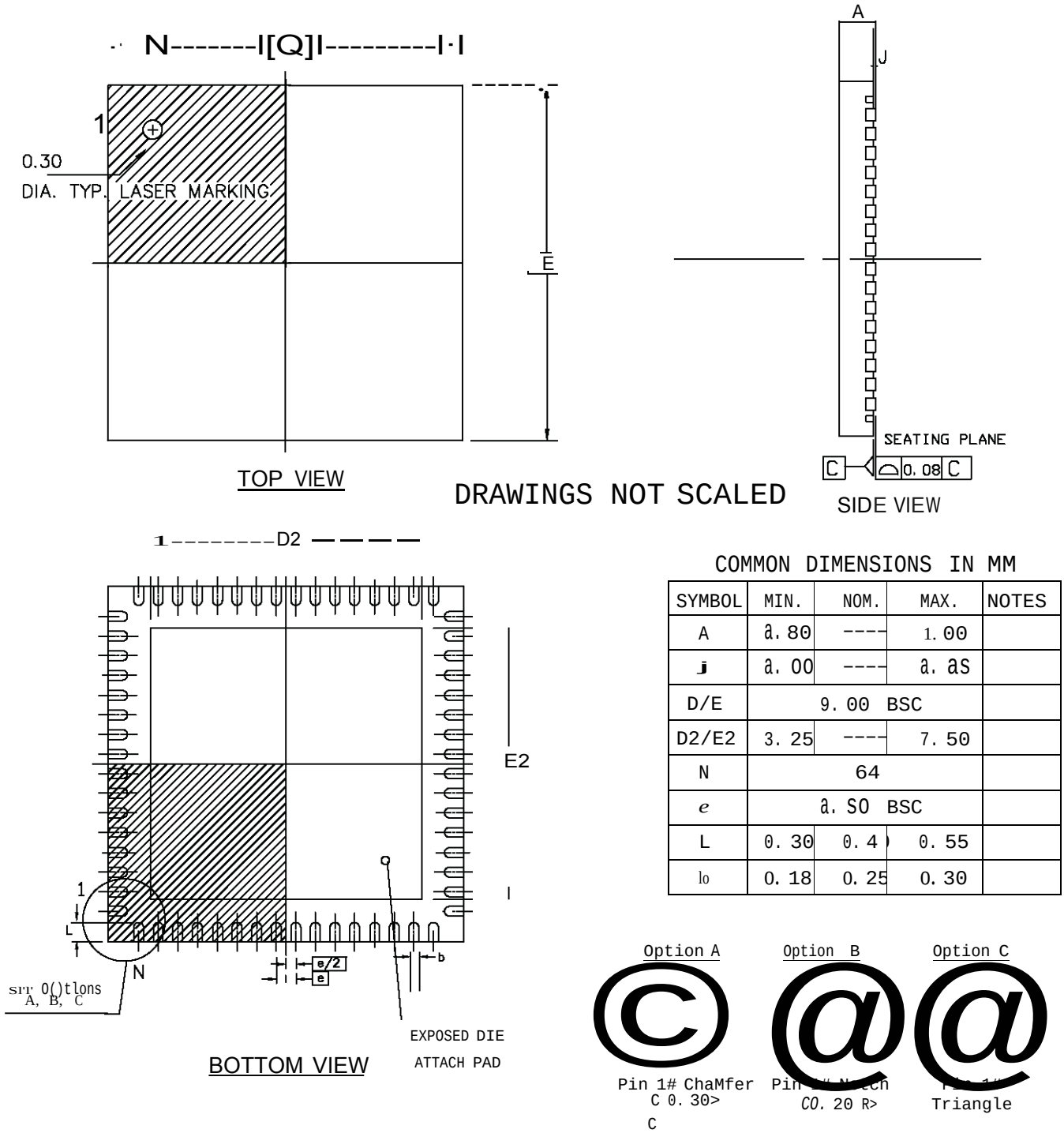


Figure 13-5. 64-pad QFN Package Drawing



COMMON DIMENSIONS IN MM

SYMBOL	MIN.	NOM.	MAX.	NOTES
A	0.80	----	1.00	
j	0.00	----	0.05	
D/E		9.00 BSC		
D2/E2	3.25	----	7.50	
N		64		
e		0.50 BSC		
L	0.30	0.40	0.55	
lo	0.18	0.25	0.30	

14. Ordering Information

Table 14-1.

Ordering Code	MRL	Flash (Kbytes)	Package	Package Type	Temperature Operating Range
ATSAM3N4CA-AU	A	256	LQFP100	Green	Industrial -40°C to 85°C
ATSAM3N4CA-CU	A	256	TFBGA100	Green	Industrial -40°C to 85°C
ATSAM3N4BA-AU	A	256	LQFP64	Green	Industrial -40°C to 85°C
ATSAM3N4BA-MU	A	256	QFN64	Green	Industrial -40°C to 85°C
ATSAM3N4AA-AU	A	256	LQFP48	Green	Industrial -40°C to 85°C
ATSAM3N4AA-MU	A	256	QFN48	Green	Industrial -40°C to 85°C
ATSAM3N2CA-AU	A	128	LQFP100	Green	Industrial -40°C to 85°C
ATSAM3N2CA-CU	A	128	TFBGA100	Green	Industrial -40°C to 85°C
ATSAM3N2BA-AU	A	128	LQFP64	Green	Industrial -40°C to 85°C
ATSAM3N2BA-MU	A	128	QFN64	Green	Industrial -40°C to 85°C
ATSAM3N2AA-AU	A	128	LQFP48	Green	Industrial -40°C to 85°C
ATSAM3N2AA-MU	A	128	QFN48	Green	Industrial -40°C to 85°C
ATSAM3N1CA-AU	A	64	LQFP100	Green	Industrial -40°C to 85°C
ATSAM3N1CB-AU	B	64	LQFP100	Green	Industrial -40°C to 85°C
ATSAM3N1CA-CU	A	64	TFBGA100	Green	Industrial -40°C to 85°C
ATSAM3N1CB-CU	B	64	TFBGA100	Green	Industrial -40°C to 85°C
ATSAM3N1BA-AU	A	64	LQFP64	Green	Industrial -40°C to 85°C
ATSAM3N1BB-AU	B	64	LQFP64	Green	Industrial -40°C to 85°C
ATSAM3N1BA-MU	A	64	QFN 64	Green	Industrial -40°C to 85°C
ATSAM3N1BB-MU	B	64	QFN 64	Green	Industrial -40°C to 85°C