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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Obsolete
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	I ² C, IrDA, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	34
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.62V ~ 3.6V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atsam3n1aa-au

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1.1 Configuration Summary

The SAM3N4/2/1/0/00 differ in memory size, package and features list. Table 1-1 summarizes the configurations of the 9 devices.

 Table 1-1.
 Configuration Summary

Device	Flash	SRAM	Package	Number of PIOs	ADC	Timer	PDC Channels	USART	DAC
SAM3N4A	256 Kbytes	24 Kbytes	LQFP48 QFN48	34	8 channels	6 ⁽¹⁾	8	1	_
SAM3N4B	256 Kbytes	24 Kbytes	LQFP64 QFN64	47	10 channels	6 ⁽²⁾	10	2	1
SAM3N4C	256 Kbytes	24 Kbytes	LQFP100 BGA100	79	16 channels	6	10	2	1
SAM3N2A	128 Kbytes	16 Kbytes	LQFP48 QFN48	34	8 channels	6 ⁽¹⁾	8	1	_
SAM3N2B	128 Kbytes	16 Kbytes	LQFP64 QFN64	47	10 channels	6(⁽²⁾	10	2	1
SAM3N2C	128 Kbytes	16 Kbytes	LQFP100 BGA100	79	16 channels	6	10	2	1
SAM3N1A	64 Kbytes	8 Kbytes	LQFP48 QFN48	34	8 channels	6 ⁽¹⁾	8	1	_
SAM3N1B	64 Kbytes	8 Kbytes	LQFP64 QFN64	47	10 channels	6 ⁽²⁾	10	2	1
SAM3N1C	64 Kbytes	8 Kbytes	LQFP100 BGA100	79	16 channels	6	10	2	1
SAM3N0A	32 Kbytes	8 Kbytes	LQFP48 QFN48	34	8 channels	6 ⁽¹⁾	8	1	_
SAM3N0B	32 Kbytes	8 Kbytes	LQFP64 QFN64	47	10 channels	6 ⁽²⁾	10	2	1
SAM3N0C	32 Kbytes	8 Kbytes	LQFP100 BGA100	79	16 channels	6	10	2	1
SAM3N00A	16 Kbytes	4 KBytes	LQFP48 QFN48	34	8 channels	6 ⁽¹⁾	8	1	_
SAM3N00B	16 Kbytes	4 KBytes	LQFP64 QFN64	47	10 channels	6 ⁽²⁾	10	2	1

Notes: 1. Only two TC channels are accessible through the PIO.

2. Only three TC channels are accessible through the PIO.











Table 3-1. Signal Description List (Continued)

Signal Name	Function	Туре	Active Level	Voltage Reference	Comments			
	Flash M	emory						
ERASE Flash and NVM Configuration Bits Erase Command		Input	High	VDDIO	Reset State: - Erase Input - Internal pull-down enabled - Schmitt Trigger enabled ⁽¹⁾			
	Reset	Test						
NRST	Microcontroller Reset	I/O	Low	VDDIO	Permanent Internal pull-up			
TST	Test Mode Select	Input		VDDIO	Permanent Internal pull-down			
Universal Asynchronous Receiver Transceiver - UARTx								
URXDx	UART Receive Data	Input						
UTXDx	UART Transmit Data	Output						
	PIO Controller - PI	OA - PIOB - PI	OC					
PA0 - PA31	0 - PA31 Parallel IO Controller A				Reset State:			
PB0 - PB14	Parallel IO Controller B	I/O			- PIO or System			
PC0 - PC31	Parallel IO Controller C	I/O		VDDIO	 Internal pull-up enabled Schmitt Trigger enabled⁽¹⁾ 			
	Universal Synchronous Asynchrono	ous Receiver	Transmitter	USARTx	-			
SCKx	USARTx Serial Clock	I/O						
TXDx	USARTx Transmit Data	I/O						
RXDx	USARTx Receive Data	Input						
RTSx	USARTx Request To Send	Output						
CTSx	USARTx Clear To Send	Input						
	Timer/Cou	nter - TC						
TCLKx	TC Channel x External Clock Input							
TIOAx	TC Channel x I/O Line A	I/O						
TIOBx	TC Channel x I/O Line B	I/O						
	Pulse Width Modulatio	on Controller-	PWMC					
PWMx	PWM Waveform Output for channel x	Output						



4.1.4 100-ball TFBGA Pinout

A1	PB1	C6	PB7	F1	PA18	H6	PC4
A2	PC29	C7	PC16	F2	PC26	H7	PA11
A3	VDDIO	C8	PA1	F3	VDDOUT	H8	PC1
A4	PB9	C9	PC17	F4	GND	H9	PA6
A5	PB8	C10	PA0	F5	VDDIO	H10	PB4
A6	PB13	D1	PB3	F6	PA27	J1	PC15
A7	PB11	D2	PB0	F7	PC8	J2	PC0
A8	PB10	D3	PC24	F8	PA28	J3	PA16
A9	PB6	D4	PC22	F9	TST	J4	PC6
A10	JTAGSEL	D5	GND	F10	PC9	J5	PA24
B1	PC30	D6	GND	G1	PA21	J6	PA25
B2	ADVREF	D7	VDDCORE	G2	PC27	J7	PA10
B3	GNDANA	D8	PA2	G3	PA15	J8	GND
B4	PB14	D9	PC11	G4	VDDCORE	J9	VDDCORE
B5	PC21	D10	PC14	G5	VDDCORE	J10	VDDIO
B6	PC20	E1	PA17	G6	PA26	K1	PA22
B7	PA31	E2	PC31	G7	PA12	K2	PC13
B8	PC19	E3	VDDIN	G8	PC28	K3	PC12
B9	PC18	E4	GND	G9	PA4	K4	PA20
B10	PB5	E5	GND	G10	PA5	K5	PC5
C1	PB2	E6	NRST	H1	PA19	K6	PC3
C2	VDDPLL	E7	PA29	H2	PA23	K7	PC2
C3	PC25	E8	PA30	H3	PC7	K8	PA9
C4	PC23	E9	PC10	H4	PA14	K9	PA8
C5	PB12	E10	PA3	H5	PA13	K10	PA7

Table 4-2. 100-ball TFBGA SAM3N4/2/1/0/00C Pinout

5.5.4 Low Power Mode Summary Table

The modes detailed above are the main low power modes. Each part can be set to on or off separately and wake up sources can be individually configured. Table 5-1 below shows a summary of the configurations of the low power modes.

 Table 5-1.
 Low Power Mode Configuration Summary

Mode	SUPC, 32 kHz Oscillator RTC RTT Backup Registers, POR (Backup Region)	Regulator	Core Memory Peripherals	Mode Entry	Potential Wake Up Sources	Core at Wake Up	PIO State while in Low Power Mode	PIO State at Wake Up	Consumption	Wake Up Time ⁽¹⁾
Backup Mode	ON	OFF	OFF (Not powered)	WFE +SLEEPDEEP bit = 1	WUP0-15 pins BOD alarm RTC alarm RTT alarm	Reset	Previous state saved	PIOA & PIOB & PIOC Inputs with pull ups	3 μA typ ⁽⁴⁾	< 0.1 ms
Wait Mode	ON	ON	Powered (Not clocked)	WFE +SLEEPDEEP bit = 0 +LPM bit = 1	Any Event from: Fast startup through WUP0-15 pins RTC alarm RTT alarm	Clocked back	Previous state saved	Unchanged	5 μΑ/15 μΑ ⁽⁵⁾	< 10 µs
Sleep Mode	ON	ON	Powered ⁽⁷⁾ (Not clocked)	WFE or WFI +SLEEPDEEP bit = 0 +LPM bit = 0	Entry mode = WFI Interrupt Only; Entry mode = WFE Any Enabled Interrupt and/or Any Event from: Fast start-up through WUP0-15 pins RTC alarm RTT alarm	Clocked back	Previous state saved	Unchanged	(6)	(6)

Notes: 1. When considering wake-up time, the time required to start the PLL is not taken into account. Once started, the device works with the 4/8/12 MHz Fast RC oscillator. The user has to add the PLL start-up time if it is needed in the system. The wake-up time is defined as the time taken for wake up until the first instruction is fetched.

- 2. The external loads on PIOs are not taken into account in the calculation.
- 3. Supply Monitor current consumption is not included.
- 4. Total Current consumption.
- 5. 5 μA on VDDCORE, 15 μA for total current consumption (using internal voltage regulator), 8 μA for total current consumption (without using internal voltage regulator).
- 6. Depends on MCK frequency.
- 7. In this mode the core is supplied and not clocked but some peripherals can be clocked.



5.7 Fast Start-Up

The SAM3N allows the processor to restart in a few microseconds while the processor is in wait mode. A fast start up can occur upon detection of a low level on one of the 19 wake-up inputs (WKUP0 to 15 + SM + RTC + RTT).

The fast restart circuitry, as shown in Figure 5-5, is fully asynchronous and provides a fast startup signal to the Power Management Controller. As soon as the fast start-up signal is asserted, the PMC automatically restarts the embedded 4 MHz fast RC oscillator, switches the master clock on this 4 MHz clock and reenables the processor clock.



Figure 5-5. Fast Start-Up Sources





6.3 Test Pin

The TST pin is used for JTAG Boundary Scan Manufacturing Test or Fast Flash programming mode of the SAM3N series. The TST pin integrates a permanent pull-down resistor of about 15 k Ω to GND, so that it can be left unconnected for normal operations. To enter fast programming mode, see the Fast Flash Programming Interface (FFPI) section. For more on the manufacturing and test mode, refer to the "Debug and Test" section of the product datasheet.

6.4 NRST Pin

The NRST pin is bidirectional. It is handled by the on-chip reset controller and can be driven low to provide a reset signal to the external components or asserted low externally to reset the microcontroller. It will reset the Core and the peripherals except the Backup region (RTC, RTT and Supply Controller). There is no constraint on the length of the reset pulse and the reset controller can guarantee a minimum pulse length. The NRST pin integrates a permanent pull-up resistor to VDDIO of about 100 k Ω . By default, the NRST pin is configured as an input.

6.5 ERASE Pin

The ERASE pin is used to reinitialize the Flash content (and some of its NVM bits) to an erased state (all bits read as logic level 1). It integrates a pull-down resistor of about 100 k Ω to GND, so that it can be left unconnected for normal operations.

This pin is debounced by SCLK to improve the glitch tolerance. When the ERASE pin is tied high during less than 100 ms, it is not taken into account. The pin must be tied high during more than 220 ms to perform a Flash erase operation.

The ERASE pin is a system I/O pin and can be used as a standard I/O. At startup, the ERASE pin is not configured as a PIO pin. If the ERASE pin is used as a standard I/O, startup level of this pin must be low to prevent unwanted erasing. Please refer to Section 11.2 "Peripheral Signals Multiplexing on I/O Lines" on page 42. Also, if the ERASE pin is used as a standard I/O output, asserting the pin to low does not erase the Flash.

7.7 Debug and Test Features

- Debug access to all memory and registers in the system, including Cortex-M3 register bank when the core is running, halted, or held in reset.
- Serial Wire Debug Port (SW-DP) and Serial Wire JTAG Debug Port (SWJ-DP) debug access
- Flash Patch and Breakpoint (FPB) unit for implementing breakpoints and code patches
- Data Watchpoint and Trace (DWT) unit for implementing watchpoints, data tracing, and system profiling
- Instrumentation Trace Macrocell (ITM) for support of printf style debugging
- IEEE1149.1 JTAG Boundary-can on All Digital Pins



SAM3N Summary

9. Memories

9.1 Embedded Memories

9.1.1 Internal SRAM

The SAM3N4 product embeds a total of 24-Kbytes high-speed SRAM.

The SAM3N2 product embeds a total of 16-Kbytes high-speed SRAM.

The SAM3N1 product embeds a total of 8-Kbytes high-speed SRAM.

The SRAM is accessible over System Cortex-M3 bus at address 0x2000 0000.

The SRAM is in the bit band region. The bit band alias region is from $0x2200\ 0000$ and 0x23FF FFFF.

RAM size must be configurable by calibration fuses.

9.1.2 Internal ROM

The SAM3N product embeds an Internal ROM, which contains the SAM Boot Assistant (SAM-BA), In Application Programming routines (IAP) and Fast Flash Programming Interface (FFPI).

At any time, the ROM is mapped at address 0x0080 0000.

9.1.3 Embedded Flash

9.1.3.1 Flash Overview

The Flash of the SAM3N4 (256 Kbytes) is organized in one bank of 1024 pages of 256 bytes (Single plane).

The Flash of the SAM3N2 (128 Kbytes) is organized in one bank of 512 pages of 256 bytes (Single Plane).

The Flash of the SAM3N1 (64 Kbytes) is organized in one bank of 256 pages of 256 bytes (Single plane).

The Flash contains a 128-byte write buffer, accessible through a 32-bit interface.

9.1.3.2 Flash Power Supply

The Flash is supplied by VDDCORE.

9.1.3.3 Enhanced Embedded Flash Controller

The Enhanced Embedded Flash Controller (EEFC) manages accesses performed by the masters of the system. It enables reading the Flash and writing the write buffer. It also contains a User Interface, mapped on the APB.

The Enhanced Embedded Flash Controller ensures the interface of the Flash block with the 32bit internal bus. Its 128-bit wide memory interface increases performance.

The user can choose between high performance or lower current consumption by selecting either 128-bit or 64-bit access. It also manages the programming, erasing, locking and unlocking sequences of the Flash using a full set of commands.

One of the commands returns the embedded Flash descriptor definition that informs the system about the Flash organization, thus making the software generic.





9.1.3.4 Flash Speed

The user needs to set the number of wait states depending on the frequency used.

For more details, refer to the AC Characteristics sub section in the product Electrical Characteristics Section.

9.1.3.5 Lock Regions

Several lock bits used to protect write and erase operations on lock regions. A lock region is composed of several consecutive pages, and each lock region has its associated lock bit.

Product	Number of lock bits	Lock region size
SAM3N4	16	16 kbytes (64 pages)
SAM3N2	8	16 kbytes (64 pages)
SAM3N1	4	16 kbytes (64 pages)

Table 9-1. Lock bit number

If a locked-region's erase or program command occurs, the command is aborted and the EEFC triggers an interrupt.

The lock bits are software programmable through the EEFC User Interface. The command "Set Lock Bit" enables the protection. The command "Clear Lock Bit" unlocks the lock region.

Asserting the ERASE pin clears the lock bits, thus unlocking the entire Flash.

9.1.3.6 Security Bit Feature

The SAM3N features a security bit, based on a specific General Purpose NVM bit (GPNVM bit 0). When the security is enabled, any access to the Flash, either through the ICE interface or through the Fast Flash Programming Interface, is forbidden. This ensures the confidentiality of the code programmed in the Flash.

This security bit can only be enabled, through the command "Set General Purpose NVM Bit 0" of the EEFC User Interface. Disabling the security bit can only be achieved by asserting the ERASE pin at 1, after a full Flash erase is performed. When the security bit is deactivated, all accesses to the Flash are permitted.

It is important to note that the assertion of the ERASE pin should always be longer than 200 ms.

As the ERASE pin integrates a permanent pull-down, it can be left unconnected during normal operation. However, it is safer to connect it directly to GND for the final application.

9.1.3.7 Calibration Bits

NVM bits are used to calibrate the brownout detector and the voltage regulator. These bits are factory configured and cannot be changed by the user. The ERASE pin has no effect on the calibration bits.

9.1.3.8 Unique Identifier

Each device integrates its own 128-bit unique identifier. These bits are factory configured and cannot be changed by the user. The ERASE pin has no effect on the unique identifier.

The reset circuitry is based on a zero-power power-on reset cell and a brownout detector cell. The zero-power power-on reset allows the Supply Controller to start properly, while the software-programmable brownout detector allows detection of either a battery discharge or main voltage loss.

The Slow Clock generator is based on a 32 kHz crystal oscillator and an embedded 32 kHz RC oscillator. The Slow Clock defaults to the RC oscillator, but the software can enable the crystal oscillator and select it as the Slow Clock source.

The Supply Controller starts up the device by sequentially enabling the internal power switches and the Voltage Regulator, then it generates the proper reset signals to the core power supply.

It also enables to set the system in different low power modes and to wake it up from a wide range of events.

10.5 Clock Generator

The Clock Generator is made up of:

- One Low Power 32768Hz Slow Clock Oscillator with bypass mode
- One Low-Power RC Oscillator
- · One 3-20 MHz Crystal or Ceramic resonator Oscillator, which can be bypassed
- One Fast RC Oscillator factory programmed, 3 output frequencies can be selected: 4, 8 or 12 MHz. By default 4 MHz is selected.
- One 60 to 130 MHz programmable PLL, capable to provide the clock MCK to the processor and to the peripherals. The input frequency of PLL is from 3.5 to 20 MHz.

Figure 10-2. Clock Generator Block Diagram







Instance ID	Instance Name	NVIC Interrupt	PMC Clock Control	Instance Description
25	TC2	X	X	Timer/Counter 2
26	TC3	x	X	Timer/Counter 3
27	TC4	X	X	Timer/Counter 4
28	TC5	x	x	Timer/Counter 5
29	ADC	X	X	Analog-to-Digital Converter
30	DACC	x	x	Digital-to-Analog Converter
31	PWM	X	X	Pulse Width Modulation

Table 11-1. Peripheral Identifiers (Continued)

11.2 Peripheral Signals Multiplexing on I/O Lines

The SAM3N product features 2 PIO controllers (48-pin and 64-pin version) or 3 PIO controllers (100-pin version), PIOA, PIOB and PIOC, that multiplex the I/O lines of the peripheral set.

The SAM3N 64-pin and 100-pin PIO Controller controls up to 32 lines (see Table 10-2, "PIO available according to pin count," on page 40). Each line can be assigned to one of three peripheral functions: A, B or C. The multiplexing tables in the following paragraphs define how the I/O lines of the peripherals A, B and C are multiplexed on the PIO Controllers. The column "Comments" has been inserted in this table for the user's own comments; it may be used to track how pins are defined in an application.

Note that some peripheral functions which are output only, might be duplicated within the tables.



11.2.2 PIO Controller B Multiplexing

I/O Line	Peripheral A	Peripheral B	Peripheral C	Extra Function	System Function	Comments
PB0	PWM0			AD4		
PB1	PWM1			AD5		
PB2	URXD1	NPCS2		AD6/WKUP12		
PB3	UTXD1	PCK2		AD7		
PB4	TWD1	PWM2			TDI	
PB5	TWCK1			WKUP13	TDO/ TRACESWO	
PB6					TMS/SWDIO	
PB7					TCK/SWCLK	
PB8					XOUT	
PB9					XIN	
PB10						
PB11						
PB12					ERASE	
PB13		PCK0		DAC0		64/100-pin versions
PB14	NPCS1	PWM3				64/100-pin versions

Table 11-3. Multiplexing on PIO Controller B (PIOB)



12. Embedded Peripherals Overview

12.1 Serial Peripheral Interface (SPI)

- Supports communication with serial external devices
 - Four chip selects with external decoder support allow communication with up to 15 peripherals
 - Serial memories, such as DataFlash and 3-wire EEPROMs
 - Serial peripherals, such as ADCs, DACs, LCD Controllers, CAN Controllers and Sensors
 - External co-processors
- · Master or slave serial peripheral bus interface
 - 8- to 16-bit programmable data length per chip select
 - Programmable phase and polarity per chip select
 - Programmable transfer delays between consecutive transfers and between clock and data per chip select
 - Programmable delay between consecutive transfers
 - Selectable mode fault detection
- · Very fast transfers supported
 - Transfers with baud rates up to MCK
 - The chip select line may be left active to speed up transfers on the same device

12.2 Two Wire Interface (TWI)

- Master, Multi-Master and Slave Mode Operation
- · Compatibility with Atmel two-wire interface, serial memory and I²C compatible devices
- One, two or three bytes for slave address
- · Sequential read/write operations
- Bit Rate: Up to 400 kbit/s
- · General Call Supported in Slave Mode
- Connecting to PDC channel capabilities optimizes data transfers in Master Mode only (for TWI0 only)
 - One channel for the receiver, one channel for the transmitter
 - Next buffer support

12.3 Universal Asynchronous Receiver Transceiver (UART)

- Two-pin UART
 - Implemented features are 100% compatible with the standard Atmel USART
 - Independent receiver and transmitter with a common programmable Baud Rate Generator
 - Even, Odd, Mark or Space Parity Generation
 - Parity, Framing and Overrun Error Detection
 - Automatic Echo, Local Loopback and Remote Loopback Channel Modes

4 SAM3N Summary

 Support for two PDC channels with connection to receiver and transmitter (for UART0 only)

12.4 USART

- Programmable Baud Rate Generator
- 5- to 9-bit full-duplex synchronous or asynchronous serial communications
 - 1, 1.5 or 2 stop bits in Asynchronous Mode or 1 or 2 stop bits in Synchronous Mode
 - Parity generation and error detection
 - Framing error detection, overrun error detection
 - MSB- or LSB-first
 - Optional break generation and detection
 - By 8 or by-16 over-sampling receiver frequency
 - Hardware handshaking RTS-CTS
 - Receiver time-out and transmitter timeguard
 - Optional Multi-drop Mode with address generation and detection
- RS485 with driver control signal
- ISO7816, T = 0 or T = 1 Protocols for interfacing with smart cards (Only on USART0)
 - NACK handling, error counter with repetition and iteration limit
- SPI Mode
 - Master or Slave
 - Serial Clock programmable Phase and Polarity
 - SPI Serial Clock (SCK) Frequency up to MCK/4
- IrDA modulation and demodulation (Only on USART0)
 - Communication at up to 115.2 Kbps
- Test Modes
 - Remote Loopback, Local Loopback, Automatic Echo
- PDC support (for USART0 only)

12.5 Timer Counter (TC)

- Six 16-bit Timer Counter Channels
- Wide range of functions including:
 - Frequency Measurement
 - Event Counting
 - Interval Measurement
 - Pulse Generation
 - Delay Timing
 - Pulse Width Modulation
 - Up/down Capabilities
- Each channel is user-configurable and contains:
 - Three external clock inputs
 - Five internal clock inputs





- Two multi-purpose input/output signals
- Two global registers that act on all three TC Channels
- Quadrature decoder
 - Advanced line filtering
 - Position/revolution/speed
- 2-bit Gray Up/Down Counter for Stepper Motor

12.6 Pulse Width Modulation Controller (PWM)

- Four channels, one 16-bit counter per channel
- · Common clock generator, providing thirteen different clocks
 - One Modulo n counter providing eleven clocks
 - Two independent linear dividers working on modulo n counter outputs
- Independent channel programming
 - Independent enable/disable commands
 - Independent clock selection
 - Independent period and duty cycle, with double buffering
 - Programmable selection of the output waveform polarity

12.7 10-bit Analog-to-Digital Converter

- Up to 16-channel ADC
- 10-bit 384 Ksamples/sec. or 8-bit 583 Ksamples/sec. Successive Approximation Register ADC
- ±2 LSB Integral Non Linearity, ±1 LSB Differential Non Linearity
- Integrated 8-to-1 multiplexer, offering eight independent 3.3V analog inputs
- · External voltage reference for better accuracy on low voltage inputs
- · Individual enable and disable of each channel
- Multiple trigger source
 - Hardware or software trigger
 - External trigger pin
 - Timer Counter 0 to 2 outputs TIOA0 to TIOA2 trigger
- · Sleep Mode and conversion sequencer
 - Automatic wakeup on trigger and back to sleep mode after conversions of all enabled channels

12.8 Digital-to-Analog Converter (DAC)

- 1 channel 10-bit DAC
- Up to 500 ksamples/s conversion rate
- · Flexible conversion range
- Multiple trigger sources
- One PDC channel



Table 13-1.	Table 13-1. 48-lead LQFP Package Dimensions (in mm)									
Cumhal		Millimeter			Inch					
Symbol	Min	Nom	Мах	Min	Nom	Max				
А	-	-	1.60	-	-	0.063				
A1	0.05	-	0.15	0.002	-	0.006				
A2	1.35	1.40	1.45	0.053	0.055	0.057				
D		9.00 BSC			0.354 BSC					
D1		7.00 BSC			0.276 BSC					
E		9.00 BSC			0.354 BSC					
E1		7.00 BSC			0.276 BSC					
R2	0.08	-	0.20	0.003	-	0.008				
R1	0.08	-	_	0.003	-	_				
q	0°	3.5°	7 °	0°	3.5°	7°				
θ1	0°	-	_	0°	-	_				
θ2	11°	12°	13°	11°	12°	13°				
θ3	11°	12°	13°	11°	12°	13°				
с	0.09	-	0.20	0.004	-	0.008				
L	0.45	0.60	0.75	0.018	0.024	0.030				
L1		1.00 REF		0.039 REF						
S	0.20	-	-	0.008	-	-				
b	0.17	0.20	0.27	0.007	0.008	0.011				
е		0.50 BSC.			0.020 BSC.					
D2		5.50		0.217						
E2		5.50	0.217							
		Toleranc	es of Form and	d Position						
ааа		0.20		0.008						
bbb		0.20		0.008						
ссс		0.08			0.003					
ddd		0.08		0.003						







s4 SAM3N Summary



Figure 13-5. 64-pad QFN Package Drawing



sG

SAM3N Summar

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