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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	I ² C, IrDA, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	34
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.62V ~ 3.6V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-VFQFN Exposed Pad
Supplier Device Package	48-QFN (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/atmel/atsam3n1aa-mu

Figure 2-2. SAM3N 64-pin version Block Diagram

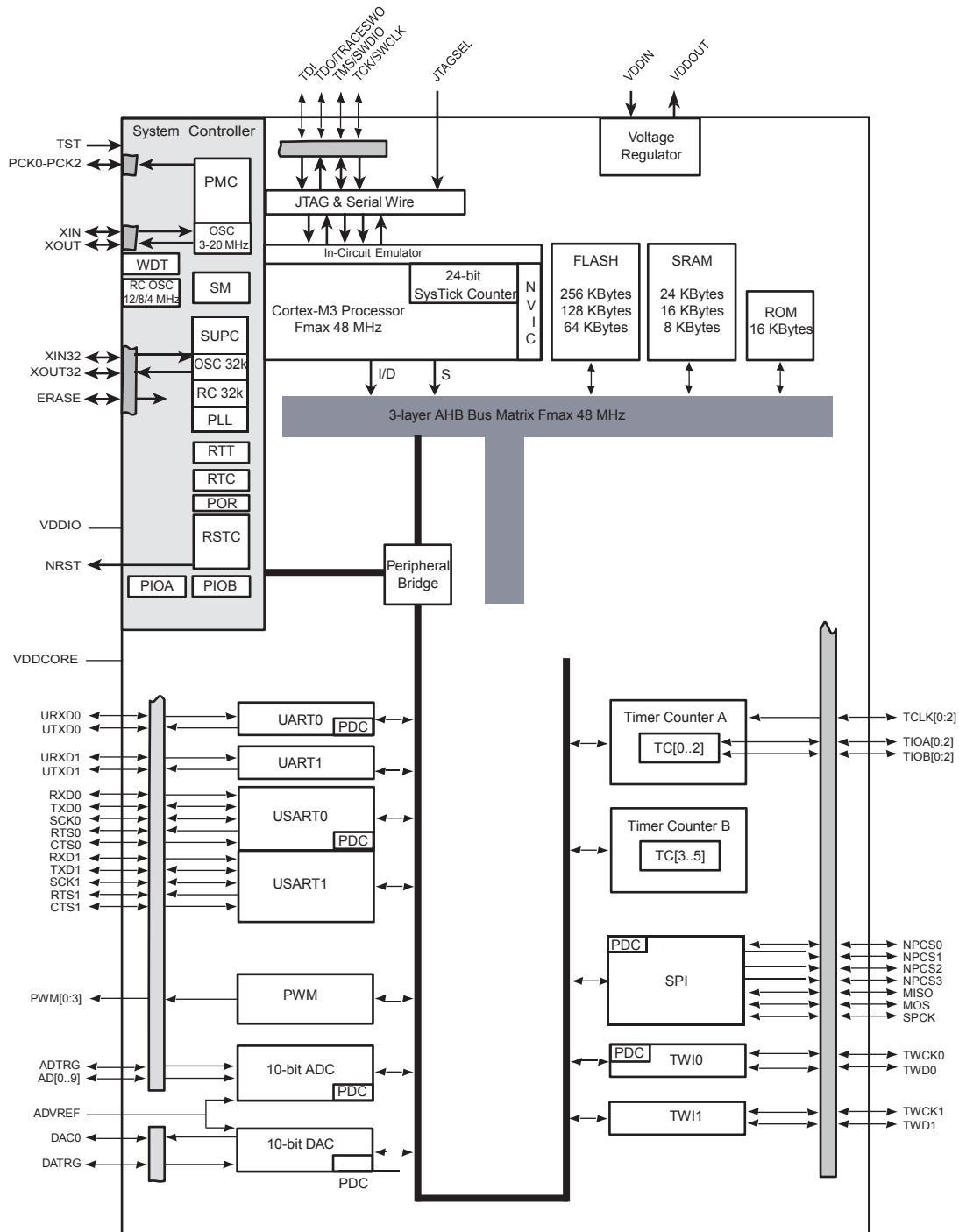


Figure 2-3. SAM3N 48-pin version Block Diagram

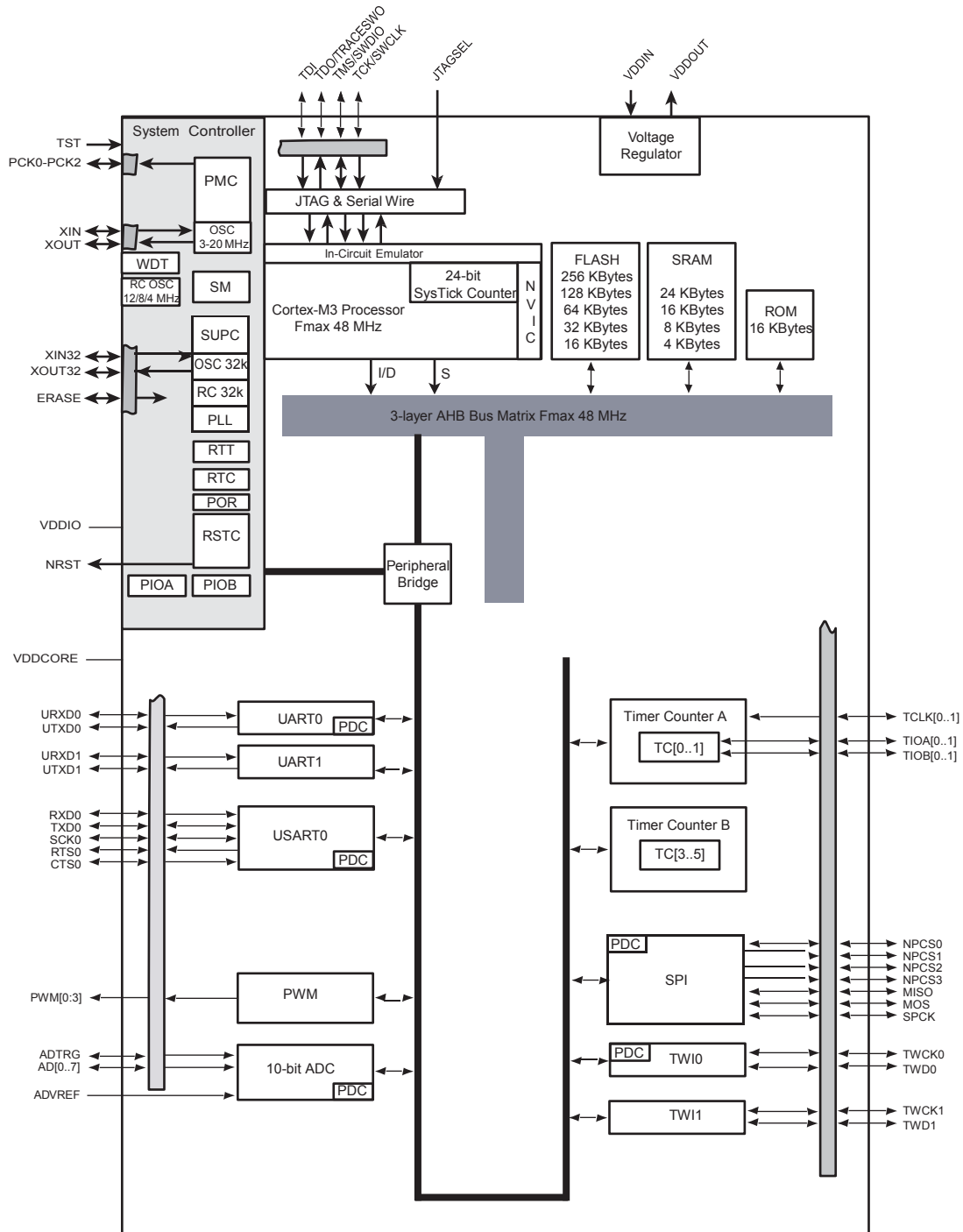


Table 3-1. Signal Description List (Continued)

Signal Name	Function	Type	Active Level	Voltage Reference	Comments
Serial Peripheral Interface - SPI					
MISO	Master In Slave Out	I/O			
MOSI	Master Out Slave In	I/O			
SPCK	SPI Serial Clock	I/O			
SPI_NPCS0	SPI Peripheral Chip Select 0	I/O	Low		
SPI_NPCS1 - SPI_NPCS3	SPI Peripheral Chip Select	Output	Low		
Two-Wire Interface- TWI_x					
TWD _x	TWI _x Two-wire Serial Data	I/O			
TWCK _x	TWI _x Two-wire Serial Clock	I/O			
Analog					
ADVREF	ADC and DAC Reference	Analog			
10-bit Analog-to-Digital Converter - ADC					
AD0 - AD15	Analog Inputs	Analog			
ADTRG	ADC Trigger	Input		VDDIO	
Digital-to-Analog Converter Controller- DACC					
DAC0	DACC channel analog output	Analog			
DATR	DACC Trigger	Input		VDDIO	
Fast Flash Programming Interface					
PGMEN0-PGMEN2	Programming Enabling	Input		VDDIO	
PGMM0-PGMM3	Programming Mode	Input			
PGMD0-PGMD15	Programming Data	I/O			
PGMRDY	Programming Ready	Output	High		
PGMNVALID	Data Direction	Output	Low		
PGMNOE	Programming Read	Input	Low		
PGMCK	Programming Clock	Input			
PGMNCMD	Programming Command	Input	Low		

- Notes:
1. Schmitt Triggers can be disabled through PIO registers.
 2. Some PIO lines are shared with System IOs.
 3. See [Section 5.3 “Typical Powering Schematics”](#) for restriction on voltage range of Analog Cells.

4.1.4 100-ball TFBGA Pinout

Table 4-2. 100-ball TFBGA SAM3N4/2/1/0/00C Pinout

A1	PB1	C6	PB7	F1	PA18	H6	PC4
A2	PC29	C7	PC16	F2	PC26	H7	PA11
A3	VDDIO	C8	PA1	F3	VDDOUT	H8	PC1
A4	PB9	C9	PC17	F4	GND	H9	PA6
A5	PB8	C10	PA0	F5	VDDIO	H10	PB4
A6	PB13	D1	PB3	F6	PA27	J1	PC15
A7	PB11	D2	PB0	F7	PC8	J2	PC0
A8	PB10	D3	PC24	F8	PA28	J3	PA16
A9	PB6	D4	PC22	F9	TST	J4	PC6
A10	JTAGSEL	D5	GND	F10	PC9	J5	PA24
B1	PC30	D6	GND	G1	PA21	J6	PA25
B2	ADVREF	D7	VDDCORE	G2	PC27	J7	PA10
B3	GNDANA	D8	PA2	G3	PA15	J8	GND
B4	PB14	D9	PC11	G4	VDDCORE	J9	VDDCORE
B5	PC21	D10	PC14	G5	VDDCORE	J10	VDDIO
B6	PC20	E1	PA17	G6	PA26	K1	PA22
B7	PA31	E2	PC31	G7	PA12	K2	PC13
B8	PC19	E3	VDDIN	G8	PC28	K3	PC12
B9	PC18	E4	GND	G9	PA4	K4	PA20
B10	PB5	E5	GND	G10	PA5	K5	PC5
C1	PB2	E6	NRST	H1	PA19	K6	PC3
C2	VDDPLL	E7	PA29	H2	PA23	K7	PC2
C3	PC25	E8	PA30	H3	PC7	K8	PA9
C4	PC23	E9	PC10	H4	PA14	K9	PA8
C5	PB12	E10	PA3	H5	PA13	K10	PA7

4.3 SAM3N4/2/1/0/00A Package and Pinout

Figure 4-5. Orientation of the 48-pad QFN Package

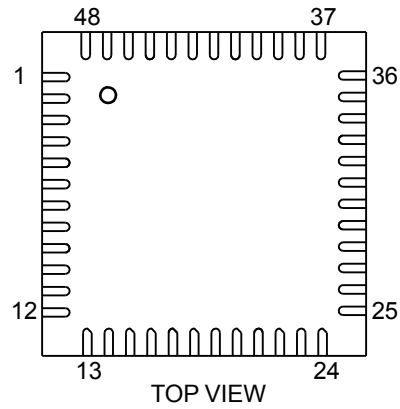
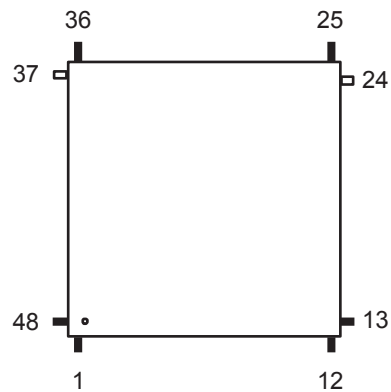


Figure 4-6. Orientation of the 48-lead LQFP Package



5. Power Considerations

5.1 Power Supplies

The SAM3N product has several types of power supply pins:

- VDDCORE pins: Power the core, including the processor, the embedded memories and the peripherals. Voltage ranges from 1.62V and 1.95V.
- VDDIO pins: Power the Peripherals I/O lines, Backup part, 32 kHz crystal oscillator and oscillator pads. Voltage ranges from 1.62V and 3.6V
- VDDIN pin: Voltage Regulator, ADC and DAC Power Supply. Voltage ranges from 1.8V to 3.6V for the Voltage Regulator
- VDDPLL pin: Powers the PLL, the Fast RC and the 3 to 20 MHz oscillators. Voltage ranges from 1.62V and 1.95V.

5.2 Voltage Regulator

The SAM3N embeds a voltage regulator that is managed by the Supply Controller.

This internal regulator is intended to supply the internal core of SAM3N. It features two different operating modes:

- In Normal mode, the voltage regulator consumes less than 700 μ A static current and draws 60 mA of output current. Internal adaptive biasing adjusts the regulator quiescent current depending on the required load current. In Wait Mode quiescent current is only 7 μ A.
- In Backup mode, the voltage regulator consumes less than 1 μ A while its output (VDDOUT) is driven internally to GND. The default output voltage is 1.80V and the start-up time to reach Normal mode is less than 100 μ s.

For adequate input and output power supply decoupling/bypassing, refer to the Voltage Regulator section in the Electrical Characteristics section of the datasheet.

5.3 Typical Powering Schematics

The SAM3N supports a 1.62V-3.6V single supply mode. The internal regulator input connected to the source and its output feeds VDDCORE. [Figure 5-1](#) shows the power schematics.

As VDDIN powers the voltage regulator and the ADC/DAC, when the user does not want to use the embedded voltage regulator, it can be disabled by software via the SUPC (note that it is different from Backup mode).

6. Input/Output Lines

The SAM3N has several kinds of input/output (I/O) lines such as general purpose I/Os (GPIO) and system I/Os. GPIOs can have alternate functionality due to multiplexing capabilities of the PIO controllers. The same PIO line can be used whether in IO mode or by the multiplexed peripheral. System I/Os include pins such as test pins, oscillators, erase or analog inputs.

6.1 General Purpose I/O Lines

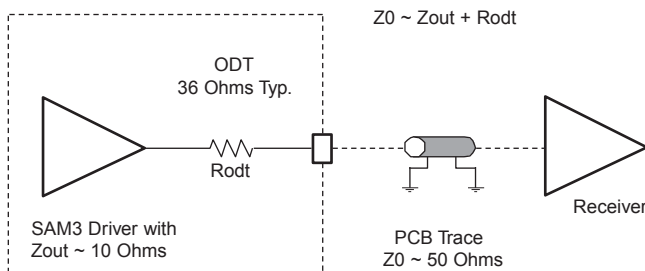
GPIO Lines are managed by PIO Controllers. All I/Os have several input or output modes such as pull-up or pull-down, input Schmitt triggers, multi-drive (open-drain), glitch filters, debouncing or input change interrupt. Programming of these modes is performed independently for each I/O line through the PIO controller user interface. For more details, refer to the product PIO controller section.

The input output buffers of the PIO lines are supplied through VDDIO power supply rail.

The SAM3N embeds high speed pads able to handle up to 45 MHz for SPI clock lines and 35 MHz on other lines. See AC Characteristics Section in the Electrical Characteristics Section of the datasheet for more details. Typical pull-up and pull-down value is 100 kΩ for all I/Os.

Each I/O line also embeds an ODT (On-Die Termination), (see [Figure 6-1](#)). It consists of an internal series resistor termination scheme for impedance matching between the driver output (SAM3N) and the PCB trace impedance preventing signal reflection. The series resistor helps to reduce I/O switching current (di/dt) thereby reducing in turn, EMI. It also decreases overshoot and undershoot (ringing) due to inductance of interconnect between devices or between boards. In conclusion ODT helps diminish signal integrity issues.

Figure 6-1. On-Die Termination



6.2 System I/O Lines

System I/O lines are pins used by oscillators, test mode, reset and JTAG to name but a few. Described below are the SAM3N system I/O lines shared with PIO lines:

These pins are software configurable as general purpose I/O or system pins. At startup the default function of these pins is always used.

6.3 Test Pin

The TST pin is used for JTAG Boundary Scan Manufacturing Test or Fast Flash programming mode of the SAM3N series. The TST pin integrates a permanent pull-down resistor of about 15 kΩ to GND, so that it can be left unconnected for normal operations. To enter fast programming mode, see the Fast Flash Programming Interface (FFPI) section. For more on the manufacturing and test mode, refer to the “Debug and Test” section of the product datasheet.

6.4 NRST Pin

The NRST pin is bidirectional. It is handled by the on-chip reset controller and can be driven low to provide a reset signal to the external components or asserted low externally to reset the microcontroller. It will reset the Core and the peripherals except the Backup region (RTC, RTT and Supply Controller). There is no constraint on the length of the reset pulse and the reset controller can guarantee a minimum pulse length. The NRST pin integrates a permanent pull-up resistor to VDDIO of about 100 kΩ. By default, the NRST pin is configured as an input.

6.5 ERASE Pin

The ERASE pin is used to reinitialize the Flash content (and some of its NVM bits) to an erased state (all bits read as logic level 1). It integrates a pull-down resistor of about 100 kΩ to GND, so that it can be left unconnected for normal operations.

This pin is debounced by SCLK to improve the glitch tolerance. When the ERASE pin is tied high during less than 100 ms, it is not taken into account. The pin must be tied high during more than 220 ms to perform a Flash erase operation.

The ERASE pin is a system I/O pin and can be used as a standard I/O. At startup, the ERASE pin is not configured as a PIO pin. If the ERASE pin is used as a standard I/O, startup level of this pin must be low to prevent unwanted erasing. Please refer to [Section 11.2 “Peripheral Signals Multiplexing on I/O Lines” on page 42](#). Also, if the ERASE pin is used as a standard I/O output, asserting the pin to low does not erase the Flash.

7. Processor and Architecture

7.1 ARM Cortex-M3 Processor

- Version 2.0
- Thumb-2 (ISA) subset consisting of all base Thumb-2 instructions, 16-bit and 32-bit.
- Harvard processor architecture enabling simultaneous instruction fetch with data load/store.
- Three-stage pipeline.
- Single cycle 32-bit multiply.
- Hardware divide.
- Thumb and Debug states.
- Handler and Thread modes.
- Low latency ISR entry and exit.

7.2 APB/AHB Bridge

The SAM3N4/2/1/0/00 product embeds one peripheral bridge:

The peripherals of the bridge are clocked by MCK.

7.3 Matrix Masters

The Bus Matrix of the SAM3N product manages 3 masters, which means that each master can perform an access concurrently with others, to an available slave.

Each master has its own decoder, which is defined specifically for each master. In order to simplify the addressing, all the masters have the same decodings.

Table 7-1. List of Bus Matrix Masters

Master 0	Cortex-M3 Instruction/Data
Master 1	Cortex-M3 System
Master 2	Peripheral DMA Controller (PDC)

7.4 Matrix Slaves

The Bus Matrix of the SAM3N product manages 4 slaves. Each slave has its own arbiter, allowing a different arbitration per slave.

Table 7-2. List of Bus Matrix Slaves

Slave 0	Internal SRAM
Slave 1	Internal ROM
Slave 2	Internal Flash
Slave 3	Peripheral Bridge

9. Memories

9.1 Embedded Memories

9.1.1 Internal SRAM

The SAM3N4 product embeds a total of 24-Kbytes high-speed SRAM.

The SAM3N2 product embeds a total of 16-Kbytes high-speed SRAM.

The SAM3N1 product embeds a total of 8-Kbytes high-speed SRAM.

The SRAM is accessible over System Cortex-M3 bus at address 0x2000 0000.

The SRAM is in the bit band region. The bit band alias region is from 0x2200 0000 and 0x23FF FFFF.

RAM size must be configurable by calibration fuses.

9.1.2 Internal ROM

The SAM3N product embeds an Internal ROM, which contains the SAM Boot Assistant (SAM-BA), In Application Programming routines (IAP) and Fast Flash Programming Interface (FFPI).

At any time, the ROM is mapped at address 0x0080 0000.

9.1.3 Embedded Flash

9.1.3.1 Flash Overview

The Flash of the SAM3N4 (256 Kbytes) is organized in one bank of 1024 pages of 256 bytes (Single plane).

The Flash of the SAM3N2 (128 Kbytes) is organized in one bank of 512 pages of 256 bytes (Single Plane).

The Flash of the SAM3N1 (64 Kbytes) is organized in one bank of 256 pages of 256 bytes (Single plane).

The Flash contains a 128-byte write buffer, accessible through a 32-bit interface.

9.1.3.2 Flash Power Supply

The Flash is supplied by VDDCORE.

9.1.3.3 Enhanced Embedded Flash Controller

The Enhanced Embedded Flash Controller (EEFC) manages accesses performed by the masters of the system. It enables reading the Flash and writing the write buffer. It also contains a User Interface, mapped on the APB.

The Enhanced Embedded Flash Controller ensures the interface of the Flash block with the 32-bit internal bus. Its 128-bit wide memory interface increases performance.

The user can choose between high performance or lower current consumption by selecting either 128-bit or 64-bit access. It also manages the programming, erasing, locking and unlocking sequences of the Flash using a full set of commands.

One of the commands returns the embedded Flash descriptor definition that informs the system about the Flash organization, thus making the software generic.

9.1.3.4 Flash Speed

The user needs to set the number of wait states depending on the frequency used.

For more details, refer to the AC Characteristics sub section in the product Electrical Characteristics Section.

9.1.3.5 Lock Regions

Several lock bits used to protect write and erase operations on lock regions. A lock region is composed of several consecutive pages, and each lock region has its associated lock bit.

Table 9-1. Lock bit number

Product	Number of lock bits	Lock region size
SAM3N4	16	16 kbytes (64 pages)
SAM3N2	8	16 kbytes (64 pages)
SAM3N1	4	16 kbytes (64 pages)

If a locked-region's erase or program command occurs, the command is aborted and the EEFC triggers an interrupt.

The lock bits are software programmable through the EEFC User Interface. The command "Set Lock Bit" enables the protection. The command "Clear Lock Bit" unlocks the lock region.

Asserting the ERASE pin clears the lock bits, thus unlocking the entire Flash.

9.1.3.6 Security Bit Feature

The SAM3N features a security bit, based on a specific General Purpose NVM bit (GPNVM bit 0). When the security is enabled, any access to the Flash, either through the ICE interface or through the Fast Flash Programming Interface, is forbidden. This ensures the confidentiality of the code programmed in the Flash.

This security bit can only be enabled, through the command "Set General Purpose NVM Bit 0" of the EEFC User Interface. Disabling the security bit can only be achieved by asserting the ERASE pin at 1, after a full Flash erase is performed. When the security bit is deactivated, all accesses to the Flash are permitted.

It is important to note that the assertion of the ERASE pin should always be longer than 200 ms.

As the ERASE pin integrates a permanent pull-down, it can be left unconnected during normal operation. However, it is safer to connect it directly to GND for the final application.

9.1.3.7 Calibration Bits

NVM bits are used to calibrate the brownout detector and the voltage regulator. These bits are factory configured and cannot be changed by the user. The ERASE pin has no effect on the calibration bits.

9.1.3.8 Unique Identifier

Each device integrates its own 128-bit unique identifier. These bits are factory configured and cannot be changed by the user. The ERASE pin has no effect on the unique identifier.

10.1 System Controller and Peripherals Mapping

Please refer to [Figure 8-1, "SAM3N4/2/1/0/00 Product Mapping" on page 30](#).

All the peripherals are in the bit band region and are mapped in the bit band alias region.

10.2 Power-on-Reset, Brownout and Supply Monitor

The SAM3N embeds three features to monitor, warn and/or reset the chip:

- Power-on-Reset on VDDIO
- Brownout Detector on VDDCORE
- Supply Monitor on VDDIO

10.2.1 Power-on-Reset

The Power-on-Reset monitors VDDIO. It is always activated and monitors voltage at start up but also during power down. If VDDIO goes below the threshold voltage, the entire chip is reset. For more information, refer to the Electrical Characteristics section of the datasheet.

10.2.2 Brownout Detector on VDDCORE

The Brownout Detector monitors VDDCORE. It is active by default. It can be deactivated by software through the Supply Controller (SUPC_MR). It is especially recommended to disable it during low-power modes such as wait or sleep modes.

If VDDCORE goes below the threshold voltage, the reset of the core is asserted. For more information, refer to the Supply Controller (SUPC) and Electrical Characteristics sections of the datasheet.

10.2.3 Supply Monitor on VDDIO

The Supply Monitor monitors VDDIO. It is inactive by default. It can be activated by software and is fully programmable with 16 steps for the threshold (between 1.9V to 3.4V). It is controlled by the Supply Controller (SUPC). A sample mode is possible. It allows to divide the supply monitor power consumption by a factor of up to 2048. For more information, refer to the SUPC and Electrical Characteristics sections of the datasheet.

10.3 Reset Controller

The Reset Controller is based on a Power-on-Reset cell, and a Supply Monitor on VDDCORE.

The Reset Controller is capable to return to the software the source of the last reset, either a general reset, a wake-up reset, a software reset, a user reset or a watchdog reset.

The Reset Controller controls the internal resets of the system and the NRST pin input/output. It is capable to shape a reset signal for the external devices, simplifying to a minimum connection of a push-button on the NRST pin to implement a manual reset.

The configuration of the Reset Controller is saved as supplied on VDDIO.

10.4 Supply Controller (SUPC)

The Supply Controller controls the power supplies of each section of the processor and the peripherals (via Voltage regulator control)

The Supply Controller has its own reset circuitry and is clocked by the 32 kHz slow clock generator.

The reset circuitry is based on a zero-power power-on reset cell and a brownout detector cell. The zero-power power-on reset allows the Supply Controller to start properly, while the software-programmable brownout detector allows detection of either a battery discharge or main voltage loss.

The Slow Clock generator is based on a 32 kHz crystal oscillator and an embedded 32 kHz RC oscillator. The Slow Clock defaults to the RC oscillator, but the software can enable the crystal oscillator and select it as the Slow Clock source.

The Supply Controller starts up the device by sequentially enabling the internal power switches and the Voltage Regulator, then it generates the proper reset signals to the core power supply.

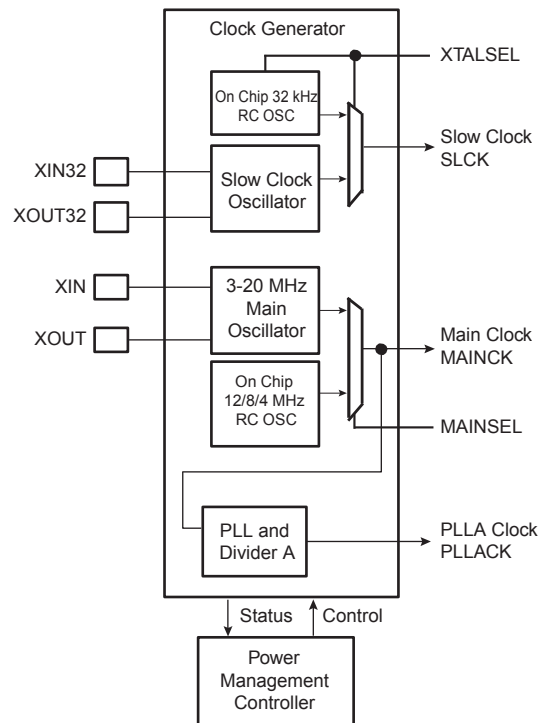
It also enables to set the system in different low power modes and to wake it up from a wide range of events.

10.5 Clock Generator

The Clock Generator is made up of:

- One Low Power 32768Hz Slow Clock Oscillator with bypass mode
- One Low-Power RC Oscillator
- One 3-20 MHz Crystal or Ceramic resonator Oscillator, which can be bypassed
- One Fast RC Oscillator factory programmed, 3 output frequencies can be selected: 4, 8 or 12 MHz. By default 4 MHz is selected.
- One 60 to 130 MHz programmable PLL, capable to provide the clock MCK to the processor and to the peripherals. The input frequency of PLL is from 3.5 to 20 MHz.

Figure 10-2. Clock Generator Block Diagram



10.13 Chip Identification

- Chip Identifier (CHIPID) registers permit recognition of the device and its revision.

Table 10-1. SAM3N Chip ID Register

Chip Name	CHIPID_CIDR	CHIPID_EXID
ATSAM3N4C (Rev A)	0x29540960	0x0
ATSAM3N2C (Rev A)	0x29590760	0x0
ATSAM3N1C (Rev A)	0x29580560	0x0
ATSAM3N4B (Rev A)	0x29440960	0x0
ATSAM3N2B (Rev A)	0x29490760	0x0
ATSAM3N1B (Rev A)	0x29480560	0x0
ATSAM3N4A (Rev A)	0x29340960	0x0
ATSAM3N2A (Rev A)	0x29390760	0x0
ATSAM3N1A (Rev A)	0x29380560	0x0

- JTAG ID: 0x05B2E03F

10.14 UART

- Two-pin UART
 - Implemented features are 100% compatible with the standard Atmel USART
 - Independent receiver and transmitter with a common programmable Baud Rate Generator
 - Even, Odd, Mark or Space Parity Generation
 - Parity, Framing and Overrun Error Detection
 - Automatic Echo, Local Loopback and Remote Loopback Channel Modes
 - Support for two PDC channels with connection to receiver and transmitter

10.15 PIO Controllers

- 3 PIO Controllers, PIOA, PIOB and PIOC (100-pin version only) controlling a maximum of 79 I/O Lines
- Each PIO Controller controls up to 32 programmable I/O Lines
- Fully programmable through Set/Clear Registers

Table 10-2. PIO available according to pin count

Version	48 pin	64 pin	100 pin
PIOA	21	32	32
PIOB	13	15	15
PIOC	-	-	32

- Multiplexing of four peripheral functions per I/O Line
- For each I/O Line (whether assigned to a peripheral or used as general purpose I/O)
 - Input change, rising edge, falling edge, low level and level interrupt
 - Debouncing and Glitch filter

11.2.1 PIO Controller A Multiplexing

Table 11-2. Multiplexing on PIO Controller A (PIOA)

I/O Line	Peripheral A	Peripheral B	Peripheral C	Extra Function	System Function	Comments
PA0	PWM0	TIOA0		WKUP0		High drive
PA1	PWM1	TIOB0		WKUP1		High drive
PA2	PWM2	SCK0	DATRG	WKUP2		High drive
PA3	TWD0	NPCS3				High drive
PA4	TWCK0	TCLK0		WKUP3		
PA5	RXD0	NPCS3		WKUP4		
PA6	TXD0	PCK0				
PA7	RTS0	PWM3			XIN32	
PA8	CTS0	ADTRG		WKUP5	XOUT32	
PA9	URXD0	NPCS1		WKUP6		
PA10	UTXD0	NPCS2				
PA11	NPCS0	PWM0		WKUP7		
PA12	MISO	PWM1				
PA13	MOSI	PWM2				
PA14	SPCK	PWM3		WKUP8		
PA15		TIOA1		WKUP14		
PA16		TIOB1		WKUP15		
PA17		PCK1		AD0		
PA18		PCK2		AD1		
PA19				AD2/WKUP9		
PA20				AD3/WKUP10		
PA21	RXD1	PCK1		AD8		64/100-pin versions
PA22	TXD1	NPCS3		AD9		64/100-pin versions
PA23	SCK1	PWM0				64/100-pin versions
PA24	RTS1	PWM1				64/100-pin versions
PA25	CTS1	PWM2				64/100-pin versions
PA26		TIOA2				64/100-pin versions
PA27		TIOB2				64/100-pin versions
PA28		TCLK1				64/100-pin versions
PA29		TCLK2				64/100-pin versions
PA30		NPCS2		WKUP11		64/100-pin versions
PA31	NPCS1	PCK2				64/100-pin versions

11.2.2 PIO Controller B Multiplexing

Table 11-3. Multiplexing on PIO Controller B (PIOB)

I/O Line	Peripheral A	Peripheral B	Peripheral C	Extra Function	System Function	Comments
PB0	PWM0			AD4		
PB1	PWM1			AD5		
PB2	URXD1	NPCS2		AD6/WKUP12		
PB3	UTXD1	PCK2		AD7		
PB4	TWD1	PWM2			TDI	
PB5	TWCK1			WKUP13	TDO/ TRACESWO	
PB6					TMS/SWDIO	
PB7					TCK/SWCLK	
PB8					XOUT	
PB9					XIN	
PB10						
PB11						
PB12					ERASE	
PB13		PCK0		DAC0		64/100-pin versions
PB14	NPCS1	PWM3				64/100-pin versions

11.2.3 PIO Controller C Multiplexing

I/O Line	Peripheral A	Peripheral B	Peripheral C	Extra Function	System Function	Comments
PC0						100-pin version
PC1						100-pin version
PC2						100-pin version
PC3						100-pin version
PC4		NPCS1				100-pin version
PC5						100-pin version
PC6						100-pin version
PC7		NPCS2				100-pin version
PC8		PWM0				100-pin version
PC9		PWM1				100-pin version
PC10		PWM2				100-pin version
PC11		PWM3				100-pin version
PC12				AD12		100-pin version
PC13				AD10		100-pin version
PC14		PCK2				100-pin version
PC15				AD11		100-pin version
PC16		PCK0				100-pin version
PC17		PCK1				100-pin version
PC18		PWM0				100-pin version
PC19		PWM1				100-pin version
PC20		PWM2				100-pin version
PC21		PWM3				100-pin version
PC22		PWM0				100-pin version
PC23		TIOA3				100-pin version
PC24		TIOB3				100-pin version
PC25		TCLK3				100-pin version
PC26		TIOA4				100-pin version
PC27		TIOB4				100-pin version
PC28		TCLK4				100-pin version
PC29		TIOA5		AD13		100-pin version
PC30		TIOB5		AD14		100-pin version
PC31		TCLK5		AD15		100-pin version

Table 13-2. 64-lead LQFP Package Dimensions (in mm)

Symbol	Millimeter			Inch		
	Min	Nom	Max	Min	Nom	Max
A	—	—	1.60	—	—	0.063
A1	0.05	—	0.15	0.002	—	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
D	12.00 BSC			0.472 BSC		
D1	10.00 BSC			0.383 BSC		
E	12.00 BSC			0.472 BSC		
E1	10.00 BSC			0.383 BSC		
R2	0.08	—	0.20	0.003	—	0.008
R1	0.08	—	—	0.003	—	—
q	0°	3.5°	7°	0°	3.5°	7°
θ ₁	0°	—	—	0°	—	—
θ ₂	11°	12°	13°	11°	12°	13°
θ ₃	11°	12°	13°	11°	12°	13°
c	0.09	—	0.20	0.004	—	0.008
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF			0.039 REF		
S	0.20	—	—	0.008	—	—
b	0.17	0.20	0.27	0.007	0.008	0.011
e	0.50 BSC.			0.020 BSC.		
D2	7.50			0.285		
E2	7.50			0.285		
Tolerances of Form and Position						
aaa	0.20			0.008		
bbb	0.20			0.008		
ccc	0.08			0.003		
ddd	0.08			0.003		

Figure 13-4. 48-pad QFN Package Drawing

