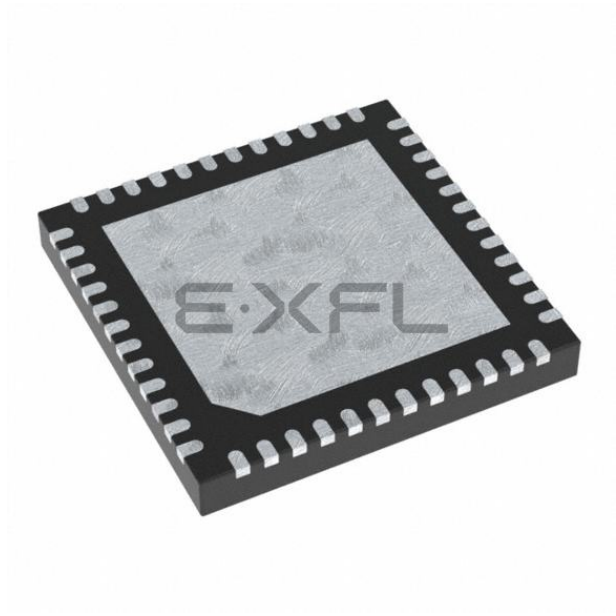

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4F
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	EBI/EMI, I²C, IrDA, LINbus, MMC/SD, QSPI, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM
Number of I/O	37
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.63V
Data Converters	A/D 20x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-VFQFN Exposed Pad
Supplier Device Package	48-QFN (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atsamd51g18a-mut

Package	Cluster	GPIO	Supply/GND Pins Connected to the Cluster
		PB31, PB30, PB25, PB24, PB23, PB22, PB21, PB20, PB19, PB18, PB17, PB16, PB15, PB14, PB13, PB12, PB11, PB10, PB09, PB08, PB07, PB06, PB05, PB04	
		PC28, PC27, PC26, PC25, PC24, PC21, PC20, PC19, PC18, PC17, PC16, PC15, PC14, PC13, PC12, PC11, PC10	
	VDDANA	PA07, PA06, PA05, PA04, PA03, PA02	V_{DDANA} pin 12 GNDANA pin 11
		PB09, PB08, PB07, PB06, PB05, PB04	
		PC03, PC02	
	VSWOUT	PA01, PA00	VSWOUT
		PB03, PB02, PB01, PB00	
		PC01, PC00	
64 Pins	VDDIOB	PA11, PA10, PA09, PA08	VDDIOB pin 21 GND pin 22
		PB11, PB10	
	VDDIO	PB12,PB13,PB14,PB15,PB16,PB17,PB30,PB31	VDDIO pins 34,48 GND pins 33,47,54
		PA12,PA13,PA16,PA17,PA18,PA19, PA20, PA21,PA22,PA23,PA24,PA25,PA27,PA30,PA31	
		PA14,PA15,PB22,PB23	
	VDDANA	PA2,PA3,PB4,PB5,PB6,PB7,PB8,PA4,PA5,PA6,PA7	VDDANA pin 8 GNDANA pin 7
	VSWOUT	PB0,PB1,PB2,PB3,PA0,PA1	VSWOUT
48 pins	VDDIO	PA8, PA9,PA10,PA11	VDDIOB pin 21 GND pin 22
		PB10,PB11,PA12,PA13,PA14,PA15	
		PA16,PA17,PA18,P19,PA20,PA21,PA22,PA23,PA24,PA25	
		PB22,PB23	VDDIO pins 17, 36, 44 GND pins 18, 35, 42
		PA27	
		PA28	
		PA30, PA31	
	VDDANA	PA2,PA3,PB8,PB9,PA4,PA5,PA6,PA7	VDDANA pin 6 GNDANA pin 5
	VSWOUT	PB2,PB3,PA0,PA1	VSWOUT

Value	Name	Description
0xB	DIV4096	Divide clock by 4096
0xC	DIV8192	Divide clock by 8192
0xD	DIV16384	Divide clock by 16384
0xE	DIV32768	Divide clock by 32768
0xF	DIV65536	Divide clock by 65536

Bit 8 – ACTCFG BOD12 Configuration in Active Sleep Mode
This field is not synchronized.

Value	Description
0	In active mode, the BOD12 operates in continuous mode.
1	In active mode, the BOD12 operates in sampling mode.

Bit 6 – RUNSTDBY Run in Standby
This bit is not synchronized.

Value	Description
0	In standby sleep mode, the BOD12 is disabled.
1	In standby sleep mode, the BOD12 is enabled.

Bit 5 – STDBYCFG BOD12 Configuration in Standby Sleep Mode
If the RUNSTDBY bit is set to 1, the STDBYCFG bit sets the BOD12 configuration in standby sleep mode.

This field is not synchronized.

Value	Description
0	In standby sleep mode, the BOD12 is enabled and configured in continuous mode.
1	In standby sleep mode, the BOD12 is enabled and configured in sampling mode.

Bits 4:3 – ACTION[1:0] BOD12 Action
These bits are used to select the BOD12 action when the supply voltage crosses below the BOD12 threshold.

These bits are loaded from NVM User Row at start-up.

This field is not synchronized.

Value	Name	Description
0x0	NONE	No action.
0x1	RESET	The BOD12 generates a reset.
0x2	INT	The BOD12 generates an interrupt.
0x3	-	Reserved

Bit 2 – HYST Hysteresis
This bit indicates whether hysteresis is enabled for the BOD12 threshold voltage:

This bit is not synchronized.

Value	Description
0	No hysteresis.
1	Hysteresis enabled.

19.8.8 Voltage References System (VREF) Control

Name: VREF
Offset: 0x1C
Reset: 0x00000000
Property: PAC Write-Protection

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
					SEL[3:0]			
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
	ONDEMAND	RUNSTDBY			TSSEL	VREFOE	TSEN	
Access	R/W	R/W			R/W	R/W	R/W	
Reset	0	0			0	0	0	

Bits 19:16 – SEL[3:0] Voltage Reference Selection
These bits select the Voltage Reference for the ADC/DAC.

Value	Name	Description
0x0	1V0	1.0V voltage reference typical value
0x1	1V1	1.1V voltage reference typical value
0x2	1V2	1.2V voltage reference typical value
0x3	1V25	1.25V voltage reference typical value
0x4	2V0	2.0V voltage reference typical value
0x5	2V2	2.2V voltage reference typical value
0x6	2V4	2.4V voltage reference typical value
0x7	2V5	2.5V voltage reference typical value
Others		Reserved

Bit 7 – ONDEMAND On Demand Control
The On Demand operation mode allows to enable or disable the voltage reference depending on peripheral requests.

Value	Description
0	The voltage reference is always on, if enabled.
1	The voltage reference is enabled when a peripheral is requesting it. The voltage reference is disabled if no peripheral is requesting it.

Value	Description
0	The output is not enabled.
1	The output is enabled and driven by the SUPC.

21.3 Block Diagram

Figure 21-1. RTC Block Diagram (Mode 0 — 32-Bit Counter)

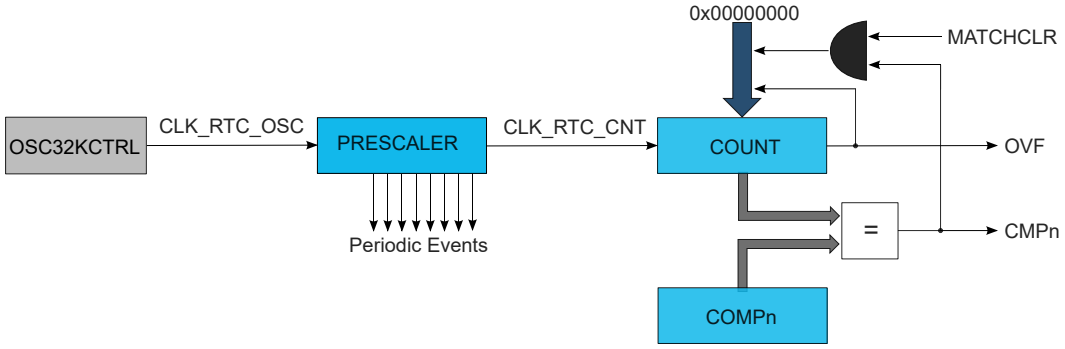


Figure 21-2. RTC Block Diagram (Mode 1 — 16-Bit Counter)

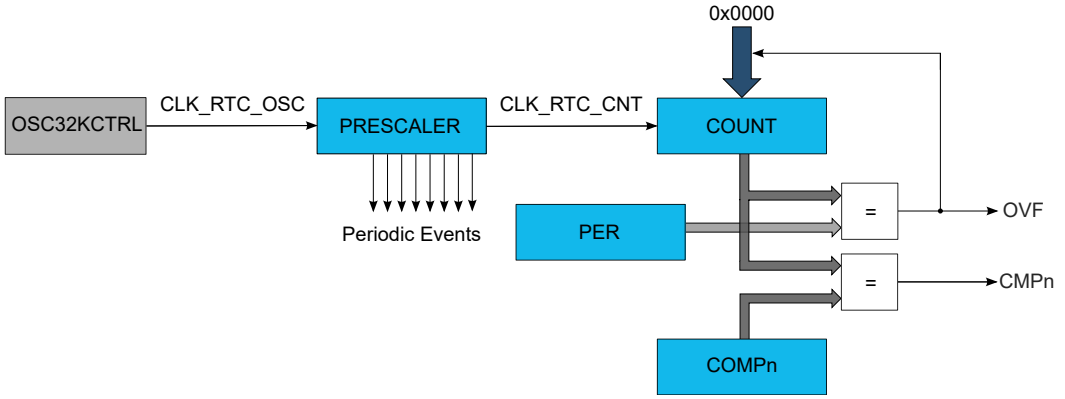
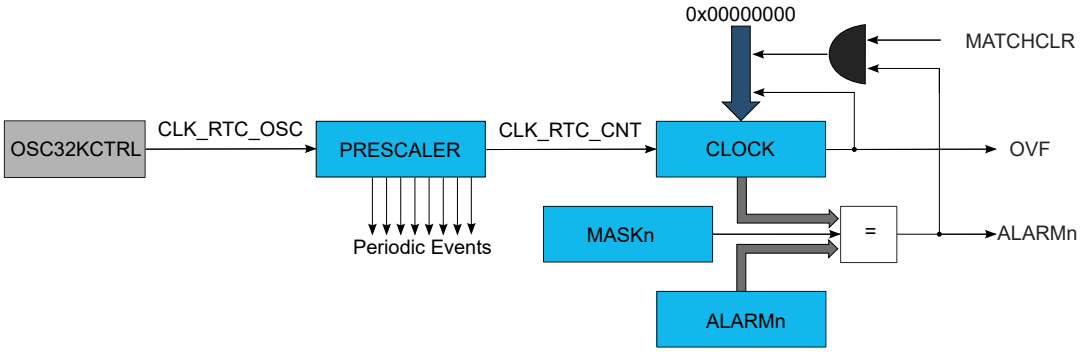


Figure 21-3. RTC Block Diagram (Mode 2 — Clock/Calendar)



21.10.2 Control B in COUNT16 mode (CTRLA.MODE=1)

Name: CTRLB
Offset: 0x02
Reset: 0x0000
Property: PAC Write-Protection, Enable-Protected

Bit	15	14	13	12	11	10	9	8
		ACTF[2:0]				DEBF[2:0]		
Access		R/W	R/W	R/W		R/W	R/W	R/W
Reset		0	0	0		0	0	0

Bit	7	6	5	4	3	2	1	0
	DMAEN	RTCOUT	DEBASYNC	DEBMAJ			GP2EN	GP0EN
Access	R/W	R/W	R/W	R/W			R/W	R/W
Reset	0	0	0	0			0	0

Bits 14:12 – ACTF[2:0] Active Layer Frequency
These bits define the prescaling factor for the RTC clock output (OUT) used during active layer protection in terms of the CLK_RTC.

Value	Name	Description
0x0	DIV2	CLK_RTC_OUT = CLK_RTC / 2
0x1	DIV4	CLK_RTC_OUT = CLK_RTC / 4
0x2	DIV8	CLK_RTC_OUT = CLK_RTC / 8
0x3	DIV16	CLK_RTC_OUT = CLK_RTC / 16
0x4	DIV32	CLK_RTC_OUT = CLK_RTC / 32
0x5	DIV64	CLK_RTC_OUT = CLK_RTC / 64
0x6	DIV128	CLK_RTC_OUT = CLK_RTC / 128
0x7	DIV256	CLK_RTC_OUT = CLK_RTC / 256

Bits 10:8 – DEBF[2:0] Debounce Frequency
These bits define the prescaling factor for the input debouncers in terms of the CLK_RTC.

Value	Name	Description
0x0	DIV2	CLK_RTC_DEB = CLK_RTC / 2
0x1	DIV4	CLK_RTC_DEB = CLK_RTC / 4
0x2	DIV8	CLK_RTC_DEB = CLK_RTC / 8
0x3	DIV16	CLK_RTC_DEB = CLK_RTC / 16
0x4	DIV32	CLK_RTC_DEB = CLK_RTC / 32
0x5	DIV64	CLK_RTC_DEB = CLK_RTC / 64
0x6	DIV128	CLK_RTC_DEB = CLK_RTC / 128
0x7	DIV256	CLK_RTC_DEB = CLK_RTC / 256

Bit 7 – DMAEN DMA Enable
The RTC can trigger a DMA request when the timestamp is ready in the TIMESTAMP register.

22.8.5 CRC Status

Name: CRCSTATUS
Offset: 0x0C
Reset: 0x00
Property: PAC Write-Protection

Bit	7	6	5	4	3	2	1	0
						CRCERR	CRCZERO	CRCBUSY
Access						R	R	R/W
Reset						0	0	0

Bit 2 – CRCERR CRC Error
This bit is read '1' when the memory CRC monitor detects data corruption.

Bit 1 – CRCZERO CRC Zero
This bit is cleared when a new CRC source is selected.

This bit is set when the CRC generation is complete and the CRC Checksum is zero.

Bit 0 – CRCBUSY CRC Module Busy
When used with an I/O interface (CRCCTRL.CRCSRC=0x1):

- This bit is cleared by writing a '1' to it
- This bit is set when the CRC Data Input (CRCDATAIN) register is written
- Writing a '1' to this bit will clear the CRC Module Busy bit
- Writing a '0' to this bit has no effect

When used with a DMA channel (CRCCTRL.CRCSRC=0x20..,0x3F):

- This bit is cleared when the corresponding DMA channel is disabled
- This bit is set when the corresponding DMA channel is enabled
- Writing a '1' to this bit has no effect
- Writing a '0' to this bit has no effect

24.9.2 GMAC Network Configuration Register

Name: NCFGR
Offset: 0x004
Reset: 0x00080000
Property: R/W

Bit	31	30	29	28	27	26	25	24
		IRXER	RXBP	IPGSEN		IRXFCS	EFRHD	RXCOEN
Access		R/W	R/W	R/W		R/W	R/W	R/W
Reset		0	0	0		0	0	0

Bit	23	22	21	20	19	18	17	16
	DCPF			CLK[2:0]			RFCS	LFERD
Access	R/W			R/W	R/W	R/W	R/W	R/W
Reset	0			0	1	0	0	0

Bit	15	14	13	12	11	10	9	8
	RXBUFO[1:0]		PEN	RTY				MAXFS
Access	R/W	R/W	R/W	R/W				R/W
Reset	0	0	0	0				0

Bit	7	6	5	4	3	2	1	0
	UNIHEN	MTIHEN	NBC	CAF	JFRAME	DNVLAN	FD	SPD
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 30 – IRXER Ignore IPG GRXER
When this bit is written to '1', the Receive Error signal (GRXER) has no effect on the GMAC operation when Receive Data Valid signal (GRXDV) is low.

Bit 29 – RXBP Receive Bad Preamble
When written to '1', frames with non-standard preamble are not rejected.

Bit 28 – IPGSEN IP Stretch Enable
Writing a '1' to this bit allows the transmit IPG to increase above 96 bit times, depending on the previous frame length using the IPG Stretch Register.

Bit 26 – IRXFCS Ignore RX FCS
For normal operation this bit must be written to zero.

When this bit is written to '1', frames with FCS/CRC errors will not be rejected. FCS error statistics will still be collected for frames with bad FCS, and FCS status will be recorded in the DMA descriptor of the frame.

Bit 25 – EFRHD Enable Frames Received in half-duplex
Writing a '1' to this bit enables frames to be received in half-duplex mode while transmitting.

24.9.79 GMAC Receive Overruns Register

Name: ROE
Offset: 0x1A4
Reset: 0x00000000
Property: Read-Only

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
							RXOVR[9:8]	
Access							R	R
Reset							0	0

Bit	7	6	5	4	3	2	1	0
	RXOVR[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 9:0 – RXOVR[9:0] Receive Overruns
This bit field counts the number of frames that are address recognized but were not copied to memory due to a receive overrun.

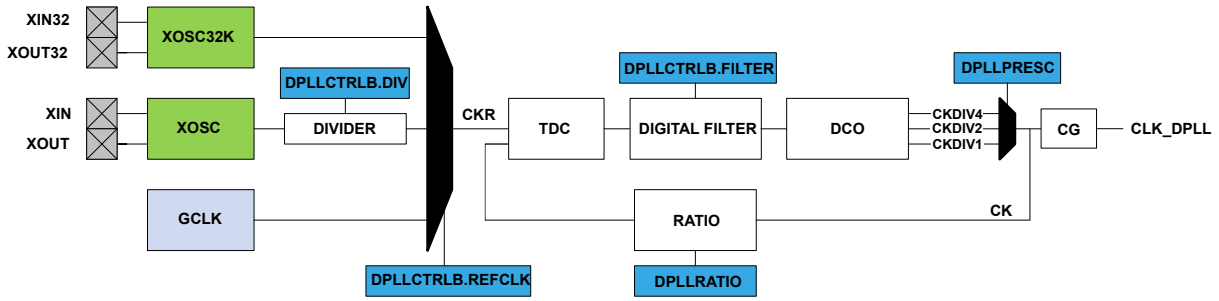
- XOSC0 and XOSC1: this clock is provided by the External Multipurpose Crystal Oscillator (XOSC).
- GCLK: this clock is provided by the Generic Clock Controller.

When the controller is enabled, the relationship between the reference clock frequency and the output clock frequency is:

$$f_{CLK\_DPLLn} = f_{CKR} \times \left(LDR + 1 + \frac{LDRFRAC}{32}\right)$$

Where f_{CLK_DPLLn} is the frequency of the DPLL output clock, LDR is the loop divider ratio integer part, LDRFRAC is the loop divider ratio fractional part, f_{CKR} is the frequency of the selected reference clock, and PRESC is the output prescaler value.

Figure 28-2. DPLL Block Diagram



When the controller is disabled, the output clock is low. If the Loop Divider Ratio Fractional part bit field in the DPLL Ratio register (DPLLRATIO.LDRFRAC) is zero, the DPLL works in Integer mode. Otherwise, the fractional mode is activated. Note that the fractional part has a negative impact on the jitter of the DPLL.

Example (integer mode only): assuming f_{CKR} = 32 kHz and f_{CLK_DPLLn} = 112 MHz, the multiplication ratio is 3500. It means that LDR shall be set to 3499.

Example (fractional mode): assuming f_{CKR} = 32 kHz and f_{CLK_DPPLn} = 112.003000 MHz, the multiplication ratio is 3500.9375 (3500 + 3/32). Thus LDR is set to 3499 and LDRFRAC to 3.

Related Links

14. GCLK - Generic Clock Controller
29. OSC32KCTRL – 32KHz Oscillators Controller

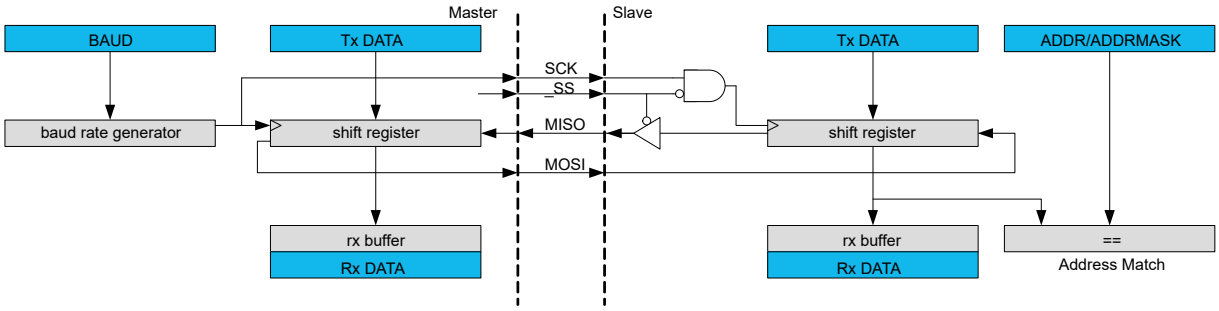
28.6.5.1 Basic Operation

Initialization, Enabling, Disabling, and Resetting

The DPLLCn is enabled by writing a one to the Enable bit in the Control register (DPLLnCTRLA.ENABLE). The DPLLCn is disabled by writing a zero to DPLLnCTRLA.ENABLE. The DPLLnSYNCBUSY.ENABLE is set when the DPLLnCTRLA.ENABLE bit is modified. It is cleared when the DPLLCn output clock CLK_DPLLn has sampled the bit at the high level, or cleared when the output clock is no longer running (for disable operation).

35.3 Block Diagram

Figure 35-1. Full-Duplex SPI Master Slave Interconnection



35.4 Signal Description

Table 35-1. SERCOM SPI Signals

Signal Name	Type	Description
PAD[3:0]	Digital I/O	General SERCOM pins

One signal can be mapped to one of several pins.

Related Links

6. I/O Multiplexing and Considerations

35.5 Product Dependencies

In order to use this peripheral, other parts of the system must be configured correctly, as described below.

35.5.1 I/O Lines

In order to use the SERCOM's I/O lines, the I/O pins must be configured using the IO Pin Controller (PORT).

When the SERCOM is configured for SPI operation, the SERCOM controls the direction and value of the I/O pins according to the table below. Both PORT control bits PINCFGn.PULLEN and PINCFGn.DRVSTR are still effective. If the receiver is disabled, the data input pin can be used for other purposes. In master mode, the slave select line ($\overline{SS}$) is hardware controlled when the Master Slave Select Enable bit in the Control B register (CTRLB.MSSEN) is '1'.

Table 35-2. SPI Pin Configuration

Pin	Master SPI	Slave SPI
MOSI	Output	Input
MISO	Input	Output
SCK	Output	Input
$\overline{SS}$	Output (CTRLB.MSSEN=1)	Input

35.8.4 Baud Rate

Name: BAUD
Offset: 0x0C
Reset: 0x00
Property: PAC Write-Protection, Enable-Protected

Bit	7	6	5	4	3	2	1	0
	BAUD[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 7:0 – BAUD[7:0] Baud Register
These bits control the clock generation, as described in the *SERCOM Clock Generation – Baud-Rate Generator*.

Related Links

33.6.2.3 Clock Generation – Baud-Rate Generator

33.6.2.3.1 Asynchronous Arithmetic Mode BAUD Value Selection

When a debug message is stored, neither the respective New Data flag nor IR.DRX are set. The reception of debug messages can be monitored via RXF1S.DMS.

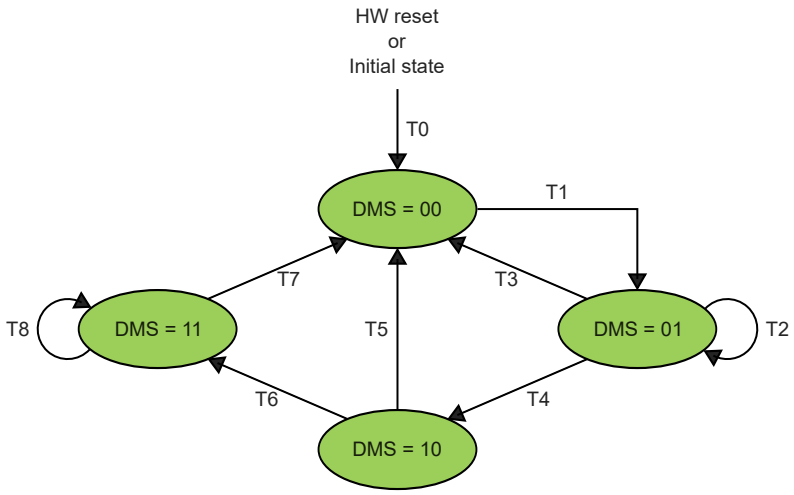
Table 39-5. Example Filter Configuration for Debug Messages

Filter Element	SFID1[10:0] / EFID1[28:0]	SFID2[10:9] / EFID2[10:9]	SFID2[5:0] / EFID2[5:0]
0	ID debug message A	01	11 1101
1	ID debug message B	10	11 1110
2	ID debug message C	11	11 1111

Debug Message Handling

The debug message handling state machine assures that debug messages are stored to three consecutive Rx Buffers in correct order. In case of missing messages the process is restarted. The DMA request is activated only when all three debug messages A, B, C have been received in correct order.

Figure 39-9. Debug Message Handling State Machine



T0: Reset DMA request output, enable reception of debug message A, B, and C
T1: Reception of debug message A
T2: Reception of debug message A
T3: Reception of debug message C
T4: Reception of debug message B
T5: Reception of debug message A, B
T6: Reception of debug message C
T7: DMA transfer completed
T8: Reception of debug message A, B, C (message rejected)

39.6.6 Tx Handling

The Tx Handler handles transmission requests for the dedicated Tx Buffers, the Tx FIFO, and the Tx Queue. It controls the transfer of transmit messages to the CAN Core, the Put and Get Indices, and the Tx Event FIFO. Up to 32 Tx Buffers can be set up for message transmission. The CAN mode for transmission (Classic CAN or CAN FD) can be configured separately for each Tx Buffer element. The Tx Buffer element is described in 39.9.3 Tx Buffer Element. The table below describes the possible configurations for frame transmission.

Bit 2 – ASM Restricted Operation Mode
This bit field is write-restricted.

Writing a 0 to this field is always allowed.

Writing a 1 to this field is only allowed if bit fields CCE = 1 and INIT = 1.

Value	Description
0	Normal CAN operation.
1	Restricted Operation Mode active.

Bit 1 – CCE Configuration Change Enable
This bit field is write-restricted and only writable if bit field INIT = 1.

Value	Description
0	The CPU has no write access to the protected configuration registers.
1	The CPU has write access to the protected configuration registers (while CCCR.INIT = 1).

Bit 0 – INIT Initialization
Due to the synchronization mechanism between the two clock domains, there may be a delay until the value written to INIT can be read back. The programmer has to assure that the previous value written to INIT has been accepted by reading INIT before setting INIT to a new value.

Value	Description
0	Normal Operation.
1	Initialization is started.

Type of response	Meaning of response	Response field	Response register
R5, R5b	SDIO response	R[39:8]	RR0[31:0]
R6 (Published RCA response)	New published RCA[31:16] and Card status bits	R[39:8]	RR0[31:0]

Table 43-31. Square Service Options

Option	Purpose	Required Parameters
SET_MULTIPLIEROPTION(PUKCL_SQUARE_ONLY)	Perform R = X^2 + CarryOperand	nu1RBase, nu1ZBase, nu1XBase, u2XLength
SET_MULTIPLIEROPTION(PUKCL_SQUARE_ADD)	Perform R = Z + X^2 + CarryOperand	nu1RBase, nu1ZBase, nu1XBase, u2XLength
SET_MULTIPLIEROPTION(PUKCL_SQUARE_SUB)	Perform R = Z - (X^2 + CarryOperand)	nu1RBase, nu1ZBase, nu1Xlength, u2XLength

43.3.4.10.6 Code Example

```
PUKCL_PARAM PUKCLParam;
PPUKCL_PARAM pvPUKCLParam = &PUKCLParam;


// Gf2n and CarryIn shall be beforehand filled (with zero or one)
PUKCL(Specific).Gf2n = ...;
PUKCL(Specific).CarryIn = ...;

PUKCL(u2Option) =...;
// Depending on the option specified, not all fields should be filled
PUKCL_Fmult(nu1XBase) = <Base of the ram location of X>;
PUKCL_Fmult(u2XLength) = <Length of X>;
PUKCL_Fmult(nu1ZBase) = <Base of the ram location of Z>;

// vPUKCL_Process() is a macro command, which populates the service name
// and then calls the library...
vPUKCL_Process(Square,pvPUKCLParam);
if (PUKCL(u2Status) == PUKCL_OK)
            {
            // The Squaring has been executed correctly
            ...
            }
else // Manage the error
```

43.3.4.10.7 Important Considerations for Modular Reduction of a Square Computation

Note:
Additional options are available through the use of a modular reduction to be executed at the end of this operation. Some important considerations have to be taken into account concerning the length of resulting operands to get a mathematically correct result.

The output of this operation is not obviously compatible with the modular reduction as it may be either smaller or bigger. In the case (most of the time) the result (pointed by nu1RBase) is smaller in size than “twice the modulus plus one word” by one word, a padding word must be added to zero. Otherwise, the reduced value will be taken considering the high order words (potentially uninitialized) as part of the number, thus resulting in getting a mathematically correct but unexpected result.

In the case that the result is greater than twice the modulus plus one word, the modular reduction feature has to be executed as a separate operation, using an Euclidean division.

43.3.4.10.8 Constraints

When the options only indicate a square, the constraints involving nu1ZBase are not checked. The following conditions must be avoided to ensure that the service works correctly:

- nu1XBase, nu1RBase or nu1ZBase are not aligned on 32-bit boundaries

Parameter	Type	Direction	Location	Data Length	Before Executing the Service	After Executing the Service
nu1ABBase	nu1	I	Crypto RAM	u2ModLength + 4	Parameter a of the elliptic curve	Unchanged
nu1Workspace	nu1	I	Crypto RAM	7*u2ModLength + 40	–	Corrupted workspace

43.3.7.2.5 Code Example

```
PUKCL_PARAM PUKCLParam;
PPUKCL_PARAM pvPUKCLParam = &PUKCLParam;
//Depending on the function the Random Number Generator
//must be initialized and started
//following the directives given for the RNG on the chip
PUKCL(u2Option) = 0;
PUKCL_GF2NEccAdd(nu1ModBase) = <Base of the ram location of P>;
PUKCL_GF2NEccAdd(nu1CnsBase) = <Base of the ram location of Cns>;
PUKCL_GF2NEccAdd(u2ModLength) = <Byte length of P>;
PUKCL_GF2NEccAdd(nu1PointABase) = <Base of the ram location of the A point>;
PUKCL_GF2NEccAdd(nu1PointBBase) = <Base of the ram location of the B point>;
PUKCL_GF2NEccAdd(nu1ABBase) = <Base of the ram location of the a Parameter>;
PUKCL_GF2NEccAdd(nu1Workspace) = <Base of the ram location of the workspace>;
. . .
// vPUKCL_Process() is a macro command, which populates the service name
// and then calls the library...
vPUKCL_Process(GF2NEccAddFast, pvPUKCLParam);
if (PUKCL(u2Status) == PUKCL_OK)
                {
                ...
                }
else // Manage the error
```

43.3.7.2.6 Constraints

No overlapping between either input and output are allowed The following conditions must be avoided to ensure the service works correctly:

- nu1ModBase,nu1CnsBase, nu1PointABase, nu1PointBBase, nu1ABBase, nu1Workspace are not aligned on 32-bit boundaries
- {nu1ModBase, u2ModLength + 4}, {nu1CnsBase, u2ModLength + 8}, {nu1PointABase, 3*u2ModLength+ 12}, {nu1PointBBase, 3*u2ModLength + 12}, {nu1ABase,u2ModLength + 4}, {nu1Workspace, <WorkspaceLength>} are not in Crypto RAM
- u2ModLength is either: < 12, > 0xffc or not a 32-bit length
- All overlapping between {nu1ModBase, u2ModLength + 4}, {nu1CnsBase, u2ModLength +8}, {nu1PointABase, 3*u2ModLength + 12}, {nu1PointBBase, 3*u2ModLength + 12}, {nu1ABase,u2ModLength + 4} and {nu1Workspace, 5*u2ModLength + 32}

43.3.7.2.7 Status Returned Values

Table 43-95. GF2NEccAddFast Service Return Codes

Returned Status	Importance	Meaning
PUKCL_OK	–	The computation passed without errors.

43.3.7.3 Point Doubling

43.3.7.3.1 Purpose

This service is used to perform a Point Doubling, based on a given elliptic curve over GF(2^n).

48.7.3.11 Debug Control

Name: DBGCTRL
Offset: 0x0F
Reset: 0x00
Property: PAC Write-Protection

Bit	7	6	5	4	3	2	1	0
								DBGRUN
Access								R/W
Reset								0

Bit 0 – DBGRUN Run in Debug Mode
This bit is not affected by a software Reset, and should not be changed by software while the TC is enabled.

Value	Description
0	The TC is halted when the device is halted in debug mode.
1	The TC continues normal operation when the device is halted in debug mode.

Symbol	Parameters	Conditions	Min.	Typ.	Max.	Unit
V_{OUTmin}	Min Output Voltage	-	-	-	0.15	V
V_{OUTmax}	Max Output Voltage	-	V_{DDANA}-0.15	-	-	
V_{REF}	External Reference input	CTRLB.REFSEL[1:0]=0x2 (VREFAB)	1	-	V_{DDANA}-0.15	V
		CTRLB.REFSEL[1:0]=0x0 (VREFAU)	1	-	V_{DDANA}	
C_{VREF}	External decoupling capacitor	-	-	220	-	nF
C_{LOAD}	Output capacitor load	-	-	-	50	pF
R_{LOAD}	Output resistance load	-	5	-	-	kΩ
t_S	Settling time	For reaching ±1LSB of the final value. Step size < 500 LSB - C_{load} = 50pF	-	-	1	µs
t_{S_FS}	Settling time 0x080 to 0xF7F	For reaching ±1LSB of the final value. Step size from 0% to 100% - C_{load} = 50pF	-	5	7	µs

Note:

1. These values are based on simulation. They are not covered by production test limits or characterization.

Table 54-29. Differential Mode

Symbol	Parameters	Conditions	Min.	Typ.	Max.	Unit
INL	Integral Non Linearity, Best-fit curve from 0x080 to 0xF7F	i12clk = 12 MHz, V_{DDANA} = 3.0V, External Ref. = 2.0V, C_{LOAD} = 50 pF	-	±2.4	±3.4	LSB
		i12clk = 12 MHz, V_{DDANA} = 3.0V - 1V Internal Ref (1) = 2.0V, C_{LOAD} = 50 pF	-	±3.2	±4.2	
DNL	Differential Non Linearity, Best-fit curve from 0x080 to 0xF7F	i12clk = 12 MHz, V_{DDANA} = 3.0V,External Ref. = 2.0V, C_{LOAD} = 50 pF	-	±2.4	±3.6	LSB
		i12clk = 12 MHz, V_{DDANA} = 3.0V - 1V Internal Ref (1) = 2.0V, C_{LOAD} = 50 pF	-	±3.5	±4.4	
Gerr	Gain Error	External Reference voltage	-	±0.4	±1.7	% FSR
		1.0V Internal Reference voltage	-	±0.8	±8.0	
Offerr	Offset Error	External Reference voltage	-	±13	±40	mV
		1.0V Internal Reference voltage	-	±8	±74	
ENOB	Effective Number Of Bits	Fs = 1 Ms/s - External Ref - CCTRL = 0x2	9.9	10.7	10.9	Bits
SNR	Signal to Noise ratio		63.5	68.6	72.6	dB
THD	Total Harmonic Distortion		-79.1	-72.5	-61.0	dB

Note: Specified only at Temp > 0°C when 1V internal reference is used.