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### What is "[Embedded - Microcontrollers](#)"?

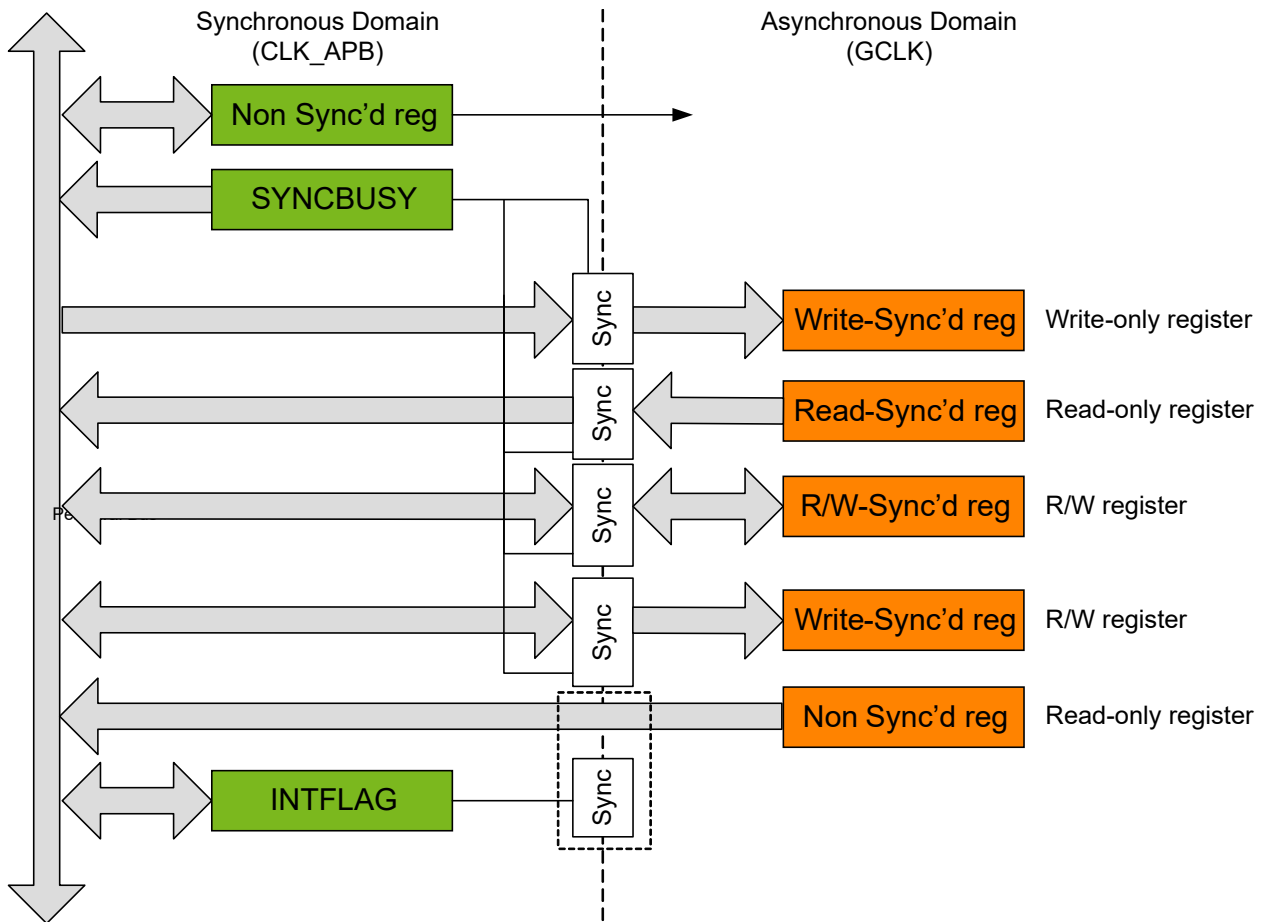
"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Active
Core Processor	ARM® Cortex®-M4F
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	EBI/EMI, I <sup>2</sup> C, IrDA, LINbus, MMC/SD, QSPI, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I <sup>2</sup> S, POR, PWM
Number of I/O	51
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.63V
Data Converters	A/D 24x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad
Supplier Device Package	64-QFN (9x9)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/microchip-technology/atsamd51j18a-mut">https://www.e-xfl.com/product-detail/microchip-technology/atsamd51j18a-mut</a>

**Figure 13-3. Register Synchronization Overview**



### 13.3.2 General Write Synchronization

Write-Synchronization is triggered by writing to a register in the peripheral clock domain (GCLK). The respective bit in the Synchronization Busy register (SYNCBUSY) will be set when the write-synchronization starts and cleared when the write-synchronization is complete. Refer also to [13.3.7 Synchronization Delay](#).

When write-synchronization is ongoing for a register, any subsequent write attempts to this register will be discarded, and an error will be reported through the Peripheral Access Controller (PAC).

#### Example:

REGA, REGB are 8-bit core registers. REGC is a 16-bit core register.

Offset	Register
0x00	REGA
0x01	REGB
0x02	REGC
0x03	

Synchronization is per register, so multiple registers can be synchronized in parallel. Consequently, after REGA (8-bit access) was written, REGB (8-bit access) can be written immediately without error.

# SAMD5x/E5x Family Data Sheet

## RTC – Real-Time Counter

### 21.12.10 Clock Value in Clock/Calendar mode (CTRLA.MODE=2)

**Name:** CLOCK  
**Offset:** 0x18  
**Reset:** 0x00000000  
**Property:** PAC Write-Protection, Write-Synchronized, Read-Synchronized

Bit	31	30	29	28	27	26	25	24
	YEAR[5:0]					MONTH[3:2]		
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
Bit	23	22	21	20	19	18	17	16
	MONTH[1:0]		DAY[4:0]				HOUR[4:4]	
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
	HOUR[3:0]				MINUTE[5:2]			
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
	MINUTE[1:0]		SECOND[5:0]					
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

#### Bits 31:26 – YEAR[5:0] Year

The year offset with respect to the reference year (defined in software).

The year is considered a leap year if YEAR[1:0] is zero.

#### Bits 25:22 – MONTH[3:0] Month

1 – January

2 – February

...

12 – December

#### Bits 21:17 – DAY[4:0] Day

Day starts at 1 and ends at 28, 29, 30, or 31, depending on the month and year.

#### Bits 16:12 – HOUR[4:0] Hour

When CTRLA.CLKREP=0, the Hour bit group is in 24-hour format, with values 0-23. When CTRLA.CLKREP=1, HOUR[3:0] has values 1-12, and HOUR[4] represents AM (0) or PM (1).

#### Bits 11:6 – MINUTE[5:0] Minute

0 – 59

# SAMD5x/E5x Family Data Sheet

## DMAC – Direct Memory Access Controller

### 22.8.16 Channel Control A

**Name:** CHCTRLA  
**Offset:** 0x40 + n\*0x10 [n=0..31]  
**Reset:** 0x00000000  
**Property:** PAC Write-Protection, Enable-Protected

This register affects the DMA channel that is selected in the Channel ID register (CHID.ID).

Bit	31	30	29	28	27	26	25	24
			THRESHOLD[1:0]		BURSTLEN[3:0]			
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			0	0	0	0	0	0
Bit	23	22	21	20	19	18	17	16
			TRIGACT[1:0]					
Access			R/W	R/W				
Reset			0	0				
Bit	15	14	13	12	11	10	9	8
	TRIGSRC[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
		RUNSTDBY					ENABLE	SWRST
Access		R/W					R/W	R/W
Reset		0					0	0

#### Bits 29:28 – THRESHOLD[1:0] FIFO Threshold

These bits define the threshold from which the DMA starts to write to the destination. These bits have no effect in the case of single beat transfers.

These bits are not enable-protected.

Value	Name	Description
0x0	1BEAT	Destination write starts after each beat source address read
0x1	2BEATS	Destination write starts after 2-beats source address read
0x2	4BEATS	Destination write starts after 4-beats source address read
0x3	8BEATS	Destination write starts after 8-beats source address read

#### Bits 27:24 – BURSTLEN[3:0] Burst Length

These bits define the burst mode.

These bits are not enable-protected.

Value	Name	Description
0x0	SINGLE	Single-beat burst
0x1	2BEAT	2-beats burst length
0x2	3BEAT	3-beats burst length
0x3	4BEAT	4-beats burst length
0x4	5BEAT	5-beats burst length

### 23.8.8 Interrupt Flag Status and Clear

**Name:** INTFLAG  
**Offset:** 0x14  
**Reset:** 0x00000000  
**Property:** -

Bit	31	30	29	28	27	26	25	24
Access								
Reset								
Bit	23	22	21	20	19	18	17	16
Access								
Reset								
Bit	15	14	13	12	11	10	9	8
	EXTINT[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
	EXTINT[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

#### Bits 15:0 – EXTINT[15:0] External Interrupt

The flag bit x is cleared by writing a '1' to it.

This flag is set when EXTINTx pin matches the external interrupt sense configuration and will generate an interrupt request if [INTENCLR/SET](#).EXTINT[x] is '1'.

Writing a '0' to this bit has no effect.

Writing a '1' to this bit clears the External Interrupt x flag.

### 24.9.54 GMAC Excessive Collisions Register

**Name:** EC  
**Offset:** 0x140  
**Reset:** 0x00000000  
**Property:** Read-only

Bit	31	30	29	28	27	26	25	24
Access								
Reset								
Bit	23	22	21	20	19	18	17	16
Access								
Reset								
Bit	15	14	13	12	11	10	9	8
							XCOL[9:8]	
Access							R	R
Reset							0	0
Bit	7	6	5	4	3	2	1	0
	XCOL[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

#### Bits 9:0 – XCOL[9:0] Excessive Collisions

This register counts the number of frames that failed to be transmitted because they experienced 16 collisions.

### 24.9.76 GMAC Receive Symbol Errors Register

**Name:** RSE  
**Offset:** 0x198  
**Reset:** 0x00000000  
**Property:** Read-only

Bit	31	30	29	28	27	26	25	24
Access								
Reset								
Bit	23	22	21	20	19	18	17	16
Access								
Reset								
Bit	15	14	13	12	11	10	9	8
							RXSE[9:8]	
Access							R	R
Reset							0	0
Bit	7	6	5	4	3	2	1	0
	RXSE[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

#### Bits 9:0 – RXSE[9:0] Receive Symbol Errors

This bit field counts the number of frames that had GRXER asserted during reception. For 10/100 mode symbol errors are counted regardless of frame length checks. Receive symbol errors will also be counted as an FCS or alignment error if the frame is between 64 and 1518 Bytes (1536 Bytes if NCFGR.MAXFS=1). If the frame is larger it will be recorded as a jabber error.

# SAMD5x/E5x Family Data Sheet

## NVMCTRL – Nonvolatile Memory Controller

### 25.8.10 Page Buffer Load Data x

**Name:** PBLDATAn  
**Offset:** 0x1C + n\*0x04 [n=0..1]  
**Reset:** 0xFFFFFFFF  
**Property:** -

Bit	31	30	29	28	27	26	25	24
	DATA[31:24]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0
Bit	23	22	21	20	19	18	17	16
	DATA[23:16]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
	DATA[15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
	DATA[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	1

**Bits 31:0 – DATA[31:0] Page Buffer Data**



### 27.7.4 Interrupt Enable Set

**Name:** INTENSET  
**Offset:** 0x09  
**Reset:** 0x00  
**Property:** PAC Write-Protection

This register allows the user to enable an interrupt without doing a read-modify-write operation. Changes in this register will also be reflected in the Interrupt Enable Set register (INTENCLR).

Bit	7	6	5	4	3	2	1	0
								ERR
Access								RW
Reset								0

#### Bit 0 – ERR Peripheral Access Error Interrupt Enable

This bit indicates that the Peripheral Access Error Interrupt is enabled and an interrupt request will be generated when one of the interrupt flag registers bits (INTFLAGAHB, INTFLAGn) is set:

Writing a '0' to this bit has no effect.

Writing a '1' to this bit will set the Peripheral Access Error interrupt Enable bit and enables the corresponding interrupt request.

Value	Description
0	Peripheral Access Error interrupt is disabled.
1	Peripheral Access Error interrupt is enabled.

# SAMD5x/E5x Family Data Sheet

## SERCOM SPI – SERCOM Serial Peripheral Interface

### 35.8.8 Status

**Name:** STATUS  
**Offset:** 0x1A  
**Reset:** 0x0000  
**Property:** –

Bit	15	14	13	12	11	10	9	8
					LENERR			
Access					R/W			
Reset					0			

Bit	7	6	5	4	3	2	1	0
						BUFOVF		
Access						R/W		
Reset						0		

#### Bit 11 – LENERR Transaction Length Error

This bit is set in slave mode when the length counter is enabled (LENGTH.LENEN=1) and the transfer length while  $\overline{SS}$  is low is not a multiple of LENGTH.LEN.

Writing '0' to this bit has no effect.

Writing '1' to this bit will clear it.

Value	Description
0	No Length Error has occurred.
1	A Length Error has occurred.

#### Bit 2 – BUFOVF Buffer Overflow

Reading this bit before reading DATA will indicate the error status of the next character to be read.

This bit is cleared by writing '1' to the bit or by disabling the receiver.

This bit is set when a buffer overflow condition is detected. See also [CTRLA.IBON](#) for overflow handling.

When set, the corresponding RxDATA will be zero.

Writing '0' to this bit has no effect.

Writing '1' to this bit will clear it.

Value	Description
0	No Buffer Overflow has occurred.
1	A Buffer Overflow has occurred.

### 36.10.5 Interrupt Enable Clear

**Name:** INTENCLR  
**Offset:** 0x14  
**Reset:** 0x00  
**Property:** PAC Write-Protection

This register allows the user to disable an interrupt without doing a read-modify-write operation. Changes in this register will also be reflected in the Interrupt Enable Set register (INTENSET).

Bit	7	6	5	4	3	2	1	0
	ERROR						SB	MB
Access	R/W						R/W	R/W
Reset	0						0	0

#### Bit 7 – ERROR Error Interrupt Enable

Writing '0' to this bit has no effect.

Writing '1' to this bit will clear the Error Interrupt Enable bit, which disables the Error interrupt.

Value	Description
0	Error interrupt is disabled.
1	Error interrupt is enabled.

#### Bit 1 – SB Slave on Bus Interrupt Enable

Writing '0' to this bit has no effect.

Writing '1' to this bit will clear the Slave on Bus Interrupt Enable bit, which disables the Slave on Bus interrupt.

Value	Description
0	The Slave on Bus interrupt is disabled.
1	The Slave on Bus interrupt is enabled.

#### Bit 0 – MB Master on Bus Interrupt Enable

Writing '0' to this bit has no effect.

Writing '1' to this bit will clear the Master on Bus Interrupt Enable bit, which disables the Master on Bus interrupt.

Value	Description
0	The Master on Bus interrupt is disabled.
1	The Master on Bus interrupt is enabled.

### Bit 6 – UPRSM Upstream Resume from Device Interrupt Disable

Writing a zero to this bit has no effect.

Writing a one to this bit will clear the Upstream Resume interrupt Enable bit and disable the corresponding interrupt request.

Value	Description
0	The Upstream Resume interrupt is disabled.
1	The Upstream Resume interrupt is enabled and an interrupt request will be generated when the Upstream Resume interrupt Flag is set.

### Bit 5 – DNRSM Down Resume Interrupt Disable

Writing a zero to this bit has no effect.

Writing a one to this bit will clear the Down Resume interrupt Enable bit and disable the corresponding interrupt request.

Value	Description
0	The Down Resume interrupt is disabled.
1	The Down Resume interrupt is enabled and an interrupt request will be generated when the Down Resume interrupt Flag is set.

### Bit 4 – WAKEUP Wake Up Interrupt Disable

Writing a zero to this bit has no effect.

Writing a one to this bit will clear the Wake Up interrupt Enable bit and disable the corresponding interrupt request.

Value	Description
0	The Wake Up interrupt is disabled.
1	The Wake Up interrupt is enabled and an interrupt request will be generated when the Wake Up interrupt Flag is set.

### Bit 3 – RST BUS Reset Interrupt Disable

Writing a zero to this bit has no effect.

Writing a one to this bit will clear the Bus Reset interrupt Enable bit and disable the corresponding interrupt request.

Value	Description
0	The Bus Reset interrupt is disabled.
1	The Bus Reset interrupt is enabled and an interrupt request will be generated when the Bus Reset interrupt Flag is set.

### Bit 2 – HSOF Host Start-of-Frame Interrupt Disable

Writing a zero to this bit has no effect.

Writing a one to this bit will clear the Host Start-of-Frame interrupt Enable bit and disable the corresponding interrupt request.

Value	Description
0	The Host Start-of-Frame interrupt is disabled.
1	The Host Start-of-Frame interrupt is enabled and an interrupt request will be generated when the Host Start-of-Frame interrupt Flag is set.

When PFREEZE bit is set while a transaction is in progress on the USB bus, this transaction will be properly completed. PFREEZE bit will be read as “1” only when the ongoing transaction will have been completed.

Value	Description
0	The Pipe operates in normal operation.
1	The Pipe is frozen and no additional requests will be sent to the device on this pipe address.

### Bit 2 – CURBK Current Bank

Value	Description
0	The bank0 is the bank that will be used in the next single/multi USB packet.
1	The bank1 is the bank that will be used in the next single/multi USB packet.

### Bit 0 – DTGL Data Toggle Sequence

Writing a one to the bit EPSTATUSCLR.DTGL will clear this bit.

Writing a one to the bit EPSTATUSSET.DTGL will set this bit.

This bit is toggled automatically by hardware after a data transaction.

This bit will reflect the data toggle in regards of the token type (IN/OUT/SETUP).

Value	Description
0	The PID of the next expected transaction will be zero: data 0.
1	The PID of the next expected transaction will be one: data 1.

# SAMD5x/E5x Family Data Sheet

## CAN - Control Area Network

### 39.8.21 Standard ID Filter Configuration

**Name:** SIDFC  
**Offset:** 0x84  
**Reset:** 0x00000000  
**Property:** Write-restricted

This register is write-restricted and only writable if bit fields CCCR.CCE = 1 and CCCR.INIT = 1.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								
Bit	23	22	21	20	19	18	17	16
	LSS[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
	FLSSA[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
	FLSSA[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

#### Bits 23:16 – LSS[7:0] List Size Standard

Value	Description
0	No standard Message ID filter.
1 – 128	Number of standard Message ID filter elements.
> 128	Values greater than 128 are interpreted as 128.

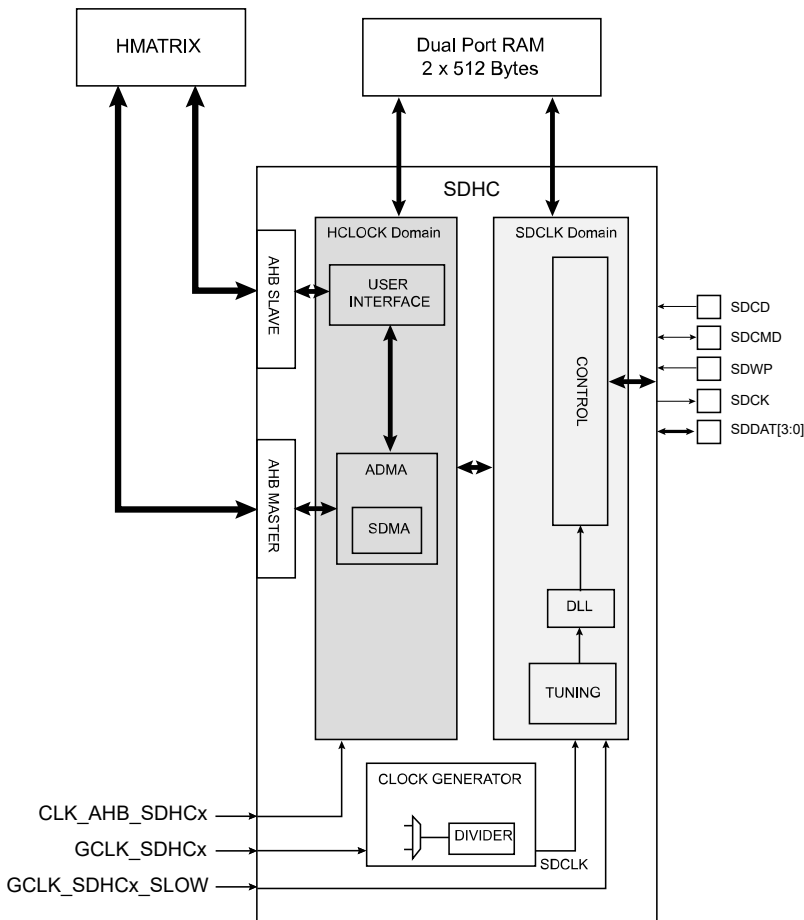
#### Bits 15:0 – FLSSA[15:0] Filter List Standard Start Address

Start address of standard Message ID filter list. When the CAN module addresses the Message RAM it addresses 32-bit words, not single bytes. The configurable start addresses are 32-bit word addresses, i.e. only bits 15 to 2 are evaluated, the two least significant bits are ignored. Bits 1 to 0 will always be read back as “00”.

- Internal 1024-byte Dual Port RAM
- Support for both synchronous and asynchronous abort
- Supports for SDIO Card Interrupt

### 40.3 Block Diagrams

#### 40.3.1 Block Diagram



- Enable bit in control register (CTRLA.ENABLE)
- Enable bit in Comparator Control register (COMPCTRLn.ENABLE)

The following registers are synchronized when written:

- Window Control register (WINCTRL)

Required write-synchronization is denoted by the "Write-Synchronized" property in the register description.

### Related Links

[13.3 Register Synchronization](#)



### 48.7.1.6 Interrupt Enable Set

**Name:** INTENSET  
**Offset:** 0x09  
**Reset:** 0x00  
**Property:** PAC Write-Protection

This register allows the user to enable an interrupt without doing a read-modify-write operation. Changes in this register will also be reflected in the Interrupt Enable Clear register (INTENCLR).

Bit	7	6	5	4	3	2	1	0
			MC1	MC0			ERR	OVF
Access			R/W	R/W			R/W	R/W
Reset			0	0			0	0

#### Bit 5 – MC1 Match or Capture Channel x Interrupt Enable

Writing a '0' to these bits has no effect.

Writing a '1' to MCx will set the corresponding Match or Capture Channel x Interrupt Enable bit, which enables the Match or Capture Channel x interrupt.

Value	Description
0	The Match or Capture Channel x interrupt is disabled.
1	The Match or Capture Channel x interrupt is enabled.

#### Bit 4 – MC0 Match or Capture Channel x Interrupt Enable

Writing a '0' to these bits has no effect.

Writing a '1' to MCx will set the corresponding Match or Capture Channel x Interrupt Enable bit, which enables the Match or Capture Channel x interrupt.

Value	Description
0	The Match or Capture Channel x interrupt is disabled.
1	The Match or Capture Channel x interrupt is enabled.

#### Bit 1 – ERR Error Interrupt Enable

Writing a '0' to this bit has no effect.

Writing a '1' to this bit will set the Error Interrupt Enable bit, which enables the Error interrupt.

Value	Description
0	The Error interrupt is disabled.
1	The Error interrupt is enabled.

#### Bit 0 – OVF Overflow Interrupt Enable

Writing a '0' to this bit has no effect.

Writing a '1' to this bit will set the Overflow Interrupt Enable bit, which enables the Overflow interrupt request.

Value	Description
0	The Overflow interrupt is disabled.
1	The Overflow interrupt is enabled.

<b>Channel Capture (MCx)</b>	For a capture channel, the request is set when valid data is present in the CCx register, and cleared once the CCx register is read. In this operation mode, the CTRLA.DMAOS bit value is ignored.
------------------------------	-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------

### DMA Operation with Circular Buffer

When circular buffer operation is enabled, the buffer registers must be written in a correct order and synchronized to the update times of the timer. The DMA triggers of the TCC provide a way to ensure a safe and correct update of circular buffers.

**Note:** Circular buffer are intended to be used with RAMP2, RAMP2A and DSBOTH operation only.

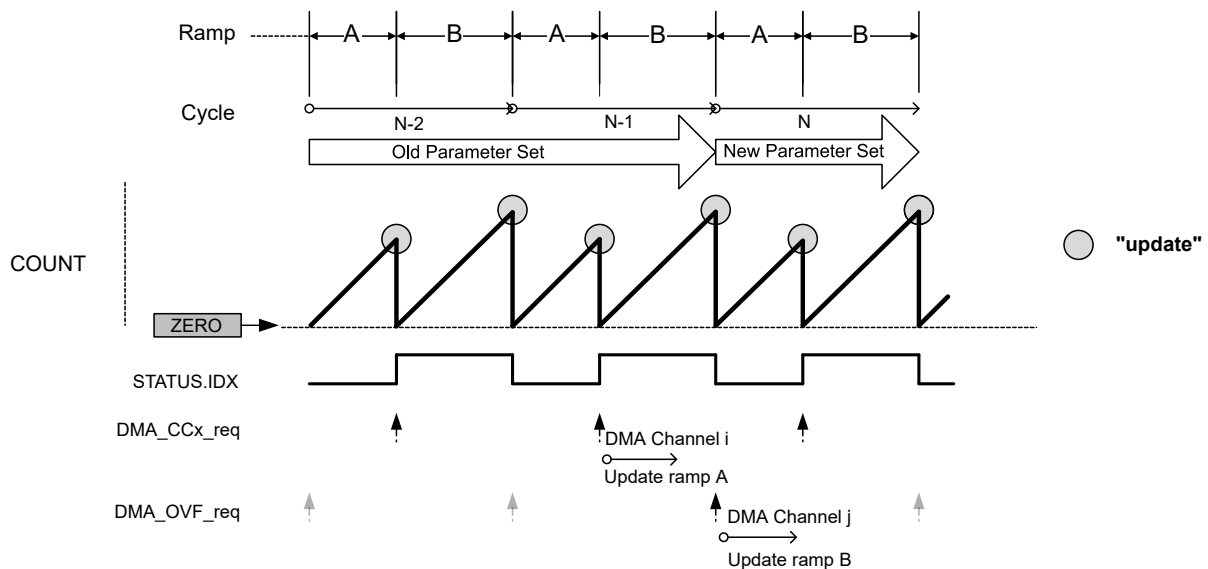
#### DMA Operation with Circular Buffer in RAMP2 and RAMP2A Mode

When a CCx channel is selected as a circular buffer, the related DMA request is not set on a compare match detection, but on start of ramp B.

If at least one circular buffer is enabled, the DMA overflow request is conditioned to the start of ramp A with an effective DMA transfer on previous ramp B (DMA acknowledge).

The update of all circular buffer values for ramp A can be done through a DMA channel triggered on a MC trigger. The update of all circular buffer values for ramp B, can be done through a second DMA channel triggered by the overflow DMA request.

**Figure 49-38. DMA Triggers in RAMP and RAMP2 Operation Mode and Circular Buffer Enabled**



#### DMA Operation with Circular Buffer in DSBOTH Mode

When a CC channel is selected as a circular buffer, the related DMA request is not set on a compare match detection, but on start of down-counting phase.

If at least one circular buffer is enabled, the DMA overflow request is conditioned to the start of up-counting phase with an effective DMA transfer on previous down-counting phase (DMA acknowledge).

When up-counting, all circular buffer values can be updated through a DMA channel triggered by MC trigger. When down-counting, all circular buffer values can be updated through a second DMA channel, triggered by the OVF DMA request.

### 50.3 Block Diagram

Figure 50-1. PTC Block Diagram Mutual-Capacitance

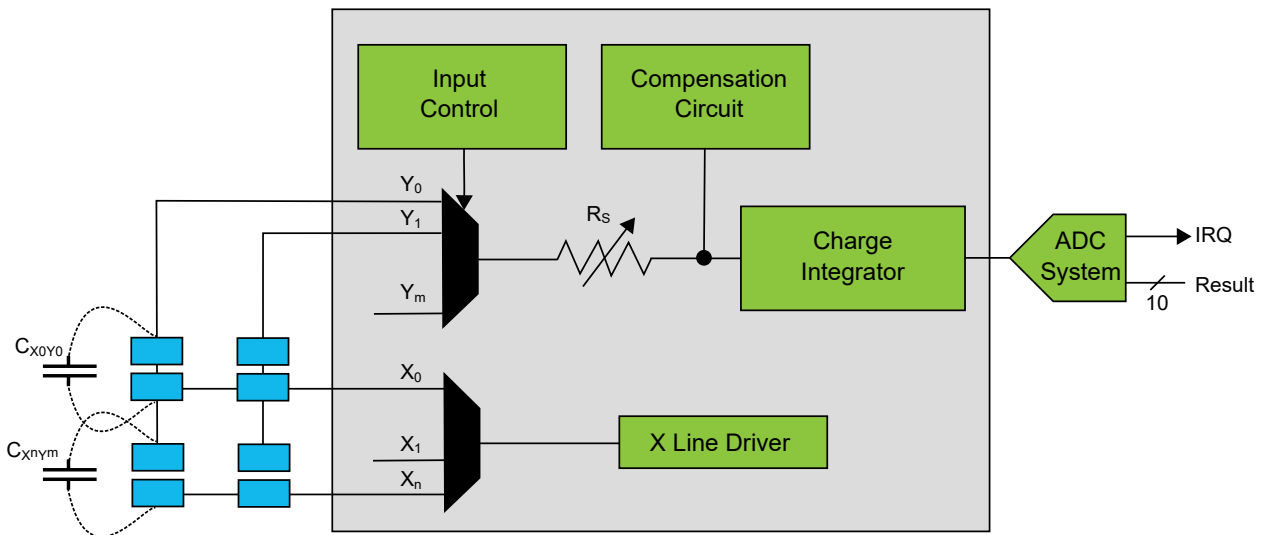
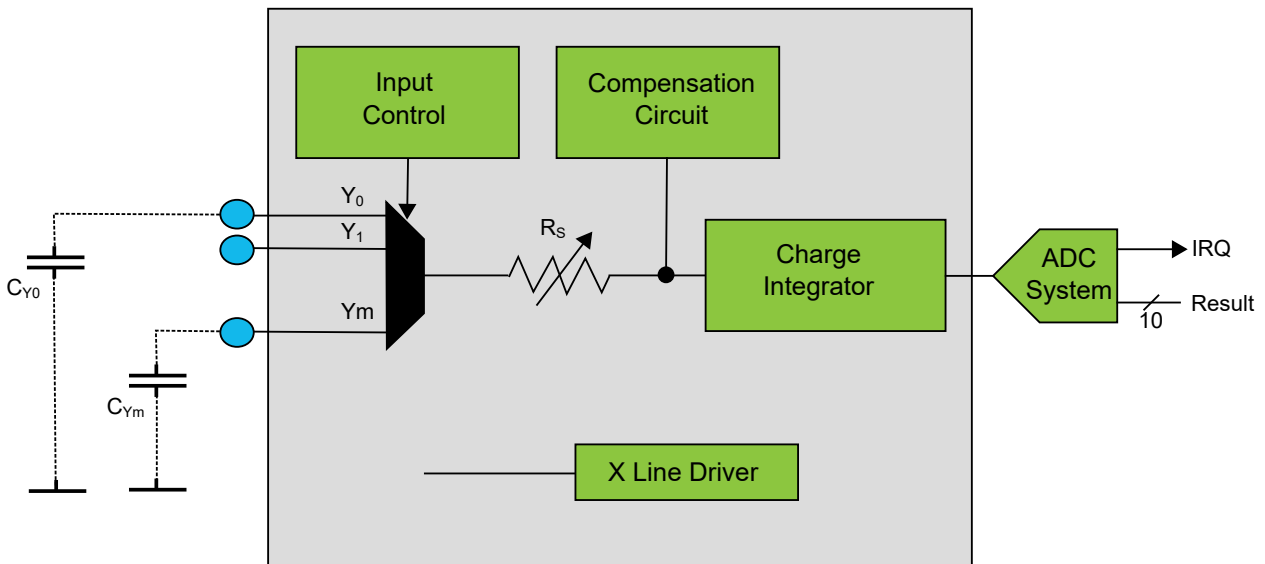


Figure 50-2. PTC Block Diagram Self-Capacitance



### 50.4 Signal Description

Table 50-1. Signal Description for PTC

Name	Type	Description
Y[m:0]	Analog	Y-line (Input/Output)
X[n:0]	Digital	X-line (Output)

**Note:** The number of X- and Y-lines are device dependent. Refer to *Configuration Summary* for details.

- Clock Unit x Enable bits in the Control A register (CTRLA.CKENx). SYNCBUSY.CKENx is set to '1' while synchronization is in progress.
- Serializer Enable bits in the Control A register (CTRLA.TXEN and CTRLA.RXEN). SYNCBUSY.TXEN/RXEN is set to '1' while synchronization is in progress.

The following registers require synchronization when read or written:

- Transmit Data register (TXDATA) is Write-Synchronized. SYNCBUSY.TXDATA is set to '1' while synchronization is in progress.
- Receive Data register (RXDATA) is Read-Synchronized. SYNCBUSY.RXDATA is set to '1' while synchronization is in progress.

Synchronization is denoted by the Read-Synchronized or Write-Synchronized property in the register description.

### 51.6.11 Loop-Back Mode

For debugging purposes, the I<sup>2</sup>S can be configured to loop back the Transmitter to the Receiver. Writing a '1' to the Loop-Back Test Mode bit in the Rx Serializer Control register (RXCTRL.RXLOOP) will connect SDO to SDI, so that transmitted data is also received.

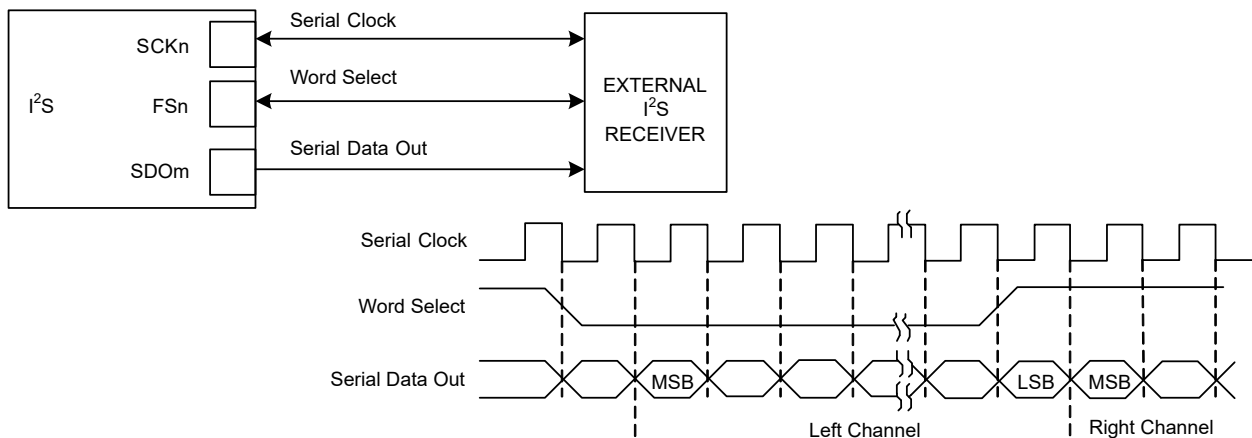
Writing RXCTRL.RXLOOP=0 will restore the normal behavior and connection between Receive Serializer and SDI pin input. As for other changes to the Serializers configuration, the Receive Serializer must be disabled before writing the TXCTRL register to update TXCTRL.RXLOOP.

## 51.7 I<sup>2</sup>S Application Examples

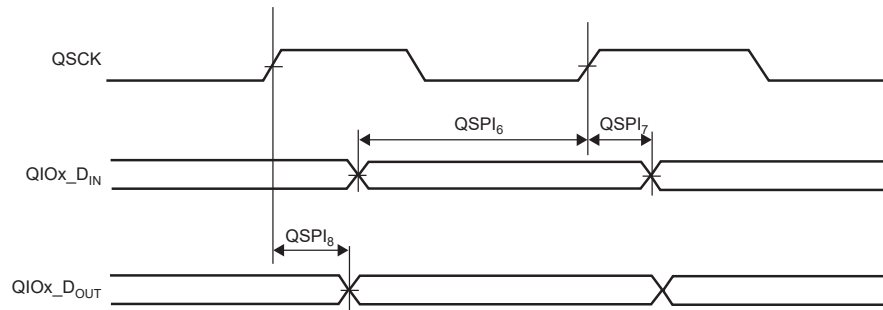
The I<sup>2</sup>S can support several serial communication modes used in audio or high-speed serial links. Some standard applications are shown in the following figures.

**Note:** The following examples are not a complete list of serial link applications supported by the I<sup>2</sup>S.

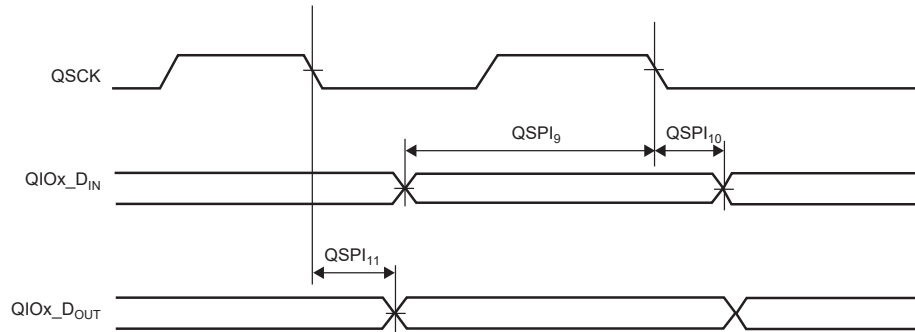
**Figure 51-7. Audio Application Block Diagram**



**Figure 54-13. QSPI SDR Master Mode 2**



**Figure 54-14. QSPI SDR Master Mode 3**



**Figure 54-15. QSPI DDR Mode 0 READ**

