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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4F
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	EBI/EMI, I²C, IrDA, LINbus, MMC/SD, QSPI, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM
Number of I/O	51
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	192K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.63V
Data Converters	A/D 24x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad
Supplier Device Package	64-VQFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atsamd51j19a-mut

14.8.3 Generator Control

Name: GENCTRLn
Offset: 0x20 + n*0x04 [n=0..11]
Reset: 0x00000106
Property: PAC Write-Protection, Write-Synchronized

GENCTRLn controls the settings of Generic Generator n (n=[11:0]). The reset value is 0x00000106 for Generator n=0, else 0x00000000

Bit	31	30	29	28	27	26	25	24
	DIV[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	DIV[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
			RUNSTDBY	DIVSEL	OE	OOV	IDC	GENEN
Access								
Reset			0	0	0	0	0	1

Bit	7	6	5	4	3	2	1	0
				SRC[4:0]				
Access				R/W	R/W	R/W	R/W	R/W
Reset				0	0	0	0	0

Bits 31:16 – DIV[15:0] Division Factor
These bits represent a division value for the corresponding Generator. The actual division factor is dependent on the state of DIVSEL. The number of relevant DIV bits for each Generator can be seen in this table. Written bits outside of the specified range will be ignored.

Table 14-3. Division Factor Bits

Generic Clock Generator	Division Factor Bits	Maximum Division Factor
Generator 0	8 division factor bits - DIV[7:0]	512
Generator 1	16 division factor bits - DIV[15:0]	131072
Generator 2 - 11	8 division factor bits - DIV[7:0]	512

Bit 13 – RUNSTDBY Run in Standby
This bit is used to keep the Generator running in Standby as long as it is configured to output to a dedicated GCLK_IO pin. If GENCTRLn.OE is zero, this bit has no effect and the generator will only be running if a peripheral requires the clock.

19.8.8 Voltage References System (VREF) Control

Name: VREF
Offset: 0x1C
Reset: 0x00000000
Property: PAC Write-Protection

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
					SEL[3:0]			
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
	ONDEMAND	RUNSTDBY			TSSEL	VREFOE	TSEN	
Access	R/W	R/W			R/W	R/W	R/W	
Reset	0	0			0	0	0	

Bits 19:16 – SEL[3:0] Voltage Reference Selection
These bits select the Voltage Reference for the ADC/DAC.

Value	Name	Description
0x0	1V0	1.0V voltage reference typical value
0x1	1V1	1.1V voltage reference typical value
0x2	1V2	1.2V voltage reference typical value
0x3	1V25	1.25V voltage reference typical value
0x4	2V0	2.0V voltage reference typical value
0x5	2V2	2.2V voltage reference typical value
0x6	2V4	2.4V voltage reference typical value
0x7	2V5	2.5V voltage reference typical value
Others		Reserved

Bit 7 – ONDEMAND On Demand Control
The On Demand operation mode allows to enable or disable the voltage reference depending on peripheral requests.

Value	Description
0	The voltage reference is always on, if enabled.
1	The voltage reference is enabled when a peripheral is requesting it. The voltage reference is disabled if no peripheral is requesting it.

20.8.6 Interrupt Flag Status and Clear

Name: INTFLAG
Offset: 0x06
Reset: 0x00
Property: N/A

Bit	7	6	5	4	3	2	1	0
								EW
Access								R/W
Reset								0

Bit 0 – EW Early Warning
This flag is cleared by writing a '1' to it.

This flag is set when an Early Warning interrupt occurs, as defined by the EWOFFSET bit group in EWCTRL.

Writing a '0' to this bit has no effect.

Writing a '1' to this bit clears the Early Warning interrupt flag.

Offset	Name	Bit Pos.								
0xB8	WOL	7:0	IP[7:0]							
		15:8	IP[15:8]							
		23:16					MTI	SA1	ARP	MAG
		31:24								
0xBC	IPGS	7:0	FL[7:0]							
		15:8	FL[15:8]							
		23:16								
		31:24								
0xC0	SVLAN	7:0	VLAN_TYPE[7:0]							
		15:8	VLAN_TYPE[15:8]							
		23:16								
		31:24	ESVLAN							
0xC4	TPFCP	7:0	PEV[7:0]							
		15:8	PQ[7:0]							
		23:16								
		31:24								
0xC8	SAMB1	7:0	ADDR[7:0]							
		15:8	ADDR[15:8]							
		23:16	ADDR[23:16]							
		31:24	ADDR[31:24]							
0xCC	SAMT1	7:0	ADDR[7:0]							
		15:8	ADDR[15:8]							
		23:16								
		31:24								
0xD0 ... 0xDB	Reserved									
0xDC	NSC	7:0	NANOSEC[7:0]							
		15:8	NANOSEC[15:8]							
		23:16			NANOSEC[21:16]					
		31:24								
0xE0	SCL	7:0	SEC[7:0]							
		15:8	SEC[15:8]							
		23:16	SEC[23:16]							
		31:24	SEC[31:24]							
0xE4	SCH	7:0	SEC[7:0]							
		15:8	SEC[15:8]							
		23:16								
		31:24								
0xE8	EFTSH	7:0	RUD[7:0]							
		15:8	RUD[15:8]							
		23:16								
		31:24								
0xEC	EFRSH	7:0	RUD[7:0]							
		15:8	RUD[15:8]							
		23:16								

24.9.10 GMAC Interrupt Status Register

Name: ISR
Offset: 0x024
Reset: 0x00000000
Property: -

This register indicates the source of the interrupt. An interrupt source must be enabled in the mask register first so the corresponding bits of this register will be set and the GMAC interrupt signal will be asserted in the system.

Bit	31	30	29	28	27	26	25	24
				WOL		SRI	PDRSFT	PDRQFT
Access				R		R	R	R
Reset				0		0	0	0

Bit	23	22	21	20	19	18	17	16
	PDRSFR	PDRQFR	SFT	DRQFT	SFR	DRQFR		
Access	R	R	R	R	R	R		
Reset	0	0	0	0	0	0		

Bit	15	14	13	12	11	10	9	8
		PFTR	PTZ	PFNZ	HRESP	ROVR		
Access		R	R	R	R	R		
Reset		0	0	0	0	0		

Bit	7	6	5	4	3	2	1	0
	TCOMP	TFC	RLEX	TUR	TXUBR	RXUBR	RCOMP	MFS
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit 28 – WOL Wake On LAN
WOL interrupt. Indicates a WOL message has been received.

Bit 26 – SRI TSU Seconds Register Increment
Indicates the register has incremented.

Cleared on read.

Bit 25 – PDRSFT PDelay Response Frame Transmitted
Indicates a PTP pdelay_resp frame has been transmitted.

Cleared on read.

Bit 24 – PDRQFT PDelay Request Frame Transmitted
Indicates a PTP pdelay_req frame has been transmitted.

Cleared on read.

Bit 23 – PDRSFR PDelay Response Frame Received
Indicates a PTP pdelay_resp frame has been received.

24.9.61 GMAC Broadcast Frames Received Register

Name: BCFR
Offset: 0x15C
Reset: 0x00000000
Property: Read-only

Bit	31	30	29	28	27	26	25	24
	BFRX[31:24]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	BFRX[23:16]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	BFRX[15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	BFRX[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – BFRX[31:0] Broadcast Frames Received without Error
Broadcast frames received without error. This bit field counts the number of broadcast frames successfully received. This excludes pause frames, and is only incremented if the frame is successfully filtered and copied to memory.

ECCERR.TYPEL and ECCERR.TYPEH are reset to the NONE value when ECCERR is read. If an error occurs while reading ECCERR, the previous error information is sent to the APB and ECCERR is updated with the next error information.

If a single-error has been detected and INTFLAG.ECCSE or INTFLAG.ECCDE is not clear:

- Any incoming single-errors is ignored
- First incoming dual-error overrides ECCERR.ADDR, ECCERR.TYPEL and ECCERR.TYPEH

If a dual-error has been detected and INTFLAG.ECCDE is not clear:

- incoming single-errors are ignored
- incoming dual-errors are ignored

ECCERR.ADDR is always quad-word aligned. If jumping to a word that is not quad-word aligned, e.g. jumping to address 0x100C, INTFLAG.ECCDE and INTFLAG.ECCSE are updated according to the types of detected errors, and ECCERR.ADDR will read 0x1000, irrespective of whether the ECC error was in address 0x1000, 0x1004, 0x1008, or 0x100C.

25.6.13 Reset During Operation

Program or erase operations must not be interrupted. The content of a block or a page is unpredictable in case of reset during either an erase or a write operation. To reduce the risk of having a BOD reset due to a power loss one can monitor the external voltage before issuing any program or erase operation. The user can also prefer the WQW command instead of the WP command as a short command is more likely to complete successfully than a long one with a given external decoupling capacitor. In case of reset during a write or erase operation the impacted block must be erased before being read or programmed as its content is unknown.

25.6.14 Chip Erase

The Chip Erase operation is system-wide, and issued through the DSU.

Chip-Erase procedure:

1. Volatile memories are cleared and NVM array is erased simultaneously (except the BOOTPROT section)
2. Special individual fuses are set as follow:
   – If no BOOTPROT section is defined then NVMCTRL STATUS.AFIRST=1 otherwise it is left unchanged
   – NVMCTRL SEESTAT.ASEES=1
   – NVMCTRL SEESTAT.LOCK=0
   – DSU STATUSB.CELCK=0
3. Security bit is cleared provided no internal error has been detected in the previous steps
   – If all internal NVM verify operations succeeded: goto 4
   – otherwise set DSU.STATUSA.DONE and DSU.STATUSA.FAIL and exit.
4. DSU STATUSB.PROT is cleared, system is no more protected

Note: CB, FS, USER pages (in the auxiliary address space) and the section allocated as a boot loader using BOOTPROT are not affected by the Chip-Erase operation.

25.8.10 Page Buffer Load Data x

Name: PBLDATAn
Offset: 0x1C + n*0x04 [n=0..1]
Reset: 0xFFFFFFFF
Property: -

Bit	31	30	29	28	27	26	25	24
	DATA[31:24]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	DATA[23:16]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	DATA[15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	DATA[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	1

Bits 31:0 – DATA[31:0] Page Buffer Data

35.8.2 Control B

Name: CTRLB
Offset: 0x04
Reset: 0x00000000
Property: PAC Write-Protection, Enable-Protected, Write-Synchronized

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
							RXEN	
Access							R/W	
Reset							0	

Bit	15	14	13	12	11	10	9	8
	AMODE[1:0]		MSSEN				SSDE	
Access	R/W	R/W	R/W				R/W	
Reset	0	0	0				0	

Bit	7	6	5	4	3	2	1	0
		PLOADEN				CHSIZE[2:0]		
Access		R/W				R/W	R/W	R/W
Reset		0				0	0	0

Bit 17 – RXEN Receiver Enable
Writing '0' to this bit will disable the SPI receiver immediately. The receive buffer will be flushed, data from ongoing receptions will be lost and STATUS.BUFOVF will be cleared.

Writing '1' to CTRLB.RXEN when the SPI is disabled will set CTRLB.RXEN immediately. When the SPI is enabled, CTRLB.RXEN will be cleared, SYNCBUSY.CTRLB will be set and remain set until the receiver is enabled. When the receiver is enabled CTRLB.RXEN will read back as '1'.

Writing '1' to CTRLB.RXEN when the SPI is enabled will set SYNCBUSY.CTRLB, which will remain set until the receiver is enabled, and CTRLB.RXEN will read back as '1'.

This bit is not enable-protected.

Value	Description
0	The receiver is disabled or being enabled.
1	The receiver is enabled or it will be enabled when SPI is enabled.

Bits 15:14 – AMODE[1:0] Address Mode
These bits set the slave addressing mode when the frame format (CTRLA.FORM) with address is used. They are unused in master mode.

37.8.13 Scrambling Mode

Name: SCRAMBCTRL
Offset: 0x40
Reset: 0x00000000
Property: PAC Write-Protection

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
							RANDOMDIS	ENABLE
Access							R/W	R/W
Reset							0	0

Bit 1 – RANDOMDIS Scrambling/Unscrambling Random Value Disable

Value	Description
0	The scrambling/unscrambling algorithm includes the scrambling user key plus a random value that may differ from chip to chip.
1	The scrambling/unscrambling algorithm includes only the scrambling user key.

Bit 0 – ENABLE Scrambling/Unscrambling Enable
This bit defines if the scrambling/unscrambling is enabled or disabled.

Value	Description
0	Scrambling/unscrambling is disabled.
1	Scrambling/unscrambling is enabled.

39.8.18 Interrupt Line Select

Name: ILS
Offset: 0x58
Reset: 0x00000000
Property: -

The Interrupt Line Select register assigns an interrupt generated by a specific interrupt flag from IR to one of the two module interrupt lines.

Bit	31	30	29	28	27	26	25	24
			ARAL	PEDL	PEAL	WDIL	BOL	EWL
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	EPL	ELOL	BEUL	BECL	DRXL	TOOL	MRAFL	TSWL
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	TEFLL	TEFFL	TEFWL	TEFNL	TFEL	TCFL	TCL	HPML
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	RF1LL	RF1FL	RF1WL	RF1NL	RF0LL	RF0FL	RF0WL	RF0NL
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 29 – ARAL Access to Reserved Address Interrupt Line

Value	Description
0	Interrupt assigned to CAN interrupt line 0.
1	Interrupt assigned to CAN interrupt line 1.

Bit 28 – PEDL Protocol Error in Data Phase Interrupt Line

Value	Description
0	Interrupt assigned to CAN interrupt line 0.
1	Interrupt assigned to CAN interrupt line 1.

Bit 27 – PEAL Protocol Error in Arbitration Phase Interrupt Line

Value	Description
0	Interrupt assigned to CAN interrupt line 0.
1	Interrupt assigned to CAN interrupt line 1.

Bit 26 – WDIL Watchdog Interrupt Line

40.8.25 Host Control 2 Register: SD/SDIO

Name: HC2R
Offset: 0x3E
Reset: 0x0000
Property: -

Note: The content of the HC2R register is depending on the mode. This description is for SD/SDIO mode. For e.MMC mode, see 40.8.24 HC2R.

Bit	15	14	13	12	11	10	9	8
	PVALEN	ASINTEN						
Access	R/W	R/W						
Reset	0	0						

Bit	7	6	5	4	3	2	1	0
Access								
Reset								

Bit 15 – PVALEN Preset Value Enable
As the operating SDCLK frequency depends on the system implementation, it is difficult to determine these parameters in the standard host driver. When Preset Value Enable (PVALEN) is set to 1, automatic SDCLK frequency generationis performed without considering system-specific conditions. This bit enables the functions defined in PVR.

If this bit is written to 0, the Clock Generator Select bit (CCR.CLKGSEL) and the SDCLK Frequency Select bit (CCR.SDCLKFSEL) in the Clock Control Register (CCR) are selected by the user.

If this bit is set to 1, CCR.SDCLKFSEL and .CLKGSEL and HC2R.DRVSEL are set by the peripheral as specified in the Preset Value Register (PVR).

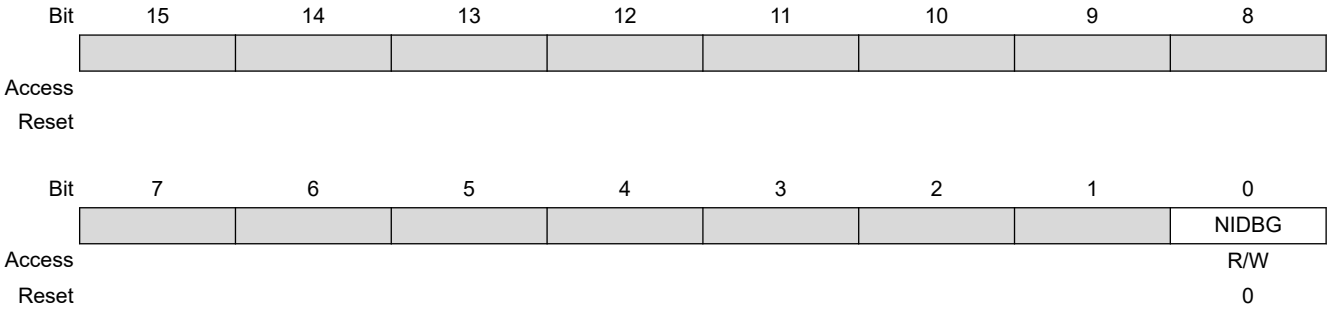
Value	Description
0	CCR.SDCLK, CCR.SDCLKFSEL controlled by the user.
1	Automatic selection by Preset Value is enabled.

Bit 14 – ASINTEN Asynchronous Interrupt Enable
This bit can be set to 1 if a card support asynchronous interrupts and Asynchronous Interrupt Support (ASINTSUP) is set to 1 in CA0R. Asynchronous interrupt is effective when DAT[1] interrupt is used in 4-bit SD mode. If this bit is set to 1, the user can stop the SDCLK during the asynchronous interrupt period to save power. During this period, the peripheral continues to deliver the Card Interrupt to the host when it is asserted by the card.

Value	Description
0	Disabled
1	Enabled

40.8.42 Debug Register

Name: DBGR
Offset: 0x234
Reset: 0x00
Property: -

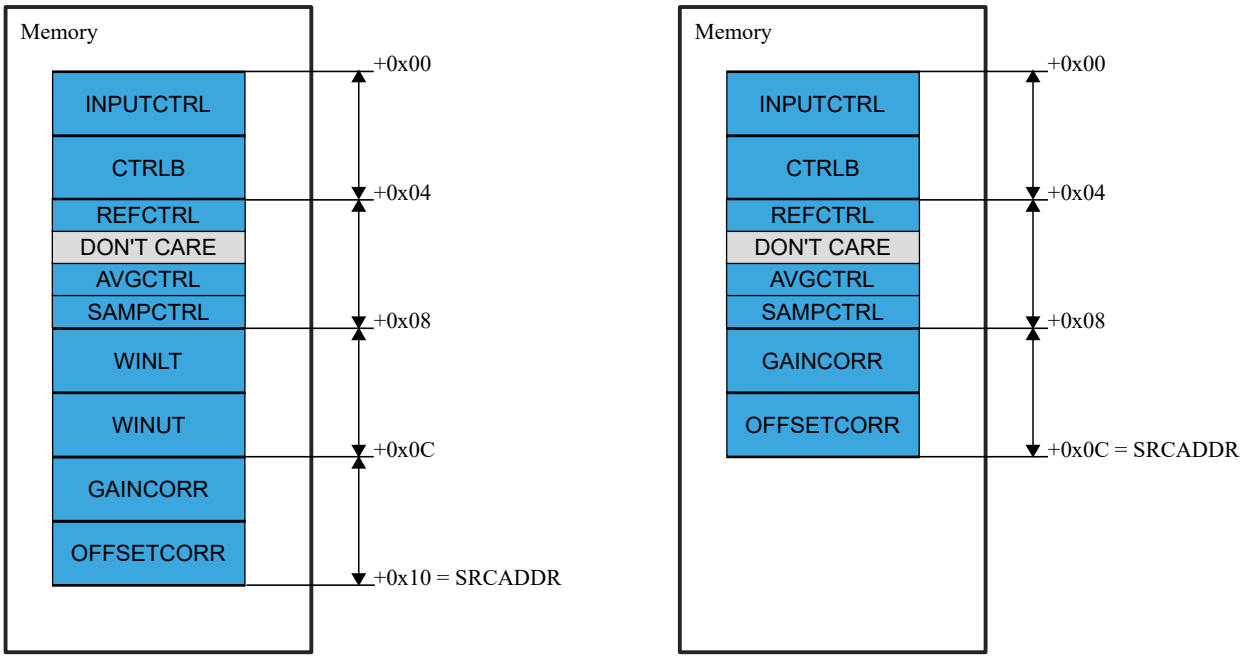


Bit 0 – NIDBG Non-Intrusive Debug

Value	Name	Description
0	DISABLED	Reading the BDPR via debugger increments the dual port RAM read pointer.
1	ENABLED	Reading the BDPR via debugger does not increment the dual port RAM read pointer.

- Enable the source address increment options (DMAC.BTCTRL.SRCINC = 1, DMAC.BTCTRL.STEPSEL = SRC, DMAC.BTCTRL.STEPSIZE = X1).
- Disable the destination address increment (DMAC.BTCTRL.DSTINC=0).
- Set the block transfer count value (DMAC.BTCNT).
- Set the block transfer source address (DMAC.SRCADDR), as described in the DMAC Addressing section. The address corresponds to the memory section from where the DMA reads the data.
- Select the ADC.DSEQDATA address as value for the block transfer destination address (DMAC.DSTADDR = ADC.DSEQDATA address).
- Select the channel single transfer type (DMAC.CHCTRLA.BURSTLEN=SINGLE)
- Select the channel burst trigger action (DMAC.CHCTRLA.TRIGACT=BURST)
- Select the ADC DMA Sequencing trigger as channel trigger source (DMAC.CHCTRLA.TRIGSRC=DSEQ)
- Enable optional channel interrupts (DMAC.CHINTENSET)
- Enable the corresponding DMA channel (DMAC.CHCTRLA.ENABLE)

When an ADC condition is enabled to trigger a DMA transfer, one word (32-bit) will be read by the DMA from the memory source location. Since the source address is incrementing by 0x1, the data memory must be organized in a contiguous memory area. As consequence, if an ADC group of registers does not generate any DMA trigger, no data must be reserved in the memory area for this register group. The next figure shows an example of memory organization when all ADC registers are part of the sequence, and a second example where WINLT and WINUT registers are not part of the sequence.

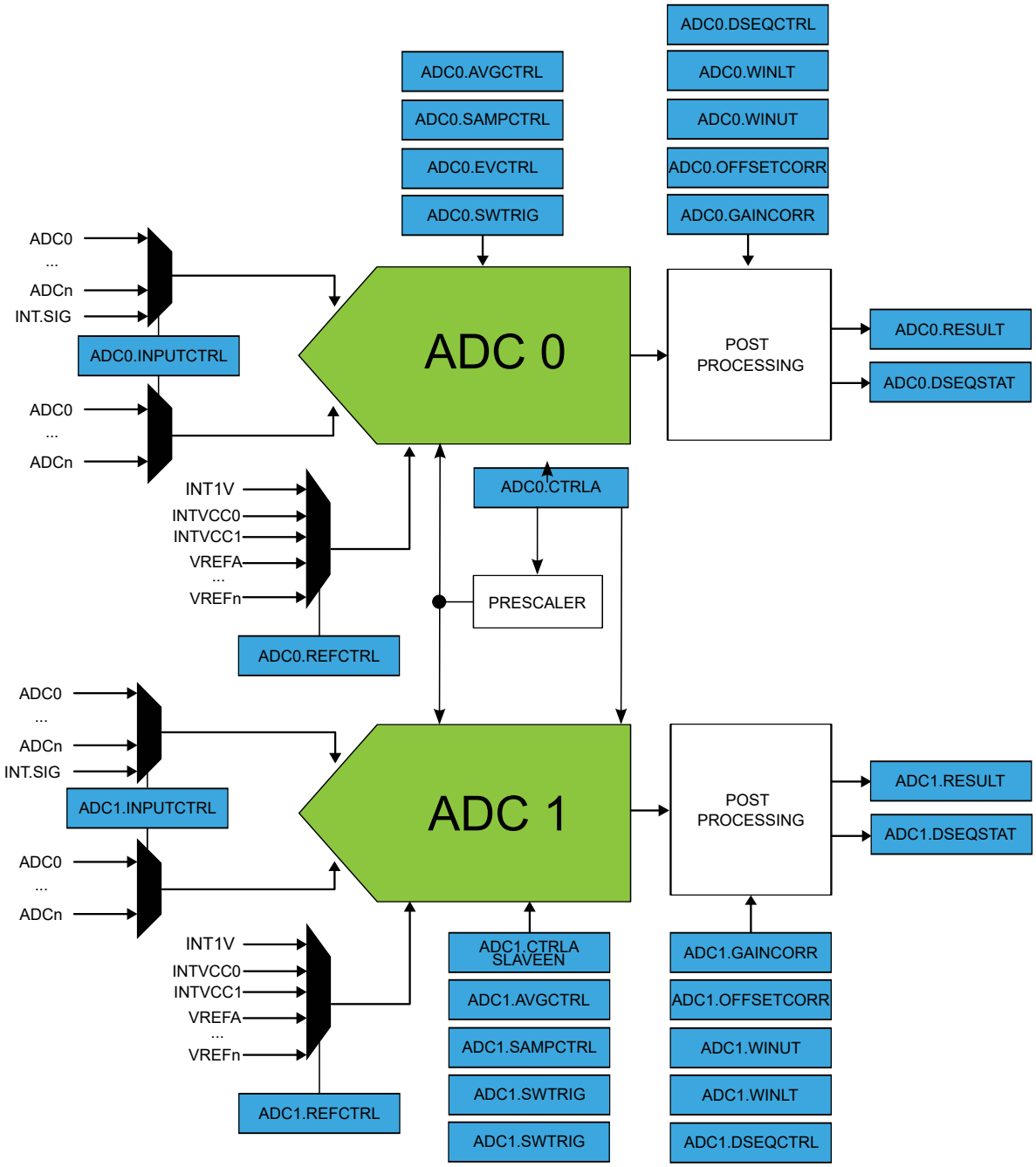


All registers are in the sequence

WINLT / WINUT registers are not in the sequence

Automatic Start Conversion

By default, a new conversion starts when a new start software or event trigger is received. It is also possible to automatically enable an ADC conversion by writing '1' to the AUTOSTART bit in DSEQCTRL register (DSEQCTRL.AUTOSTART). When set, the ADC automatically starts a new conversion when a DMA sequence is complete.



In this mode of operation, the slave ADC1 is enabled by accessing the CTRLA register of the master ADC0. In the same way, the master ADC event inputs will be automatically routed to the slave ADC, meaning that the input events configuration must be done in the master ADC (ADC0.EVCTRL).

ADC measurements can either start simultaneously on both ADCs, or be interleaved. The trigger mode selection is available in the master ADC Control A register (ADC0.CTRLA.DUALSEL).

Note: The interleaved sampling is only usable in single conversion mode (ADC.CTRLB.FREERUN=0).

To restart an interleaved sequence, the user can apply different options:

- Flush the master ADC (ADC0.SWTRIG.FLUSH = 1)
- Disable/re-enable the master ADC (ADC0.CTRLA.ENABLE)

48.7.2.5 Interrupt Enable Clear

Name: INTENCLR
Offset: 0x08
Reset: 0x00
Property: PAC Write-Protection

This register allows the user to disable an interrupt without doing a read-modify-write operation. Changes in this register will also be reflected in the Interrupt Enable Set register (INTENSET).

Bit	7	6	5	4	3	2	1	0
			MC1	MC0			ERR	OVF
Access			R/W	R/W			R/W	R/W
Reset			0	0			0	0

Bit 5 – MC1 Match or Capture Channel x Interrupt Enable
Writing a '0' to these bits has no effect.

Writing a '1' to MCx will clear the corresponding Match or Capture Channel x Interrupt Enable bit, which disables the Match or Capture Channel x interrupt.

Value	Description
0	The Match or Capture Channel x interrupt is disabled.
1	The Match or Capture Channel x interrupt is enabled.

Bit 4 – MC0 Match or Capture Channel x Interrupt Enable
Writing a '0' to these bits has no effect.

Writing a '1' to MCx will clear the corresponding Match or Capture Channel x Interrupt Enable bit, which disables the Match or Capture Channel x interrupt.

Value	Description
0	The Match or Capture Channel x interrupt is disabled.
1	The Match or Capture Channel x interrupt is enabled.

Bit 1 – ERR Error Interrupt Disable
Writing a '0' to this bit has no effect.

Writing a '1' to this bit will clear the Error Interrupt Enable bit, which disables the Error interrupt.

Value	Description
0	The Error interrupt is disabled.
1	The Error interrupt is enabled.

Bit 0 – OVF Overflow Interrupt Disable
Writing a '0' to this bit has no effect.

Writing a '1' to this bit will clear the Overflow Interrupt Enable bit, which disables the Overflow interrupt request.

Value	Description
0	The Overflow interrupt is disabled.
1	The Overflow interrupt is enabled.

49.8 Register Description

Registers can be 8, 16, or 32 bits wide. Atomic 8-, 16-, and 32-bit accesses are supported. In addition, the 8-bit quarters and 16-bit halves of a 32-bit register, and the 8-bit halves of a 16-bit register can be accessed directly.

Some registers require synchronization when read and/or written. Synchronization is denoted by the "Read-Synchronized" and/or "Write-Synchronized" property in each individual register description.

Optional write-protection by the Peripheral Access Controller (PAC) is denoted by the "PAC Write-Protection" property in each individual register description.

Some registers are enable-protected, meaning they can only be written when the module is disabled. Enable-protection is denoted by the "Enable-Protected" property in each individual register description.

Writing a '1' to this bit will disable the one-shot operation.

Value	Description
0	The TCC will update the counter value on overflow/underflow condition and continue operation.
1	The TCC will stop counting on the next underflow/overflow condition.

Bit 1 – LUPD Lock Update
This bit controls the update operation of the TCC buffered registers.

When CTRLB.LUPD is cleared, the hardware UPDATE registers with value from their buffered registers is enabled.

This bit has no effect when input capture operation is enabled.

Writing a '0' to this bit has no effect.

Writing a '1' to this bit will enable the registers updates on hardware UPDATE condition.

Value	Description
0	The CCBx, PERB, PGVB, PGOB, and SWAPBx buffer registers values *are* copied into the corresponding CCx, PER, PGV, PGO and SWAPx registers on hardware update condition.
1	The CCBx, PERB, PGVB, PGOB, and SWAPBx buffer registers values are *not* copied into the corresponding CCx, PER, PGV, PGO and SWAPx registers on hardware update condition.

Bit 0 – DIR Counter Direction
This bit is used to change the direction of the counter.

Writing a '0' to this bit has no effect

Writing a '1' to this bit will clear the bit and make the counter count up.

Value	Description
0	The timer/counter is counting up (incrementing).
1	The timer/counter is counting down (decrementing).

Refer to *I/O Multiplexing and Considerations* for details on the pin mapping for this peripheral. One signal can be mapped on several pins.

Related Links

6. I/O Multiplexing and Considerations

50.5 System Dependencies

In order to use this Peripheral, configure the other components of the system as described in the following sections.

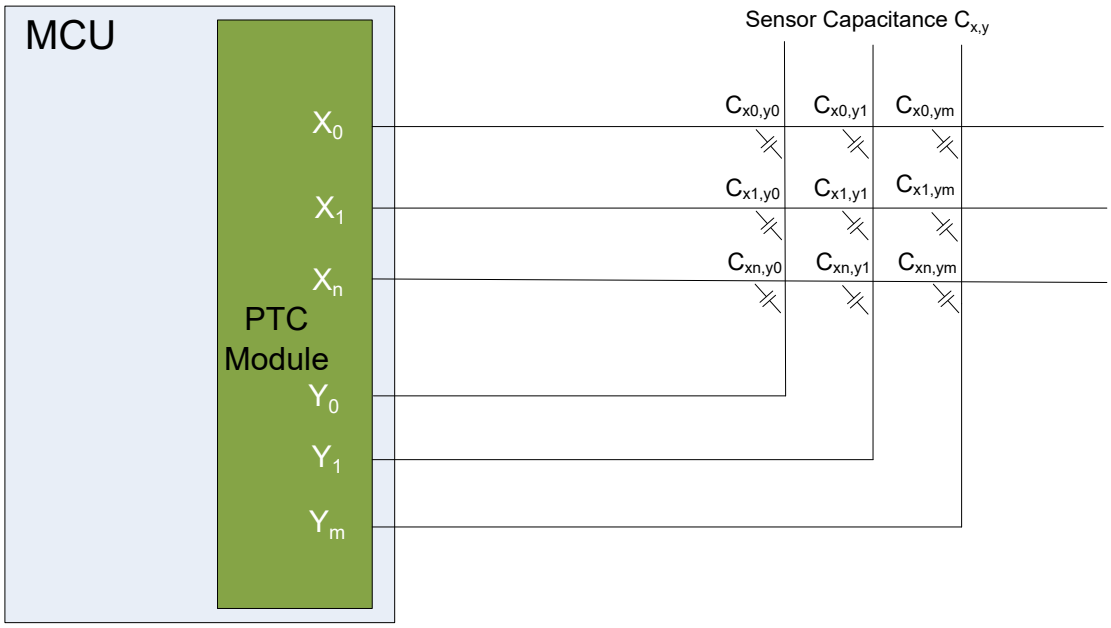
50.5.1 I/O Lines

The I/O lines used for analog X-lines and Y-lines must be connected to external capacitive touch sensor electrodes. External components are not required for normal operation. However, to improve the EMC performance, a series resistor of 1 kΩ or more can be used on X-lines and Y-lines.

50.5.1.1 Mutual-Capacitance Sensor Arrangement

A mutual-capacitance sensor is formed between two I/O lines - an X electrode for transmitting and Y electrode for sensing. The mutual capacitance between the X and Y electrode is measured by the Peripheral Touch Controller.

Figure 50-3. Mutual Capacitance Sensor Arrangement



50.5.1.2 Self-Capacitance Sensor Arrangement

A self-capacitance sensor is connected to a single pin on the Peripheral Touch Controller through the Y electrode for sensing the signal. The sense electrode capacitance is measured by the Peripheral Touch Controller.

limiting resistor is calculated as R = |(GND - 0.6V - V_{PIN}) / Inj2|. If V_{PIN} is greater than V_{DD} + 0.6V, a current limiting resistor is required. The positive DC injection current limiting resistor is calculated as R = (V_{PIN} - (V_{DD} + 0.6)) / Inj2.

54.5 Supply Characteristics

Table 54-4. Supply Characteristics

Symbol	Conditions	Voltage		
		Min.	Max.	Units
V_{DDIO}	Full Voltage Range	1.71	3.63	V
V_{DDIOB}				
V_{DDANA}				
V_{BAT}				

Table 54-5. Supply Rates(1)

Symbol	Conditions	Fall Rate	Rise Rate		Units
		Max.	Min.	Max.	
V_{DDIO}	DC Supply Peripheral I/Os, Internal Regulator, and Analog Supply Voltage	50	0.2	100	mV/µs
V_{DDIOB}					
V_{DDANA}					
V_{BAT}					

Note: 1. These values are based on simulation. They are not covered by production test limits or characterization.

Table 54-6. Power Supply Current Requirement

Symbol	Conditions	Current	Units
		Max	
I_{input}	Power-up Maximum Current	7	mA

Note: I_{input} is the minimum requirement for the power supply connected to the device.