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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | ARM® Cortex®-M4F |
| Core Size | 32-Bit Single-Core |
| Speed | 120MHz |
| Connectivity | EBI/EMI, I²C, IrDA, LINbus, MMC/SD, QSPI, SPI, UART/USART, USB |
| Peripherals | Brown-out Detect/Reset, DMA, I²S, POR, PWM |
| Number of I/O | 81 |
| Program Memory Size | 1MB (1M x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 256K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.71V ~ 3.63V |
| Data Converters | A/D 28x12b; D/A 2x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 100-TQFP |
| Supplier Device Package | 100-TQFP (14x14) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/atsamd51n20a-aut |

### 11.6.7 Tightly Coupled Memory (TCM)

It is possible to use a part of the cache as TCM. The cache size is determined by the Cache Size Configuration by Software bits in the Cache Configuration register (CFG.CSIZESW). The relation between cache and TCM is:

TCM size = maximum Cache size - configured Cache size.

The TCM start address can be obtained from the product memory mapping. The Cache memory starts first from the address followed by the TCM memory. Size of the Way is fixed and the number of ways varies according to the available size for the cache memory. For more information, refer to Product Memory Mapping.

**Table 11-1. TCM Sizes**

| Max. Cache | Configured Cache | TCM Size |
|---|---|---|
| 4 KB | 4 KB | 0 KB |
| 4 KB | 1 KB | 3 KB |
| 4 KB | 2 KB | 2 KB |
| 4 KB | 0 KB | 4 KB |

The TCM is also accessible in its maximum size when the CMCC is disabled. The TCM does not need to be locked in order to operate.

**Note:** Writing into the cache DATA RAM region through the CPU can overwrite valid cache lines. This can result in data corruption when the cache controller is accessing the data for cache transactions. Access the DATA RAM region only after configuring it as TCM.

### 11.6.8 Cache Maintenance

#### 11.6.8.1 Cache Invalidate by Line Operation

When an invalidate by line command is issued, the CMCC resets the valid bit information of the decoded cache line. As the line is no longer valid, the replacement counter points to that line.

- Disable the cache controller by writing a zero to the Cache Controller Enable bit in the Cache Control register (CTRL.CEN).
- Check SR.CSTS to verify that the CMCC is successfully disabled.
- Perform an invalidate by line by writing the set {index,way} in the Cache Maintenance 1 register (MAINT1.INDEX, MAINT1.WAY).
- Enable the CMCC by writing a '1' to CTRL.CEN.

#### 11.6.8.2 Cache Invalidate All Operation

Use the following sequence to invalidate all cache entries.

- Disable the cache controller by writing a zero to the Cache Enable bit in the Cache Control register (CTRL.CEN).
- Check SR.CSTS to verify that the CMCC is successfully disabled.
- Perform a full invalidate operation by writing a '1' to the Cache Controller Invalidate All bit in the Cache Maintenance 0 register (MAINT0.INVALL).
- Enable the CMCC by writing a '1' to CTRL.CEN.

**Figure 12-3. Hot-Plugging Detection Timing Diagram**


The presence of a debugger probe is detected when either Hot-Plugging or Cold-Plugging is detected. Once detected, the Debugger Present bit of the Status B register (STATUSB.DBGPRES) is set. For security reasons, Hot-Plugging is not available when the device is protected by the NVMCTRL security bit.

This detection requires that pads are correctly powered. Thus, at cold startup, this detection cannot be done until POR is released. If the device is protected, Cold-Plugging is the only way to detect a debugger probe, and so the external reset timing must be longer than the POR timing. If external reset is deasserted before POR release, the user must retry the procedure above until it gets connected to the device.

**Related Links**

25. NVMCTRL – Nonvolatile Memory Controller

## 12.7 Chip Erase

Chip-Erase consists of removing all sensitive information stored in the chip and clearing the NVMCTRL security bit. Therefore, all volatile memories and the Flash memory (including the EEPROM emulation area) will be erased. The Flash auxiliary rows, including the user row, will not be erased.

When the device is protected, the debugger must first reset the device in order to be detected. This ensures that internal registers are reset after the protected state is removed. The Chip-Erase operation is triggered by writing a '1' to the Chip-Erase bit in the Control register (CTRL.CE). This command will be discarded if the DSU is protected by the Peripheral Access Controller (PAC). Once issued, the module clears volatile memories prior to erasing the Flash array. To ensure that the Chip-Erase operation is completed, check the Done bit of the Status A register (STATUSA.DONE).

The Chip-Erase operation depends on clocks and power management features that can be altered by the CPU. For that reason, it is recommended to issue a Chip- Erase after a Cold-Plugging procedure to ensure that the device is in a known and safe state.

The recommended sequence is as follows:

1. Issue the Cold-Plugging procedure (refer to 12.6.3.1 Cold Plugging). The device then:
   1.1. Detects the debugger probe.
   1.2. Holds the CPU in reset.
2. Issue the Chip-Erase command by writing a '1' to CTRL.CE. The device then:
   2.1. Clears the system volatile memories.
   2.2. Erases the whole Flash array (including the EEPROM emulation area, not including auxiliary rows).

| Value | Description |
|---|---|
| 0 | In standby sleep mode, the BOD33 is enabled and configured in normal mode. |
| 1 | In standby sleep mode, the BOD33 is enabled and configured in low power mode. |

**Bits 3:2 – ACTION[1:0]** BOD33 Action
These bits are used to select the BOD33 action when the supply voltage crosses below the BOD33 threshold.

These bits are loaded from NVM User Row at start-up.

This field is not synchronized.

| Value | Name | Description |
|---|---|---|
| 0x0 | NONE | No action |
| 0x1 | RESET | The BOD33 generates a reset |
| 0x2 | INT | The BOD33 generates an interrupt |
| 0x3 | BKUP- | The BOD33 puts the device in battery backup sleep mode. |

**Bit 1 – ENABLE** Enable
This bit is loaded from NVM User Row at start-up.

This bit is not enable-protected.

| Value | Description |
|---|---|
| 0 | BOD33 is disabled. |
| 1 | BOD33 is enabled. |

**Related Links**
9.4 NVM User Page Mapping

**Bit 6 – RUNSTDBY** Run In Standby
The bit controls how the voltage reference behaves during standby sleep mode.

| Value | Description |
|---|---|
| 0 | The voltage reference is halted during standby sleep mode. |
| 1 | The voltage reference is not stopped in standby sleep mode. If VREF.ONDEMAND=1, the voltage reference will be running when a peripheral is requesting it. If VREF.ONDEMAND=0, the voltage reference will always be running in standby sleep mode. |

**Bit 3 – TSSEL** Temperature Sensor Channel Selection

| Value | Description |
|---|---|
| 0 | The Temperature Sensor PTAT channel is selected. |
| 1 | The Temperature Sensor CTAT channel is selected. |

**Bit 2 – VREFOE** Voltage Reference Output Enable

| Value | Description |
|---|---|
| 0 | The Voltage Reference output (INTREF) is not available as an ADC input channel. |
| 1 | The Voltage Reference output (INTREF) is routed to an ADC input channel. |

**Bit 1 – TSEN** Temperature Sensor Enable

| Value | Description |
|---|---|
| 0 | Temperature Sensor is disabled. |
| 1 | Temperature Sensor is enabled and routed to an ADC input channel. |

In *Synchronous Edge Detection Mode*, the external interrupt (EXTINT) or the non-maskable interrupt (NMI) pins are sampled using the EIC clock as defined by the Clock Selection bit in the Control A register (CTRLA.CKSEL). The External Interrupt flag (INTFLAG.EXTINT[x]) or Non-Maskable Interrupt flag (NMIFLAG.NMI) is set when the last sampled state of the pin differs from the previously sampled state. In this mode, the EIC clock is required.

The Synchronous Edge Detection Mode can be used in Idle and Standby sleep modes.

In *Asynchronous Edge Detection Mode*, the external interrupt (EXTINT) pins or the non-maskable interrupt (NMI) pins set the External Interrupt flag or Non-Maskable Interrupt flag (INTFLAG.EXTINT[x] or NMIFLAG) directly. In this mode, the EIC clock is not requested.

The asynchronous edge detection mode can be used in Idle and Standby sleep modes.

#### 23.6.4.3 Interrupt Pin Debouncing

The external interrupt pin (EXTINT) edge detection can use a debouncer to improve input noise immunity. When selected, the debouncer can work in the synchronous mode or the asynchronous mode, depending on the configuration of the ASYNCH.ASYNCH[x] bit for the pin. The debouncer uses the EIC clock as defined by the bit CTRLA.CKSEL to clock the debouncing circuitry. The debouncing time frame is set with the debouncer prescaler DPRESCALER.DPRESCALERn, which provides the *low frequency clock* tick that is used to reject higher frequency signals.

The debouncing mode for pin EXTINT x can be selected only if the Sense bits in the Configuration y register (CONFIGy.SENSEx) are set to RISE, FALL or BOTH. If the debouncing mode for pin EXTINT x is selected, the filter mode for that pin (CONFIGy.FILTENx) can not be selected.

The debouncer manages an internal “valid pin state” that depends on the external interrupt (EXTINT) pin transitions, the debouncing mode and the debouncer prescaler frequency. The valid pin state reflects the pin value after debouncing. The external interrupt pin (EXTINT) is sampled continously on EIC clock. The sampled value is evaluated on each *low frequency clock* tick to detect a transitional edge when the sampled value is different of the current valid pin state. The sampled value is evaluated on each EIC clock when DPRESCALER.TICKON=0 or on each *low frequency clock* tick when DPRESCALER.TICKON=1, to detect a bounce when the sampled value is equal to the current valid pin state. Transitional edge detection increments the transition counter of the EXTINT pin, while bounce detection resets the transition counter. The transition counter must exceed the transition count threshold as defined by the DPRESCALER.STATESn bitfield. In the synchronous mode the threshold is 4 when DPRESCALER.STATESn=0 or 8 when DPRESCALER.STATESn=1. In the asynchronous mode the threshold is 4.

The valid pin state for the pins can be accessed by reading the register PINSTATE for both synchronous or asynchronous debouncing mode.

**Synchronous edge detection** In this mode the external interrupt (EXTINT) pin is sampled continously on EIC clock.

1. A pin edge transition will be validated when the sampled value is consistently different of the current valid pin state for 4 (or 8 depending on bit DPRESCALER.STATESn) consecutive ticks of the low frequency clock.
2. Any pin sample, at the *low frequency clock* tick rate, with a value opposite to the current valid pin state will increment the transition counter.
3. Any pin sample, at EIC clock rate (when DPRESCALER.TICKON=0) or the *low frequency clock* tick (when DPRESCALER.TICKON=1), with a value identical to the current valid pin state will return the transition counter to zero.

| Frame Segment | Value |
|---|---|
| UDP (Octet 23) | 11 |
| IP stuff (Octets 24–29) | — |
| IP DA (Octets 30–33) | E000006B |
| Source IP port (Octets 34–35) | — |
| Dest IP port (Octets 36–37) | 013F |
| Other stuff (Octets 38–41) | — |
| Message type (Octet 42) | 02 |
| Version PTP (Octet 43) | 02 |

**Table 24-9. Example of Sync Frame in 1588 Version 2 (UDP/IPv6) Format**

| Frame Segment | Value |
|---|---|
| Preamble/SFD | 55555555555555D5 |
| DA (Octets 0–5) | — |
| SA (Octets 6–11) | — |
| Type (Octets 12–13) | 86dd |
| IP stuff (Octets 14–19) | — |
| UDP (Octet 20) | 11 |
| IP stuff (Octets 21–37) | — |
| IP DA (Octets 38–53) | FF0X00000000018 |
| Source IP port (Octets 54–55) | — |
| Dest IP port (Octets 56–57) | 013F |
| Other stuff (Octets 58–61) | — |
| Message type (Octet 62) | 00 |
| Other stuff (Octets 63–93) | — |
| Version PTP (Octet 94) | 02 |

**Table 24-10. Example of Pdelay_Resp Frame in 1588 Version 2 (UDP/IPv6) Format**

| Frame Segment | Value |
|---|---|
| Preamble/SFD | 55555555555555D5 |
| DA (Octets 0–5) | — |
| SA (Octets 6–11) | — |
| Type (Octets 12–13) | 86dd |
| IP stuff (Octets 14–19) | — |

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| | WZO | CLTTO | OP[1:0] | | PHYA[4:1] | | | |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| | PHYA[0:0] | REGA[4:0] | | | | | WTN[1:0] | |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| | DATA[15:8] | | | | | | | |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | DATA[7:0] | | | | | | | |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Bit 31 – WZO** Write ZERO
Must be written to '0'.

| Value | Description |
|---|---|
| 0 | Mandatory |
| 1 | Reserved |

**Bit 30 – CLTTO** Clause 22 Operation

| Value | Description |
|---|---|
| 0 | Clause 45 operation |
| 1 | Clause 22 operation |

**Bits 29:28 – OP[1:0]** Operation

| Value | Description |
|---|---|
| 01 | Write |
| 10 | Read |
| Other | Reseved |

**Bits 27:23 – PHYA[4:0]** PHY Address

**Bits 22:18 – REGA[4:0]** Register Address
Specifies the register in the PHY to access.

**Bits 17:16 – WTN[1:0]** Write Ten
Must be written to '10'.

| Value | Description |
|---|---|
| 10 | Mandatory |
| Other | Reserved |

### 24.9.61 GMAC Broadcast Frames Received Register

**Name:** BCFR
**Offset:** 0x15C
**Reset:** 0x00000000
**Property:** Read-only

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| | BFRX[31:24] | | | | | | | |
| Access | R | R | R | R | R | R | R | R |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| | BFRX[23:16] | | | | | | | |
| Access | R | R | R | R | R | R | R | R |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| | BFRX[15:8] | | | | | | | |
| Access | R | R | R | R | R | R | R | R |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | BFRX[7:0] | | | | | | | |
| Access | R | R | R | R | R | R | R | R |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Bits 31:0 – BFRX[31:0]** Broadcast Frames Received without Error
Broadcast frames received without error. This bit field counts the number of broadcast frames successfully received. This excludes pause frames, and is only incremented if the frame is successfully filtered and copied to memory.

### 26.8.1 Configuration Register

**Name:** CFG
**Offset:** 0x00
**Reset:** 0x0
**Property:** -

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Access | | | | | | | | |
| Reset | | | | | | | | |

| Bit | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Access | | | | | | | | |
| Reset | | | | | | | | |

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| | UALGO[2:0] | | | UIHASH | | | DUALBUFF | ASCD |
| Access | | | | | | | | R/W |
| Reset | 0 | 0 | 0 | 0 | | | 0 | 0 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | BBC[3:0] | | | | | SLBDIS | EOMDIS | WBDIS |
| Access | R/W | R/W | R/W | R/W | | R/W | R/W | R/W |
| Reset | 0 | 0 | 0 | 0 | | 0 | 0 | 0 |

**Bits 15:13 – UALGO[2:0]** User SHA Algorithm

| Value | Name | Description |
|---|---|---|
| 0 | SHA1 | SHA1 algorithm processed |
| 1 | SHA256 | SHA256 algorithm processed |
| 4 | SHA224 | SHA224 algorithm processed |
| Other | - | Reserved |

**Bit 12 – UIHASH** User Initial Hash Value

| Value | Description |
|---|---|
| 0 | The secure hash standard provides the initial hash value. |
| 1 | The initial hash value is programmable. Field UALGO provides the SHA algorithm. The ALGO field of the RCFGn structure member has no effect. |

**Bit 9 – DUALBUFF** Dual Input Buffer

| Value | Description |
|---|---|
| 0 | Dual Input buffer mode is disabled. |
| 1 | Dual Input buffer mode is enabled (Better performances, higher bandwidth required on system bus). |

### 30.5.1 I/O Lines

The GCLK I/O lines (GCLK_IO[7:0]) can be used as measurement or reference clock sources. This requires the I/O pins to be configured.

### 30.5.2 Power Management

The FREQM will continue to operate in idle sleep mode where the selected source clock is running. The FREQM's interrupts can be used to wake up the device from idle sleep mode. Refer to the Power Manager chapter for details on the different sleep modes.

**Related Links**

18. PM – Power Manager

### 30.5.3 Clocks

The clock for the FREQM bus interface (CLK_APB_FREQM) is enabled and disabled by the Main Clock Controller, the default state of CLK_APB_FREQM can be found in Peripheral Clock Masking.

Two generic clocks are used by the FREQM: Reference Clock (GCLK_FREQM_REF) and Measurement Clock (GCLK_FREQM_MSR).

GCLK_FREQM_REF is required to clock the internal reference timer, which acts as the frequency reference.

GCLK_FREQM_MSR is required to clock a ripple counter for frequency measurement. These clocks must be configured and enabled in the generic clock controller before using the FREQM.

**Related Links**

15. MCLK – Main Clock

15.6.2.6 Peripheral Clock Masking

14. GCLK - Generic Clock Controller

### 30.5.4 DMA

Not applicable.

### 30.5.5 Interrupts

The interrupt request line is connected to the interrupt controller. Using FREQM interrupt requires the interrupt controller to be configured first.

**Related Links**

10.2.2 Interrupt Line Mapping

### 30.5.6 Events

Not applicable

### 30.5.7 Debug Operation

When the CPU is halted in debug mode the FREQM continues its normal operation. The FREQM cannot be halted when the CPU is halted in debug mode. If the FREQM is configured in a way that requires it to be periodically serviced by the CPU, improper operation or data loss may result during debugging.

### 30.5.8 Register Access Protection

All registers with write-access can be write-protected optionally by the Peripheral Access Controller (PAC), except the following registers:

Writing a '0' to this bit has no effect.

Writing a '1' to this bit will clear it. It will also clear the corresponding flag in the Channel n Interrupt Flag Status and Clear register (CHINTFLAGn) of this peripheral, where n is determined by the Channel ID bit field (ID) in this register.

**Bits 4:0 – ID[4:0]** Channel ID
These bits store the channel number of the highest priority.

When the bits are written, indirect access to the corresponding Channel Interrupt Flag register is enabled.

| Value | Name | Description |
|---|---|---|
| 0x62 | PDEC_ERR | PDEC Error |
| 0x63 | PDEC_DIR | PDEC Direction |
| 0x64 | PDEC_VLC | PDEC VLC |
| 0x65 - 0x66 | PDEC_MCx | PDEC MCx x=0..1 |
| 0x67 | ADC0_RESRDY | ADC0 RESRDY |
| 0x68 | ADC0_WINMON | ADC0 Window Monitor |
| 0x69 | ADC1_RESRDY | ADC1 RESRDY |
| 0x6A | ADC1_WINMON | ADC1 Window Monitor |
| 0x6B - 0x6C | AC_COMPx | AC Comparator, x=0..1 |
| 0x6D | AC_WIN | AC0 Window |
| 0x6E - 0x6F | DAC_EMPTYx | DAC empty, x=0..1 |
| 0x70 - 0x71 | DAC_RESRDYx | DAC RSRDY, x=0..1 |
| 0x72 | GMAC_TSU_CMP | GMAC Timestamp CMP |
| 0x73 | TRNG_READY | TRNG ready |
| 0x74 - 0x77 | CCL_LUTOUT | CCL LUTOUT |

- Master operation, CTRLA.RUNSTDBY=1: The peripheral clock GCLK_SERCOM_CORE will continue to run in idle sleep mode and in standby sleep mode. Any interrupt can wake up the device.
- Master operation, CTRLA.RUNSTDBY=0: GLK_SERCOMx_CORE will be disabled after the ongoing transaction is finished. Any interrupt can wake up the device.
- Slave operation, CTRLA.RUNSTDBY=1: The Receive Complete interrupt can wake up the device.
- Slave operation, CTRLA.RUNSTDBY=0: All reception will be dropped, including the ongoing transaction.

### 35.6.6 Synchronization

Due to asynchronicity between the main clock domain and the peripheral clock domains, some registers need to be synchronized when written or read.

The following bits are synchronized when written:

- Software Reset bit in the CTRLA register (CTRLA.SWRST)
- Enable bit in the CTRLA register (CTRLA.ENABLE)
- Receiver Enable bit in the CTRLB register (CTRLB.RXEN)

**Note:** CTRLB.RXEN is write-synchronized somewhat differently. See also *CTRLB* register for details.

Required write-synchronization is denoted by the "Write-Synchronized" property in the register description.

**Bit 0 – SUSPEND** Suspend Interrupt Enable
Writing a zero to this bit has no effect.

Writing a one to this bit will clear the Suspend Interrupt Enable bit and disable the corresponding interrupt request.

| Value | Description |
|---|---|
| 0 | The Suspend interrupt is disabled. |
| 1 | The Suspend interrupt is enabled and an interrupt request will be generated when the Suspend interrupt Flag is set. |

| Value | Description |
|---|---|
| 0 | No Data PID Error detected. |
| 1 | A Data PID error has been detected. |

**Bit 0 – DTGLER** Data Toggle Error
This bit defines the Data Toggle Error Status.

This bit is set when a Data Toggle Error has been detected.

| Value | Description |
|---|---|
| 0 | No Data Toggle Error. |
| 1 | Data Toggle Error detected. |

### 40.8.40 Clock Control 2 Register

**Name:** CC2R
**Offset:** 0x20C
**Reset:** 0x00000000
**Property:** -

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Access | | | | | | | | |
| Reset | | | | | | | | |

| Bit | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Access | | | | | | | | |
| Reset | | | | | | | | |

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Access | | | | | | | | |
| Reset | | | | | | | | |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | | | | | | | | FSDCLKD |
| Access | | | | | | | | R/W |
| Reset | | | | | | | | 0 |

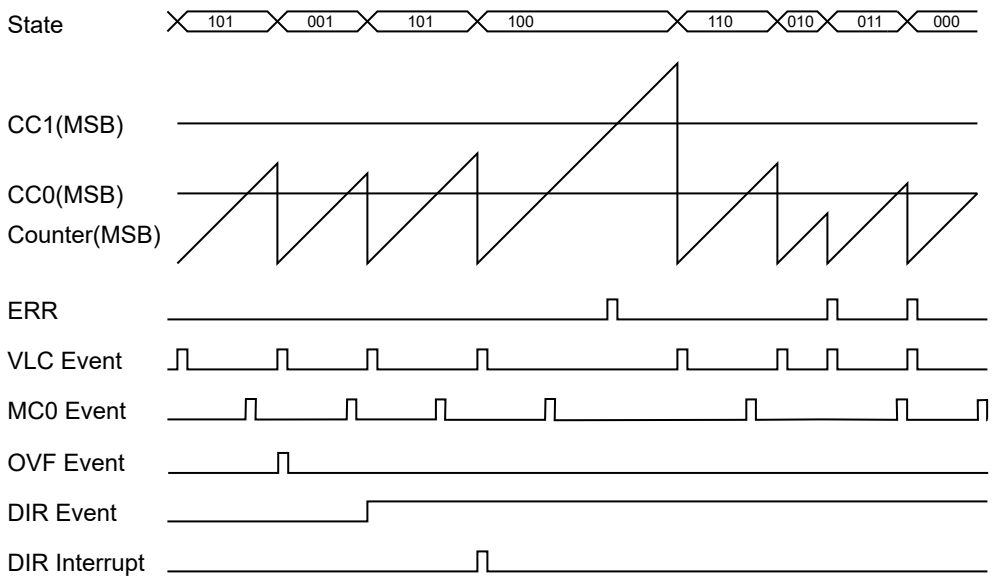
**Bit 0 – FSDCLKD** Force SDCLK Disabled
The user can choose to maintain the SDCLK during 8 SDCLK cycles after the end bit of the last data block in case of a read transaction, or after the end bit of the CRC status in case of a write transaction.

| Value | Description |
|---|---|
| 0 | The SDCLK is forced and it cannot be stopped immediately after the transaction. |
| 1 | The SDCLK is not forced and it can be stopped immediately after the transaction. |

- The filter output value is checked to be a valid Hall value. If an invalid Hall code is reported, the Hall Error bit in Status register will be set (STATUS.HERR).
- The MC0 Interrupt Flag bit is set (INTFLAG.MC0) if CC0[2:0] matches the filter output value. An optional compare match interrupt or Event output is generated on the same condition detection.
- The window counter is checked to be between CC0[MSB] and CC1[MSB] value, and reset to 0 value. If an error is detected, the Window Error bit in Status register (STATUS.WINERR) is set.
- The delay counter is started, and MC0 optional interrupt or event is generated when the delay counter matches CC0[LSB].

Any error condition will set the Error Interrupt Flag (INTFLAG.ERR). An optional interrupt or event output is generated on the same condition detection.

**Figure 53-9. Hall Waveforms**




### 53.6.3.2 Counter Operation Mode

Depending on the mode of operation, the counter (Counter Value register COUNT) is cleared, reloaded, or incremented at each counter clock input.

The counter will count for each clock tick until it reaches TOP. When TOP is reached, the counter will be set to zero on the next clock input.

This comparison will set the Overflow Interrupt Flag in the Interrupt Flag Status and Clear register (INTFLAG.OVF) and can be used to trigger an interrupt or an event.

It is possible to change the counter value when the counter is running. The write access has higher priority than count, or clear. The COUNT value will always be zero when starting the PDEC, unless a different value has been written to it, or the PDEC has been disabled at a value other than zero. Due to asynchronous clock domains, the internal counter settings are written once the synchronization is complete.

**Related Links**

14. GCLK - Generic Clock Controller

### 53.8.14 Filter Buffer Value

**Name:** FILTERBUF
**Offset:** 0x19
**Reset:** 0x00
**Property:** Write-Synchronized

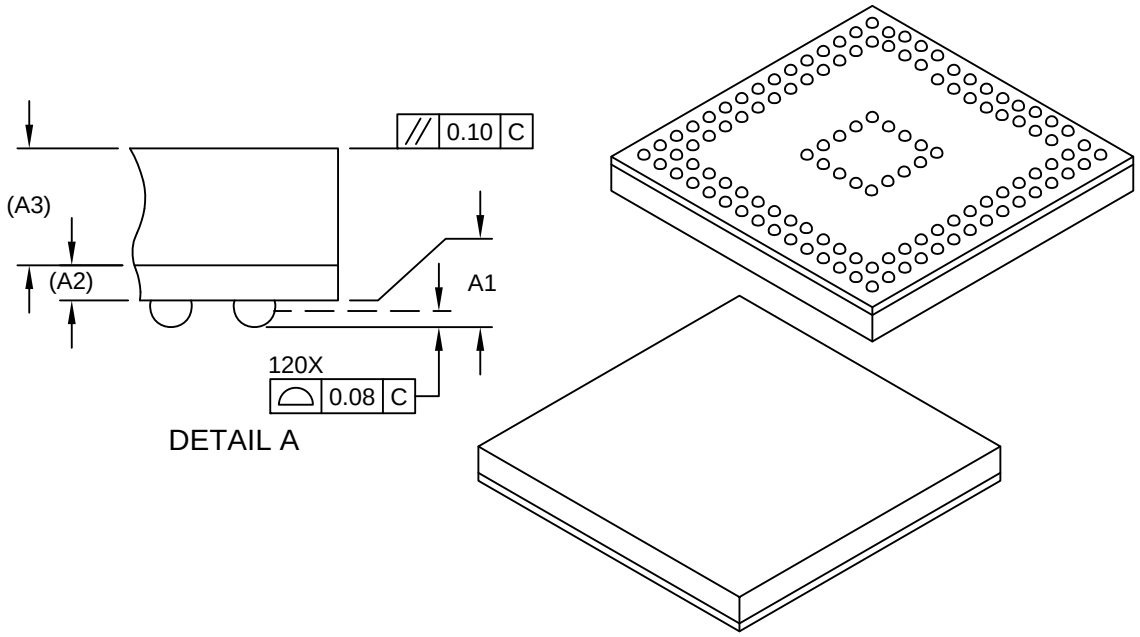
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | FILTERBUF[7:0] | | | | | | | |
| Access | RW | RW | RW | RW | RW | RW | RW | RW |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Bits 7:0 – FILTERBUF[7:0]** Filter Buffer Value
These bits hold the value of the filter buffer register. The value is copied in the corresponding FILTER register on UPDATE condition.

These bits have no effect when COUNTER operation mode is selected.

## 120-Ball Thin Fine Pitch Ball Grid Array Package (DGB) - 4x4 mm Body [TFBGA]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Terminals | N | | 120 | |
| Pitch | e | | 0.50 BSC | |
| Overall Height | A | - | - | 1.20 |
| Standoff | A1 | 0.11 | - | 0.21 |
| Substrate Thickness | A2 | | 2.10 REF | |
| Mold Cap Thickness | A3 | | 0.70 REF | |
| Overall Length | D | | 8.00 BSC | |
| Overall Ball Pitch | D1 | | 7.00 BSC | |
| Overall Width | E | | 8.00 BSC | |
| Exposed Pad Width | E1 | | 7.00 BSC | |
| Terminal Width | b | 0.20 | - | 0.30 |

Notes:

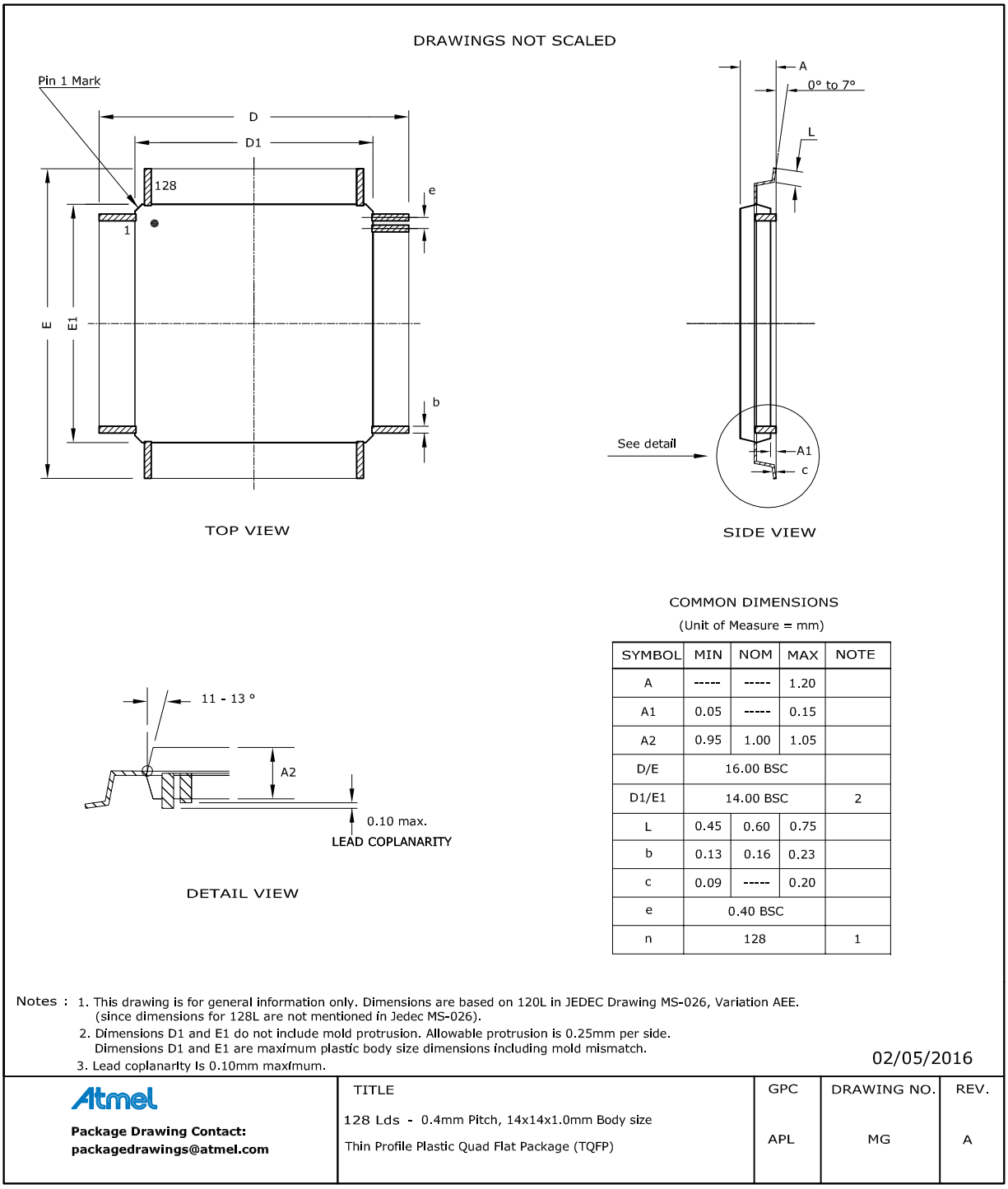
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-21465 Rev A Sheet 1 of 2

### 55.3.7 128 pin TQFP




COMMON DIMENSIONS

(Unit of Measure = mm)

| SYMBOL | MIN | NOM | MAX | NOTE |
|---|---|---|---|---|
| A | ----- | ----- | 1.20 | |
| A1 | 0.05 | ----- | 0.15 | |
| A2 | 0.95 | 1.00 | 1.05 | |
| D/E | | 16.00 BSC | | |
| D1/E1 | | 14.00 BSC | | 2 |
| L | 0.45 | 0.60 | 0.75 | |
| b | 0.13 | 0.16 | 0.23 | |
| c | 0.09 | ----- | 0.20 | |
| e | | 0.40 BSC | | |
| n | | 128 | | 1 |

Notes :
1. This drawing is for general information only. Dimensions are based on 120L in JEDEC Drawing MS-026, Variation AEE. (since dimensions for 128L are not mentioned in Jedec MS-026).
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25mm per side. Dimensions D1 and E1 are maximum plastic body size dimensions including mold mismatch.
3. Lead coplanarity is 0.10mm maximum.

02/05/2016

| Atmel | TITLE | GPC | DRAWING NO. | REV. |
|---|---|---|---|---|
| **Package Drawing Contact:** **packagedrawings@atmel.com** | 128 Lds - 0.4mm Pitch, 14x14x1.0mm Body size Thin Profile Plastic Quad Flat Package (TQFP) | APL | MG | A |

**Table 55-14. Device and Package Maximum Weight**

| | |
|---|---|
| 520 | mg |

**Table 55-15. Package Characteristics**

| | |
|---|---|
| Moisture Sensitivity Level | MSL3 |