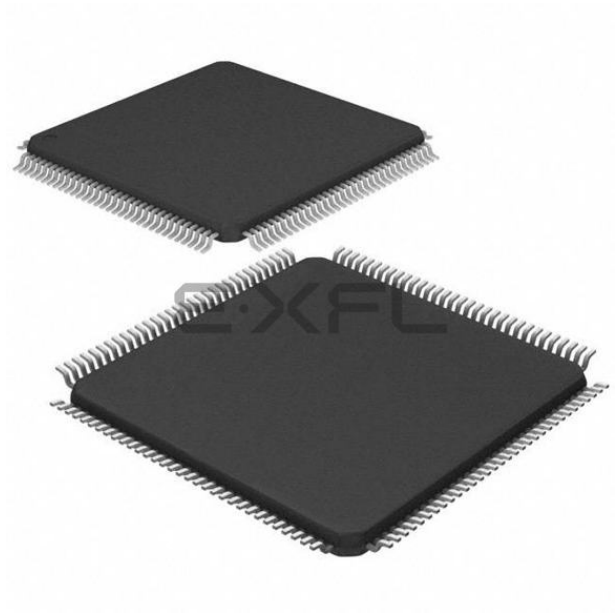

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4F
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	EBI/EMI, I²C, IrDA, LINbus, MMC/SD, QSPI, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM
Number of I/O	99
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.63V
Data Converters	A/D 32x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	128-TQFP
Supplier Device Package	128-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atsamd51p20a-aut

12.13.4 Address

Name: ADDR
Offset: 0x0004
Reset: 0x00000000
Property: PAC Write-Protection

Bit	31	30	29	28	27	26	25	24
	ADDR[29:22]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	ADDR[21:14]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	ADDR[13:6]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	ADDR[5:0]						AMOD[1:0]	
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:2 – ADDR[29:0] Address
Initial word start address needed for memory operations.

Bits 1:0 – AMOD[1:0] Access Mode
The functionality of these bits is dependent on the operation mode.

Bit description when operating CRC32: refer to 12.11.3 32-bit Cyclic Redundancy Check CRC32

Bit description when testing onboard memories (MBIST): refer to 12.11.6 Testing of On-Board Memories MBIST

12.13.14 Peripheral Identification 4

Name: PID4
Offset: 0x1FD0
Reset: 0x00000000
Property: -

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
	FKBC[3:0]				JEPCC[3:0]			
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 7:4 – FKBC[3:0] 4KB Count
These bits will always return zero when read, indicating that this debug component occupies one 4KB block.

Bits 3:0 – JEPCC[3:0] JEP-106 Continuation Code
These bits will always return zero when read.

13.2 Synchronous and Asynchronous Clocks

As the CPU and the peripherals can be in different clock domains, i.e. they are clocked from different clock sources and/or with different clock speeds, some peripheral accesses by the CPU need to be synchronized. In this case the peripheral includes a Synchronization Busy (SYNCBUSY) register that can be used to check if a sync operation is in progress.

For a general description, see 13.3 Register Synchronization. Some peripherals have specific properties described in their individual sub-chapter “Synchronization”.

In the datasheet, references to Synchronous Clocks are referring to the CPU and bus clocks (MCLK), while asynchronous clocks are generated by the Generic Clock Controller (GCLK).

Related Links

14.6.6 Synchronization

13.3 Register Synchronization

13.3.1 Overview

All peripherals are composed of one digital bus interface connected to the APB or AHB bus and running from a corresponding clock in the Main Clock domain, and one peripheral core running from the peripheral Generic Clock (GCLK).

Communication between these clock domains must be synchronized. This mechanism is implemented in hardware, so the synchronization process takes place even if the peripheral generic clock is running from the same clock source and on the same frequency as the bus interface.

All registers in the bus interface are accessible without synchronization.

All registers in the peripheral core are synchronized when written. Some registers in the peripheral core are synchronized when read.

Each individual register description will have the properties "Read-Synchronized" and/or "Write-Synchronized" if a register is synchronized.

As shown in the figure below, each register that requires synchronization has its individual synchronizer and its individual synchronization status bit in the Synchronization Busy register (SYNCBUSY).
Note: For registers requiring both read- and write-synchronization, the corresponding bit in SYNCBUSY is shared.

16.8.1 Reset Cause

Name: RCAUSE
Offset: 0x00
Property: –

When a Reset occurs, the bit corresponding to the Reset source is set to '1' and all other bits are written to '0'.

Bit	7	6	5	4	3	2	1	0
	BACKUP	SYST	WDT	EXT	NVM	BOD33	BOD12	POR
Access	R	R	R	R	R	R	R	R
Reset	x	x	x	x	x	x	x	x

Bit 7 – BACKUP Backup Reset
This bit is set if either a Backup or Hibernate Reset has occurred. Refer to BKUPEXIT register to identify the source of the Backup Reset.

Bit 6 – SYST System Reset Request
This bit is set if a System Reset Request has occurred. Refer to the Cortex processor documentation for more details.

Bit 5 – WDT Watchdog Reset
This bit is set if a Watchdog Timer Reset has occurred.

Bit 4 – EXT External Reset
This bit is set if an external Reset has occurred.

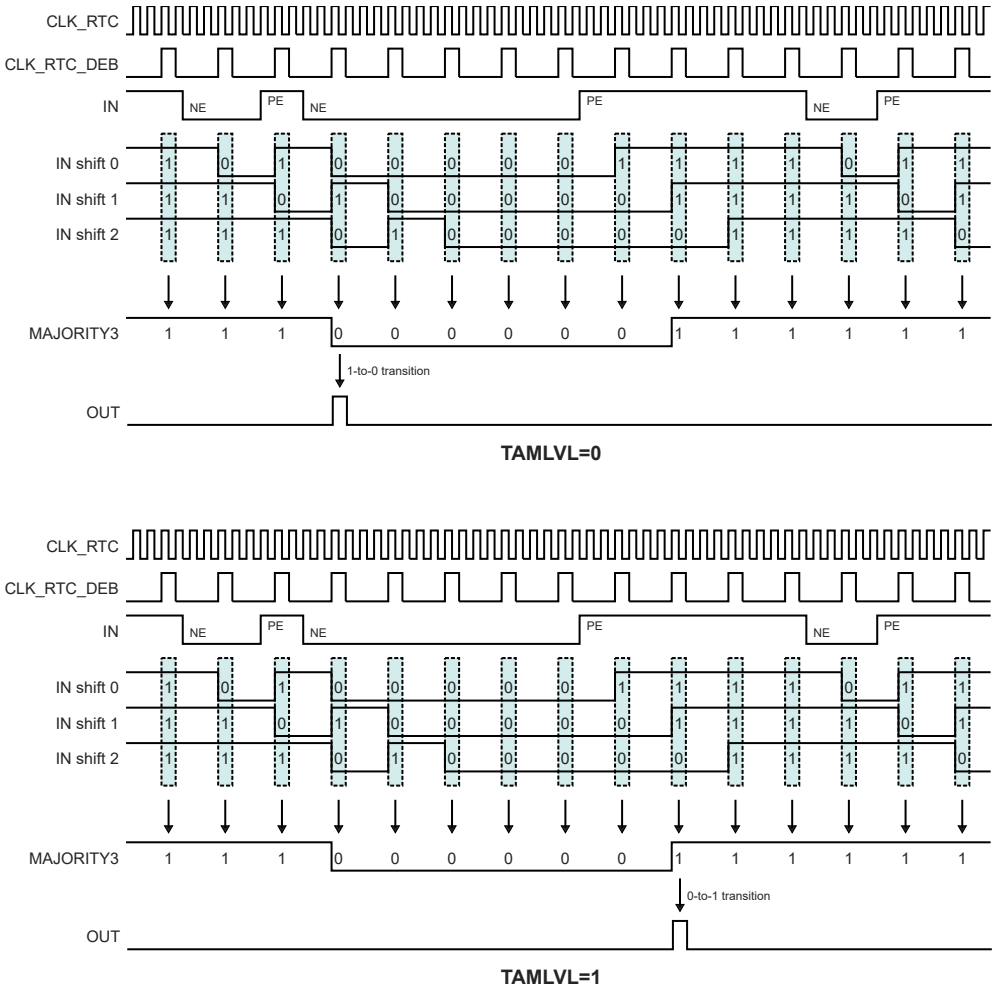
Bit 3 – NVM NVM Reset
This bit is set if an NVM Reset has occurred.

Bit 2 – BOD33 Brown Out 33 Detector Reset
This bit is set if a BOD33 Reset has occurred.

Bit 1 – BOD12 Brown Out 12 Detector Reset
This bit is set if a BOD12 Reset has occurred.

Bit 0 – POR Power On Reset
This bit is set if a POR has occurred.

Figure 21-9. Edge Detection with Majority Debouncing



Related Links

21.3 Block Diagram

21.6.8.5.1 Timestamp

21.6.8.5.2 Active Layer Protection

21.6.8.5.1 Timestamp

As part of tamper detection the RTC can capture the counter value (COUNT/CLOCK) into the TIMESTAMP register. Three CLK_RTC periods are required to detect the tampering condition and capture the value. The TIMESTAMP value can be read once the Tamper flag in the Interrupt Flag register (INTFLAG.TAMPER) is set. If the DMA Enable bit in the Control B register (CTRLB.DMAEN) is '1', a DMA request will be triggered by the timestamp. In order to determine which tamper source caused a capture, the Tamper ID register (TAMPID) provides the detection status of each tamper channel and the tamper input event. A DMA transfer can then read both TIMESTAMP and TAMPID in succession.

A new timestamp value cannot be captured until the Tamper flag is cleared, either by reading the timestamp or by writing a '1' to INTFLAG.TAMPER. If several tamper conditions occur in a short window before the flag is cleared, only the first timestamp may be logged. However, the detection of each tamper will still be recorded in TAMPID.

Related Links

10.3 High-Speed Bus System

25.6.5 Region Lock Bits

The NVM main address space is accessible through the AHB0 or AHB1 interfaces, and grouped into 32 equally sized regions regardless of BOOTPROT or SmartEEPROM settings. The region size is dependent on the flash memory size, and is given in the table below. Each region has a dedicated lock bit preventing writing and erasing pages in the region. After production, all regions will be unlocked.

Table 25-4. Region Size

Memory Size [KB]	Region Size [KB]
1024	32
512	16
256	8

To lock or unlock a region, the Lock Region and Unlock Region commands are provided. Writing one of these commands will temporarily lock/unlock the region containing the address loaded in the ADDR register. ADDR can be written by software, or the automatically loaded value from a AHB write operation can be used. The new setting will stay in effect until the next reset, or the setting can be changed again using the lock and unlock commands. The current status of the lock can be determined by reading the RUNLOCK register.

To change the default lock/unlock setting for a region, the user page must be written. Writing to the auxiliary space will take effect after the next reset. Therefore, a boot of the device is needed for changes in the lock/unlock setting to take effect. Refer to the Physical Memory Map for calibration and auxiliary space address mapping.

Related Links

9.2 Physical Memory Map

25.6.6 Command and Data Interface

The NVM Controller is addressable from the APB bus, while the NVM main address space is addressable from the AHB bus. Read and automatic page write operations are performed by addressing the NVM main address space directly, while other operations such as manual page writes and block erase must be performed by issuing commands through the NVM Controller.

To issue a command, the CTRLB.CMD bits must be written along with the CTRLB.CMDEX value. STATUS.READY is cleared when a command is issued and set when it has completed. Any command written while STATUS.READY is low will be ignored causing INTFLAG.PROGE to rise. Refer to CTRLB register description for more details.

Invalid commands are discarded and will set INTFLAG.PROGE and INTFLAG.DONE when issued.

The CTRLA register must be used to control the power reduction mode, read wait states and the write mode.

Commands that require an address use the ADDR register as an argument. ADDR APB write access is locked by the NVMCTRL while being used internally. For instance if a write operation is started by the NVMCTRL, an APB write is discarded so that the write operation is performed at the correct address. The discarded APB write is signaled by rising INTFLAG.ADDRE. Commands that needs an address will fail if issued while INTFLAG.ADDRE is set, such failure is signaled by rising INTFLAG.PROGE.

The APB ADDR register is updated upon:

- APB writes to the ADDR register address
- AHB writes to the page buffer

ADDR APB writes are discarded and report an INTFLAG.ADDRE error in the following cases:

- When written from APB while a command is reading it.
- ADDR APB write access while writing the page buffer (AHB write): ADDR is written upon AHB writes and must stay valid until the page buffer has been written and also until automatic write command has been issued to the command interface when in automatic write mode (WMODE configured as ADW or AQW or AP).
- ADDR APB write access while the command interface reads it.
- A command is executed at an illegal address

All commands that require an address are discarded when INTFLAG.ADDRE is set. INTFLAG.PROGE is set in this case. INTFLAG.ADDRE must be cleared before issuing such commands.

25.6.6.1 NVM Read

Reading from the NVM main address space is performed via the AHB bus by addressing the NVM main address space or auxiliary address space directly. Read data is available after the number of read wait states has passed as configured in NVMCTRL.CTRLA.RWS.

The number of cycles data are delayed to the AHB bus is determined by the read wait states.

It is not possible to read two banks at the same time. In case of simultaneous read operations, transactions are arbitrated by the internal matrix. Arbitration scheme is fixed priority, AHB0 has the highest priority, AHB1 has priority over AHB2. In case of conflict, AHB interfaces with lower priority are stalled.

Reading in a bank stalls the bus when it is being programmed or erased except when the suspend feature is used.

Reading in a bank does not stall the bus when the other bank is being programmed or erased.

Related Links

25.6.6.4 Suspend/Resume

25.6.6.2 NVM Write

The entire NVM main address space except the BOOTPROT section can be erased by a debugger Chip Erase command. Alternatively, blocks or pages can be individually erased using the Erase Page (EP) or Erase Block (EB) depending on the targeted address space. The NVM can be programmed using the Write Page (WP) or Write Quad Word (WQW) commands depending on the targeted address space. AHB writes automatically update the ADDR register. ADDR is write locked by the NVMCTRL until the pagebuffer write completes or until the appropriate write command has been passed to the command interface when in automatic write mode. Write commands are not supported in all address spaces, see the table below. These commands are detailed further in this section.

25.8.2 Control B

Name: CTRLB
Offset: 0x04
Reset: 0x0000
Property: PAC Write-Protection

Bit	15	14	13	12	11	10	9	8
	CMDEX[7:0]							
Access	PAC Write-Protection	PAC Write-Protection	PAC Write-Protection	PAC Write-Protection	PAC Write-Protection	PAC Write-Protection	PAC Write-Protection	PAC Write-Protection
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
		CMD[6:0]						
Access		W	W	W	W	W	W	W
Reset		0	0	0	0	0	0	0

Bits 15:8 – CMDEX[7:0] Command Execution
This bit group should be written with the key value 0xA5 to enable the command written to CMD to be executed. If the bit group is written with a different key value, the write is not performed and INTFLAG.PROGE is set. PROGE is also set if the a previously written command is not complete.

The key value must be written at the same time as CMD. If a command is issued through the APB bus on the same cycle as an AHB bus access, the AHB bus access will be given priority. The command will then be executed when the NVM block and the AHB bus are idle.

STATUS.READY must be one when the command is issued.

INTFLAG.DONE is set when the command completes.

Value	Name	Description
0xA5	KEY	Execution Key
Other	-	Reserved

Bits 6:0 – CMD[6:0] Command
These bits define the command to be executed when the CMDEX key is written.

Value	Name	Description
0x0	EP	Erase Page - Only supported in the User page in the auxiliary space.
0x1	EB	Erase Block - Erases the block addressed by the ADDR register, not supported in the user page
0x2		Reserved
0x3	WP	Write Page - Writes the contents of the page buffer to the page addressed by the ADDR register, not supported in the user page
0x4	WQW	Write Quad Word - Writes a 128-bit word at the location addressed by the ADDR register.
0x5-0xF		Reserved
0x10	SWRST	Software Reset - Power-Cycle the NVM memory and replay the device automatic calibration procedure and resets the module configuration registers

28.8.12 DPLL Control A

Name: DPLLCTRLA
Offset: 0x30 + n*0x14 [n=0..1]
Reset: 0x80
Property: PAC Write-Protection, Write-Synchronized(ENABLE), Enable-Protected (ONDEMAND, RUNSTDBY)

Bit	7	6	5	4	3	2	1	0
	ONDEMAND	RUNSTDBY					ENABLE	
Access	R/W	R/W					R/W	
Reset	1	0					0	

Bit 7 – ONDEMAND On Demand Control
The On Demand operation mode allows the DPLLn to be enabled or disabled, depending on peripheral clock requests.

If On Demand is set, the DPLLn will be running only when requested by a peripheral and enabled (DPLLnCTRLA. ENABLE=1). If there is no peripheral requesting the DPLLn's clock source, the DPLLn will be in a disabled state.

If On Demand is cleared, the DPLLn will always be running when enabled (DPLLnCTRLA.ENABLE=1).

In standby sleep mode, the On Demand operation is still active.

0: The DPLLn is always running.

1: The DPLLn is running when a peripheral is requesting the DPLLn to be used as a clock source. The DPLLn is not running if no peripheral is requesting the clock source.

Bit 6 – RUNSTDBY Run in Standby
This bit controls how the DPLLn behaves during standby sleep mode:

0: The DPLLn is not running in standby sleep mode if no peripheral requests the clock.

1: The DPLLn is running in standby sleep mode. If ONDEMAND is one, the DPLLn will be running when a peripheral is requesting the clock. If ONDEMAND is zero, the clock source will always be running in standby sleep mode.

Bit 1 – ENABLE DPLL Enable
0: The DPLLn is disabled.

1: The DPLLn is enabled.

The software operation of enabling or disabling the DPLLn takes a few clock cycles, so the DPLLnSYNCBUSY. ENABLE status bit indicates when the DPLLn is successfully enabled or disabled.

38.8.7.6 Host Control Pipe

Name: CTRL_PIPE
Offset: 0x0C
Reset: 0xXXXX
Property: PAC Write-Protection, Write-Synchronized, Read-Synchronized

Bit	15	14	13	12	11	10	9	8
	PERMAX[3:0]				PEPNUM[3:0]			
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	x	0	0	0	x

Bit	7	6	5	4	3	2	1	0
		PDADDR[6:0]						
Access		R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset		0	0	0	0	0	0	x

Bits 15:12 – PERMAX[3:0] Pipe Error Max Number
These bits define the maximum number of error for this Pipe before freezing the pipe automatically.

Bits 11:8 – PEPNUM[3:0] Pipe EndPoint Number
These bits define the number of endpoint for this Pipe.

Bits 6:0 – PDADDR[6:0] Pipe Device Address
These bits define the Device Address for this pipe.

41. CCL – Configurable Custom Logic

41.1 Overview

The Configurable Custom Logic (CCL) is a programmable logic peripheral which can be connected to the device pins, to events, or to other internal peripherals. This allows the user to eliminate logic gates for simple glue logic functions on the PCB.

Each LookUp Table (LUT) consists of three inputs, a truth table, an optional synchronizer/filter, and an optional edge detector. Each LUT can generate an output as a user programmable logic expression with three inputs. Inputs can be individually masked.

The output can be combinatorially generated from the inputs, and can be filtered to remove spikes. Optional sequential logic can be used. The inputs of the sequential module are individually controlled by two independent, adjacent LUT (LUT0/LUT1, LUT2/LUT3 etc.) outputs, enabling complex waveform generation.

41.2 Features

- Glue logic for general purpose PCB design
- Up to 4 programmable LookUp Tables (LUTs)
- Combinatorial logic functions:
  AND, NAND, OR, NOR, XOR, XNOR, NOT
- Sequential logic functions:
  Gated D Flip-Flop, JK Flip-Flop, gated D Latch, RS Latch
- Flexible LUT inputs selection:
  - I/Os
  - Events
  - Internal peripherals
  - Subsequent LUT output
- Output can be connected to the I/O pins or the Event System
- Optional synchronizer, filter, or edge detector available on each LUT output

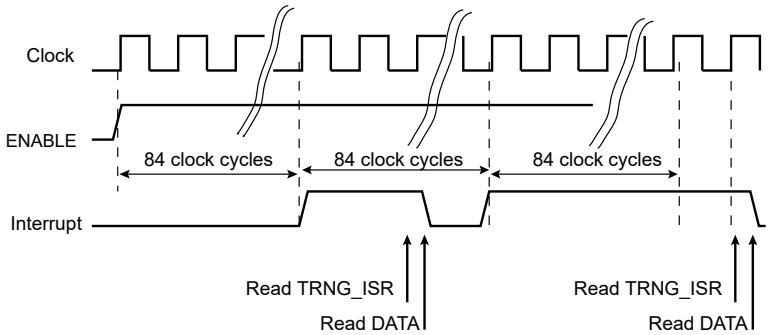
44.6 Functional Description

44.6.1 Principle of Operation

When the TRNG is enabled, the peripheral starts providing new 32-bit random numbers every 84 CLK_TRNG_APB clock cycles.

The TRNG can be configured to generate an interrupt or event when a new random number is available.

Figure 44-2. TRNG Data Generation Sequence



44.6.2 Basic Operation

44.6.2.1 Initialization

To operate the TRNG, do the following:

- Configure the clock source for CLK_TRNG_APB in the Main Clock Controller (MCLK) and enable the clock by writing a ‘1’ to the TRNG bit in the APB Mask register of the MCLK.
- Optional: Enable the output event by writing a ‘1’ to the EVCTRL.DATARDYEO bit.
- Optional: Enable the TRNG to Run in Standby sleep mode by writing a ‘1’ to CTRLA.RUNSTDBY.
- Enable the TRNG operation by writing a ‘1’ to CTRLA.ENABLE.

The following register is enable-protected, meaning that it can only be written when the TRNG is disabled (CTRLA.ENABLE is zero):

- Event Control register (EVCTRL)

Enable-protection is denoted by the Enable-Protected property in the register description.

44.6.2.2 Enabling, Disabling and Resetting

The TRNG is enabled by writing '1' to the Enable bit in the Control A register (CTRLA.ENABLE). The TRNG is disabled by writing a zero to CTRLA.ENABLE.

44.6.3 Interrupts

The TRNG has the following interrupt source:

- Data Ready (DATARDY): Indicates that a new random number is available in the DATA register and ready to be read.
  This interrupt is a synchronous wake-up source. See *Sleep Mode Controller* for details.

The interrupt source has an interrupt flag associated with it. The interrupt flag in the Interrupt Flag Status and Clear register (INTFLAG.DATARDY) is set to ‘1’ when the interrupt condition occurs. The interrupt can be enabled by writing a '1' to the corresponding bit in the Interrupt Enable Set register (INTENSET.DATARDY), and disabled by writing a '1' to the corresponding bit in the Interrupt Enable Clear (INTENCLR) register.

45.5.6 Events

The events are connected to the Event System.

Related Links

31. EVSYS – Event System

45.5.7 Debug Operation

When the CPU is halted in debug mode the ADC will halt normal operation. The ADC can be forced to continue operation during debugging. Refer to DBGCTRL register for details.

Related Links

45.8.3 DBGCTRL

45.5.8 Register Access Protection

All registers with write-access are optionally write-protected by the peripheral access controller (PAC), except the following register:

- Interrupt Flag Status and Clear (INTFLAG) register

Optional write-protection by the Peripheral Access Controller (PAC) is denoted by the "PAC Write-Protection" property in each individual register description.

PAC write-protection does not apply to accesses through an external debugger.

Related Links

27. PAC - Peripheral Access Controller

45.5.9 Analog Connections

I/O-pins (AINx), as well as the VREFA/VREFB/VREFC reference voltage pins are analog inputs to the ADC. Any internal reference source, such as a bandgap voltage reference, or DAC must be configured and enabled prior to its use with the ADC.

45.5.10 Calibration

The BIASREFBUF, BIASR2R and BIASCOMP calibration values from the production test must be loaded from the NVM Software Calibration Area into the ADC Calibration register (CALIB) by software to achieve specified accuracy.

45.6 Functional Description

45.6.1 Principle of Operation

By default, the ADC provides results with 12-bit resolution. 8-bit or 10-bit results can be selected in order to reduce the conversion time, see 45.6.2.8 Conversion Timing and Sampling Rate.

The ADC has an oversampling with decimation option that can extend the resolution to 16 bits. The input values can be either internal (e.g., an internal temperature sensor) or external (connected I/O pins). The user can also configure whether the conversion should be single-ended or differential.

45.6.2 Basic Operation

45.6.2.1 Initialization

The following registers are enable-protected, meaning that they can only be written when the ADC is disabled (CTRLA.ENABLE=0):

45.8.7 Average Control

Name: AVGCTRL
Offset: 0x0A
Reset: 0x00
Property: PAC Write-Protection, Write-Synchronized

Bit	7	6	5	4	3	2	1	0
		ADJRES[2:0]			SAMPLENUM[3:0]			
Access		R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset		0	0	0	0	0	0	0

Bits 6:4 – ADJRES[2:0] Adjusting Result / Division Coefficient
These bits define the division coefficient in 2^n steps.

Bits 3:0 – SAMPLENUM[3:0] Number of Samples to be Collected
These bits define how many samples are added together. The result will be available in the Result register (RESULT). Note: if the result width increases, CTRLB.RESSEL must be changed.

Value	Description
0x0	1 sample
0x1	2 samples
0x2	4 samples
0x3	8 samples
0x4	16 samples
0x5	32 samples
0x6	64 samples
0x7	128 samples
0x8	256 samples
0x9	512 samples
0xA	1024 samples
0xB - 0xF	Reserved

46.8.6 Interrupt Flag Status and Clear

Name: INTFLAG
Offset: 0x06
Reset: 0x00
Property: –

Bit	7	6	5	4	3	2	1	0
				WIN0			COMPx	COMPx
Access				R/W			R/W	R/W
Reset				0			0	0

Bit 4 – WIN0 Window 0
This flag is set according to the Window 0 Interrupt Selection bit group in the WINCTRL register (WINCTRL.WINTSELx) and will generate an interrupt if INTENCLR/SET.WINx is also one.

Writing a '0' to this bit has no effect.

Writing a '1' to this bit clears the Window 0 interrupt flag.

Bits 1,0 – COMPx Comparator x
Reading this bit returns the status of the Comparator x interrupt flag. If comparator x is not implemented, COMPx always reads as zero.

This flag is set according to the Interrupt Selection bit group in the Comparator x Control register (COMPCTRLx.INTSEL) and will generate an interrupt if INTENCLR/SET.COMPx is also one.

Writing a '0' to this bit has no effect.

Writing a '1' to this bit clears the Comparator x interrupt flag.

Bit 1 – ENABLE ENABLE Synchronization Busy
This bit is cleared when the synchronization of ENABLE bit between the clock domains is complete.

This bit is set when the synchronization of ENABLE bit between clock domains is started.

Bit 0 – SWRST SWRST Synchronization Busy
This bit is cleared when the synchronization of SWRST bit between the clock domains is complete.

This bit is set when the synchronization of SWRST bit between clock domains is started.

3. If down-counting operation is desired, write the Counter Direction bit in the Control B Set register (CTRLBSET.DIR) to '1'.
4. Select the Waveform Generation operation in the WAVE register (WAVE.WAVEGEN).
5. Select the Waveform Output Polarity in the WAVE register (WAVE.POL).
6. The waveform output can be inverted for the individual channels using the Waveform Output Invert Enable bit group in the Driver register (DRVCTRL.INVEN).

49.6.2.2 Enabling, Disabling, and Resetting

The TCC is enabled by writing a '1' to the Enable bit in the Control A register (CTRLA.ENABLE). The TCC is disabled by writing a zero to CTRLA.ENABLE.

The TCC is reset by writing '1' to the Software Reset bit in the Control A register (CTRLA.SWRST). All registers in the TCC, except DBGCTRL, will be reset to their initial state, and the TCC will be disabled. Refer to Control A (49.8.1 CTRLA) register for details.

The TCC should be disabled before the TCC is reset to avoid undefined behavior.

49.6.2.3 Prescaler Selection

The GCLK_TCCx clock is fed into the internal prescaler.

The prescaler consists of a counter that counts up to the selected prescaler value, whereupon the output of the prescaler toggles.

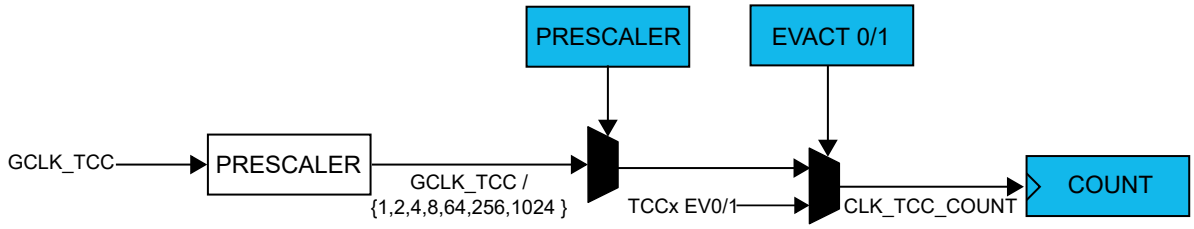
If the prescaler value is higher than one, the counter update condition can be optionally executed on the next GCLK_TCC clock pulse or the next prescaled clock pulse. For further details, refer to the Prescaler (CTRLA.PRESCALER) and Counter Synchronization (CTRLA.PRESYNC) descriptions.

Prescaler outputs from 1 to 1/1024 are available. For a complete list of available prescaler outputs, see the register description for the Prescaler bit group in the Control A register (CTRLA.PRESCALER).

Note: When counting events, the prescaler is bypassed.

The joint stream of prescaler ticks and event action ticks is called CLK_TCC_COUNT.

Figure 49-2. Prescaler



49.6.2.4 Counter Operation

Depending on the mode of operation, the counter is cleared, reloaded, incremented, or decremented at each TCC clock input (CLK_TCC_COUNT). A counter clear or reload mark the end of current counter cycle and the start of a new one.

The counting direction is set by the Direction bit in the Control B register (CTRLB.DIR). If the bit is zero, it's counting up and one if counting down.

The counter will count up or down for each tick (clock or event) until it reaches TOP or ZERO. When it's counting up and TOP is reached, the counter will be set to zero at the next tick (overflow) and the Overflow Interrupt Flag in the Interrupt Flag Status and Clear register (INTFLAG.OVF) will be set. When down-counting, the counter is reloaded with the TOP value when ZERO is reached (underflow), and INTFLAG.OVF is set.

Figure 49-26. Waveform Generation in RAMP1 mode with Restart Action

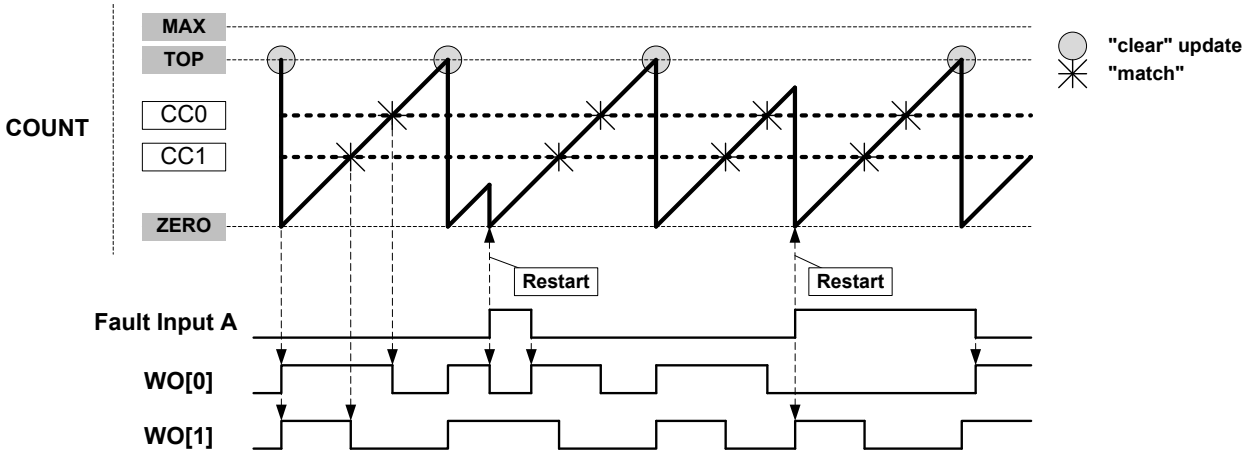
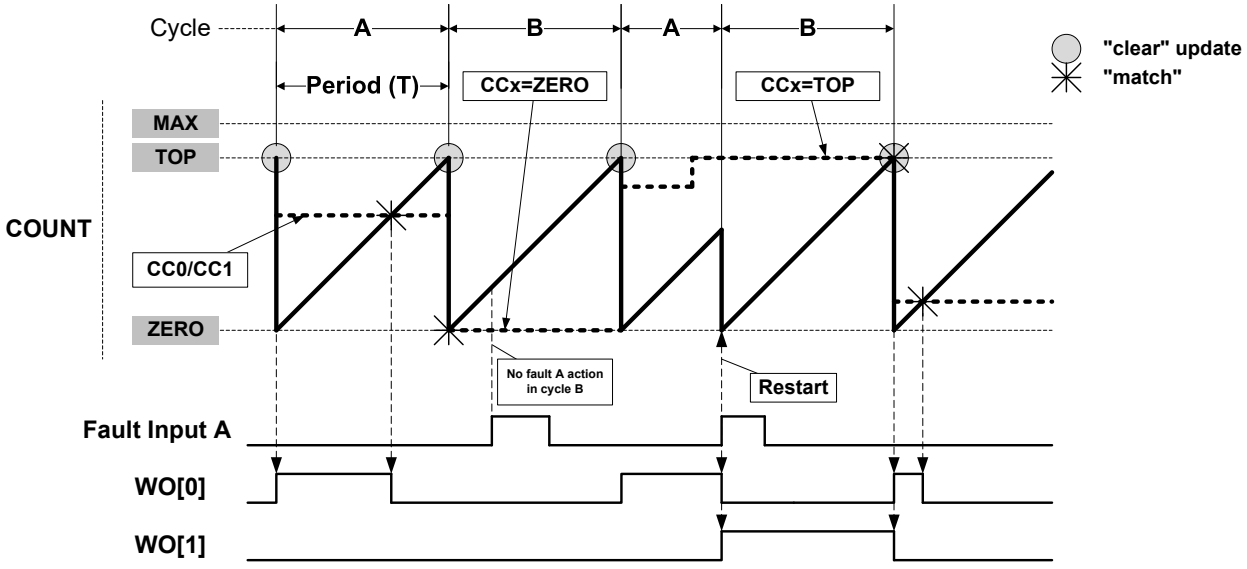


Figure 49-27. Waveform Generation in RAMP2 mode with Restart Action



Capture Action

Several capture actions can be selected by writing the Fault n Capture Action bits in the Fault n Control register (FCTRLn.CAPTURE). When one of the capture operations is selected, the counter value is captured when the fault occurs. These capture operations are available:

- CAPT - the equivalent to a standard capture operation, for further details refer to 49.6.2.7 Capture Operations
- CAPTMIN - gets the minimum time stamped value: on each new local minimum captured value, an event or interrupt is issued.
- CAPTMAX - gets the maximum time stamped value: on each new local maximum captured value, an event or interrupt (IT) is issued, see Figure 49-28.
- LOCMIN - notifies by event or interrupt when a local minimum captured value is detected.
- LOCMAX - notifies by event or interrupt when a local maximum captured value is detected.
- DERIV0 - notifies by event or interrupt when a local extreme captured value is detected, see Figure 49-29.

limiting resistor is calculated as R = |(GND - 0.6V - V_{PIN}) / Inj2|. If V_{PIN} is greater than V_{DD} + 0.6V, a current limiting resistor is required. The positive DC injection current limiting resistor is calculated as R = (V_{PIN} - (V_{DD} + 0.6)) / Inj2.

54.5 Supply Characteristics

Table 54-4. Supply Characteristics

Symbol	Conditions	Voltage		
		Min.	Max.	Units
V_{DDIO}	Full Voltage Range	1.71	3.63	V
V_{DDIOB}				
V_{DDANA}				
V_{BAT}				

Table 54-5. Supply Rates(1)

Symbol	Conditions	Fall Rate	Rise Rate		Units
		Max.	Min.	Max.	
V_{DDIO}	DC Supply Peripheral I/Os, Internal Regulator, and Analog Supply Voltage	50	0.2	100	mV/µs
V_{DDIOB}					
V_{DDANA}					
V_{BAT}					

Note: 1. These values are based on simulation. They are not covered by production test limits or characterization.

Table 54-6. Power Supply Current Requirement

Symbol	Conditions	Current	Units
		Max	
I_{input}	Power-up Maximum Current	7	mA

Note: I_{input} is the minimum requirement for the power supply connected to the device.

56. Schematic Checklist

56.1 Introduction

This chapter describes a common checklist which should be used when starting and reviewing the schematics for a SAM D5x/E5x design. This chapter illustrates recommended power supply connections, how to connect external analog references, programmer, debugger, oscillator and crystal.

56.1.1 Operation in Noisy Environment

If the device is operating in an environment with much electromagnetic noise, it must be protected from this noise to ensure reliable operation. In addition to following best practice EMC design guidelines, the recommendations listed in the schematic checklist sections must be followed. In particular, placing decoupling capacitors very close to the power pins, an RC-filter on the $\overline{\text{RESET}}$ pin, and a pull-up resistor on the SWCLK pin is critical for reliable operations. It is also relevant to eliminate or attenuate noise in order to avoid that it reaches supply pins, I/O pins and crystals.

56.2 Power Supply

The SAM D5x/E5x supports a single or dual power supply from 1.71V to 3.63V. The same voltage must be applied to both VDDIO and VDDANA. VDDIOB level must be lower or equal to VDDIO / VDDANA.

When I/O pads in the VDDIOB cluster are multiplexed as analog pads, VDDANA is used to power the I/O. Using this configuration may result in an electrical conflict if the VDDIOB voltage is different from that of VDDIO / VDDANA. If the application has such requirements, it is required to power VDDIOB, VDDIO, and VDDANA from the same supply source to ensure that they are always at the same voltage.

The internal voltage regulator has four different modes:

- Linear mode: This mode does not require any external inductor. This is the default mode when CPU and peripherals are running
- Switching mode (Buck): The most efficient mode when the CPU and peripherals are running.
- Low Power (LP) mode: This is the default mode used when the device is in Standby mode
- Shutdown mode: When the device is in Backup mode, the internal regulator is turned off

Selecting between switching mode and linear mode can be done by software on the fly, but the power supply must be designed according to which mode is to be used.

56.2.1 Power Supply Connections

The following figures shows the recommended power supply connections for switched/linear mode, linear mode only and with battery backup.