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What is "Embedded - Microcontrollers"?

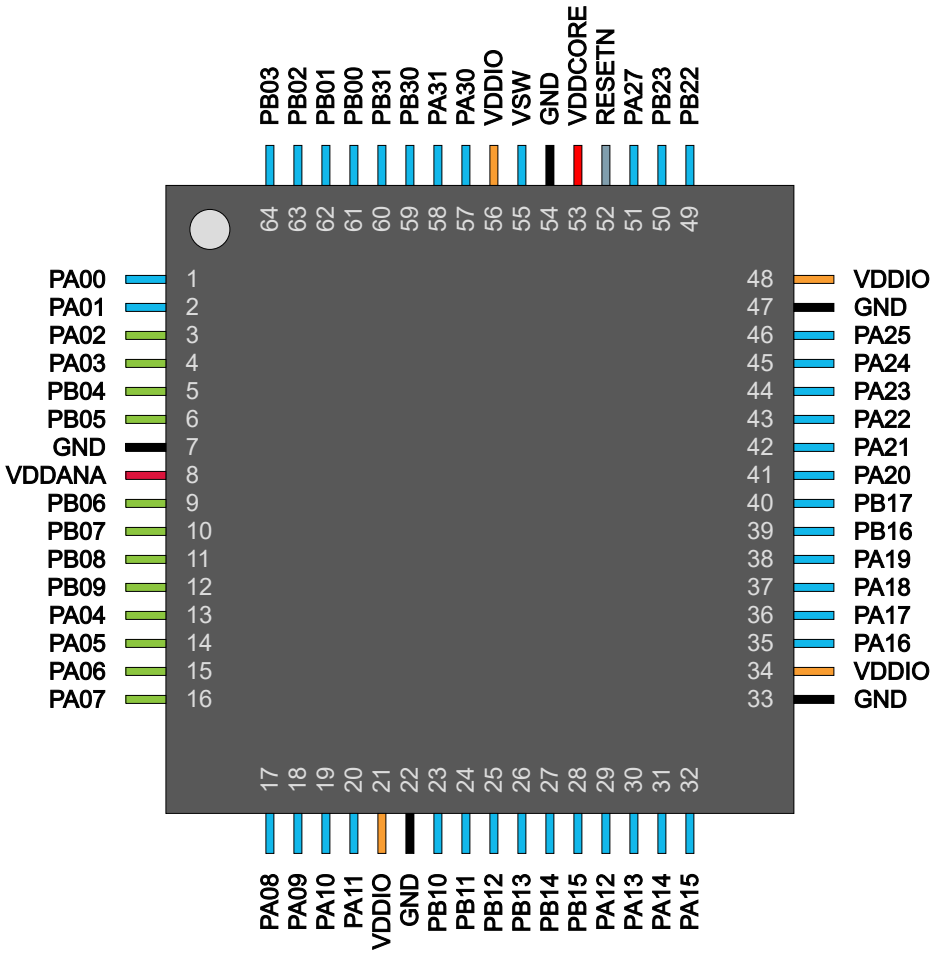
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4F
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, EBI/EMI, I²C, IrDA, LINbus, MMC/SD, QSPI, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM
Number of I/O	81
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	192K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.63V
Data Converters	A/D 28x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atsame51n19a-aut

4.2 Pin Count 64 (J)

Figure 4-1. 64-Pin TQFP and QFN Package



Module	Source	Line
	OVR 3	
	EVD 4..11	40
	OVR 4..11	
PAC - Peripheral Access Controller	ERR	41
RAM ECC	0	45
	1	
SERCOM0 - Serial Communication Interface 0(1)	0	46
	1	47
	2	48
	3	49
	4	
	5	
	6	
SERCOM1 - Serial Communication Interface 1(1)	0	50
	1	51
	2	52
	3	53
	4	
	5	
	6	
SERCOM2 - Serial Communication Interface 2(1)	0	54
	1	55
	2	56
	3	57
	4	
	5	
	6	
SERCOM3 - Serial Communication Interface 3(1)	0	58
	1	59
	2	60
	3	61
	4	

Module	Source	Line
SDHC1 - SD/MMC Host Controller 1	SDHC1	136
	TIMER	

Note:

1. The integer number specified in the source refers to the respective bit position in the INTFLAG register of respective peripheral.

Note: Lines not listed here are reserved.

10.3 High-Speed Bus System

10.3.1 Features

High-Speed Bus Matrix has the following features:

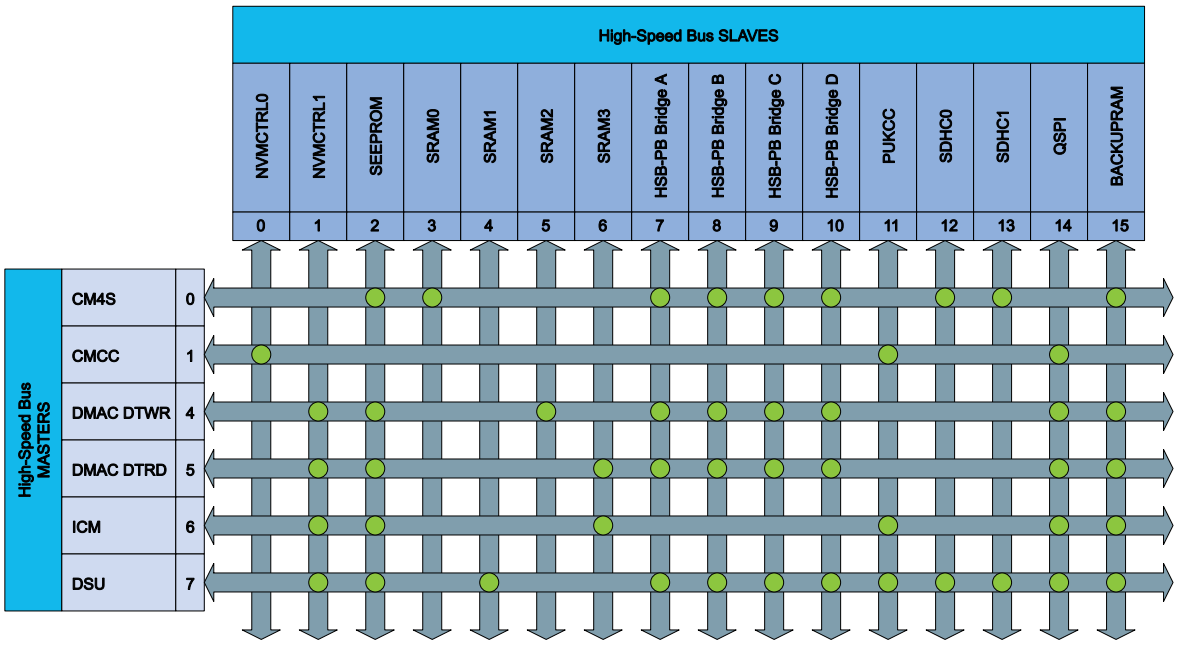
- Symmetric crossbar bus switch implementation
- Allows concurrent accesses from different masters to different slaves
- 32-bit data bus
- Operation at a one-to-one clock frequency with the bus masters

FlexRAM Memory has the following features:

- Unified System Memory area
- Allows concurrent accesses from different masters
- Offers privileged accesses from specific masters

10.3.2 Configuration

Figure 10-1. Master-Slave Relations High-Speed Bus Matrix



12.13.14 Peripheral Identification 4

Name: PID4
Offset: 0x1FD0
Reset: 0x00000000
Property: -

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
	FKBC[3:0]				JEPCC[3:0]			
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 7:4 – FKBC[3:0] 4KB Count
These bits will always return zero when read, indicating that this debug component occupies one 4KB block.

Bits 3:0 – JEPCC[3:0] JEP-106 Continuation Code
These bits will always return zero when read.

13.6 Power Consumption vs. Speed

When targeting for either a low-power or a fast acting system, some considerations have to be taken into account due to the nature of the asynchronous clocking of the peripherals:

If clocking a peripheral with a very low clock, the active power consumption of the peripheral will be lower. At the same time the synchronization to the synchronous (CPU) clock domain is dependent on the peripheral clock speed, and will take longer with a slower peripheral clock. This will cause worse response times and longer synchronization delays.

13.7 Clocks after Reset

On any Reset the synchronous clocks start to their initial state:

- DFLL48M is enabled and configured to run at 48MHz
- Generic Generator 0 uses DFLL48M as source and generates GCLK_MAIN
- CPU and BUS clocks are undivided

On a Power-on Reset, the 32KHz clock sources are reset and the GCLK module starts to its initial state:

- All Generic Clock Generators are disabled except
  - Generator 0 is using DFLL48M at 48MHz as source and generates GCLK_MAIN
- All Peripheral Channels in GCLK are disabled.

On a User Reset the GCLK module starts to its initial state, except for:

- Generic Clocks that are write-locked, i.e., the according WRTLOCK is set to 1 prior to Reset

Related Links

16. RSTC – Reset Controller

18.8.7 Standby Configuration

Name: STDBYCFG
Offset: 0x08
Reset: 0x00
Property: PAC Write-Protection

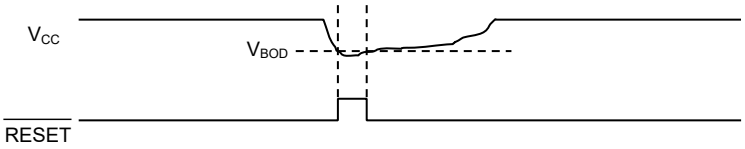
Bit	7	6	5	4	3	2	1	0
			FASTWKUP[1:0]				RAMCFG[1:0]	
Access			R/W	R/W			R/W	R/W
Reset			0	0			0	0

Bits 5:4 – FASTWKUP[1:0] Fast Wakeup

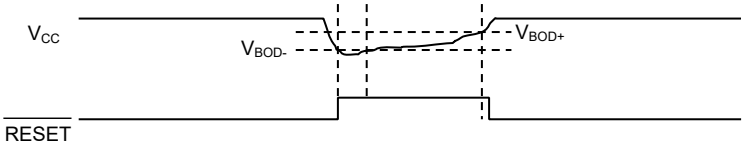
Value	Name	Description
0x0	NO	Fast Wakeup is disabled.
0x1	NVM	Fast Wakeup is enabled on NVM.
0x2	MAINVREG	Fast Wakeup is enabled on the main voltage regulator (MAINVREG).
0x3	BOTH	Fast Wakeup is enabled on both NVM and MAINVREG..

Bits 1:0 – RAMCFG[1:0] RAM Configuration

Value	Name	Description
0x0	RET	In standby mode, all the system RAM is retained.
0x1	PARTIAL	In standby mode, only the first 32Kbytes of the system RAM is retained.
0x2	OFF	In standby mode, all the system RAM is turned OFF.
0x3	Reserved	Reserved.



Hysteresis ON:



Enabling the BOD33 hysteresis by writing the Hysteresis bit field in the BOD33 register (BOD33.HYST) to a non-null value will add hysteresis to the BOD33 threshold level.

The hysteresis functionality can be used in Sampling Mode.

Related Links

9.4 NVM User Page Mapping

19.6.5.3.4 Standby Sleep Mode

The BOD33 can be used in standby mode if the BOD is enabled and the Run in Standby bit is written to '1' (BOD33.RUNSTDBY).

It is set in Low Power mode if the BOD33.STDBYCFG bit is written to '1'.

Related Links

9.4 NVM User Page Mapping

19.6.5.3.5 Backup and Hibernate sleep Modes

To enable the BOD33 in Backup or Hibernate sleep mode, the Run in Backup or Hibernate sleep mode bits in the BOD33 register (BOD33.RUNBKUP, BOD33.RUNHIB) must be written to '1'. The BOD33 is automatically set in BOD33 Ultra Low-Power mode. Additionnaly, the BOD33 will operate in Sampling mode if the BOD33.PSEL bit is non-null. In this state, the voltage monitored by BOD33 is always the supply of the backup domain, i.e. VDD or VBAT.

Related Links

9.4 NVM User Page Mapping

19.6.5.4 1.2V Brown-Out Detector (BOD12)

The BOD12 is calibrated in production and its calibration configuration is stored in the NVM User Row. This configuration must not be changed to assure the correct behavior of the BOD12. The BOD12 generates a reset when 1.2V crosses below the preset brown-out level. The BOD12 is always disabled in Standby, Hibernate, and Backup Sleep modes.

Related Links

9.4 NVM User Page Mapping

19.6.5.4.1 BOD12 Continuous Mode

Continuous mode is the default mode for BOD12.

The *BOD12* is continuously monitoring the VDDCORE supply voltage if it is enabled (BOD12.ENABLE = 1), and if the BOD12 Configuration bit in the BOD12 register is cleared (BOD12.ACTCFG = 0 for Active mode and BOD12.STDBYCFG = 0 for Standby mode).

initial checksum value (CHKINIT) stored in the Block Transfer Destination Address register (DSTADDR). The DMA read and calculate the checksum over the data from the source address.When the checksum calculation is completed, the CRC value is stored in the CRC Checksum register (CRCCHKSUM), the Transfer Complete interrupt flag is set (CHINTFLAGn.TCMPL) and optional interrupt is generated.

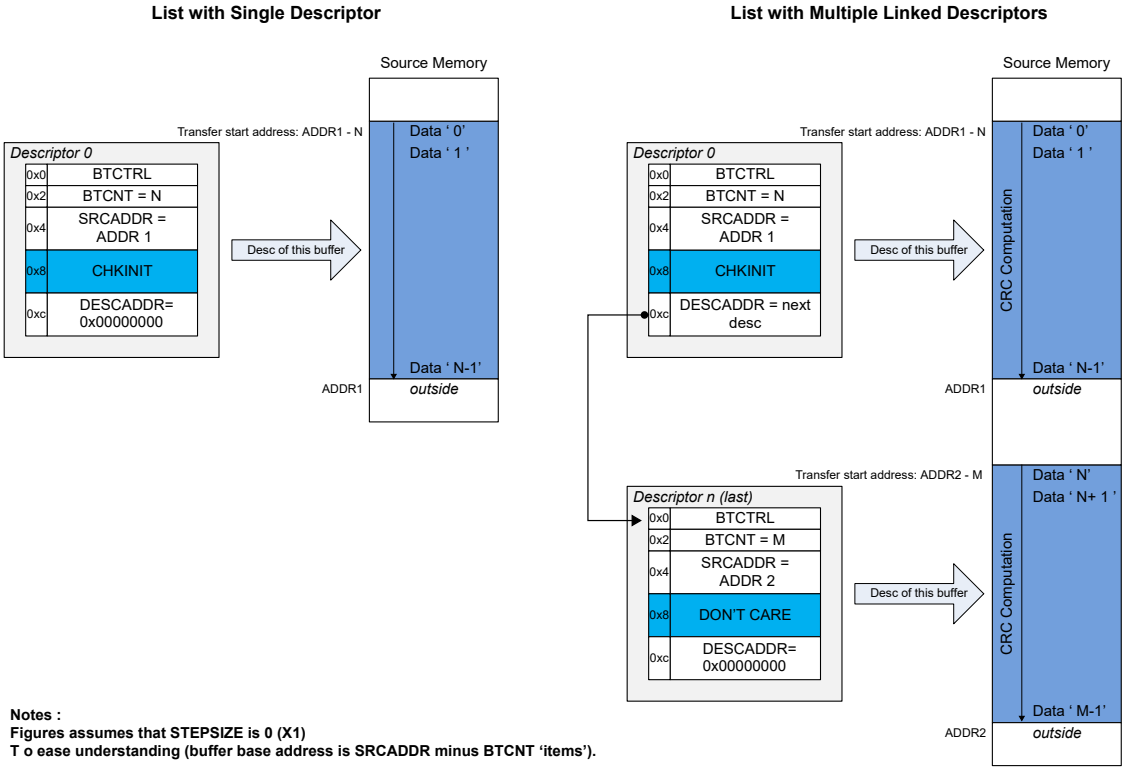
If linked descriptor is in the list (DESCADDR !=0), the DMA will fetch the next descriptor and CRC calculation continues as described above. When the last list descriptor is executed, the channel is automatically disabled.

In order to enable the memory CRC generation, the following actions must be performed:

1. The CRC module must be set to be used with a DMA channel (CRCCTRL.CRCSRC)
2. Reserve memory space addresses to configure a descriptor or a list of descriptors
3. Configure each descriptor:
   – Set the next descriptor address (DESCADDR)
   – Set the destination address with the initial checksum value (DSTADDR = CHKINIT) in the first descriptior in a list
   – Set the transfer source address (SRCADDR)
   – Set the block transfer count (BTCNT)
   – Set the memory CRC generation operation mode (CRCCTRL.CRCMODE = CRCGEN)
   – Enable optional interrupts
4. Enable the corresponding DMA channel (CHCTRLAn.ENABLE)

The figure below shows the CRC computation slots and descriptor configuration when single or linked-descriptors transfers are enabled.

Figure 22-20. CRC Computation with Single Linked Transfers



Bit 2 – RLE Retry Limit Exceeded
This bit is cleared by writing a '1' to it.

Bit 1 – COL Collision Occurred
When operating in 10/100Mbps mode, this bit is set by the assertion of either a collision or a late collision.

This bit is cleared by writing a '1' to it.

Bit 0 – UBR Used Bit Read
This bit is set when a transmit buffer descriptor is read with its used bit set.

This bit is cleared by writing a '1' to it.

30. FREQM – Frequency Meter

30.1 Overview

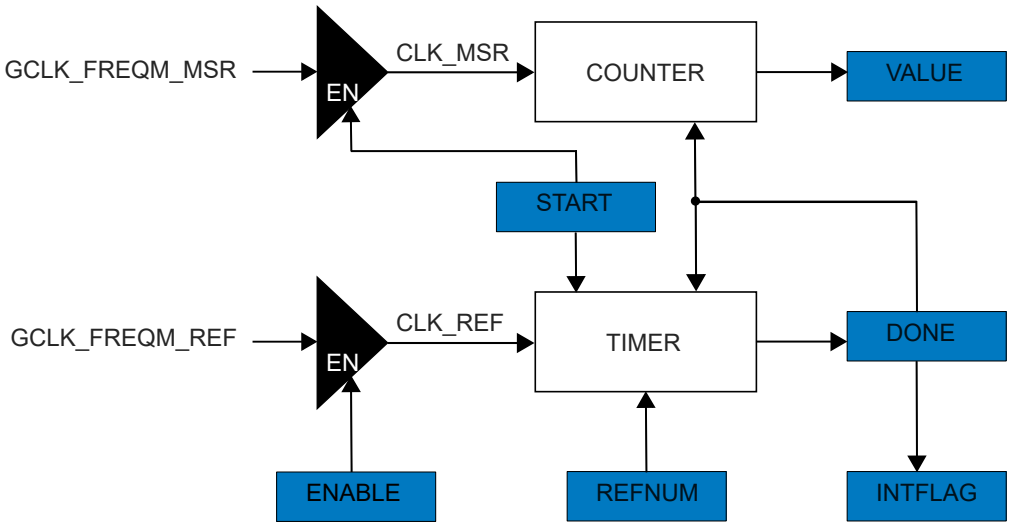
The Frequency Meter (FREQM) can be used to accurately measure the frequency of a clock by comparing it to a known reference clock.

30.2 Features

- Ratio can be measured with 24-bit accuracy
- Accurately measures the frequency of an input clock with respect to a reference clock
- Reference clock can be selected from the available GCLK_FREQM_REF sources
- Measured clock can be selected from the available GCLK_FREQM_MSR sources

30.3 Block Diagram

Figure 30-1. FREQM Block Diagram



30.4 Signal Description

Not applicable.

30.5 Product Dependencies

In order to use this peripheral, other parts of the system must be configured correctly, as described below.

35.8.1 Control A

Name: CTRLA
Offset: 0x00
Reset: 0x00000000
Property: PAC Write-Protection, Enable-Protected

Bit	31	30	29	28	27	26	25	24
		DORD	CPOL	CPHA	FORM[3:0]			
Access		R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset		0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
			DIPO[1:0]				DOPO[1:0]	
Access			R/W	R/W			R/W	R/W
Reset			0	0			0	0

Bit	15	14	13	12	11	10	9	8
								IBON
Access								R/W
Reset								0

Bit	7	6	5	4	3	2	1	0
	RUNSTDBY			MODE[2:0]			ENABLE	SWRST
Access	R/W			R/W	R/W	R/W	R/W	R/W
Reset	0			0	0	0	0	0

Bit 30 – DORD Data Order
This bit selects the data order when a character is shifted out from the shift register.

This bit is not synchronized.

Value	Description
0	MSB is transferred first.
1	LSB is transferred first.

Bit 29 – CPOL Clock Polarity
In combination with the Clock Phase bit (CPHA), this bit determines the SPI transfer mode.

This bit is not synchronized.

Value	Description
0	SCK is low when idle. The leading edge of a clock cycle is a rising edge, while the trailing edge is a falling edge.
1	SCK is high when idle. The leading edge of a clock cycle is a falling edge, while the trailing edge is a rising edge.

Bit 28 – CPHA Clock Phase
In combination with the Clock Polarity bit (CPOL), this bit determines the SPI transfer mode.

DOPO	DO	SCK	Slave $\overline{SS}$	Master $\overline{SS}$
0x0	PAD[0]	PAD[1]	PAD[2]	System configuration
0x1	Reserved			
0x2	PAD[3]	PAD[1]	PAD[2]	System configuration
0x3	Reserved			

Bit 8 – IBON Immediate Buffer Overflow Notification
This bit controls when the buffer overflow status bit (STATUS.BUFOVF) is set when a buffer overflow occurs.

This bit is not synchronized.

Value	Description
0	STATUS.BUFOVF is set when it occurs in the data stream.
1	STATUS.BUFOVF is set immediately upon buffer overflow.

Bit 7 – RUNSTDBY Run In Standby
This bit defines the functionality in standby sleep mode.

These bits are not synchronized.

RUNSTDBY	Slave	Master
0x0	Disabled. All reception is dropped, including the ongoing transaction.	Generic clock is disabled when ongoing transaction is finished. All interrupts can wake up the device.
0x1	Ongoing transaction continues, wake on Receive Complete interrupt.	Generic clock is enabled while in sleep modes. All interrupts can wake up the device.

Bits 4:2 – MODE[2:0] Operating Mode
These bits must be written to 0x2 or 0x3 to select the SPI serial communication interface of the SERCOM.

0x2: SPI slave operation

0x3: SPI master operation

These bits are not synchronized.

Bit 1 – ENABLE Enable
Due to synchronization, there is delay from writing CTRLA.ENABLE until the peripheral is enabled/disabled. The value written to CTRL.ENABLE will read back immediately and the Synchronization Enable Busy bit in the Synchronization Busy register (SYNCBUSY.ENABLE) will be set. SYNCBUSY.ENABLE is cleared when the operation is complete.

This bit is not enable-protected.

Value	Description
0	The peripheral is disabled or being disabled.
1	The peripheral is enabled or being enabled.

38.8.5.2 Host Start-of-Frame Control

Name: HSOFC
Offset: 0x0A
Reset: 0x00
Property: PAC Write-Protection

During a very short period just before transmitting a Start-of-Frame, this register is locked. Thus, after writing, it is recommended to check the register value, and write this register again if necessary. This register is cleared upon a USB reset.

Bit	7	6	5	4	3	2	1	0
	FLENCE				FLENC[3:0]			
Access	R/W				R/W	R/W	R/W	R/W
Reset	0				0	0	0	0

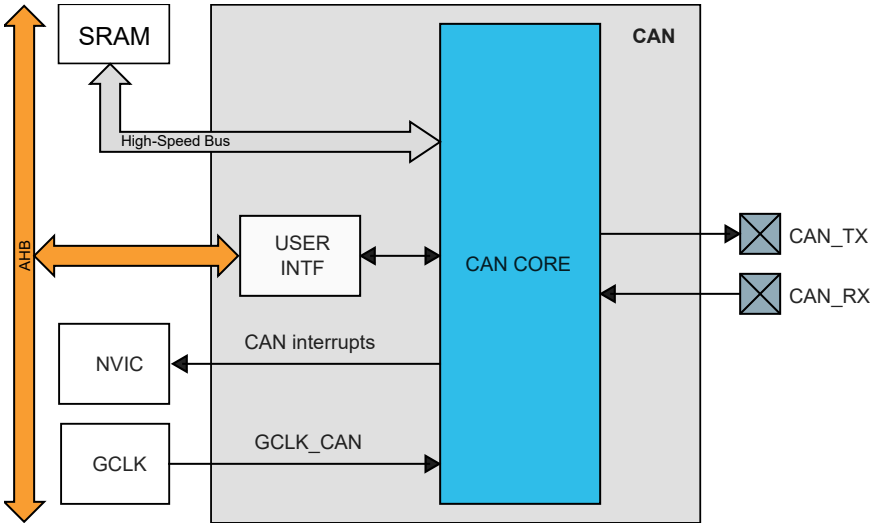
Bit 7 – FLENCE Frame Length Control Enable
When this bit is '1', the time between Start-of-Frames can be tuned by up to +/-0.06% using FLENC[3:0].
Note: In Low Speed mode, FLENCE must be '0'.

Value	Description
0	Start-of-Frame is generated every 1ms.
1	Start-of-Frame generation depends on the signed value of FLENC[3:0]. USB Start-of-Frame period equals 1ms + (FLENC[3:0]/12000)ms

Bits 3:0 – FLENC[3:0] Frame Length Control
These bits define the signed value of the 4-bit FLENC that is added to the Internal Frame Length when FLENCE is '1'. The internal Frame length is the top value of the frame counter when FLENCE is zero.

39.3 Block Diagram

Figure 39-1. CAN Block Diagram



39.4 Signal Description

Table 39-1. Signal Description

Signal	Description	Type
CAN_TX	CAN transmit	Digital output
CAN_RX	CAN receive	Digital input

Refer to for details on the pin mapping for this peripheral. One signal can be mapped to one of several pins.

39.5 Product Dependencies

In order to use this peripheral, other parts of the system must be configured correctly, as described below.

39.5.1 I/O Lines

Using the CAN's I/O lines requires the I/O pins to be configured.

Related Links

32. PORT - I/O Pin Controller

39.5.2 Power Management

The CAN will continue to operate in any Idle Sleep mode where the selected source clock is running. The CAN interrupts can be used to wake up the device from sleep modes. Refer to the Power Manager chapter for details on the different sleep modes.

The CAN module has its own Low-Power mode. The clock sources cannot be halted while the CAN is enabled unless this mode is used. Refer to the section "Sleep Mode Operation" for additional information.

Related Links

- For the Setup:
  - RLength = 64bytes
  - CnsLength = u2ModLength +12
- For the Fast Reduction and Normalize:
  - RLength = u2ModLength +4
  - CnsLength = u2ModLength +8
- For the BigRedMod:
  - RLength = u2ModLength +4
  - CnsLength =64

The following combinations of input values should be avoided in the case of a modular reduction ‘alone’, meaning that it has not been requested as an option of any other command:

- nu1ModBase, nu1CnsBase, nu1RBase, nu1XBase are not aligned on 32-bit boundaries
- {nu1ModBase, u2ModLength + 4}, {nu1CnsBase, u2CnsLength}, {nu1XBase, 2*u2XLength + 8 + s} or {nu1RBase, u2RLength} are not in Crypto RAM
- u2ModLength is either: < 4, > 0xffc or not a 32-bit length
- Overlaps exist between two or more of the areas: {nu1ModBase, u2ModLength + 4},{nu1CnsBase, u2CnsLength}, {nu1XBase, 2*u2XLength + 8 + s} or {nu1RBase, u2RLength}

Note: Overlaps between {nu1RBase, RLength} and {nu1XBase, 2*u2XLength + 8} are forbidden; but if the operation is the Fast, Normalized or Big Modular Reduction, the equality between nu1RBase and nu1XBase is authorized.

43.3.5.1.13 Status Returned Values

Table 43-49. RedMod Service Return Codes

Returned Status	Importance	Meaning
PUKCL_OK	–	Service functioned correctly
PUKCL_DIVISION_BY_ZERO	Severe	When computing an Euclidean division, the Modulus was found to be zero. This occurs ONLY when either reducing using an Euclidean division or computing the reduction constant usable for a Fast or Normalize Reduction.
PUKCL_UNEXPLOITABLE_OPTIONS	Severe	A bad combination of options has been detected.
PUKCL_MALFORMED_MODULUS	Severe	The Msw of the modulus is not zero.

43.3.5.2 Modular Exponentiation (Without CRT)

43.3.5.2.1 Purpose

This service is used to perform the Modular Exponentiation computation. This service processes integers in GF(p) only.

The options available for this service are:

- Fast implementation
- Regular implementation
- Exponent is located in Crypto RAM or not in Crypto RAM
- Exponent window size

43.3.6.2.4 Parameters Definition

Table 43-68. ZpEccAddFast Service Parameters

Parameter	Type	Direction	Location	Data Length	Before Executing the Service	After Executing the Service
nu1ModBase	nu1	I	Crypto RAM	u2ModLength + 4	Base of Modulus P	Base of Modulus P
nu1CnsBase	nu1	I	Crypto RAM	u2ModLength + 8	Base of Cns	Base of Cns
u2ModLength	u2	I	–	–	Length of modulo	Length of modulo
nu1PointABase	nu1	I/O	Crypto RAM	3*u2ModLength + 12	Input point A (projective coordinates)	Resulting point C (projective coordinates)
nu1PointBBase	nu1	I	Crypto RAM	3*u2ModLength + 12	Input point B (projective coordinates)	Input point B
nu1Workspace	nu1	I	Crypto RAM	5*u2ModLength + 32	–	Corrupted workspace

43.3.6.2.5 Code Example

```
PUKCL_PARAM PUKCLParam;
PPUKCL_PARAM pvPUKCLParam = &PUKCLParam;

PUKCL (u2Option) = 0;

PUKCL _ZpEccAdd(nu1ModBase) = <Base of the ram location of P>;
PUKCL _ZpEccAdd(nu1CnsBase) = <Base of the ram location of Cns>;
PUKCL _ZpEccAdd(u2ModLength) = <Byte length of P>;
PUKCL _ZpEccAdd(nu1PointABase) = <Base of the ram location of the A point>;
PUKCL _ZpEccAdd(nu1PointBBase) = <Base of the ram location of the B point>;
PUKCL _ZpEccAdd(nu1Workspace) = <Base of the ram location of the workspace>;
...

// vPUKCL_Process() is a macro command, which populates the service name
// and then calls the library...
vPUKCL_Process(ZpEccAddFast,&PUKCLParam);
if (PUKCL (u2Status) == PUKCL_OK)
            {
            ...
            }
else // Manage the error
```

43.3.6.2.6 Constraints

No overlapping between either input and output are allowed. The following conditions must be avoided to ensure that the service works correctly:

- nu1ModBase, nu1CnsBase, nu1PointABase, nu1PointBBase, nu1Workspace are not aligned on 32-bit boundaries
- {nu1ModBase, u2ModLength + 4}, {nu1CnsBase, u2ModLength + 8}, {nu1PointABase, 3*u2ModLength + 12}, {nu1PointBBase, 3*u2ModLength + 12}, {nu1Workspace, <WorkspaceLength>} are not in Crypto RAM
- u2ModLength is either: < 12, > 0xffc or not a 32-bit length

46.8.12 Comparator Control n

Name: COMPCTRL
Offset: 0x10 + n*0x04 [n=0..1]
Reset: 0x00000000
Property: PAC Write-Protection

Bit	31	30	29	28	27	26	25	24
			OUT[1:0]			FLEN[2:0]		
Access			R/W	R/W		R/W	R/W	R/W
Reset			0	0		0	0	0

Bit	23	22	21	20	19	18	17	16
			HYST[1:0]		HYSTEN		SPEED[1:0]	
Access			R/W	R/W	R/W		R/W	R/W
Reset			0	0	0		0	0

Bit	15	14	13	12	11	10	9	8
	SWAP	MUXPOS[2:0]				MUXNEG[2:0]		
Access	R/W	R/W	R/W	R/W		R/W	R/W	R/W
Reset	0	0	0	0		0	0	0

Bit	7	6	5	4	3	2	1	0
		RUNSTDBY		INTSEL[1:0]		SINGLE	ENABLE	
Access		R/W		R/W	R/W	R/W	R/W	
Reset		0		0	0	0	0	

Bits 29:28 – OUT[1:0] Output
These bits configure the output selection for comparator n. COMPCTRLn.OUT can be written only while COMPCTRLn.ENABLE is zero.

Note: For internal use of the comparison results by the CCL, this bit must be 0x1 or 0x2.

These bits are not synchronized.

Value	Name	Description
0x0	OFF	The output of COMPn is not routed to the COMPn I/O port
0x1	ASYNC	The asynchronous output of COMPn is routed to the COMPn I/O port
0x2	SYNC	The synchronous output (including filtering) of COMPn is routed to the COMPn I/O port
0x3	N/A	Reserved

Bits 26:24 – FLEN[2:0] Filter Length
These bits configure the filtering for comparator n. COMPCTRLn.FLEN can only be written while COMPCTRLn.ENABLE is zero.

These bits are not synchronized.

- Control B Clear and Control B Set registers (CTRLBCLR and CTRLBSET)
- Status register (STATUS)
- Prescaler and Prescaler Buffer registers (PRESC and PRESCBUF)
- Compare Value x and Compare Value x Buffer registers (CCx and CCBUFx)
- Filter Value and Filter Buffer Value registers (FILTER and FILTERBUF)
- Counter Value register (COUNT)

Required write-synchronization is denoted by the "Write-Synchronized" property in the register description.

The following registers are synchronized when read:

- Counter Value register (COUNT): the synchronization is done on demand through READSYNC software command (CTRLBSET.CMD)

Required read-synchronization is denoted by the "Read-Synchronized" property in the register description.

Related Links

13.3 Register Synchronization

Mode	Conditions	VDD	Ta	Typ.	Max.	Units	
	+VDDANA consumption No backup RAM retained (PM.BKUPCFG.BRAMCFG = 0x2)	3.3V		3.3	43.6		
	Powered by VDDIO, no RTC running VDDIO+VDDANA consumption 4 KB backup RAM retained (PM.BKUPCFG.BRAMCFG = 0x1)	1.8V		2.4	48.4		
		3.3V		2.8	49.1		
	Powered by VDDIO, no RTC running VDDIO+VDDANA consumption 8 KB backup RAM retained (PM.BKUPCFG.BRAMCFG = 0x0)	1.8V		2.7	55.1		
		3.3V		3.1	55.8		
OFF		1.8V		0.191	2.30	µA	
		3.3V		0.331	3.35		

54.8 Wake-Up Time

Conditions:

- V_{DD} = 3.3V
- LDO Regulation mode (default mode)
- CPU clock = DFLL48 in open loop (default configuration)
- NVM automatic wait state and cache enabled (default configuration)

Measurement Methods

For IDLE and STANDBY, the exit of mode is done through asynchronous EIC wake-up. The wake-up time is measured between the toggle of the EIC pin and the set of the IO pin done by the first executed instructions in EIC interrupt handler.

For Backup and hibernate, the exit of mode is done through RTC wake-up. The wake-up time is measured between the toggle of the RTC pin (SUPC_BKOUT_RTCTGL) and the set of the IO done by the first executed instructions after reset.

For OFF mode, the exit of mode is done through Reset pin, the time is measured between the rising edge of the RESETN signal and the set of the IO done by the first executed instructions after Reset.

Table 54-13. Wake-Up Timing

Sleep Mode	Conditions	Typ	Unit
IDLE		230	ns
STANDBY	STDBYCFG.FASTWKUP = 0	110	µs
	STDBYCFG.FASTWKUP = 1 Fast Wakeup is enabled on NVM.	92	µs

Figure 56-6. External Analog Reference Schematic With One Reference

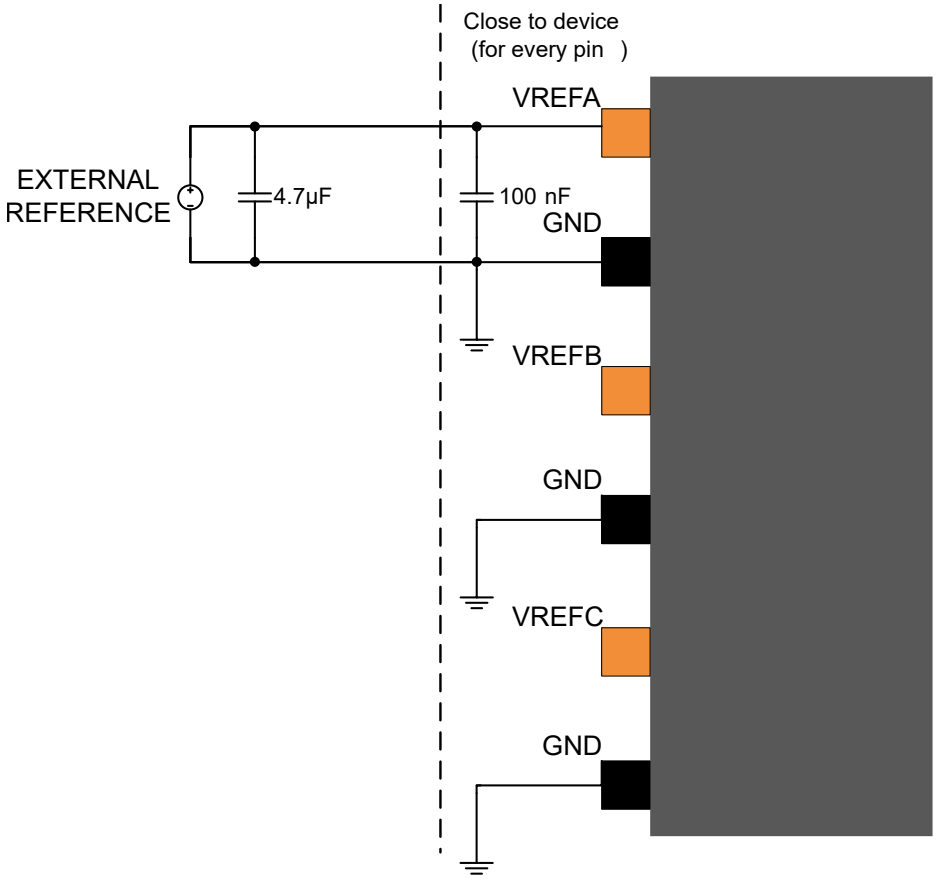


Table 56-2. External Analog Reference Connections

Signal Name	Recommended Pin Connection	Description
VREFx	1.0V to (V_{DDANA} - 0.6V) for ADC 1.0V to (V_{DDANA} - 0.6V) for DAC Decoupling/filtering capacitors 100nF(1)(2) and 4.7µF(1)	External reference VREFx for the analog port
GND		Ground

1. These values are only given as a typical example.

2. Decoupling capacitor should be placed close to the device for each supply pin pair in the signal group.

56.4 External Reset Circuit

When the external Reset function is used, connect the external Reset circuit to the $\overline{\text{RESET}}$ pin as shown below. If the external Reset function is not required, the circuit is not necessary: the $\overline{\text{RESET}}$ pin can either remain unconnected, or be driven LOW externally by the application circuitry.

The Reset switch can also be removed if a manual Reset is not necessary. The $\overline{\text{RESET}}$ pin itself has an internal pull-up resistor, hence it is optional to add any external pull-up resistor.