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Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	32MHz
Connectivity	I ² C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	6
Program Memory Size	3.5KB (2K x 14)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 5.5V
Data Converters	A/D 5x10b; D/A 1x5b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	8-SOIC (0.154", 3.90mm Width)
Supplier Device Package	8-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16f15313-i-sn

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

FIGURE 1-2: PIC16(L)F15323 BLOCK DIAGRAM



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2.0 GUIDELINES FOR GETTING STARTED WITH PIC16(L)F15313/23 MICROCONTROLLERS

2.1 Basic Connection Requirements

Getting started with the PIC16(L)F15313/23 family of 8bit microcontrollers requires attention to a minimal set of device pin connections before proceeding with development.

The following pins must always be connected:

All VDD and VSS pins (see Section 2.2 "Power Supply Pins")
MCLR pin

(see Section 2.3 "Master Clear (MCLR) Pin")

These pins must also be connected if they are being used in the end application:

- ICSPCLK/ICSPDAT pins used for In-Circuit Serial Programming[™] (ICSP[™]) and debugging purposes (see **Section 2.4 "ICSP[™] Pins**")
- OSCI and OSCO pins when an external oscillator source is used

(see Section 2.5 "External Oscillator Pins")

Additionally, the following pins may be required:

• VREF+/VREF- pins are used when external voltage reference for analog modules is implemented

The minimum mandatory connections are shown in Figure 2-1.

FIGURE 2-1: RECOMMENDED MINIMUM CONNECTIONS

2.2 Power Supply Pins

2.2.1 DECOUPLING CAPACITORS

The use of decoupling capacitors on every pair of power supply pins (VDD and VSS) is required.

Consider the following criteria when using decoupling capacitors:

- Value and type of capacitor: A 0.1 μ F (100 nF), 10-25V capacitor is recommended. The capacitor should be a low-ESR device, with a resonance frequency in the range of 200 MHz and higher. Ceramic capacitors are recommended.
- Placement on the printed circuit board: The decoupling capacitors should be placed as close to the pins as possible. It is recommended to place the capacitors on the same side of the board as the device. If space is constricted, the capacitor can be placed on another layer on the PCB using a via; however, ensure that the trace length from the pin to the capacitor is no greater than 0.25 inch (6 mm).
- Handling high-frequency noise: If the board is experiencing high-frequency noise (upward of tens of MHz), add a second ceramic type capacitor in parallel to the above described decoupling capacitor. The value of the second capacitor can be in the range of 0.01 μ F to 0.001 μ F. Place this second capacitor next to each primary decoupling capacitor. In high-speed circuit designs, consider implementing a decade pair of capacitances as close to the power and ground pins as possible (e.g., 0.1 μ F in parallel with 0.001 μ F).
- Maximizing performance: On the board layout from the power supply circuit, run the power and return traces to the decoupling capacitors first, and then to the device pins. This ensures that the decoupling capacitors are first in the power chain. Equally important is to keep the trace length between the capacitor and the power pins to a minimum, thereby reducing PCB trace inductance.

2.2.2 TANK CAPACITORS

On boards with power traces running longer than six inches in length, it is suggested to use a tank capacitor for integrated circuits, including microcontrollers, to supply a local power source. The value of the tank capacitor should be determined based on the trace resistance that connects the power supply source to the device, and the maximum current drawn by the device in the application. In other words, select the tank capacitor so that it meets the acceptable voltage sag at the device. Typical values range from 4.7 μ F to 47 μ F.

4.5 Stack

All devices have a 16-level x 15-bit wide hardware stack (refer to Figure 4-4 through Figure 4-7). The stack space is not part of either program or data space. The PC is PUSHed onto the stack when CALL or CALLW instructions are executed or an interrupt causes a branch. The stack is POPed in the event of a RETURN, RETLW or a RETFIE instruction execution. PCLATH is not affected by a PUSH or POP operation.

The stack operates as a circular buffer if the STVREN bit is programmed to '0' (Configuration Words). This means that after the stack has been PUSHed sixteen times, the seventeenth PUSH overwrites the value that was stored from the first PUSH. The eighteenth PUSH overwrites the second PUSH (and so on). The STKOVF and STKUNF flag bits will be set on an Overflow/Underflow, regardless of whether the Reset is enabled.

Note 1: There are no instructions/mnemonics called PUSH or POP. These are actions that occur from the execution of the CALL, CALLW, RETURN, RETLW and RETFIE instructions or the vectoring to an interrupt address.

4.5.1 ACCESSING THE STACK

The stack is accessible through the TOSH, TOSL and STKPTR registers. STKPTR is the current value of the Stack Pointer. TOSH:TOSL register pair points to the TOP of the stack. Both registers are read/writable. TOS is split into TOSH and TOSL due to the 15-bit size of the PC. To access the stack, adjust the value of STKPTR, which will position TOSH:TOSL, then read/write to TOSH:TOSL. STKPTR is five bits to allow detection of overflow and underflow.

Note:	Care should be taken when modifying the
	STKPTR while interrupts are enabled.

During normal program operation, CALL, CALLW and interrupts will increment STKPTR while RETLW, RETURN, and RETFIE will decrement STKPTR. STKPTR can be monitored to obtain to value of stack memory left at any given time. The STKPTR always points at the currently used place on the stack. Therefore, a CALL or CALLW will increment the STKPTR and then write the PC, and a return will unload the PC value from the stack and then decrement the STKPTR.

Reference Figure 4-4 through Figure 4-7 for examples of accessing the stack.

FIGURE 4-4: ACCESSING THE STACK EXAMPLE 1

U-0	U-0	U-0	U-0	U-0	U-0	R/W/HC-1/u	U-0			
—	—	-	-	—	—	MEMV	_			
bit 7							bit 0			
Legend:										
HC = Bit is clea	ared by hardwa	are								
R = Readable b	bit	W = Writable	bit	U = Unimplemented bit, read as '0'						
u = Bit is uncha	anged	x = Bit is unkn	iown	-m/n = Value at POR and BOR/Value at all othe			other Resets			
'1' = Bit is set		'0' = Bit is clea	ared	q = Value depends on condition						

REGISTER 8-3: PCON1: POWER CONTROL REGISTER 0

bit 7-2	Unimplemented: Read as '0'
bit 1	MEMV: Memory Violation Flag bit 1 = No Memory Violation Reset occurred or set to '1' by firmware. 0 = A Memory Violation Reset occurred (set to '0' in hardware when a Memory Violation occurs))
bit 0	Unimplemented: Read as '0'

TABLE 8-5: SUMMARY OF REGISTERS ASSOCIATED WITH RESETS

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
BORCON	SBOREN							BORRDY	92
PCON0	STKOVF	STKUNF	WDTWV	RWDT	RMCLR	RI	POR	BOR	99
PCON1	—	—	—	_	—	_	MEMV	—	99
STATUS	_	_	_	TO	PD	Z	DC	С	32
WDTCON0	_	_		V		SWDTEN	150		

Legend: — = unimplemented location, read as '0'. Shaded cells are not used by Resets.

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REGISTER 9-7: OSCTUNE: HFINTOSC TUNING REGISTER

U-0	U-0	R/W-1/1	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0		
—	—		HFTUN<5:0>						
bit 7							bit 0		

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-6	Unimplemented: Read as '0'.					
bit 5-0	HFTUN<5:0>: HFINTOSC Frequency Tuning bits 01 1111 = Maximum frequency 01 1110 =					
	•••					
	00 0001 =					
	00 0000 = Center frequency. Oscillator module is running at the calibrated frequency (default value).					
	11 1111 =					
	•••					
	10 0001 =					
	10 0000 = Minimum frequency.					

						D 1 1 1 2 1			
0-0	<u>U-0</u>	U-0	<u>U-0</u>	U-0	U-0	R/W-0/0	R/W-0/0		
	—		—	—	—	TMR2IE	TMR1IE		
bit 7							bit 0		
Legend:									
R = Readabl	e bit	W = Writable	bit	U = Unimplemented bit, read as '0'					
u = Bit is und	hanged	x = Bit is unkr	nown	-n/n = Value a	at POR and BOI	R/Value at all o	ther Resets		
'1' = Bit is se	t	'0' = Bit is clea	ared	HS = Hardwa	are set				
bit 7-2	Unimplemen	ted: Read as '	כי						
bit 1	TMR2IE: TMF	R2 to PR2 Mate	ch Interrupt Er	nable bit					
	1 = Enables	the Timer2 to	PR2 match int	terrupt					
	0 = Disables	the Timer2 to	PR2 match in	terrupt					
bit 0	TMR1IE: Time	er1 Overflow Ir	terrupt Enable	e bit					
	1 = Enables	the Timer1 ov	erflow interrup	ot					
	0 = Enables	the Timer1 ov	erflow interrup	ot					
Note: B	it PEIE of the IN	TCON register	must be						
se	et to enable ar	ny peripheral	interrupt						
CC	ontrolled by regis	ters PIE1-PIE7							

REGISTER 10-6: PIE4: PERIPHERAL INTERRUPT ENABLE REGISTER 4

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REGISTER 1	1-2: CPUDOZ	E: DOZE AN	D IDLE REG	ISTER				
R/W-0/u	R/W/HC/HS-0/0	R/W-0/0	R/W-0/0	U-0	R/W-0/0	R/W-0/0	R/W-0/0	
IDLEN	DOZEN ^(1,2)	ROI	DOE	_	DOZE<2:0>			
bit 7							bit 0	
								
Legend:								
R = Readable	bit	W = Writable	bit	U = Unimple	mented bit, r	ead as '0'		
u = Bit is unch	anged	x = Bit is unkr	iown	-n/n = Value Resets	at POR and	BOR/Value at a	all other	
'1' = Bit is set		'0' = Bit is clea	ared					
bit 7	IDLEN: Idle Enal 1 = A SLEEP ins 0 = A SLEEP ins	ble bit truction inhibits truction places	s the CPU cloc	k, but not the o full Sleep m	peripheral cl ode	ock(s)		
bit 6	DOZEN: Doze E 1 = The CPU ex 0 = The CPU ex	nable bit ^(1,2) ecutes instruct ecutes all instr	ion cycles acc uction cycles (ording to DO2 fastest, highe	ZE setting st power ope	ration)		
bit 5	 ROI: Recover-on 1 = Entering the operation. 0 = Interrupt ent 	I-Interrupt bit Interrupt Servio ry does not cha	ce Routine (ISI ange DOZEN	R) makes DO2	ZEN = 0 bit, b	pringing the CPL	J to full-speed	
bit 4	DOE: Doze on E 1 = Executing R 0 = RETFIE doe	xit bit ETFIE makes I es not change I	DOZEN = 1, b DOZEN	ringing the CF	PU to reduced	d speed operati	on.	
bit 3	Unimplemented	: Read as '0'						
bit 2-0	DOZE<2:0>: Rat 111 =1:256 110 =1:128 101 =1:64 100 =1:32 011 =1:16 010 =1:8 001 =1:4 000 =1:2	tio of CPU Inst	ruction Cycles	to Peripheral	Instruction C	ycles		

- **Note 1:** When ROI = 1 or DOE = 1, DOZEN is changed by hardware interrupt entry and/or exit.
 - 2: Entering ICD overrides DOZEN, returning the CPU to full execution speed; this bit is not affected.

14.2.6 ANALOG CONTROL

The ANSELA register (Register 14-4) is used to configure the Input mode of an I/O pin to analog. Setting the appropriate ANSELA bit high will cause all digital reads on the pin to be read as '0' and allow analog functions on the pin to operate correctly.

The state of the ANSELA bits has no effect on digital output functions. A pin with its TRIS bit clear and its ANSEL bit set will still operate as a digital output, but the Input mode will be analog. This can cause unexpected behavior when executing read-modify-write instructions on the affected port.

Note:	The ANSELA bits default to the Analog
	mode after Reset. To use any pins as
	digital general purpose or peripheral
	inputs, the corresponding ANSEL bits
	must be initialized to '0' by user software.

14.2.7 WEAK PULL-UP CONTROL

The WPUA register (Register 14-5) controls the individual weak pull-ups for each PORT pin.

14.2.8 PORTA FUNCTIONS AND OUTPUT PRIORITIES

Each PORTA pin is multiplexed with other functions.

Each pin defaults to the PORT latch data after Reset. Other output functions are selected with the peripheral pin select logic or by enabling an analog output, such as the DAC. See **Section 15.0 "Peripheral Pin Select (PPS) Module"** for more information.

Analog input functions, such as ADC and comparator inputs are not shown in the peripheral pin select lists. Digital output functions may continue to control the pin when it is in Analog mode.

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
INTCON	GIE	PEIE		—	—	—	-	INTEDG	121
PIE0	—	_	TMR0IE	IOCIE	—	—	-	INTE	122
IOCAP	—	-	IOCAP5	IOCAP4	IOCAP3	IOCAP2	IOCAP1	IOCAP0	204
IOCAN	—	_	IOCAN5	IOCAN4	IOCAN3	IOCAN2	IOCAN1	IOCAN0	204
IOCAF	—		IOCAF5	IOCAF4	IOCAF3	IOCAF2	IOCAF1	IOCAF0	205
IOCCP ⁽¹⁾	—		IOCCP5	IOCCP4	IOCCP3	IOCCP2	IOCCP1	IOCCP0	206
IOCCN ⁽¹⁾	—	_	IOCCN5	IOCCN4	IOCCN3	IOCCN2	IOCCN1	IOCCN0	206
IOCCF ⁽¹⁾	_	_	IOCCF5	IOCCF4	IOCCF3	IOCCF2	IOCCF1	IOCCF0	207

TABLE 17-1: SUMMARY OF REGISTERS ASSOCIATED WITH INTERRUPT-ON-CHANGE

Legend: — = unimplemented location, read as '0'. Shaded cells are not used by interrupt-on-change.

Note 1: Present only in PIC16(L)F15323.

21.0 5-BIT DIGITAL-TO-ANALOG CONVERTER (DAC1) MODULE

The Digital-to-Analog Converter supplies a variable voltage reference, ratiometric with the input source, with 32 selectable output levels.

The input of the DAC can be connected to:

- External VREF pins
- VDD supply voltage
- FVR (Fixed Voltage Reference)

The output of the DAC can be configured to supply a reference voltage to the following:

- Comparator positive input
- · ADC input channel
- DAC1OUT pin

The Digital-to-Analog Converter (DAC) is enabled by setting the DAC1EN bit of the DAC1CON0 register.

EQUATION 21-1: DAC OUTPUT VOLTAGE

$V_{OUT} = \left(V_{SOURCE+} - V_{SOURCE-} \times \frac{DAC1R\langle 4:0 \rangle}{2^5}\right) + (V_{SOURCE-})$

 $V_{SOURCE+} = V_{DD}$ or V_{REF+} or FVR

$V_{SOURCE} = V_{SS} \text{ or } V_{REF}$

21.2 Ratiometric Output Level

The DAC output value is derived using a resistor ladder with each end of the ladder tied to a positive and negative voltage reference input source. If the voltage of either input source fluctuates, a similar fluctuation will result in the DAC output value.

The value of the individual resistors within the ladder can be found in Table 37-15.

21.3 DAC Voltage Reference Output

The DAC voltage can be output to the DAC1OUT1/2 pins by setting the DAC1OE1/2 bits of the DAC1CON0 register, respectively. Selecting the DAC reference voltage for output on the DAC1OUT1/2 pins automatically overrides the digital output buffer and digital input threshold detector functions, disables the weak pull-up, and disables the current-controlled drive function of that pin. Reading the DAC1OUT1/2 pin when it has been configured for DAC reference voltage output will always return a '0'.

Due to the limited current drive capability, a buffer must be used on the DAC voltage reference output for external connections to the DAC1OUT1/2 pins. Figure 21-2 shows an example buffering technique.

21.1 Output Voltage Selection

The DAC has 32 voltage level ranges. The 32 levels are set with the DAC1R<4:0> bits of the DAC1CON1 register.

The DAC output voltage is determined by Equation 21-1:

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29.1.6 OPERATION IN SLEEP MODE

In Sleep mode, the TMR2 register will not increment and the state of the module will not change. If the PWMx pin is driving a value, it will continue to drive that value. When the device wakes up, TMR2 will continue from its previous state.

29.1.7 CHANGES IN SYSTEM CLOCK FREQUENCY

The PWM frequency is derived from the system clock frequency. Any changes in the system clock frequency will result in changes to the PWM frequency. See Section 9.0 "Oscillator Module (with Fail-Safe Clock Monitor)" for additional details.

29.1.8 EFFECTS OF RESET

Any Reset will force all ports to Input mode and the PWMx registers to their Reset states.

TABLE 29-1: EXAMPLE PWM FREQUENCIES AND RESOLUTIONS (Fosc = 20 MHz)

PWM Frequency	1.22 kHz	4.88 kHz	19.53 kHz	78.12 kHz	156.3 kHz	208.3 kHz
Timer Prescale	16	4	1	1	1	1
PR2 Value	0xFF	0xFF	0xFF	0x3F	0x1F	0x17
Maximum Resolution (bits)	10	10	10	8	7	6.6

TABLE 29-2: EXAMPLE PWM FREQUENCIES AND RESOLUTIONS (Fosc = 8 MHz)

PWM Frequency	1.22 kHz	4.90 kHz	19.61 kHz	76.92 kHz	153.85 kHz	200.0 kHz
Timer Prescale	16	4	1	1	1	1
PR2 Value	0xFF	0xFF	0xFF	0x3F	0x1F	0x17
Maximum Resolution (bits)	10	10	10	8	7	6.6

29.1.9 SETUP FOR PWM OPERATION

The following steps should be taken when configuring the module for using the PWMx outputs:

- 1. Disable the PWMx pin output driver(s) by setting the associated TRIS bit(s).
- Configure the PWM output polarity by configuring the PWMxPOL bit of the PWMxCON register.
- 3. Load the PR2 register with the PWM period value, as determined by Equation 29-1.
- 4. Load the PWMxDCH register and bits <7:6> of the PWMxDCL register with the PWM duty cycle value, as determined by Equation 29-2.
- 5. Configure and start Timer2:
- Clear the TMR2IF interrupt flag bit of the PIR4 register.
- Select the Timer2 prescale value by configuring the CKPS<2:0> bits of the T2CON register.
- Enable Timer2 by setting the Timer2 ON bit of the T2CON register.

- 6. Wait until the TMR2IF is set.
- 7. When the TMR2IF flag bit is set:
- Clear the associated TRIS bit(s) to enable the output driver.
- Route the signal to the desired pin by configuring the RxyPPS register.
- Enable the PWMx module by setting the PWMxEN bit of the PWMxCON register.

In order to send a complete duty cycle and period on the first PWM output, the above steps must be followed in the order given. If it is not critical to start with a complete PWM signal, then the PWM module can be enabled during Step 2 by setting the PWMxEN bit of the PWMxCON register.

REGISTER 29-2: PWMxDCH: PWM DUTY CYCLE HIGH BITS

R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u
			PWMxI	DC<9:2>			
bit 7							bit 0
Legend:							
R = Readable	bit	W = Writable b	pit	U = Unimplen	nented bit, read	as '0'	
u = Bit is unch	anged	x = Bit is unkn	own	-n/n = Value a	at POR and BO	R/Value at all o	other Resets

bit 7-0 **PWMxDC<9:2>:** PWM Duty Cycle Most Significant bits These bits are the MSbs of the PWM duty cycle. The two LSbs are found in PWMxDCL Register.

REGISTER 29-3: PWMxDCL: PWM DUTY CYCLE LOW BITS

'0' = Bit is cleared

R/W-x/u	R/W-x/u	U-0	U-0	U-0	U-0	U-0	U-0
PWMxD	C<1:0>	—	—	—	—	—	—
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-6 **PWMxDC<1:0>:** PWM Duty Cycle Least Significant bits These bits are the LSbs of the PWM duty cycle. The MSbs are found in PWMxDCH Register.

bit 5-0 Unimplemented: Read as '0'

'1' = Bit is set

30.0 COMPLEMENTARY WAVEFORM GENERATOR (CWG) MODULE

The Complementary Waveform Generator (CWG) produces half-bridge, full-bridge, and steering of PWM waveforms. It is backwards compatible with previous ECCP functions.

The CWG has the following features:

- · Six operating modes:
 - Synchronous Steering mode
 - Asynchronous Steering mode
 - Full-Bridge mode, Forward
 - Full-Bridge mode, Reverse
 - Half-Bridge mode
 - Push-Pull mode
- Output polarity control
- Output steering
 - Synchronized to rising event
 - Immediate effect
- Independent 6-bit rising and falling event deadband timers
 - Clocked dead band
 - Independent rising and falling dead-band enables
- Auto-shutdown control with:
 - Selectable shutdown sources
 - Auto-restart enable
 - Auto-shutdown pin override control

The CWG modules available are shown in Table 30-1.

TABLE 30-1: AVAILABLE CWG MODULES

Device	CWG1
PIC16(L)F15313/23	•

30.1 Fundamental Operation

The CWG module can operate in six different modes, as specified by MODE of the CWG1CON0 register:

- Half-Bridge mode (Figure 30-9)
- Push-Pull mode (Figure 30-2)
 - Full-Bridge mode, Forward (Figure 30-3)
 - Full-Bridge mode, Reverse (Figure 30-3)
- Steering mode (Figure 30-10)
- Synchronous Steering mode (Figure 30-11)

It may be necessary to guard against the possibility of circuit faults or a feedback event arriving too late or not at all. In this case, the active drive must be terminated before the Fault condition causes damage. Thus, all output modes support auto-shutdown, which is covered in **30.10** "Auto-Shutdown".

30.1.1 HALF-BRIDGE MODE

In Half-Bridge mode, two output signals are generated as true and inverted versions of the input as illustrated in Figure 30-9. A non-overlap (dead-band) time is inserted between the two outputs as described in **Section 30.5 "Dead-Band Control"**.

The unused outputs CWG1C and CWG1D drive similar signals, with polarity independently controlled by the POLC and POLD bits of the CWG1CON1 register, respectively.

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0			
OVRD	OVRC	OVRB	OVRA	STRD ⁽²⁾	STRC ⁽²⁾	STRB ⁽²⁾	STRA ⁽²⁾			
bit 7							bit 0			
Legend:										
R = Readable	bit	W = Writable	bit	U = Unimplei	mented bit, read	l as '0'				
u = Bit is uncha	anged	x = Bit is unkr	nown	-n/n = Value	at POR and BO	R/Value at all c	other Resets			
'1' = Bit is set '0' = Bit is cleared q = Value depends on condition										
bit 7	OVRD: Steer	ing Data D bit								
bit 6	OVRC: Steer	ing Data C bit								
bit 5	OVRB: Steer	ing Data B bit								
bit 4	OVRA: Steer	ing Data A bit								
bit 3	STRD: Steeri	ng Enable D bi	t(2)							
	1 = CWG1D	output has the	CWG1_data	waveform with	polarity control	from POLD bit				
h it 0		output is assigi	ned the value	of OVRD bit						
DIL Z		ng Enable C bi	CWC1 data	wayoform with	polarity control	from DOL C bit				
	1 = CWG1C 0 = CWG1C	output is assig	ned the value	of OVRC bit		ITOIN POLC DI				
bit 1	STRB: Steeri	ng Enable B bit	(2)							
	1 = CWG1B	output has the	CWG1_data	waveform with	polarity control	from POLB bit				
	0 = CWG1B	0 = CWG1B output is assigned the value of OVRB bit								
bit 0	STRA: Steeri	ng Enable A bit	(2)							
	1 = CWG1A	output has the	CWG1_data	waveform with	polarity control	from POLA bit				
	0 = CWG1A	output is assign	ned the value	of OVRA bit						
Note 1: Th	e bits in this re	gister apply onl	y when MOD	E<2:0> = 00x.						

REGISTER 30-7: CWG1STR: CWG1 STEERING CONTROL REGISTER⁽¹⁾

2: This bit is effectively double-buffered when MODE<2:0> = 001.

32.2.1 SPI MODE REGISTERS

The MSSP module has five registers for SPI mode operation. These are:

- MSSP STATUS register (SSP1STAT)
- MSSP Control register 1 (SSP1CON1)
- MSSP Control register 3 (SSP1CON3)
- MSSP Data Buffer register (SSP1BUF)
- MSSP Address register (SSP1ADD)
- MSSP Shift register (SSP1SR) (Not directly accessible)

SSP1CON1 and SSP1STAT are the control and status registers in SPI mode operation. The SSP1CON1 register is readable and writable. The lower six bits of the SSP1STAT are read-only. The upper two bits of the SSP1STAT are read/write.

In one SPI master mode, SSP1ADD can be loaded with a value used in the Baud Rate Generator. More information on the Baud Rate Generator is available in **Section 32.7 "Baud Rate Generator"**.

SSP1SR is the shift register used for shifting data in and out. SSP1BUF provides indirect access to the SSP1SR register. SSP1BUF is the buffer register to which data bytes are written, and from which data bytes are read.

In receive operations, SSP1SR and SSP1BUF together create a buffered receiver. When SSP1SR receives a complete byte, it is transferred to SSP1BUF and the SSP1IF interrupt is set.

During transmission, the SSP1BUF is not buffered. A write to SSP1BUF will write to both SSP1BUF and SSP1SR.

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FIGURE 33-7: AUTO-WAKE-UP BIT (WUE) TIMING DURING NORMAL OPERATION

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FIGURE 33-8: AUTO-WAKE-UP BIT (WUE) TIMINGS DURING SLEEP

() The SURARY remains in His while the WUE is set.

33.3.4 BREAK CHARACTER SEQUENCE

The EUSART module has the capability of sending the special Break character sequences that are required by the LIN bus standard. A Break character consists of a Start bit, followed by 12 '0' bits and a Stop bit.

To send a Break character, set the SENDB and TXEN bits of the TX1STA register. The Break character transmission is then initiated by a write to the TX1REG. The value of data written to TX1REG will be ignored and all '0's will be transmitted.

The SENDB bit is automatically reset by hardware after the corresponding Stop bit is sent. This allows the user to preload the transmit FIFO with the next transmit byte following the Break character (typically, the Sync character in the LIN specification).

The TRMT bit of the TX1STA register indicates when the transmit operation is active or idle, just as it does during normal transmission. See Figure 33-9 for the timing of the Break character sequence.

33.3.4.1 Break and Sync Transmit Sequence

The following sequence will start a message frame header made up of a Break, followed by an auto-baud Sync byte. This sequence is typical of a LIN bus master.

- 1. Configure the EUSART for the desired mode.
- 2. Set the TXEN and SENDB bits to enable the Break sequence.
- 3. Load the TX1REG with a dummy character to initiate transmission (the value is ignored).
- 4. Write '55h' to TX1REG to load the Sync character into the transmit FIFO buffer.
- 5. After the Break has been sent, the SENDB bit is reset by hardware and the Sync character is then transmitted.

When the TX1REG becomes empty, as indicated by the TX1IF, the next data byte can be written to TX1REG.

					SYNC	C = 0, BRGH	l = 1, BRC	G16 = 0					
BAUD	Fosc	Fosc = 32.000 MHz		Fosc	= 20.00	0 MHz	Fosc = 18.432 MHz			Fosc	Fosc = 11.0592 MHz		
RATE	Actual Rate	% Error	SPBRG value (decimal)	Actual Rate	% Error	SPBRG value (decimal)	Actual Rate	% Error	SPBRG value (decimal)	Actual Rate	% Error	SPBRG value (decimal)	
300	—	—	—	—	—	_		_	—		—		
1200	—	—	—	—	—	—	—	—	—	—	—	—	
2400	—	_	—	—	_	—	—	_	_	—	_	—	
9600	9615	0.16	207	9615	0.16	129	9600	0.00	119	9600	0.00	71	
10417	10417	0.00	191	10417	0.00	119	10378	-0.37	110	10473	0.53	65	
19.2k	19.23k	0.16	103	19.23k	0.16	64	19.20k	0.00	59	19.20k	0.00	35	
57.6k	57.14k	-0.79	34	56.82k	-1.36	21	57.60k	0.00	19	57.60k	0.00	11	
115.2k	117.64k	2.12	16	113.64k	-1.36	10	115.2k	0.00	9	115.2k	0.00	5	

TABLE 33-4: BAUD RATE FOR ASYNCHRONOUS MODES (CONTINUED)

					SYNC	C = 0, BRGH	H = 1, BRG	316 = 0					
BAUD	AUD Fosc = 8.000 MHz			Fosc = 4.000 MHz			Fosc = 3.6864 MHz			Fos	Fosc = 1.000 MHz		
RATE	Actual Rate	% Error	SPBRG value (decimal)	Actual Rate	% Error	SPBRG value (decimal)	Actual Rate	% Error	SPBRG value (decimal)	Actual Rate	% Error	SPBRG value (decimal)	
300	—	_	_	_	_	_	_	_	_	300	0.16	207	
1200	—	—	—	1202	0.16	207	1200	0.00	191	1202	0.16	51	
2400	2404	0.16	207	2404	0.16	103	2400	0.00	95	2404	0.16	25	
9600	9615	0.16	51	9615	0.16	25	9600	0.00	23	—	_	_	
10417	10417	0.00	47	10417	0.00	23	10473	0.53	21	10417	0.00	5	
19.2k	19231	0.16	25	19.23k	0.16	12	19.2k	0.00	11	—	_	_	
57.6k	55556	-3.55	8	—	_	_	57.60k	0.00	3	—	_	_	
115.2k	—	_	_	—	_	—	115.2k	0.00	1	—	_	_	

					SYNC	C = 0, BRGH	l = 0, BRC	616 = 1				
BAUD	Fosc = 32.000 MHz			Fosc = 20.000 MHz			Fosc = 18.432 MHz			Fosc = 11.0592 MHz		
RATE	Actual Rate	% Error	SPBRG value (decimal)	Actual Rate	% Error	SPBRG value (decimal)	Actual Rate	% Error	SPBRG value (decimal)	Actual Rate	% Error	SPBRG value (decimal)
300	300.0	0.00	6666	300.0	-0.01	4166	300.0	0.00	3839	300.0	0.00	2303
1200	1200	-0.02	3332	1200	-0.03	1041	1200	0.00	959	1200	0.00	575
2400	2401	-0.04	832	2399	-0.03	520	2400	0.00	479	2400	0.00	287
9600	9615	0.16	207	9615	0.16	129	9600	0.00	119	9600	0.00	71
10417	10417	0.00	191	10417	0.00	119	10378	-0.37	110	10473	0.53	65
19.2k	19.23k	0.16	103	19.23k	0.16	64	19.20k	0.00	59	19.20k	0.00	35
57.6k	57.14k	-0.79	34	56.818	-1.36	21	57.60k	0.00	19	57.60k	0.00	11
115.2k	117.6k	2.12	16	113.636	-1.36	10	115.2k	0.00	9	115.2k	0.00	5

DECFSZ	Decrement f, Skip if 0
Syntax:	[label] DECFSZ f,d
Operands:	$\begin{array}{l} 0 \leq f \leq 127 \\ d \in [0,1] \end{array}$
Operation:	(f) - 1 \rightarrow (destination); skip if result = 0
Status Affected:	None
Description:	The contents of register 'f' are decre- mented. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is placed back in register 'f'. If the result is '1', the next instruction is executed. If the result is '0', then a NOP is executed instead, making it a 2-cycle instruction.

GOTO	Unconditional Branch				
Syntax:	[<i>label</i>] GOTO k				
Operands:	$0 \le k \le 2047$				
Operation:	$k \rightarrow PC<10:0>$ PCLATH<6:3> \rightarrow PC<14:11>				
Status Affected:	None				
Description:	GOTO is an unconditional branch. The 11-bit immediate value is loaded into PC bits <10:0>. The upper bits of PC are loaded from PCLATH<4:3>. GOTO is a 2-cycle instruction.				

INCFSZ Increment f, Skip if 0				
Syntax:	[<i>label</i>] INCFSZ f,d			
Operands:	$0 \le f \le 127$ $d \in [0,1]$			
Operation:	(f) + 1 \rightarrow (destination), skip if result = 0			
Status Affected:	None			
Description:	The contents of register 'f' are incre- mented. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is placed back in register 'f'. If the result is '1', the next instruction is executed. If the result is '0', a NOP is executed instead, making it a 2-cycle instruction.			
	Inclusive OR literal with W			

	Inclusive OR literal with w			
Syntax:	[<i>label</i>] IORLW k			
Operands:	$0 \leq k \leq 255$			
Operation:	(W) .OR. $k \rightarrow$ (W)			
Status Affected:	Z			
Description:	The contents of the W register are OR'ed with the 8-bit literal 'k'. The result is placed in the W register.			

INCF	Increment f		
Syntax:	[<i>label</i>] INCF f,d		
Operands:	$\begin{array}{l} 0 \leq f \leq 127 \\ d \in [0,1] \end{array}$		
Operation:	(f) + 1 \rightarrow (destination)		
Status Affected:	Z		
Description:	The contents of register 'f' are incre- mented. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is placed back in register 'f'.		

IORWF	Inclusive OR W with f				
Syntax:	[<i>label</i>] IORWF f,d				
Operands:	$0 \le f \le 127$ $d \in [0,1]$				
Operation:	(W) .OR. (f) \rightarrow (destination)				
Status Affected:	Z				
Description:	Inclusive OR the W register with regis- ter 'f'. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is placed back in register 'f'.				

Standard Operating Conditions (unless otherwise stated)							
Param. No.	Sym.	Characteristic	Тур.	Units	Conditions		
TH01	θJA	Thermal Resistance Junction to Ambient	70	°C/W	8-pin PDIP package		
			95.3C	°C/W	8-pin SOIC package		
			100.0	°C/W	8-pin DFN package		
			100.0	°C/W	14-pin PDIR package		
			100.0	°C/W	14-pin TSSOP package		
			77.7	°C/W	14-pin SOIC package		
			51.5	°C/W/	16-pin UQFN 4x4mm package		
TH02	θJC	Thermal Resistance Junction to Case	32.75	°C/W\	8-pin-PDIP package		
			31.0	°C/W	8-pin SØIC package		
			24.4	∕_°C/W	&-pin∕DFN package		
			5.4	wx3° ∕	14 pin PDIP package		
			27,5	>€\M ∕	14-pm TSSOP package		
			31.1	°C/W	1∳-pin SOIC package		
			23.1	<u>°C/₩</u>	16-pin UQFN 4x4mm package		
TH03	Тјмах	Maximum Junction Temperature	150	<u> </u>			
TH04	PD	Power Dissipation		Ŵ	PD = PINTERNAL + PI/O		
TH05	PINTERNAL	Internal Power Dissipation	<u> </u>	∖ w	PINTERNAL = IDD x VDD ⁽¹⁾		
TH06	Pi/o	I/O Power Dissipation	$\langle - \rangle$	∕w	$PI/O = \Sigma (IOL * VOL) + \Sigma (IOH * (VDD - VOH))$		
TH07	Pder	Derated Power	$\langle - \rangle$	W	Pder = PDmax (Τj - Τa)/θja ⁽²⁾		

TABLE 37-6: THERMAL CHARACTERISTICS

Note 1: IDD is current to run the chip alone without driving any load on the output pins.
2: TA = Ambient Temperature, TJ = Junction Temperature

14-Lead PDIP (300 mil)

