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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

E·XF

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	32MHz
Connectivity	I ² C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	12
Program Memory Size	3.5KB (2K x 14)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 5.5V
Data Converters	A/D 11x10b; D/A 1x5b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	14-TSSOP (0.173", 4.40mm Width)
Supplier Device Package	14-TSSOP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16f15323t-i-st

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

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Name	Function	Input Type	Output Type	Description
RA0/ANA0/C1IN0+/DAC1OUT/TX1/	RA0	TTL/ST	CMOS/OD	General purpose I/O.
CKT 7CLUINS 7ICSPDAT/IOCAU	ANA0	AN	_	ADC Channel A0 input.
	C1IN0+	AN	_	Comparator 1 positive input.
	DAC1OUT	_	AN	Digital-to-Analog Converter output.
	TX1	_	CMOS	EUSART1 asynchronous transmit.
	CK1 ⁽¹⁾	TTL/ST	CMOS/OD	EUSART1 synchronous mode clock input/output.
	CLCIN3 ⁽¹⁾	TTL/ST	_	Configurable Logic Cell source input.
	ICSPDAT	ST	CMOS	In-Circuit Serial Programming [™] and debugging data input/ output.
	IOCA0	TTL/ST		Interrupt-on-change input.
RA1/ANA1/VREF+/C1IN0-/DAC1REF+/	RA1	TTL/ST	CMOS/OD	General purpose I/O.
DT1 ⁽¹⁾ /CLCIN2 ⁽¹⁾ /ICSPCLK/IOCA1	ANA1	AN	_	ADC Channel A1 input.
	VREF+	AN	_	External ADC and/or DAC positive reference input.
	C1IN0-	AN		Comparator 1 negative input.
	DAC1REF+	TTL/ST	AN	DAC positive reference.
	T0CKI ⁽¹⁾	TTL/ST	-	Timer0 clock input.
	SCK1 ⁽⁴⁾	I ² C	OD	I ² C, OD, MSSP1 I ² C input/output.
	SCL1 ^(1,4)	TTL/ST	CMOS/OD	MSSP1 SPI clock input/output (default input location, SCK1 is a PPS remappable input and output).
	RX1	TTL/ST	_	EUSART1 Asynchronous mode receiver data input.
	DT1 ⁽¹⁾	TTL/ST	CMOS/OD	EUSART1 Synchronous mode data input/output.
	CLCIN2 ⁽¹⁾	TTL/ST	_	Configurable Logic Cell source input.
	ICSPCLK	ST	_	In-Circuit Serial Programming [™] and debugging clock input.
	IOCA1	TTL/ST	_	Interrupt-on-change input.
RA2/ANA2/CWG1IN ⁽¹⁾ /SDA1 ^(1,4) / SDI1 ⁽¹⁾ /ZCD1/INT ⁽¹⁾ /IOCA2	RA2	TTL/ST	CMOS/OD	General purpose I/O.
	ANA2	AN	_	ADC Channel A2 input.
	CWG1IN ⁽¹⁾	TTL/ST		Complementary Waveform Generator 1 input.
	SDA1 ^(1,4)	l ² C	OD	MSSP1 I ² C serial data input/output.
	SDI1 ⁽¹⁾	TTL/ST	_	MSSP1 SPI serial data input.
	ZCD1	AN	AN	Zero-cross detect input pin (with constant current sink/ source).
	INT ⁽¹⁾	TTL/ST	_	External interrupt request input.
	IOCA2	TTL/ST	_	Interrupt-on-change input.

TABLE 1-2: PIC16(L)F15313 PINOUT DESCRIPTION

Legend: AN = Analog input or output TTL = TTL compatible input ST XTAL

CMOS = CMOS compatible input or output = Schmitt Trigger input with CMOS levels = Crystal levels

OD = Open-Drain = Schmitt Trigger input with I²C

I²C

ΗV = High Voltage This is a PPS remappable input signal. The input function may be moved from the default location shown to one of several other PORTx pins. Refer to Table 15-3 for details on which PORT pins may be used for this signal. Note 1:

2: All output signals shown in this row are PPS remappable. These signals may be mapped to output onto one of several PORTx pin options as described in Table 15-3.

This is a bidirectional signal. For normal module operation, the firmware should map this signal to the same pin in both the PPS input and 3: PPS output registers.

4: These pins are configured for I²C logic levels. The SCLx/SDAx signals may be assigned to any of the RB1/RB2/RC3/RC4 pins. PPS assignments to the other pins (e.g., RA5) will operate, but input logic levels will be standard TTL/ST, as selected by the INLVL register, instead of the I²C specific or SMBus input buffer thresholds.

TABLE 4-10: SPECIAL FUNCTION REGISTER SUMMARY BANKS 0-63 (CONTINUED)

			ILE OIOTEIL		Brance		.020)				
Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	V <u>alue o</u> n: MCLR
Bank 1	3ank 1										
	CPU CORE REGISTERS; see Table 4-3 for specifics										
08Ch 09Ah	_	Unimplemented								_	-
09Bh	ADRESL	ADC Result Register I	_OW							XXXX XXXX	uuuu uuuu
09Ch	ADRESH	ADC Result Register H	ligh							XXXX XXXX	uuuu uuuu
09Dh	ADCON0		CHS<5:0> GO/DONE ADON							0000 0000	0000 0000
09Eh	ADCON1	ADFM	ADCS<2:0> — — ADPREF<1:0>				000000	000000			
09Fh	ADACT	— — — ADACT<4:0>								0 0000	0 0000

Legend: x = unknown, u = unchanged, q = depends on condition, - = unimplemented, read as '0', r = reserved. Shaded locations unimplemented, read as '0'.

TABLE 4-10:	SPECIAL FUNCTION REGISTER SUMMARY BANKS 0-63	(CONTINUED)
-------------	--	-------------

							,					
Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	V <u>alue o</u> n: MCLR	
Bank 5												
	CPU CORE REGISTERS; see Table 4-3 for specifics											
28Ch	T2TMR	Holding Register for the 8-bit TMR2 Register								0000 0000	0000 0000	
28Dh	T2PR	TMR2 Period Registe	r							1111 1111	1111 1111	
28Eh	T2CON	ON		CKPS<2:0>			OUT	PS<3:0>		0000 0000	0000 0000	
28Fh	T2HLT	PSYNC	CKPOL	CKSYNC			MODE<4:0>			0000 0000	0000 0000	
290h	T2CLKCON	-					CS	S<3:0>		0000	0000	
291h	T2RST	_	— — — RSEL<3:0>					0000	0000			
292h — 29Fh	Unimplemented							_	_			

Legend: x = unknown, u = unchanged, q = depends on condition, - = unimplemented, read as '0', r = reserved. Shaded locations unimplemented, read as '0'.

						(- /			1	
Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	V <u>alue o</u> n: MCLR
Bank 14											
70Ch	PIR0	—	_	TMR0IF	IOCIF	_	—	—	INTF	000	000
70Dh	PIR1	OSFIF	CSWIF		_	_	_	—	ADIF	0000	0000
70Eh	PIR2	—	ZCDIF	—	—	_	—	C2IF ⁽¹⁾	C1IF	-000	-000
70Fh	PIR3	_	_	RC1IF	TX1IF	_	_	BCL1IF	SSP1IF	0000	0000
710h	PIR4	—	—	—	_	—	—	TMR2IF	TMR1IF	00	00
711h	PIR5	CLC4IF	CLC3IF	CLC2IF	CLC1IF	—	—	—	TMR1GIF	00000	00000
712h	PIR6	—	—	—	—	—	—	CCP2IF	CCP1IF	00	00
713h	PIR7	—		NVMIF	NCO1IF	—		—	CWG1IF	000	000
714h	—				Unimple	mented				—	—
715h	—				Unimple	mented				—	—
716h	PIE0	—	—	TMR0IE	IOCIE	—	—	—	INTE	000	000
717h	PIE1	OSFIE	CSWIE	—	—	—	—	—	ADIE	0000	0000
718h	PIE2	—	ZCDIE	—	—	—	—	C2IE ⁽¹⁾	C1IE	-000	-000
719h	PIE3	_	_	RC1IE	TX1IE	_	_	BCL1IE	SSP1IE	0000	0000
71Ah	PIE4	—	—	—	_	—	—	TMR2IE	TMR1IE	00	00
71Bh	PIE5	CLC4IE	CLC3IE	CLC2IE	CLC1IE	—	—	—	TMR1GIE	00000	00000
71Ch	PIE6	_			_		_	CCP2IE	CCP1IE	00	00
71Dh	PIE7	_	_	NVMIE	NCO1IE	_	_	_	CWG1IE	000	000
71Eh	_				Unimple	mented				—	—
71Fh	_				Unimple	mented				—	—

TABLE 4-10: SPECIAL FUNCTION REGISTER SUMMARY BANKS 0-63 (CONTINUED)

Legend: x = unknown, u = unchanged, q = depends on condition, - = unimplemented, read as '0', r = reserved. Shaded locations unimplemented, read as '0'.

Note 1: Present only on PIC16(L)F15323.

9.3 Clock Switching

The system clock source can be switched between external and internal clock sources via software using the New Oscillator Source (NOSC) and New Divider selection request (NDIV) bits of the OSCCON1 register.

9.3.1 NEW OSCILLATOR SOURCE (NOSC) AND NEW DIVIDER SELECTION REQUEST (NDIV) BITS

The New Oscillator Source (NOSC) and New Divider selection request (NDIV) bits of the OSCCON1 register select the system clock source and the frequency that are used for the CPU and peripherals.

When new values of NOSC and NDIV are written to OSCCON1, the current oscillator selection will continue to operate while waiting for the new clock source to indicate that it is stable and ready. In some cases, the newly requested source may already be in use, and is ready immediately. In the case of a divider-only change, the new and old sources are the same, and will be immediately ready. The device may enter Sleep while waiting for the switch as described in **Section 9.3.3 "Clock Switch and Sleep"**.

When the new oscillator is ready, the New Oscillator is Ready (NOSCR) bit of OSCCON3 and the Clock Switch Interrupt Flag (CSWIF) bit of PIR1 become set (CSWIF = 1). If Clock Switch Interrupts are enabled (CSWIE = 1), an interrupt will be generated at that time. The Oscillator Ready (ORDY) bit of OSCCON3 can also be polled to determine when the oscillator is ready in lieu of an interrupt.

If the Clock Switch Hold (CSWHOLD) bit of OSCCON3 is clear, the oscillator switch will occur when the new Oscillator's READY bit (NOSCR) is set, and the interrupt (if enabled) will be serviced at the new oscillator setting.

If CSWHOLD is set, the oscillator switch is suspended, while execution continues using the current (old) clock source. When the NOSCR bit is set, software should:

- set CSWHOLD = 0 so the switch can complete, or
- copy COSC into NOSC to abandon the switch.

If DOZE is in effect, the switch occurs on the next clock cycle, whether or not the CPU is operating during that cycle.

Changing the clock post-divider without changing the clock source (e.g., changing Fosc from 1 MHz to 2 MHz) is handled in the same manner as a clock source change, as described previously. The clock source will already be active, so the switch is relatively quick. CSWHOLD must be clear (CSWHOLD = 0) for the switch to complete.

The current COSC and CDIV are indicated in the OSCCON2 register up to the moment when the switch actually occurs, at which time OSCCON2 is updated and ORDY is set. NOSCR is cleared by hardware to indicate that the switch is complete.

9.3.2 PLL INPUT SWITCH

Switching between the PLL and any non-PLL source is managed as described above. The input to the PLL is established when NOSC selects the PLL, and maintained by the COSC setting.

When NOSC and COSC select the PLL with different input sources, the system continues to run using the COSC setting, and the new source is enabled per NOSC. When the new oscillator is ready (and CSWHOLD = 0), system operation is suspended while the PLL input is switched and the PLL acquires lock.

Note: If the PLL fails to lock, the FSCM will trigger.

9.3.3 CLOCK SWITCH AND SLEEP

If OSCCON1 is written with a new value and the device is put to Sleep before the switch completes, the switch will not take place and the device will enter Sleep mode.

When the device wakes from Sleep and the CSWHOLD bit is clear, the device will wake with the 'new' clock active, and the clock switch interrupt flag bit (CSWIF) will be set.

When the device wakes from Sleep and the CSWHOLD bit is set, the device will wake with the 'old' clock active and the new clock will be requested again.

11.1.2 INTERRUPTS DURING DOZE

If an interrupt occurs and the Recover-on-Interrupt bit is clear (ROI = 0) at the time of the interrupt, the Interrupt Service Routine (ISR) continues to execute at the rate selected by DOZE<2:0>. Interrupt latency is extended by the DOZE<2:0> ratio.

If an interrupt occurs and the ROI bit is set (ROI = 1) at the time of the interrupt, the DOZEN bit is cleared and the CPU executes at full speed. The prefetched instruction is executed and then the interrupt vector sequence is executed. In Figure 11-1, the interrupt occurs during the 2^{nd} instruction cycle of the Doze period, and immediately brings the CPU out of Doze. If the Doze-On-Exit (DOE) bit is set (DOE = 1) when the RETFIE operation is executed, DOZEN is set, and the CPU executes at the reduced rate based on the DOZE<2:0> ratio.

11.2 Sleep Mode

Sleep mode is entered by executing the SLEEP instruction, while the Idle Enable (IDLEN) bit of the CPUDOZE register is clear (IDLEN = 0). If the SLEEP instruction is executed while the IDLEN bit is set (IDLEN = 1), the CPU will enter the IDLE mode (Section 11.2.3 "Low-Power Sleep Mode").

Upon entering Sleep mode, the following conditions exist:

- 1. WDT will be cleared but keeps running if enabled for operation during Sleep
- 2. The PD bit of the STATUS register is cleared
- 3. The $\overline{\text{TO}}$ bit of the STATUS register is set
- 4. CPU Clock and System Clock
- 5. 31 kHz LFINTOSC, HFINTOSC are unaffected and peripherals using them may continue operation in Sleep.
- 6. ADC is unaffected if the dedicated FRC oscillator is selected the conversion will be left abandoned if FOSC is selected and ADRES will have an incorrect value
- 7. I/O ports maintain the status they had before Sleep was executed (driving high, low, or high-impedance). This does not apply in the case of any asynchronous peripheral which is active and may affect the I/O port value
- 8. Resets other than WDT are not affected by Sleep mode

Refer to individual chapters for more details on peripheral operation during Sleep.

To minimize current consumption, the following conditions should be considered:

- I/O pins should not be floating
- External circuitry sinking current from I/O pins
- Internal circuitry sourcing current from I/O pins
- Current draw from pins with internal weak pull-ups
- Modules using any oscillator

I/O pins that are high-impedance inputs should be pulled to VDD or VSS externally to avoid switching currents caused by floating inputs.

Any module with a clock source that is not Fosc can be enabled. Examples of internal circuitry that might be sourcing current include modules such as the DAC and FVR modules. See Section 21.0 "5-Bit Digital-to-Analog Converter (DAC1) Module", Section 18.0 "Fixed Voltage Reference (FVR)" for more information on these modules.

11.2.1 WAKE-UP FROM SLEEP

The device can wake-up from Sleep through one of the following events:

- 1. External Reset input on MCLR pin, if enabled.
- 2. BOR Reset, if enabled.
- 3. POR Reset.
- 4. Watchdog Timer, if enabled.
- 5. Any external interrupt.
- 6. Interrupts by peripherals capable of running during Sleep (see individual peripheral for more information).

The first three events will cause a device Reset. The last three events are considered a continuation of program execution. To determine whether a device Reset or wake-up event occurred, refer to **Section 8.12 "Memory Execution Violation**".

When the SLEEP instruction is being executed, the next instruction (PC + 1) is prefetched. For the device to wake-up through an interrupt event, the corresponding interrupt enable bit must be enabled. Wake-up will occur regardless of the state of the GIE bit. If the GIE bit is disabled, the device continues execution at the instruction after the SLEEP instruction. If the GIE bit is enabled, the device executes the instruction after the SLEEP instruction, the device will then call the Interrupt Service Routine. In cases where the execution of the instruction following SLEEP is not desirable, the user should have a NOP after the SLEEP instruction.

The WDT is cleared when the device wakes-up from Sleep, regardless of the source of wake-up.

PIC16(L)F15313/23

U-0	R/W-0/0	U-0	R/W-0/0	U-0	U-0	U-0	R/W-0/0	
	UART1MD		MSSP1MD	—	—		CWG1MD	
bit 7							bit 0	
Legend:								
R = Readable	bit	W = Writable I	oit	U = Unimplem	nented bit, read	as '0'		
u = Bit is unch	anged	x = Bit is unkn	own	-n/n = Value a	t POR and BOF	R/Value at all o	other Resets	
'1' = Bit is set		'0' = Bit is clea	ared	q = Value dep	ends on condition	on		
bit 7	Unimplement	t ed: Read as '0	,					
bit 6	UART1MD: D	isable EUSAR	Γ1 bit					
	1 = EUSART	1 module disab	led					
6.4. C	0 = EUSART		,					
DIT 5	Unimplement	ed: Read as 'U	ŕ					
bit 4	MSSP1MD: D	isable MSSP1	bit					
	1 = MSSP1 m 0 = MSSP1 m	nodule disabled						
hit 3-1	hit 3-1 Unimplemented: Read as '0'							
bit 0			4					
	1 = CWG1 m		ι					
	0 = CWG1 m	odule enabled						

REGISTER 16-5: PMD4: PMD CONTROL REGISTER 4

20.1 ADC Configuration

When configuring and using the ADC the following functions must be considered:

- Port configuration
- · Channel selection
- ADC voltage reference selection
- ADC conversion clock source
- · Interrupt control
- Result formatting

20.1.1 PORT CONFIGURATION

The ADC can be used to convert both analog and digital signals. When converting analog signals, the I/O pin will be configured for analog by setting the associated TRIS and ANSEL bits. Refer to **Section 14.0 "I/O Ports"** for more information.

Note:	Analog voltages on any pin that is defined					
	as a digital input may cause the input					
	buffer to conduct excess current.					

20.1.2 CHANNEL SELECTION

There are several channel selections available:

- Six Port A channels
- Six Port C channels (PIC16(L)F15323 only)
- Temperature Indicator
- DAC output
- Fixed Voltage Reference (FVR)
- · AVss (Ground)

The CHS<5:0> bits of the ADCON0 register (Register 20-1) determine which channel is connected to the sample and hold circuit.

When changing channels, a delay is required before starting the next conversion. Refer to **Section 20.2** "**ADC Operation**" for more information.

Note: It is recommended that when switching from an ADC channel of a higher voltage to a channel of a lower voltage, that the user selects the VSS channel before connecting to the channel with the lower voltage. If the ADC does not have a dedicated VSS input channel, the VSS selection (DAC1R<4:0> = b'00000') through the DAC output channel can be used. If the DAC is in use, a free input channel can be connected to VSS, and can be used in place of the DAC.

20.1.3 ADC VOLTAGE REFERENCE

The ADPREF<1:0> bits of the ADCON1 register provides control of the positive voltage reference. The positive voltage reference can be:

- VREF+ pin
- Vdd
- FVR 2.048V
- FVR 4.096V (Not available on LF devices)

The ADPREF bit of the ADCON1 register provides control of the negative voltage reference. The negative voltage reference can be:

- VREF- pin
- Vss

See **Section 18.0** "Fixed Voltage Reference (FVR)" for more details on the Fixed Voltage Reference.

20.1.4 CONVERSION CLOCK

The source of the conversion clock is software selectable via the ADCS<2:0> bits of the ADCON1 register. There are seven possible clock options:

- · Fosc/2
- Fosc/4
- Fosc/8
- Fosc/16
- Fosc/32
- Fosc/64
- ADCRC (dedicated RC oscillator)

The time to complete one bit conversion is defined as TAD. One full 10-bit conversion requires 11.5 TAD periods as shown in Figure 20-2.

For correct conversion, the appropriate TAD specification must be met. Refer to Table 37-13 for more information. Table 20-1 gives examples of appropriate ADC clock selections.

Note: Unless using the ADCRC, any changes in the system clock frequency will change the ADC clock frequency, which may adversely affect the ADC result.

22.2 FIXED DUTY CYCLE MODE

In Fixed Duty Cycle (FDC) mode, every time the accumulator overflows (NCO_overflow), the output is toggled at a frequency rate half of the FOVERFLOW. This provides a 50% duty cycle, provided that the increment value remains constant. For more information, see Figure 22-2.

The FDC mode is selected by clearing the N1PFM bit in the NCO1CON register.

22.3 PULSE FREQUENCY MODE

In Pulse Frequency (PF) mode, every time the Accumulator overflows, the output becomes active for one or more clock periods. Once the clock period expires, the output returns to an inactive state. This provides a pulsed output. The output becomes active on the rising clock edge immediately following the overflow event. For more information, see Figure 22-2.

The value of the active and inactive states depends on the polarity bit, N1POL in the NCO1CON register.

The PF mode is selected by setting the N1PFM bit in the NCO1CON register.

22.3.1 OUTPUT PULSE WIDTH CONTROL

When operating in PF mode, the active state of the output can vary in width by multiple clock periods. Various pulse widths are selected with the N1PWS<2:0> bits in the NCO1CLK register.

When the selected pulse width is greater than the Accumulator overflow time frame, then NCO1 output does not toggle.

22.4 OUTPUT POLARITY CONTROL

The last stage in the NCO module is the output polarity. The N1POL bit in the NCO1CON register selects the output polarity. Changing the polarity while the interrupts are enabled will cause an interrupt for the resulting output transition.

The NCO output signal (NCO1_out) is available to the following peripherals:

- CLC
- CWG
- Timer1
- Timer2
- CLKR

22.5 Interrupts

When the accumulator overflows (NCO_overflow), the NCO Interrupt Flag bit, NCO1IF, of the PIR7 register is set. To enable the interrupt event (NCO_interrupt), the following bits must be set:

- N1EN bit of the NCO1CON register
- NCO1IE bit of the PIE7 register
- PEIE bit of the INTCON register
- · GIE bit of the INTCON register

The interrupt must be cleared by software by clearing the NCO1IF bit in the Interrupt Service Routine.

22.6 Effects of a Reset

All of the NCO registers are cleared to zero as the result of a Reset.

22.7 Operation in Sleep

The NCO module operates independently from the system clock and will continue to run during Sleep, provided that the clock source selected remains active.

The HFINTOSC remains active during Sleep when the NCO module is enabled and the HFINTOSC is selected as the clock source, regardless of the system clock source selected.

In other words, if the HFINTOSC is simultaneously selected as the system clock and the NCO clock source, when the NCO is enabled, the CPU will go idle during Sleep, but the NCO will continue to operate and the HFINTOSC will remain active.

This will have a direct effect on the Sleep mode current.

23.0 COMPARATOR MODULE

Comparators are used to interface analog circuits to a digital circuit by comparing two analog voltages and providing a digital indication of their relative magnitudes. Comparators are very useful mixed signal building blocks because they provide analog functionality independent of program execution. The analog comparator module includes the following features:

- · Programmable input selection
- Selectable voltage reference
- Programmable output polarity
- Rising/falling output edge interrupts
- CWG1 Auto-shutdown source

23.1 Comparator Overview

A single comparator is shown in Figure 23-1 along with the relationship between the analog input levels and the digital output. When the analog voltage at VIN+ is less than the analog voltage at VIN-, the output of the comparator is a digital low level. When the analog voltage at VIN+ is greater than the analog voltage at VIN-, the output of the comparator is a digital high level.

The comparators available are shown in Table 23-1.

TABLE 23-1:AVAILABLE COMPARATORS

Device	C1	C2
PIC16(L)F15313	•	
PIC16(L)F15323	•	•

FIGURE 23-1:

SINGLE COMPARATOR



26.10 Register Definitions: Timer1 Control

U-0	U-0	R/W-0/u	R/W-0/u	U-0	R/W-0/u	R/W-0/u	R/W-0/u		
	—	CKPS<1:0>		_	SYNC	RD16	ON		
bit 7							bit 0		
									
Legend:									
R = Readable	bit	W = Writable	oit	U = Unimpler	mented bit, read	d as '0'			
u = Bit is uncha	anged	x = Bit is unkn	own	-n/n = Value	at POR and BO	R/Value at all o	other Resets		
'1' = Bit is set		'0' = Bit is clea	ared						
bit 7-6	Unimplemen	ted: Read as ')'						
bit 5-4	CKPS<1:0>:	Timer1 Input C	lock Prescale	Select bits					
	11 = 1:8 Pres	cale value							
	10 = 1:4 Pres	scale value							
	01 = 12 Pres								
hit 3		ted: Read as '	ı'						
bit 2		1 Synchronizat	ion Control bit						
Dit Z	When TMP1(
	This bit is igno	ored. The timer	uses the inter	rnal clock and	no additional sv	nchronization	is performed.		
	<u>ELSE</u>						ie perioriteur		
	0 = Synchron	nize external clo	ock input with	system clock					
	1 = Do not sy	ynchronize exte	ernal clock inp	ut					
bit 1	RD16: 16-bit	Read/Write Mo	de Enable bit						
	0 = Enables register read/write of Timer1 in two 8-bit operation								
h:1 0		register read/w	me of timer1		peration				
bit U	ON: Timer1 C								
	1 = Enables	Limer1	Timor1 goto	flip flop					
	0 = Stops Timer1 and clears Timer1 gate flip-flop								

REGISTER 26-1: T1CON: TIMER1 CONTROL REGISTER

28.4 Register Definitions: CCP Control

Long bit name prefixes for the CCP peripherals are shown in **Section 1.1** "**Register and Bit Naming Conventions**".

TABLE 28-4:LONG BIT NAMES PREFIXESFOR CCP PERIPHERALS

Peripheral	Bit Name Prefix
CCP1	CCP1
CCP2	CCP2

REGISTER 28-1: CCPxCON: CCPx CONTROL REGISTER

R/W-0/0	U-0	R-x	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
EN	—	OUT	FMT		MODE	=<3:0>	
bit 7							bit 0

Legend:						
R = Readable bit		W = Writable bit	U = Unimplemented bit, read as '0'			
u = Bit is unchanged		x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Reset			
'1' = Bit is set		'0' = Bit is cleared				
bit 7	EN: CCPx Module Enable bit 1 = CCPx is enabled 0 = CCPx is disabled					
bit 6	Unimplemented: Read as '0'					
bit 5	OUT: CCPx C					
bit 4 FMT: CCPW (Pulse Width) Alignment bit <u>MODE = Capture mode</u> Unused <u>MODE = Compare mode</u> Unused <u>MODE = PWM mode</u> 1 = Left-aligned format 0 = Right-aligned format						

R/W/HS-0/0	R/W-0/0	R/W-0/0	R/W-1/1	R/W-0/0	R/W-1/1	U-0	U-0	
SHUTDOWN ^(1, 2)	2) REN LSBD<1:0>		LSAC<1:0>		—	—		
bit 7							bit 0	
Legend:	Legend:							
HC = Bit is cleared	d by hardware			HS = Bit is set by hardware				
R = Readable bit W = Writ			bit	U = Unimplemented bit, read as '0'				
u = Bit is unchang	ed	x = Bit is unk	nown	-n/n = Value at POR and BOR/Value at all othe		other Resets		
'1' = Bit is set		'0' = Bit is cle	eared	q = Value depends on condition				
				<i>(</i> , , , , , , , , , , , , , , , , , , ,				
bit 7	7 SHUTDOWN: Auto-Shutdown Event Status bit ^(1, 2)							
1 = An Auto-Shutdown state is in effect								
	0 = No Auto-shutdown event has occurred							
bit 6 REN: Auto-Restart Enable bit								
	1 = Auto-res 0 = Auto-res	tart enabled						
bit 5-4	LSBD<1:0>: CWG1B and CWG1D Auto-Shutdown State Control bits							
	11 = A logic '1' is placed on CWG1B/D when an auto-shutdown event is present							
10 =A logic '0' is placed on CWG1B/D when an auto-shutdown event is pres 01 =Pin is tri-stated on CWG1B/D when an auto-shutdown event is present			t is present					
			resent					
00 = The inactive state of the pin, including polarity, is placed on CWG1B/D after t				B/D after the re	equired dead-			
hit 3-2	t 3-2 I SAC-1:0-: CWG1A and CWG1C Auto-Shutdown State Control hits							
Sit 0 Z	11 = A logic '	=A logic '1' is placed on CWG1A/C when an auto-shutdown event is present						
	10 =A logic '0' is placed on CWG1A/C when an auto-shutdown event is present							
	01 =Pin is tri-	tri-stated on CWG1A/C when an auto-shutdown event is present						
	00 =The inac band in	tive state of th terval	e pin, includin	g polarity, is pla	ced on CWG1	IA/C after the re	equired dead-	
bit 1-0	Unimplemented: Read as '0'							
Note 1: This bit may be written while EN = 0 (CWG1CON0 register) to place the outputs into the shutdown								
configuration.								

REGISTER 30-5: CWG1AS0: CWG1 AUTO-SHUTDOWN CONTROL REGISTER 0

2: The outputs will remain in auto-shutdown state until the next rising edge of the input signal after this bit is cleared.

31.1 CLCx Setup

Programming the CLCx module is performed by configuring the four stages in the logic signal flow. The four stages are:

- · Data selection
- · Data gating
- Logic function selection
- Output polarity

Each stage is setup at run time by writing to the corresponding CLCx Special Function Registers. This has the added advantage of permitting logic reconfiguration on-the-fly during program execution.

31.1.1 DATA SELECTION

There are 40 signals available as inputs to the configurable logic. Four 40-input multiplexers are used to select the inputs to pass on to the next stage.

Data selection is through four multiplexers as indicated on the left side of Figure 31-2. Data inputs in the figure are identified by a generic numbered input name.

Table 31-2 correlates the generic input name to the actual signal for each CLC module. The column labeled 'LCxDyS<4:0> Value' indicates the MUX selection code for the selected data input. LCxDyS is an abbreviation to identify specific multiplexers: LCxD1S<4:0> through LCxD4S<4:0>.

Data inputs are selected with CLCxSEL0 through CLCxSEL3 registers (Register 31-3 through Register 31-6).

TABLE 31-2: CLCx DATA INPUT SELECTION

LCxDyS<4:0> Value	CLCx Input Source
101000 to 111111 [40+]	Reserved
100111 [39]	CWG1B output
100110 [38]	CWG1A output
100101 [37]	Reserved
100100 [36]	Reserved
100011 [35]	MSSP1 SCK output
100010 [34]	MSSP1 SDO output
100001 [33]	Reserved
100000 [32]	Reserved
011111 [31]	EUSART1 (TX/CK) output
011110 [30]	EUSART1 (DT) output
011101 [29]	CLC4 output
011100 [28]	CLC3 output
011011 [27]	CLC2 output
011010 [26]	CLC1 output
011001 [25]	IOCIF
011000 [24]	ZCD output
010111 [23]	C2OUT ⁽¹⁾
010110 [22]	C1OUT
010101 [21]	NCO1 output
010100 [20]	PWM6 output
010011 [19]	PWM5 output
010010 [18]	PWM4 output
010001 [17]	PWM3 output
010000 [16]	CCP2 output
001111 [15]	CCP1 output
001110 [14]	Timer2 overflow
001101 [13]	Timer1 overflow
001100 [12]	Timer0 overflow
001011 [11]	CLKR
001010 [10]	ADCRC
001001 [9]	Reserved
001000 [8]	MFINTOSC (32 kHz)
000111 [7]	MFINTOSC (500 kHz)
000110 [6]	LFINTOSC
000101 [5]	HFINTOSC
000100 [4]	Fosc
000011 [3]	CLCIN3PPS
000010 [2]	CLCIN2PPS
000001 [1]	CLCIN1PPS

Note 1: Present on PIC16(L)F15323 only.

31.2 CLCx Interrupts

An interrupt will be generated upon a change in the output value of the CLCx when the appropriate interrupt enables are set. A rising edge detector and a falling edge detector are present in each CLC for this purpose.

The CLCxIF bit of the associated PIR5 register will be set when either edge detector is triggered and its associated enable bit is set. The LCxINTP enables rising edge interrupts and the LCxINTN bit enables falling edge interrupts. Both are located in the CLCxCON register.

To fully enable the interrupt, set the following bits:

- · CLCxIE bit of the PIE5 register
- LCxINTP bit of the CLCxCON register (for a rising edge detection)
- LCxINTN bit of the CLCxCON register (for a falling edge detection)
- · PEIE and GIE bits of the INTCON register

The CLCxIF bit of the PIR5 register, must be cleared in software as part of the interrupt service. If another edge is detected while this flag is being cleared, the flag will still be set at the end of the sequence.

31.3 Output Mirror Copies

Mirror copies of all LCxCON output bits are contained in the CLCxDATA register. Reading this register reads the outputs of all CLCs simultaneously. This prevents any reading skew introduced by testing or reading the LCxOUT bits in the individual CLCxCON registers.

31.4 Effects of a Reset

The CLCxCON register is cleared to zero as the result of a Reset. All other selection and gating values remain unchanged.

31.5 Operation During Sleep

The CLC module operates independently from the system clock and will continue to run during Sleep, provided that the input sources selected remain active.

The HFINTOSC remains active during Sleep when the CLC module is enabled and the HFINTOSC is selected as an input source, regardless of the system clock source selected.

In other words, if the HFINTOSC is simultaneously selected as the system clock and as a CLC input source, when the CLC is enabled, the CPU will go idle during Sleep, but the CLC will continue to operate and the HFINTOSC will remain active.

This will have a direct effect on the Sleep mode current.

31.6 CLCx Setup Steps

The following steps should be followed when setting up the CLCx:

- Disable CLCx by clearing the LCxEN bit.
- Select desired inputs using CLCxSEL0 through CLCxSEL3 registers (See Table 31-2).
- · Clear any associated ANSEL bits.
- Enable the chosen inputs through the four gates using CLCxGLS0, CLCxGLS1, CLCxGLS2, and CLCxGLS3 registers.
- Select the gate output polarities with the LCxGyPOL bits of the CLCxPOL register.
- Select the desired logic function with the LCxMODE<2:0> bits of the CLCxCON register.
- Select the desired polarity of the logic output with the LCxPOL bit of the CLCxPOL register. (This step may be combined with the previous gate output polarity step).
- If driving a device pin, set the desired pin PPS control register and also clear the TRIS bit corresponding to that output.
- If interrupts are desired, configure the following bits:
 - Set the LCxINTP bit in the CLCxCON register for rising event.
 - Set the LCxINTN bit in the CLCxCON register for falling event.
 - Set the CLCxIE bit of the PIE5 register.
 - Set the GIE and PEIE bits of the INTCON register.
- Enable the CLCx by setting the LCxEN bit of the CLCxCON register.

32.2.3 SPI MASTER MODE

The master can initiate the data transfer at any time because it controls the SCK line. The master determines when the slave (Processor 2, Figure 32-5) is to broadcast data by the software protocol.

In Master mode, the data is transmitted/received as soon as the SSP1BUF register is written to. If the SPI is only going to receive, the SDO output could be disabled (programmed as an input). The SSP1SR register will continue to shift in the signal present on the SDI pin at the programmed clock rate. As each byte is received, it will be loaded into the SSP1BUF register as if a normal received byte (interrupts and Status bits appropriately set). The clock polarity is selected by appropriately programming the CKP bit of the SSP1CON1 register and the CKE bit of the SSP1STAT register. This then, would give waveforms for SPI communication as shown in Figure 32-6, Figure 32-8, Figure 32-9 and Figure 32-10, where the MSB is transmitted first. In Master mode, the SPI clock rate (bit rate) is user programmable to be one of the following:

- Fosc/4 (or Tcy)
- Fosc/16 (or 4 * Tcy)
- Fosc/64 (or 16 * Tcy)
- Timer2 output/2
- Fosc/(4 * (SSP1ADD + 1))

Figure 32-6 shows the waveforms for Master mode.

When the CKE bit is set, the SDO data is valid before there is a clock edge on SCK. The change of the input sample is shown based on the state of the SMP bit. The time when the SSP1BUF is loaded with the received data is shown.







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I²C SLAVE, 7-BIT ADDRESS, RECEPTION (SEN = 0, AHEN = 0, DHEN = 0) FIGURE 32-14:

32.6.10 SLEEP OPERATION

While in Sleep mode, the I²C slave module can receive addresses or data and when an address match or complete byte transfer occurs, wake the processor from Sleep (if the MSSP interrupt is enabled).

32.6.11 EFFECTS OF A RESET

A Reset disables the MSSP module and terminates the current transfer.

32.6.12 MULTI-MASTER MODE

In Multi-Master mode, the interrupt generation on the detection of the Start and Stop conditions allows the determination of when the bus is free. The Stop (P) and Start (S) bits are cleared from a Reset or when the MSSP module is disabled. Control of the I²C bus may be taken when the P bit of the SSP1STAT register is set, or the bus is Idle, with both the S and P bits clear. When the bus is busy, enabling the SSP interrupt will generate the interrupt when the Stop condition occurs.

In multi-master operation, the SDA line must be monitored for arbitration to see if the signal level is the expected output level. This check is performed by hardware with the result placed in the BCL1IF bit.

The states where arbitration can be lost are:

- · Address Transfer
- Data Transfer
- A Start Condition
- A Repeated Start Condition
- An Acknowledge Condition

32.6.13 MULTI -MASTER COMMUNICATION, BUS COLLISION AND BUS ARBITRATION

Multi-Master mode support is achieved by bus arbitration. When the master outputs address/data bits onto the SDA pin, arbitration takes place when the master outputs a '1' on SDA, by letting SDA float high and another master asserts a '0'. When the SCL pin floats high, data should be stable. If the expected data on SDA is a '1' and the data sampled on the SDA pin is '0', then a bus collision has taken place. The master will set the Bus Collision Interrupt Flag, BCL1IF and reset the I²C port to its Idle state (Figure 32-32).

If a transmit was in progress when the bus collision occurred, the transmission is halted, the BF flag is cleared, the SDA and SCL lines are deasserted and the SSP1BUF can be written to. When the user services the bus collision Interrupt Service Routine and if the I²C bus is free, the user can resume communication by asserting a Start condition.

If a Start, Repeated Start, Stop or Acknowledge condition was in progress when the bus collision occurred, the condition is aborted, the SDA and SCL lines are deasserted and the respective control bits in the SSP1CON2 register are cleared. When the user services the bus collision Interrupt Service Routine and if the I^2C bus is free, the user can resume communication by asserting a Start condition.

The master will continue to monitor the SDA and SCL pins. If a Stop condition occurs, the SSP1IF bit will be set.

A write to the SSP1BUF will start the transmission of data at the first data bit, regardless of where the transmitter left off when the bus collision occurred.

In Multi-Master mode, the interrupt generation on the detection of Start and Stop conditions allows the determination of when the bus is free. Control of the I^2C bus can be taken when the P bit is set in the SSP1STAT register, or the bus is Idle and the S and P bits are cleared.

FIGURE 32-32: BUS COLLISION TIMING FOR TRANSMIT AND ACKNOWLEDGE



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