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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

-XF

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	32MHz
Connectivity	I ² C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	12
Program Memory Size	3.5KB (2K x 14)
Program Memory Type	FLASH
EEPROM Size	224 x 8
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 11x10b; D/A 1x5b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	16-UQFN Exposed Pad
Supplier Device Package	16-UQFN (4x4)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16lf15323-e-jq

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

2.3 Master Clear (MCLR) Pin

The MCLR pin provides two specific device functions: Device Reset, and Device Programming and Debugging. If programming and debugging are not required in the end application, a direct connection to VDD may be all that is required. The addition of other components, to help increase the application's resistance to spurious Resets from voltage sags, may be beneficial. A typical configuration is shown in Figure 2-1. Other circuit designs may be implemented, depending on the application's requirements.

During programming and debugging, the resistance and capacitance that can be added to the pin must be considered. Device programmers and debuggers drive the MCLR pin. Consequently, specific voltage levels (VIH and VIL) and fast signal transitions must not be adversely affected. Therefore, specific values of R1 and C1 will need to be adjusted based on the application and PCB requirements. For example, it is recommended that the capacitor, C1, be isolated from the MCLR pin during programming and debugging operations by using a jumper (Figure 2-2). The jumper is replaced for normal run-time operations.

Any components associated with the $\overline{\text{MCLR}}$ pin should be placed within 0.25 inch (6 mm) of the pin.

FIGURE 2-2: EXAMPLE OF MCLR PIN CONNECTIONS



2.4 ICSP[™] Pins

The ICSPCLK and ICSPDAT pins are used for In-Circuit Serial ProgrammingTM (ICSPTM) and debugging purposes. It is recommended to keep the trace length between the ICSP connector and the ICSP pins on the device as short as possible. If the ICSP connector is expected to experience an ESD event, a series resistor is recommended, with the value in the range of a few tens of ohms, not to exceed 100 Ω .

Pull-up resistors, series diodes and capacitors on the ICSPCLK and ICSPDAT pins are not recommended as they will interfere with the programmer/debugger communications to the device. If such discrete components are an application requirement, they should be removed from the circuit during programming and debugging. Alternatively, refer to the AC/DC characteristics and timing requirements information in the respective device Flash programming specification for information on capacitive loading limits, and pin input voltage high (VIH) and input low (VIL) requirements.

For device emulation, ensure that the "Communication Channel Select" (i.e., ICSPCLK/ICSPDAT pins), programmed into the device, matches the physical connections for the ICSP to the Microchip debugger/ emulator tool.

For more information on available Microchip development tools connection requirements, refer to **Section 39.0 "Development Support"**.

TABLE 4-10: SPECIAL FUNCTION REGISTER SUMMARY BANKS 0-63 (CONTINUED)	
--	--

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	V <u>alue o</u> n: MCLR
Bank 2											
	CPU CORE REGISTERS; see Table 4-3 for specifics										
10Ch 118h	Unimplemented									_	—
119h	RC1REG	RC1REG EUSART Receive Data Register									0000 0000
11Ah	Ah TX1REG EUSART Transmit Data Register									0000 0000	0000 0000
11Bh SP1BRGL SP1BRG<7:0>										0000 0000	0000 0000
11Ch	SP1BRGH	H SP1BRG<15:8>								0000 0000	0000 0000
11Dh	RC1STA	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	0000 0000	0000 0000
11Eh	TX1STA	CSRC	TX9	TXEN	SYNC	SENDB	BRGH	TRMT	TX9D	0000 0010	0000 0010
11Fh	BAUD1CON	ABDOVF	RCIDL	_	SCKP	BRG16	_	WUE	ABDEN	01-0 0-00	01-0 0-00

Legend: x = unknown, u = unchanged, q = depends on condition, - = unimplemented, read as '0', r = reserved. Shaded locations unimplemented, read as '0'.

9.4 Fail-Safe Clock Monitor

The Fail-Safe Clock Monitor (FSCM) allows the device to continue operating should the external oscillator fail. The FSCM is enabled by setting the FCMEN bit in the Configuration Words. The FSCM is applicable to all external Oscillator modes (LP, XT, HS, ECL, ECM, ECH.



9.4.1 FAIL-SAFE DETECTION

The FSCM module detects a failed oscillator by comparing the external oscillator to the FSCM sample clock. The sample clock is generated by dividing the LFINTOSC by 64. See Figure 9-8. Inside the fail detector block is a latch. The external clock sets the latch on each falling edge of the external clock. The sample clock clears the latch on each rising edge of the sample clock. A failure is detected when an entire half-cycle of the sample clock elapses before the external clock goes low.

FIGURE 9-9: FSCM TIMING DIAGRAM

9.4.2 FAIL-SAFE OPERATION

When the external clock fails, the FSCM switches the device clock to the HFINTOSC at 1 MHz clock frequency and sets the bit flag OSFIF of the PIR1 register. Setting this flag will generate an interrupt if the OSFIE bit of the PIE1 register is also set. The device firmware can then take steps to mitigate the problems that may arise from a failed clock. The system clock will continue to be sourced from the internal clock source until the device firmware successfully restarts the external oscillator and switches back to external operation, by writing to the NOSC and NDIV bits of the OSCCON1 register.

9.4.3 FAIL-SAFE CONDITION CLEARING

The Fail-Safe condition is cleared after a Reset, executing a SLEEP instruction or changing the NOSC and NDIV bits of the OSCCON1 register. When switching to the external oscillator, or external oscillator and PLL, the OST is restarted. While the OST is running, the device continues to operate from the INTOSC selected in OSCCON1. When the OST times out, the Fail-Safe condition is cleared after successfully switching to the external clock source. The OSFIF bit should be cleared prior to switching to the external clock source. If the Fail-Safe condition still exists, the OSFIF flag will again become set by hardware.

9.4.4 RESET OR WAKE-UP FROM SLEEP

The FSCM is designed to detect an oscillator failure after the Oscillator Start-up Timer (OST) has expired. The OST is used after waking up from Sleep and after any type of Reset. The OST is not used with the EC Clock modes so that the FSCM will be active as soon as the Reset or wake-up has completed. Therefore, the device will always be executing code while the OST is operating.



10.3 Interrupts During Sleep

Interrupts can be used to wake from Sleep. To wake from Sleep, the peripheral must be able to operate without the system clock. The interrupt source must have the appropriate Interrupt Enable bit(s) set prior to entering Sleep.

On waking from Sleep, if the GIE bit is also set, the processor will branch to the interrupt vector. Otherwise, the processor will continue executing instructions after the SLEEP instruction. The instruction directly after the SLEEP instruction will always be executed before branching to the ISR. Refer to **Section 11.0 "Power-Saving Operation Modes"** for more details.

10.4 INT Pin

The INT pin can be used to generate an asynchronous edge-triggered interrupt. Refer to Figure 10-3. This interrupt is enabled by setting the INTE bit of the PIE0 register. The INTEDG bit of the INTCON register determines on which edge the interrupt will occur. When the INTEDG bit is set, the rising edge will cause the interrupt. When the INTEDG bit is clear, the falling edge will cause the interrupt. The INTF bit of the PIR0 register will be set when a valid edge appears on the INT pin. If the GIE and INTE bits are also set, the processor will redirect program execution to the interrupt vector.

10.5 Automatic Context Saving

Upon entering an interrupt, the return PC address is saved on the stack. Additionally, the following registers are automatically saved in the shadow registers:

- W register
- STATUS register (except for TO and PD)
- BSR register
- FSR registers
- PCLATH register

Upon exiting the Interrupt Service Routine, these registers are automatically restored. Any modifications to these registers during the ISR will be lost. If modifications to any of these registers are desired, the corresponding shadow register should be modified and the value will be restored when exiting the ISR. The shadow registers are available in Bank 31 and are readable and writable. Depending on the user's application, other registers may also need to be saved.

PIC16(L)F15313/23

REGISTER 10-14: PIR4: PERIPHERAL INTERRUPT REQUEST REGISTER 4

U-0	U-0	U-0	U-0	U-0	U-0	R/W/HS-0/0	R/W/HS-0/0
_	-			_	_	TMR2IF	TMR1IF
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	HS = Hardware set

bit 7-2	Unimplemented: Read as '0'
bit 1	TRM2IF: Timer2 Interrupt Flag bit
	 1 = The TMR2 postscaler overflowed, or in 1:1 mode, a TMR2 to PR2 match occurred (must be cleared in software) 0 = No TMR2 event has occurred
bit 0	TRM1IF: Timer1 Overflow Interrupt Flag bit 1 = Timer1 overflow occurred (must be cleared in software) 0 = No Timer1 overflow occurred
Note:	Interrupt flag bits are set when an interrupt

Note: Interrupt flag bits are set when an interrupt condition occurs, regardless of the state of its corresponding enable bit or the Global Enable bit, GIE, of the INTCON register. User software should ensure the appropriate interrupt flag bits are clear prior to enabling an interrupt.

16.0 PERIPHERAL MODULE DISABLE

The PIC16(L)F15313/23 provides the ability to disable selected modules, placing them into the lowest possible Power mode.

For legacy reasons, all modules are ON by default following any Reset.

16.1 Disabling a Module

Disabling a module has the following effects:

- All clock and control inputs to the module are suspended; there are no logic transitions, and the module will not function.
- The module is held in Reset:
 - Writing to SFRs is disabled
 - Reads return 00h

16.2 Enabling a module

When the register bit is cleared, the module is reenabled and will be in its Reset state; SFR data will reflect the POR Reset values.

Depending on the module, it may take up to one full instruction cycle for the module to become active. There should be no interaction with the module (e.g., writing to registers) for at least one instruction after it has been re-enabled.

16.3 Disabling a Module

When a module is disabled, all the associated PPS selection registers (Registers xxxPPS Register 15-1, 15-2, and 15-3), are also disabled.

16.4 System Clock Disable

Setting SYSCMD (PMD0, Register 16-1) disables the system clock (Fosc) distribution network to the peripherals. Not all peripherals make use of SYSCLK, so not all peripherals are affected. Refer to the specific peripheral description to see if it will be affected by this bit.

PIC16(L)F15313/23

REGISTER	16-2: PMD	1: PMD CON	ROL REGIS	STER 1				
R/W-0/0	U-0	U-0	U-0	U-0	R/W-0/0	R/W-0/0	R/W-0/0	
NCO1MD		—		—	TMR2MD	TMR1MD	TMR0MD	
bit 7							bit 0	
Legend:								
R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'								
u = Bit is und	hanged	x = Bit is unkr	iown	-n/n = Value a	t POR and BO	R/Value at all c	other Resets	
'1' = Bit is se	t	'0' = Bit is clea	ared	q = Value dep	ends on condit	ion		
bit 7	 7 NCO1MD: Disable Numerically Control Oscillator bit 1 = NCO1 module disabled 0 = NCO1 module enabled 							
bit 6-3	Unimplemer	nted: Read as ')'					
bit 2	TMR2MD: Disable Timer TMR2 bit 1 = Timer2 module disabled 0 = Timer2 module enabled							
bit 1	TMR1MD: Disable Timer TMR1 bit 1 = Timer1 module disabled 0 = Timer1 module enabled							
bit 0	TMR0MD: D 1 = Timer0 r 0 = Timer0 r	isable Timer TM nodule disabled nodule enabled	IR0 bit					



FIGURE 21-2: VOLTAGE REFERENCE OUTPUT BUFFER EXAMPLE



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REGISTER 23-5: CMOUT: COMPARATOR OUTPUT REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	R-0/0	R-0/0
—		_	_	_		MC2OUT	MC10UT
bit 7							bit 0

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-2 Unimplemented: Read as '0'

bit 1 MC2OUT: Mirror Copy of C2OUT bit

bit 0 MC1OUT: Mirror Copy of C1OUT bit

TABLE 23-3: SUMMARY OF REGISTERS ASSOCIATED WITH COMPARATOR MODULE

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page	
CMxCON0	ON	OUT	—	POL	—	—	HYS	SYNC	250	
CMxCON1	—	—	_		_	_	INTP	INTN	251	
CMOUT	—	—	_		_	_	MC2OUT	MC1OUT	253	
FVRCON	FVREN	FVRRDY	TSEN	TSRNG	CDAFV	'R<1:0>	ADFVF	R<1:0>	210	
DAC1CON0	DAC1EN	—	DAC10E1	DAC10E2 DAC1PSS<1:0> — DAC1NSS				232		
DAC1CON1	—	—	_		DAC1R<4:0>					
INTCON	GIE	PEIE	_					INTEDG	121	
PIE2	—	ZCDIE	—	_	—	—	C2IE	C1IE	124	
PIR2	—	ZCDIF	_		_	_	C2IF	C1IF	132	
RxyPPS	—	—	—	RxyPPS<4:0>						
CLCINxPPS	_	_		CLCIN0PPS<5:0>						
T1GPPS	—	_			T1GP	PS<5:0>			191	

Legend: — = unimplemented location, read as '0'. Shaded cells are unused by the comparator module.

PIC16(L)F15313/23

EXAMPLE 24-1:

VRMS = 120 VPEAK =VRMS* $\sqrt{2}$ = 169.7 f = 60 Hz C = 0.1 uF Z = VPEAK/3x10⁻⁴ = 169.7/(3x10⁻⁴) = 565.7 kOhms Xc = 1/(2 Π fC) = 1/(2 Π *60*1*10⁻⁷) = 26.53 kOhms R = $\sqrt{(Z^2 - Xc^2)}$ = 565.1 kOhms (computed) R = 560 kOhms (used) ZR = $\sqrt{(R^2 + Xc^2)}$ = 560.6 kOhms (using actual resistor) IPEAK = VPEAK/ZR = 302.7*10⁻⁶ VC = Xc* IPEAK = 8.0 V Φ = Tan⁻¹(Xc/R) = 0.047 radians T $_{\Phi}$ = $\Phi/(2\Pi$ f) = 125.6 us

24.5.2 CORRECTION BY OFFSET CURRENT

When the waveform is varying relative to Vss, then the zero cross is detected too early as the waveform falls and too late as the waveform rises. When the waveform is varying relative to VDD, then the zero cross is detected too late as the waveform rises and too early as the waveform falls. The actual offset time can be determined for sinusoidal waveforms with the corresponding equations shown in Equation 24-3.

EQUATION 24-3: ZCD EVENT OFFSET

When External Voltage Source is relative to Vss:

$$TOFFSET = \frac{\operatorname{asin}\left(\frac{Vcpinv}{VPEAK}\right)}{2\pi \bullet Freq}$$

When External Voltage Source is relative to VDD:

$$TOFFSET = \frac{\operatorname{asin}\left(\frac{VDD - Vcpinv}{VPEAK}\right)}{2\pi \bullet Freq}$$

This offset time can be compensated for by adding a pull-up or pull-down biasing resistor to the ZCD pin. A pull-up resistor is used when the external voltage source is varying relative to Vss. A pull-down resistor is used when the voltage is varying relative to VDD. The resistor adds a bias to the ZCD pin so that the target external voltage source must go to zero to pull the pin voltage to the VCPINV switching voltage. The pull-up or pull-down value can be determined with the equation shown in Equation 24-4.

EQUATION 24-4: ZCD PULL-UP/DOWN

When External Signal is relative to Vss:

$$R_{PULLUP} = \frac{R_{SERIES}(V_{PULLUP} - V_{cpinv})}{V_{cpinv}}$$

When External Signal is relative to VDD:

$$\left(RPULLDOWN = \frac{RSERIES \times (Vcpinv)}{(VDD - Vcpinv)}\right)$$

24.6 Handling VPEAK variations

If the peak amplitude of the external voltage is expected to vary, the series resistor must be selected to keep the ZCD current source and sink below the design maximum range of $\pm 600 \,\mu$ A and above a reasonable minimum range. A general rule of thumb is that the maximum peak voltage can be no more than six times the minimum peak voltage. To ensure that the maximum current does not exceed $\pm 600 \,\mu$ A and the minimum is at least $\pm 100 \,\mu$ A, compute the series resistance as shown in Equation 24-5. The compensating pull-up for this series resistance can be determined with Equation 24-4 because the pull-up value is not dependent from the peak voltage.

EQUATION 24-5: SERIES R FOR V RANGE

$$R_{SERIES} = \frac{V_{MAXPEAK} + V_{MINPEAK}}{7 \times 10^{-4}}$$

27.5.8 LEVEL RESET, EDGE-TRIGGERED HARDWARE LIMIT ONE-SHOT MODES

In Level -Triggered One-Shot mode the timer count is reset on the external signal level and starts counting on the rising/falling edge of the transition from Reset level to the active level while the ON bit is set. Reset levels are selected as follows:

- Low Reset level (MODE<4:0> = 01110)
- High Reset level (MODE<4:0> = 01111)

When the timer count matches the PRx period count, the timer is reset and the ON bit is cleared. When the ON bit is cleared by either a PRx match or by software control a new external signal edge is required after the ON bit is set to start the counter.

When Level-Triggered Reset One-Shot mode is used in conjunction with the CCP PWM operation the PWM drive goes active with the external signal edge that starts the timer. The PWM drive goes inactive when the timer count equals the CCPRx pulse width count. The PWM drive does not go active when the timer count clears at the PRx period count match.

FIGURE 27-11: LOW LEVEL RESET, EDGE-TRIGGERED HARDWARE LIMIT ONE-SHOT MODE TIMING DIAGRAM (MODE = 01110)



28.2.1 CCPX PIN CONFIGURATION

The software must configure the CCPx pin as an output by clearing the associated TRIS bit and defining the appropriate output pin through the RxyPPS registers. See **Section 15.0 "Peripheral Pin Select (PPS) Module"** for more details.

The CCP output can also be used as an input for other peripherals.

Note: Clearing the CCPxCON register will force the CCPx compare output latch to the default low level. This is not the PORT I/O data latch.

28.2.2 TIMER1 MODE RESOURCE

In Compare mode, Timer1 must be running in either Timer mode or Synchronized Counter mode. The compare operation may not work in Asynchronous Counter mode.

See **Section 26.0 "Timer1 Module with Gate Control"** for more information on configuring Timer1.

Note: Clocking Timer1 from the system clock (Fosc) should not be used in Compare mode. In order for Compare mode to recognize the trigger event on the CCPx pin, TImer1 must be clocked from the instruction clock (Fosc/4) or from an external clock source.

28.2.3 AUTO-CONVERSION TRIGGER

All CCPx modes set the CCP interrupt flag (CCPxIF). When this flag is set and a match occurs, an Auto-conversion Trigger can take place if the CCP module is selected as the conversion trigger source.

Refer to **Section 20.2.4 "Auto-Conversion Trigger"** for more information.

Note:	Removing the match condition by
	changing the contents of the CCPRxH
	and CCPRxL register pair, between the
	clock edge that generates the
	Auto-conversion Trigger and the clock
	edge that generates the Timer1 Reset, will
	preclude the Reset from occurring

28.2.4 COMPARE DURING SLEEP

Since Fosc is shut down during Sleep mode, the Compare mode will not function properly during Sleep, unless the timer is running. The device will wake on interrupt (if enabled).

28.3 PWM Overview

Pulse-Width Modulation (PWM) is a scheme that provides power to a load by switching quickly between fully on and fully off states. The PWM signal resembles a square wave where the high portion of the signal is considered the on state and the low portion of the signal is considered the off state. The high portion, also known as the pulse width, can vary in time and is defined in steps. A larger number of steps applied, which lengthens the pulse width, also supplies more power to the load. Lowering the number of steps applied, which shortens the pulse width, supplies less power. The PWM period is defined as the duration of one complete cycle or the total amount of on and off time combined.

PWM resolution defines the maximum number of steps that can be present in a single PWM period. A higher resolution allows for more precise control of the pulse width time and in turn the power that is applied to the load.

The term duty cycle describes the proportion of the on time to the off time and is expressed in percentages, where 0% is fully off and 100% is fully on. A lower duty cycle corresponds to less power applied and a higher duty cycle corresponds to more power applied.

Figure 28-3 shows a typical waveform of the PWM signal.

28.3.1 STANDARD PWM OPERATION

The standard PWM mode generates a Pulse-Width Modulation (PWM) signal on the CCPx pin with up to ten bits of resolution. The period, duty cycle, and resolution are controlled by the following registers:

- · PR2 registers
- T2CON registers
- CCPRxL registers
- CCPxCON registers

Figure 28-4 shows a simplified block diagram of PWM operation.

Note: The corresponding TRIS bit must be cleared to enable the PWM output on the CCPx pin.

FIGURE 28-3: CC

CCP PWM OUTPUT SIGNAL



30.0 COMPLEMENTARY WAVEFORM GENERATOR (CWG) MODULE

The Complementary Waveform Generator (CWG) produces half-bridge, full-bridge, and steering of PWM waveforms. It is backwards compatible with previous ECCP functions.

The CWG has the following features:

- · Six operating modes:
 - Synchronous Steering mode
 - Asynchronous Steering mode
 - Full-Bridge mode, Forward
 - Full-Bridge mode, Reverse
 - Half-Bridge mode
 - Push-Pull mode
- Output polarity control
- Output steering
 - Synchronized to rising event
 - Immediate effect
- Independent 6-bit rising and falling event deadband timers
 - Clocked dead band
 - Independent rising and falling dead-band enables
- Auto-shutdown control with:
 - Selectable shutdown sources
 - Auto-restart enable
 - Auto-shutdown pin override control

The CWG modules available are shown in Table 30-1.

TABLE 30-1: AVAILABLE CWG MODULES

Device	CWG1
PIC16(L)F15313/23	•

30.1 Fundamental Operation

The CWG module can operate in six different modes, as specified by MODE of the CWG1CON0 register:

- Half-Bridge mode (Figure 30-9)
- Push-Pull mode (Figure 30-2)
 - Full-Bridge mode, Forward (Figure 30-3)
 - Full-Bridge mode, Reverse (Figure 30-3)
- Steering mode (Figure 30-10)
- Synchronous Steering mode (Figure 30-11)

It may be necessary to guard against the possibility of circuit faults or a feedback event arriving too late or not at all. In this case, the active drive must be terminated before the Fault condition causes damage. Thus, all output modes support auto-shutdown, which is covered in **30.10** "Auto-Shutdown".

30.1.1 HALF-BRIDGE MODE

In Half-Bridge mode, two output signals are generated as true and inverted versions of the input as illustrated in Figure 30-9. A non-overlap (dead-band) time is inserted between the two outputs as described in **Section 30.5 "Dead-Band Control"**.

The unused outputs CWG1C and CWG1D drive similar signals, with polarity independently controlled by the POLC and POLD bits of the CWG1CON1 register, respectively.

TABLE 31-4:	SUMMARY OF REGISTERS ASSOCIATED WITH CLCx (continued)	
-------------	---	--

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
CLC4GLS1	—		LC4G2D3T	LC4G2D3N	LC4G2D2T	LC4G2D2N	LC4G2D1T	LC4G2D1N	354
CLC4GLS2	—		LC4G3D3T	LC4G3D3N	LC4G3D2T	LC4G3D2N	LC4G3D1T	LC4G3D1N	355
CLC4GLS3	_	_	LC4G4D3T	LC4G4D3N	LC4G4D2T	LC4G4D2N	LC4G4D1T	LC4G4D1N	356
CLCIN0PPS	_	_		CLCIN0PPS<5:0>					191
CLCIN1PPS	—			CLCIN1PPS<5:0>					191
CLCIN2PPS	_	_		CLCIN2PPS<5:0>					191
CLCIN3PPS	_	_	CLCIN3PPS<5:0>						191

Legend: — = unimplemented, read as '0'. Shaded cells are unused by the CLCx modules.

37.2 Standard Operating Conditions

The standard operating conditions for any device are defined as:	
Operating Voltage: VDDMIN ≤ VDD ≤ VDDMAX Operating Temperature: Ta_MIN ≤ Ta ≤ Ta_MAX	
VDD — Operating Supply Voltage ⁽¹⁾	
PIC16LF15313/23	
VDDMIN (Fosc ≤ 16 MHz) +1.8	V
VDDMIN (Fosc ≤ 32 MHz)	V
VDDMAX	V
PIC16F15313/23	
VDDMIN (Fosc ≤ 16 MHz)	V
VDDMIN (Fosc ≤ 32 MHz)	V
VDDMAX	V
TA — Operating Ambient Temperature Range	
Industrial Temperature	
Ta_min	С
Ta_max	С
Extended Temperature	
Ta_min	С
Ta_max	С
Note 1: See Parameter Supply Voltage, DS Characteristics: Supply Voltage.	

TABLE	37-5:	MEMORY PROGRAMMING S	PECIFICA	TIONS			\bigwedge		
Standard Operating Conditions (unless otherwise stated)									
Param. No.	Sym.	Characteristic	Min.	Тур†	Max.	Units	Conditions		
High Voltage Entry Programming Mode Specifications									
MEM01	V _{IHH}	Voltage on MCLR/VPP pin to enter programming mode	8	_	9	><	(Note 2) Note 3)		
MEM02	I _{PPGM}	Current on MCLR/VPP pin during programming mode		1	_	mA	(Note 2)		
Program	nming Mo	de Specifications					$\overline{}$		
MEM10	V_{BE}	VDD for Bulk Erase		2.7	$- \setminus$	¥			
MEM11	I _{DDPGM}	Supply Current during Programming operation		—	10	mA			
Program	Program Flash Memory Specifications								
MEM30	E _P	Flash Memory Cell Endurance	10k	~	-/	E/W	-40°C ≤ TA ≤ +85°C (Note 1)		
MEM32	T _{P_RET}	Characteristic Retention	-	40		-Year	Provided no other specifications are violated		
MEM33	V _{P_RD}	VDD for Read operation	VDDMIN	\neq $/$	VDOMAX	V			
MEM34	V _{P_REW}	VDD for Row Erase or Write operation	VDOMIN	_	VDDMAX	V			
MEM35	T _{P_REW}	Self-Timed Row Erase or Self-Timed Write		20	2.5	ms			

Data in "Typ" column is at 3.0V, 25° Chaless otherwise stated. These parameters are for design guidance only and are t not tested.

Flash Memory Cell Endurance for the Flash memory is defined as: One Row Erase operation and one Self-Timed Note 1: Write.

Required only if CONFIG4, bit LVP is disabled. 2:

3: The MPLAB® ICD2 does not support variable VPP output. Circuitry to limit the ICD2 VPP voltage must be placed between the ICD2 and target system when programming or debugging with the ICD2.

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37.4 AC Characteristics



8-Lead Plastic Dual In-Line (P) - 300 mil Body [PDIP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



ALTERNATE LEAD DESIGN (VENDOR DEPENDENT)



	INCHES						
Dimension	MIN	NOM	MAX				
Number of Pins	N	8					
Pitch	е	.100 BSC					
Top to Seating Plane	Α	-	-	.210			
Molded Package Thickness	A2	.115	.130	.195			
Base to Seating Plane	A1	.015	-	-			
Shoulder to Shoulder Width	E	.290	.310	.325			
Molded Package Width	E1	.240	.250	.280			
Overall Length	D	.348	.365	.400			
Tip to Seating Plane	L	.115	.130	.150			
Lead Thickness	С	.008	.010	.015			
Upper Lead Width	b1	.040	.060	.070			
Lower Lead Width	b	.014	.018	.022			
Overall Row Spacing §	eB	-	-	.430			

Notes:

- 1. Pin 1 visual index feature may vary, but must be located within the hatched area.
- 2. § Significant Characteristic
- 3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
- 4. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-018D Sheet 2 of 2

14-Lead Plastic Thin Shrink Small Outline (ST) - 4.4 mm Body [TSSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging





Microchip Technology Drawing C04-087C Sheet 1 of 2

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