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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | PIC |
| Core Size | 8-Bit |
| Speed | 32MHz |
| Connectivity | I²C, LINbus, SPI, UART/USART |
| Peripherals | Brown-out Detect/Reset, POR, PWM, WDT |
| Number of I/O | 12 |
| Program Memory Size | 3.5KB (2K x 14) |
| Program Memory Type | FLASH |
| EEPROM Size | 224 x 8 |
| RAM Size | 256 x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.8V ~ 3.6V |
| Data Converters | A/D 11x10b; D/A 1x5b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 125°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 14-SOIC (0.154", 3.90mm Width) |
| Supplier Device Package | 14-SOIC |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/pic16lf15323-e-sl |

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**TABLE 4-10: SPECIAL FUNCTION REGISTER SUMMARY BANKS 0-63 (CONTINUED)**

| Address | Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Value on: POR, BOR | Value on: MCLR |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **Bank 7** | | | | | | | | | | | |
| CPU CORE REGISTERS; see Table 4-3 for specifics | | | | | | | | | | | |
| 38Ch | PWM6DCL | DC<1:0> | | — | — | — | — | — | — | xx-- ---- | uu-- ---- |
| 38Dh | PWM6DCH | DC<9:0> | | | | | | | | xxxx xxxx | uuuu uuuu |
| 38Eh | PWM6CON | EN | — | OUT | POL | — | — | — | — | 0-00 ---- | 0-00 ---- |
| 38Fh — 39Fh | — | Unimplemented | | | | | | | | — | — |

**Legend:** x = unknown, u = unchanged, q = depends on condition, - = unimplemented, read as '0', r = reserved. Shaded locations unimplemented, read as '0'.

**REGISTER 5-7: REVISIONID: REVISION ID REGISTER**

| R | R | R | R | R | R | R | R | R | R | R | R | R | R |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | 0 | MJRREV<5:0> | | | | | | MNRREV<5:0> | | | | | |
| bit 13 | | | | | | | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| | R = Readable bit | | |
| | '0' = Bit is cleared | '1' = Bit is set | x = Bit is unknown |

bit 13-12 **Fixed Value**: Read-only bits
These bits are fixed with value '10' for all devices included in this data sheet.

bit 11-6 **MJRREV<5:0>**: Major Revision ID bits
These bits are used to identify a major revision.

bit 5-0 **MNRREV<5:0>**: Minor Revision ID bits
These bits are used to identify a minor revision.

## 8.4 Low-Power Brown-out Reset (LPBOR)

The Low-Power Brown-out Reset (LPBOR) is an important part of the Reset subsystem. Refer to Figure 8-1 to see how the BOR and LPBOR interact with other modules.

The LPBOR is used to monitor the external VDD pin. When too low of a voltage is detected, the device is held in Reset.

### 8.4.1 ENABLING LPBOR

The LPBOR is controlled by the $\overline{\text{LPBOR}}$ bit of the Configuration Word (Register 5-1). When the device is erased, the LPBOR module defaults to disabled.

### 8.4.2 LPBOR MODULE OUTPUT

The output of the LPBOR module is a signal indicating whether or not a Reset is to be asserted. When this occurs, a register bit ($\overline{\text{BOR}}$) is changed to indicate that a BOR Reset has occurred. The same bit is set for either the BOR or the LPBOR (refer to Register 8-3). This signal is OR'd with the output of the BOR module to provide the generic $\overline{\text{BOR}}$ signal, which goes to the PCON register and to the power control block. Refer to Figure 8-1 for the OR gate connections of the BOR and LPBOR Reset signals, which eventually generates one common BOR Reset.

## 8.5 $\overline{\text{MCLR}}$

The $\overline{\text{MCLR}}$ is an optional external input that can reset the device. The $\overline{\text{MCLR}}$ function is controlled by the MCLRE bit of Configuration Words and the LVP bit of Configuration Words (Table 8-2).

**TABLE 8-2: $\overline{\text{MCLR}}$ CONFIGURATION**

| MCLRE | LVP | $\overline{\text{MCLR}}$ |
|---|---|---|
| 0 | 0 | Disabled |
| 1 | 0 | Enabled |
| x | 1 | Enabled |

### 8.5.1 $\overline{\text{MCLR}}$ ENABLED

When $\overline{\text{MCLR}}$ is enabled and the pin is held low, the device is held in Reset. The $\overline{\text{MCLR}}$ pin is connected to VDD through an internal weak pull-up. Refer to **Section 2.3 "Master Clear (MCLR) Pin"** for recommended $\overline{\text{MCLR}}$ connections.

The device has a noise filter in the $\overline{\text{MCLR}}$ Reset path. The filter will detect and ignore small pulses.

**Note:** A Reset does not drive the $\overline{\text{MCLR}}$ pin low.

### 8.5.2 $\overline{\text{MCLR}}$ DISABLED

When $\overline{\text{MCLR}}$ is disabled, the pin functions as a general purpose input and the internal weak pull-up is under software control. See **Section 14.1 "I/O Priorities"** for more information.

## 8.6 Windowed Watchdog Timer (WWDT) Reset

The Watchdog Timer generates a Reset if the firmware does not issue a CLRWDT instruction within the time-out period and the window is open. The $\overline{\text{TO}}$ and $\overline{\text{PD}}$ bits in the STATUS register and the $\overline{\text{WDT}}$ bit in PCON are changed to indicate a WDT Reset caused by the timer overflowing, and WDTWV bit in the PCON register is changed to indicate a WDT Reset caused by a window violation. See **Section 12.0 "Windowed Watchdog Timer (WWDT)"** for more information.

## 8.7 RESET Instruction

A RESET instruction will cause a device Reset. The $\overline{\text{RI}}$ bit in the PCON register will be set to '0'. See Table 8-4 for default conditions after a RESET instruction has occurred.

## 8.8 Stack Overflow/Underflow Reset

The device can reset when the Stack Overflows or Underflows. The STKOVF or STKUNF bits of the PCON register indicate the Reset condition. These Resets are enabled by setting the STVREN bit in Configuration Words. See **Section 4.5.2 "Overflow/Underflow Reset"** for more information.

## 8.9 Programming Mode Exit

Upon exit of In-Circuit Serial Programming™ (ICSP™) mode, the device will behave as if a POR had just occurred (the device does not reset upon run time self-programming/erase operations).

## 8.10 Power-up Timer

The Power-up Timer optionally delays device execution after a BOR or POR event. This timer is typically used to allow VDD to stabilize before allowing the device to start running.

The Power-up Timer is controlled by the $\overline{\text{PWRTE}}$ bit of the Configuration Words.

The Power-up Timer provides a nominal 64 ms time out on POR or Brown-out Reset. The device is held in Reset as long as PWRT is active. The PWRT delay allows additional time for the VDD to rise to an acceptable level. The Power-up Timer is enabled by clearing the $\overline{\text{PWRTE}}$ bit in the Configuration Words. The Power-up Timer starts after the release of the POR and BOR. For additional information, refer to Application Note AN607, "*Power-up Trouble Shooting*" (DS00607).

## 10.0 INTERRUPTS

The interrupt feature allows certain events to preempt normal program flow. Firmware is used to determine the source of the interrupt and act accordingly. Some interrupts can be configured to wake the MCU from Sleep mode.

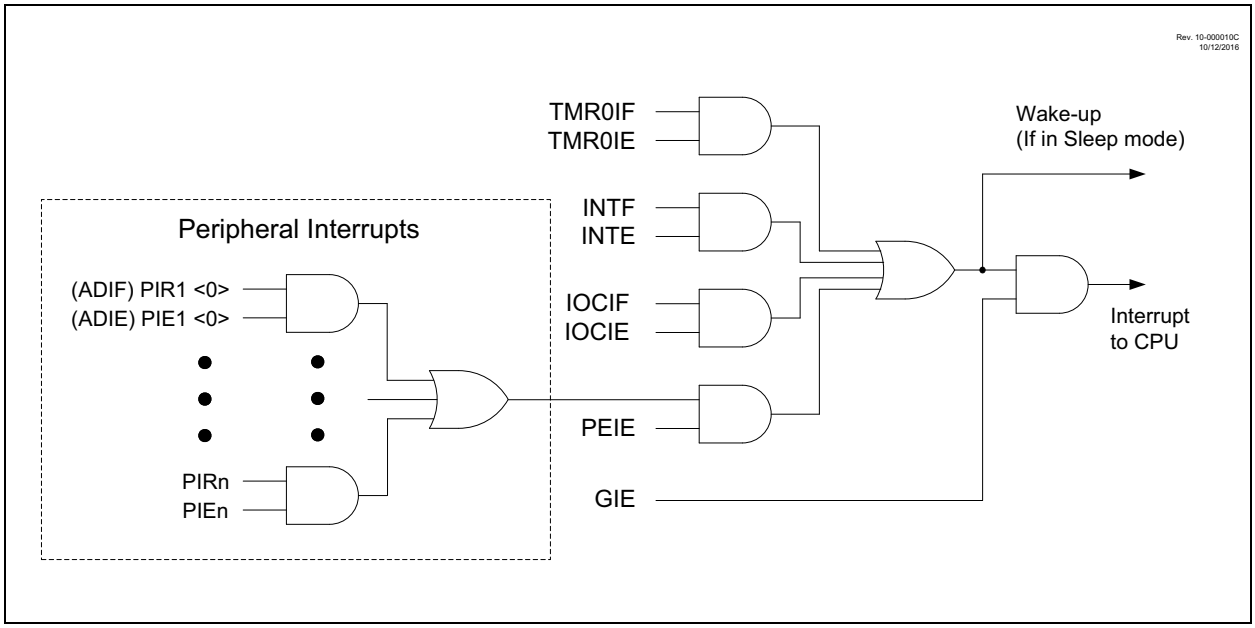
This chapter contains the following information for Interrupts:

- Operation
- Interrupt Latency
- Interrupts During Sleep
- INT Pin
- Automatic Context Saving

Many peripherals produce interrupts. Refer to the corresponding chapters for details.

A block diagram of the interrupt logic is shown in Figure 10-1.

**FIGURE 10-1: INTERRUPT LOGIC**



**REGISTER 10-10: PIR0: PERIPHERAL INTERRUPT STATUS REGISTER 0**

| U-0 | U-0 | R/W/HS-0/0 | R-0 | U-0 | U-0 | U-0 | R/W/HS-0/0 |
|---|---|---|---|---|---|---|---|
| — | — | TMR0IF | IOCIF | — | — | — | INTF(1) |
| bit 7 | | | | | | | bit 0 |

| Legend: | | |
|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' |
| u = Bit is unchanged | x = Bit is unknown | -n/n = Value at POR and BOR/Value at all other Resets |
| '1' = Bit is set | '0' = Bit is cleared | HS= Hardware Set |

bit 7-6 **Unimplemented:** Read as '0'

bit 5 **TMR0IF:** Timer0 Overflow Interrupt Flag bit
- 1 = Timer0 register has overflowed (must be cleared in software)
- 0 = Timer0 register did not overflow

bit 4 **IOCIF:** Interrupt-on-Change Interrupt Flag bit (read-only)(2)
- 1 = One or more of the IOCAF-IOCEF register bits are currently set, indicating an enabled edge was detected by the IOC module.
- 0 = None of the IOCAF-IOCEF register bits are currently set

bit 3-1 **Unimplemented:** Read as '0'

bit 0 **INTF:** INT External Interrupt Flag bit(1)
- 1 = The INT external interrupt occurred (must be cleared in software)
- 0 = The INT external interrupt did not occur

**Note 1:** The External Interrupt GPIO pin is selected by INTPPS (Register 15-1).

**2:** The IOCIF bit is the logical OR of all the IOCAF-IOCEF flags. Therefore, to clear the IOCIF flag, application firmware must clear all of the lower level IOCAF-IOCEF register bits.

**Note:** Interrupt flag bits are set when an interrupt condition occurs, regardless of the state of its corresponding enable bit or the Global Enable bit, GIE, of the INTCON register. User software should ensure the appropriate interrupt flag bits are clear prior to enabling an interrupt.

**REGISTER 11-2: CPUDOZE: DOZE AND IDLE REGISTER**

| R/W-0/u | R/W/HC/HS-0/0 | R/W-0/0 | R/W-0/0 | U-0 | R/W-0/0 | R/W-0/0 | R/W-0/0 |
|---|---|---|---|---|---|---|---|
| IDLEN | DOZEN(1,2) | ROI | DOE | — | DOZE<2:0> | | |
| bit 7 | | | | | | | bit 0 |

| Legend: | | |
|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ |
| u = Bit is unchanged | x = Bit is unknown | -n/n = Value at POR and BOR/Value at all other Resets |
| ‘1’ = Bit is set | ‘0’ = Bit is cleared | |

bit 7 **IDLEN:** Idle Enable bit
1 = A SLEEP instruction inhibits the CPU clock, but not the peripheral clock(s)
0 = A SLEEP instruction places the device into full Sleep mode

bit 6 **DOZEN:** Doze Enable bit(1,2)
1 = The CPU executes instruction cycles according to DOZE setting
0 = The CPU executes all instruction cycles (fastest, highest power operation)

bit 5 **ROI:** Recover-on-Interrupt bit
1 = Entering the Interrupt Service Routine (ISR) makes DOZEN = 0 bit, bringing the CPU to full-speed operation.
0 = Interrupt entry does not change DOZEN

bit 4 **DOE:** Doze on Exit bit
1 = Executing RETFIE makes DOZEN = 1, bringing the CPU to reduced speed operation.
0 = RETFIE does not change DOZEN

bit 3 **Unimplemented:** Read as ‘0’

bit 2-0 **DOZE<2:0>:** Ratio of CPU Instruction Cycles to Peripheral Instruction Cycles
111 =1:256
110 =1:128
101 =1:64
100 =1:32
011 =1:16
010 =1:8
001 =1:4
000 =1:2

**Note 1:** When ROI = 1 or DOE = 1, DOZEN is changed by hardware interrupt entry and/or exit.
**2:** Entering ICD overrides DOZEN, returning the CPU to full execution speed; this bit is not affected.

**TABLE 15-3: PPS INPUT REGISTER VALUES**

| Desired Input Pin | Value to Write to Register |
|---|---|
| RA0 | 0x00 |
| RA1 | 0x01 |
| RA2 | 0x02 |
| RA3 | 0x03 |
| RA4 | 0x04 |
| RA5 | 0x05 |
| RC0(1) | 0x10 |
| RC1(1) | 0x11 |
| RC2(1) | 0x12 |
| RC3(1) | 0x13 |
| RC4(1) | 0x14 |
| RC5(1) | 0x15 |

**Note 1:** Present on PIC16(L)F15323 only.

**REGISTER 17-3: IOCAF: INTERRUPT-ON-CHANGE PORTA FLAG REGISTER**

| U-0 | U-0 | R/W/HS-0/0 | R/W/HS-0/0 | R/W/HS-0/0 | R/W/HS-0/0 | R/W/HS-0/0 | R/W/HS-0/0 |
|---|---|---|---|---|---|---|---|
| — | — | IOCAF5 | IOCAF4 | IOCAF3 | IOCAF2 | IOCAF1(1) | IOCAF0(1) |
| bit 7 | | | | | | | bit 0 |

| Legend: | | |
|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' |
| u = Bit is unchanged | x = Bit is unknown | -n/n = Value at POR and BOR/Value at all other Resets |
| '1' = Bit is set | '0' = Bit is cleared | HS - Bit is set in hardware |

bit 7-6 **Unimplemented:** read as '0'

bit 5-0 **IOCAF<5:0>:** Interrupt-on-Change PORTA Flag bits
1 = An enabled change was detected on the associated pin.
Set when IOCAPx = 1 and a rising edge was detected on RAx, or when IOCANx = 1 and a falling edge was detected on RAx.
0 = No change was detected, or the user cleared the detected change.

**Note 1:** If the debugger is enabled, these bits are not available for use.

## 18.3 Register Definitions: FVR Control

**REGISTER 18-1: FVRCON: FIXED VOLTAGE REFERENCE CONTROL REGISTER**

| R/W-0/0 | R-q/q | R/W-0/0 | R/W-0/0 | R/W-0/0 | R/W-0/0 | R/W-0/0 | R/W-0/0 |
|---|---|---|---|---|---|---|---|
| FVREN | FVRRDY(1) | TSEN(3) | TSRNG(3) | CDAFVR<1:0> | | ADFVR<1:0> | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | |
|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' |
| u = Bit is unchanged | x = Bit is unknown | -n/n = Value at POR and BOR/Value at all other Resets |
| '1' = Bit is set | '0' = Bit is cleared | q = Value depends on condition |

bit 7 **FVREN:** Fixed Voltage Reference Enable bit
1 = Fixed Voltage Reference is enabled
0 = Fixed Voltage Reference is disabled

bit 6 **FVRRDY:** Fixed Voltage Reference Ready Flag bit(1)
1 = Fixed Voltage Reference output is ready for use
0 = Fixed Voltage Reference output is not ready or not enabled

bit 5 **TSEN:** Temperature Indicator Enable bit(3)
1 = Temperature Indicator is enabled
0 = Temperature Indicator is disabled

bit 4 **TSRNG:** Temperature Indicator Range Selection bit(3)
1 = Temperature in High Range VOUT = 3VT
0 = Temperature in Low Range VOUT = 2VT

bit 3-2 **CDAFVR<1:0>:** Comparator FVR Buffer Gain Selection bits
11 = Comparator FVR Buffer Gain is 4x, (4.096V)(2)
10 = Comparator FVR Buffer Gain is 2x, (2.048V)(2)
01 = Comparator FVR Buffer Gain is 1x, (1.024V)
00 = Comparator FVR Buffer is off

bit 1-0 **ADFVR<1:0>:** ADC FVR Buffer Gain Selection bit
11 = ADC FVR Buffer Gain is 4x, (4.096V)(2)
10 = ADC FVR Buffer Gain is 2x, (2.048V)(2)
01 = ADC FVR Buffer Gain is 1x, (1.024V)
00 = ADC FVR Buffer is off

**Note 1:** FVRRDY is always '1'.
**2:** Fixed Voltage Reference output cannot exceed VDD.
**3:** See **Section 19.0 "Temperature Indicator Module"** for additional information.

## 23.0 COMPARATOR MODULE

Comparators are used to interface analog circuits to a digital circuit by comparing two analog voltages and providing a digital indication of their relative magnitudes. Comparators are very useful mixed signal building blocks because they provide analog functionality independent of program execution. The analog comparator module includes the following features:

- Programmable input selection
- Selectable voltage reference
- Programmable output polarity
- Rising/falling output edge interrupts
- CWG1 Auto-shutdown source

### 23.1 Comparator Overview

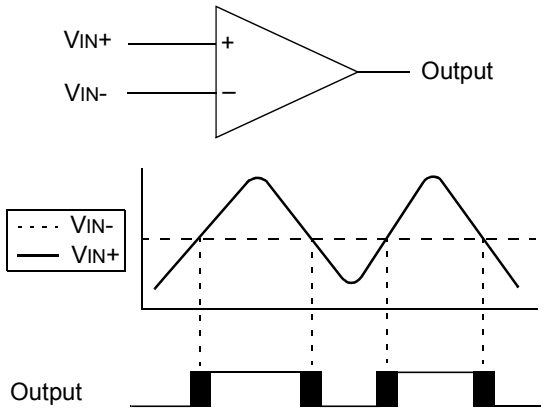
A single comparator is shown in Figure 23-1 along with the relationship between the analog input levels and the digital output. When the analog voltage at VIN+ is less than the analog voltage at VIN-, the output of the comparator is a digital low level. When the analog voltage at VIN+ is greater than the analog voltage at VIN-, the output of the comparator is a digital high level.

The comparators available are shown in Table 23-1.

**TABLE 23-1: AVAILABLE COMPARATORS**

| Device | C1 | C2 |
|---|---|---|
| PIC16(L)F15313 | • | |
| PIC16(L)F15323 | • | • |

**FIGURE 23-1: SINGLE COMPARATOR**

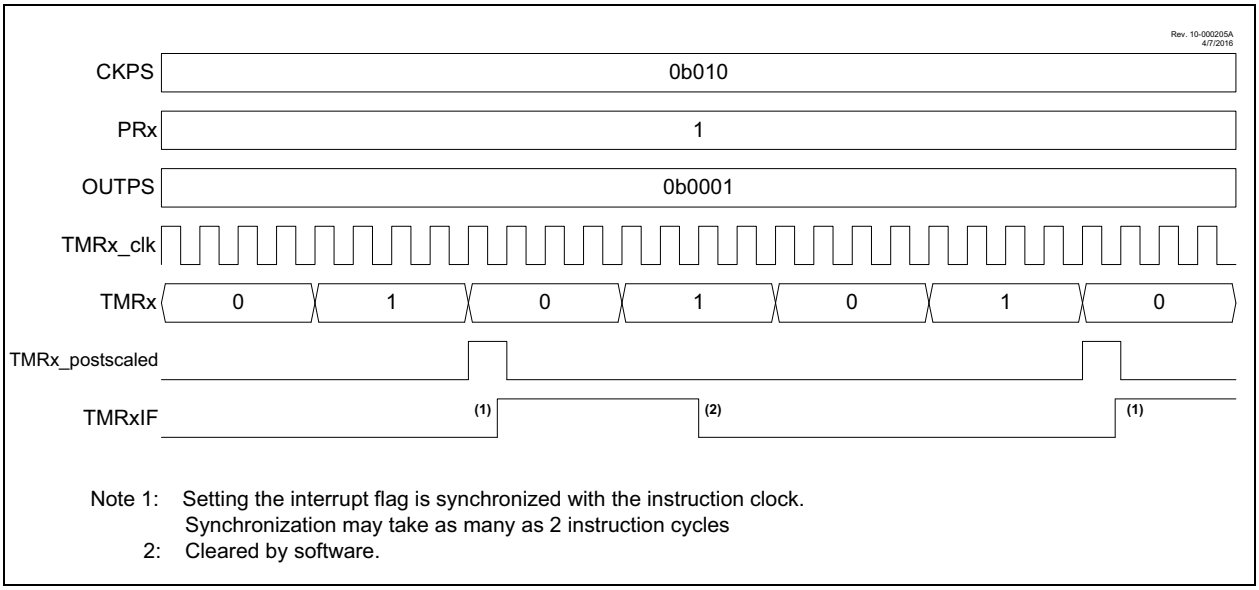



**Note:** The black areas of the output of the comparator represents the uncertainty due to input offsets and response time.

## 27.4 Timer2 Interrupt

Timer2 can also generate a device interrupt. The interrupt is generated when the postscaler counter matches one of 16 postscale options (from 1:1 through 1:16), which are selected with the postscaler control bits, OUTPS<3:0> of the T2CON register. The interrupt is enabled by setting the TMR2IE interrupt enable bit of the PIE4 register. Interrupt timing is illustrated in Figure 27-3.

**FIGURE 27-3: TIMER2 PRESCALER, POSTSCALER, AND INTERRUPT TIMING DIAGRAM**




Note 1: Setting the interrupt flag is synchronized with the instruction clock. Synchronization may take as many as 2 instruction cycles
2: Cleared by software.

## 27.5 Operation Examples

Unless otherwise specified, the following notes apply to the following timing diagrams:

- Both the prescaler and postscaler are set to 1:1 (both the CKPS and OUTPS bits in the TxCON register are cleared).
- The diagrams illustrate any clock except Fosc/4 and show clock-sync delays of at least two full cycles for both ON and Timer2_ers. When using Fosc/4, the clock-sync delay is at least one instruction period for Timer2_ers; ON applies in the next instruction period.
- The PWM Duty Cycle and PWM output are illustrated assuming that the timer is used for the PWM function of the CCP module as described in **Section 28.0 "Capture/Compare/PWM Modules"**. The signals are not a part of the Timer2 module.

### 27.5.1 SOFTWARE GATE MODE

This mode corresponds to legacy Timer2 operation. The timer increments with each clock input when ON = 1 and does not increment when ON = 0. When the TMRx count equals the PRx period count the timer resets on the next clock and continues counting from 0. Operation with the ON bit software controlled is illustrated in Figure 27-4. With PRx = 5, the counter advances until TMRx = 5, and goes to zero with the next clock.

**REGISTER 27-4: T2RST: TIMER2 EXTERNAL RESET SIGNAL SELECTION REGISTER**

| U-0 | U-0 | U-0 | U-0 | R/W-0/0 | R/W-0/0 | R/W-0/0 | R/W-0/0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | RSEL<3:0> | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | |
|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ |
| u = Bit is unchanged | x = Bit is unknown | -n/n = Value at POR and BOR/Value at all other Resets |
| ‘1’ = Bit is set | ‘0’ = Bit is cleared | |

bit 7-4 **Unimplemented:** Read as ‘0’

bit 3-0 **RSEL<3:0>:** Timer2 External Reset Signal Source Selection bits

1111 = Reserved
1101 = LC4_out
1100 = LC3_out
1011 = LC2_out
1010 = LC1_out
1001 = ZCD1_output
1000 = C2OUT_sync(1)
0111 = C1OUT_sync
0110 = PWM6_out
0101 = PWM5_out
0100 = PWM4_out
0011 = PWM3_out
0010 = CCP2_out
0001 = CCP1_out
0000 = T2INPPS

**Note 1:** Present on PIC16(L)F15323 only. Reserved for the PIC16(L)F15313.

**TABLE 27-2: SUMMARY OF REGISTERS ASSOCIATED WITH TIMER2**

| Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Register on Page |
|---|---|---|---|---|---|---|---|---|---|
| CCP1CON | EN | — | OUT | FMT | MODE<3:0> | | | | 306 |
| CCP2CON | EN | — | OUT | FMT | MODE<3:0> | | | | 306 |
| INTCON | GIE | PEIE | — | — | — | — | — | INTEDG | 121 |
| PIE1 | OSFIE | CSWIE | — | — | — | — | — | ADIE | 123 |
| PIR1 | OSFIF | CSWIF | — | — | — | — | — | ADIF | 131 |
| PR2 | Timer2 Module Period Register | | | | | | | | 280* |
| TMR2 | Holding Register for the 8-bit TMR2 Register | | | | | | | | 280* |
| T2CON | ON | CKPS<2:0> | | | OUTPS<3:0> | | | | 295 |
| T2CLKCON | — | — | — | — | CS<3:0> | | | | 294 |
| T2RST | — | — | — | — | RSEL<3:0> | | | | 297 |
| T2HLT | PSYNC | CKPOL | CKSYNC | MODE<4:0> | | | | | 296 |

**Legend:** — = unimplemented location, read as '0'. Shaded cells are not used for Timer2 module.

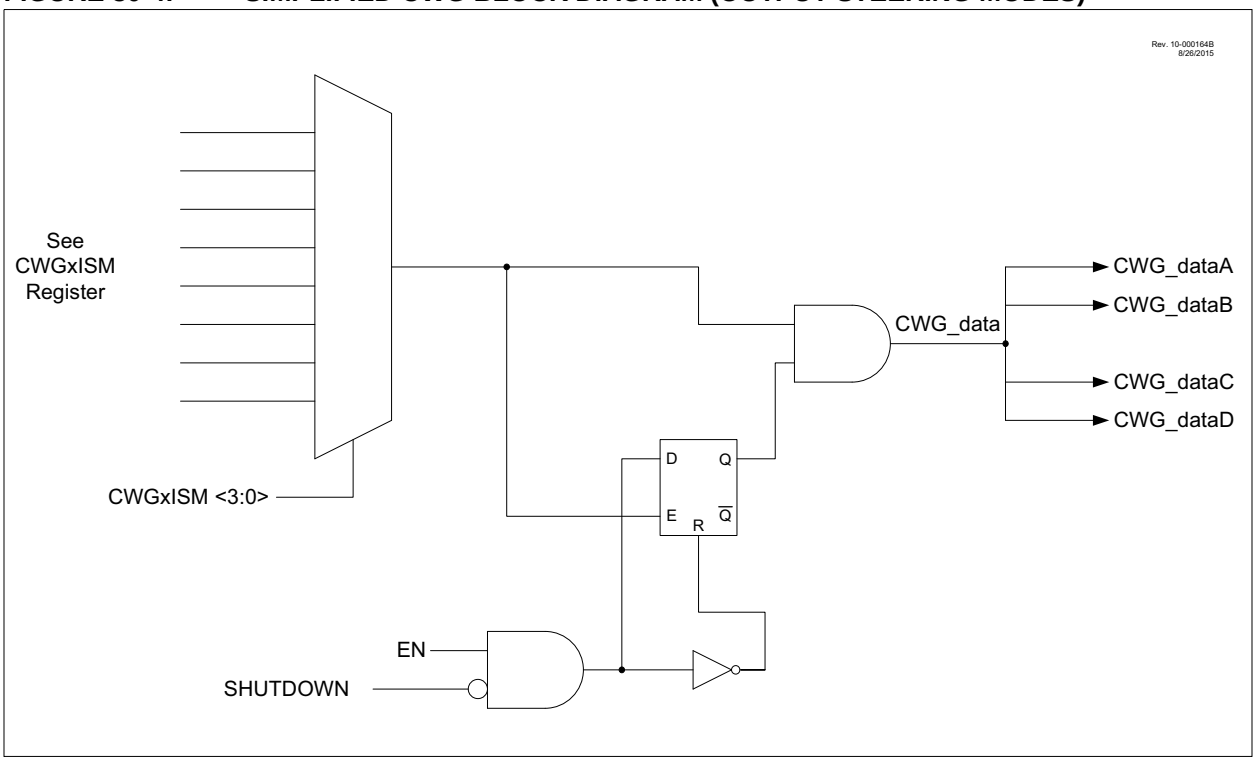
* Page provides register information.

### 30.1.4 STEERING MODES

In Steering modes, the data input can be steered to any or all of the four CWG output pins. In Synchronous Steering mode, changes to steering selection registers take effect on the next rising input.

In Non-Synchronous mode, steering takes effect on the next instruction cycle. Additional details are provided in **Section 30.9 “CWG Steering Mode”**.

**FIGURE 30-4: SIMPLIFIED CWG BLOCK DIAGRAM (OUTPUT STEERING MODES)**




## 30.2 Clock Source

The CWG module allows the following clock sources to be selected:

- Fosc (system clock)
- HFINTOSC (16 MHz only)

The clock sources are selected using the CS bit of the CWG1CLKCON register.

## 33.2 Clock Accuracy with Asynchronous Operation

The factory calibrates the internal oscillator block output (INTOSC). However, the INTOSC frequency may drift as $V_{DD}$ or temperature changes, and this directly affects the asynchronous baud rate. Two methods may be used to adjust the baud rate clock, but both require a reference clock source of some kind.

The first (preferred) method uses the OSCTUNE register to adjust the INTOSC output. Adjusting the value in the OSCTUNE register allows for fine resolution changes to the system clock source. See **Section 9.2.2.2 "Internal Oscillator Frequency Adjustment"** for more information.

The other method adjusts the value in the Baud Rate Generator. This can be done automatically with the Auto-Baud Detect feature (see **Section 33.3.1 "Auto-Baud Detect"**). There may not be fine enough resolution when adjusting the Baud Rate Generator to compensate for a gradual change in the peripheral clock frequency.

#### 33.4.1.6 Slave Clock

Synchronous data transfers use a separate clock line, which is synchronous with the data. A device configured as a slave receives the clock on the TX/CK line. The TX/CK pin output driver is automatically disabled when the device is configured for synchronous slave transmit or receive operation. Serial data bits change on the leading edge to ensure they are valid at the trailing edge of each clock. One data bit is transferred for each clock cycle. Only as many clock cycles should be received as there are data bits.

| | |
|---|---|
| **Note:** | If the device is configured as a slave and the TX/CK function is on an analog pin, the corresponding ANSEL bit must be cleared. |

#### 33.4.1.7 Receive Overrun Error

The receive FIFO buffer can hold two characters. An overrun error will be generated if a third character, in its entirety, is received before RC1REG is read to access the FIFO. When this happens the OERR bit of the RC1STA register is set. Previous data in the FIFO will not be overwritten. The two characters in the FIFO buffer can be read, however, no additional characters will be received until the error is cleared. The OERR bit can only be cleared by clearing the overrun condition. If the overrun error occurred when the SREN bit is set and CREN is clear then the error is cleared by reading RC1REG. If the overrun occurred when the CREN bit is set then the error condition is cleared by either clearing the CREN bit of the RC1STA register or by clearing the SPEN bit which resets the EUSART.

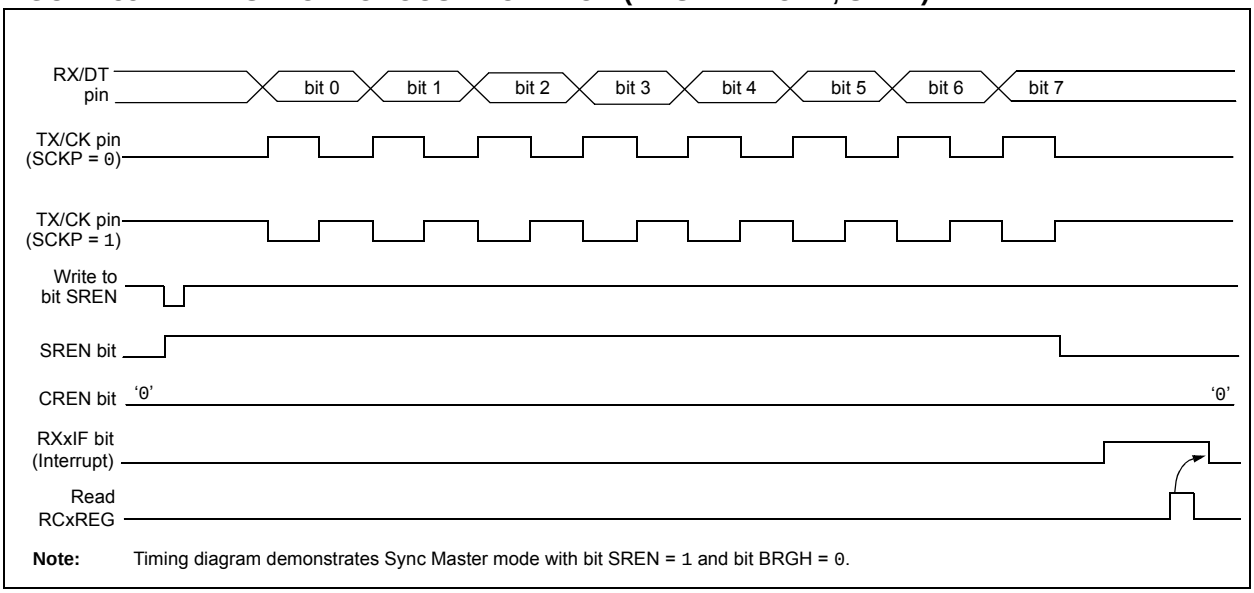
#### 33.4.1.8 Receiving 9-bit Characters

The EUSART supports 9-bit character reception. When the RX9 bit of the RC1STA register is set the EUSART will shift nine bits into the RSR for each character received. The RX9D bit of the RC1STA register is the ninth, and Most Significant, data bit of the top unread character in the receive FIFO. When reading 9-bit data from the receive FIFO buffer, the RX9D data bit must be read before reading the eight Least Significant bits from the RC1REG.

#### 33.4.1.9 Synchronous Master Reception Set-up:

1. Initialize the SP1BRGH, SP1BRGL register pair for the appropriate baud rate. Set or clear the BRGH and BRG16 bits, as required, to achieve the desired baud rate.
2. Clear the ANSEL bit for the RX pin (if applicable).
3. Enable the synchronous master serial port by setting bits SYNC, SPEN and CSRC.
4. Ensure bits CREN and SREN are clear.
5. If interrupts are desired, set the RX1IE bit of the PIE3 register and the GIE and PEIE bits of the INTCON register.
6. If 9-bit reception is desired, set bit RX9.
7. Start reception by setting the SREN bit or for continuous reception, set the CREN bit.
8. Interrupt flag bit RX1IF will be set when reception of a character is complete. An interrupt will be generated if the enable bit RX1IE was set.
9. Read the RC1STA register to get the ninth bit (if enabled) and determine if any error occurred during reception.
10. Read the 8-bit received data by reading the RC1REG register.
11. If an overrun error occurs, clear the error by either clearing the CREN bit of the RC1STA register or by clearing the SPEN bit which resets the EUSART.

**FIGURE 33-12: SYNCHRONOUS RECEPTION (MASTER MODE, SREN)**




**Note:** Timing diagram demonstrates Sync Master mode with bit SREN = 1 and bit BRGH = 0.

**FIGURE 34-1: CLOCK REFERENCE BLOCK DIAGRAM**

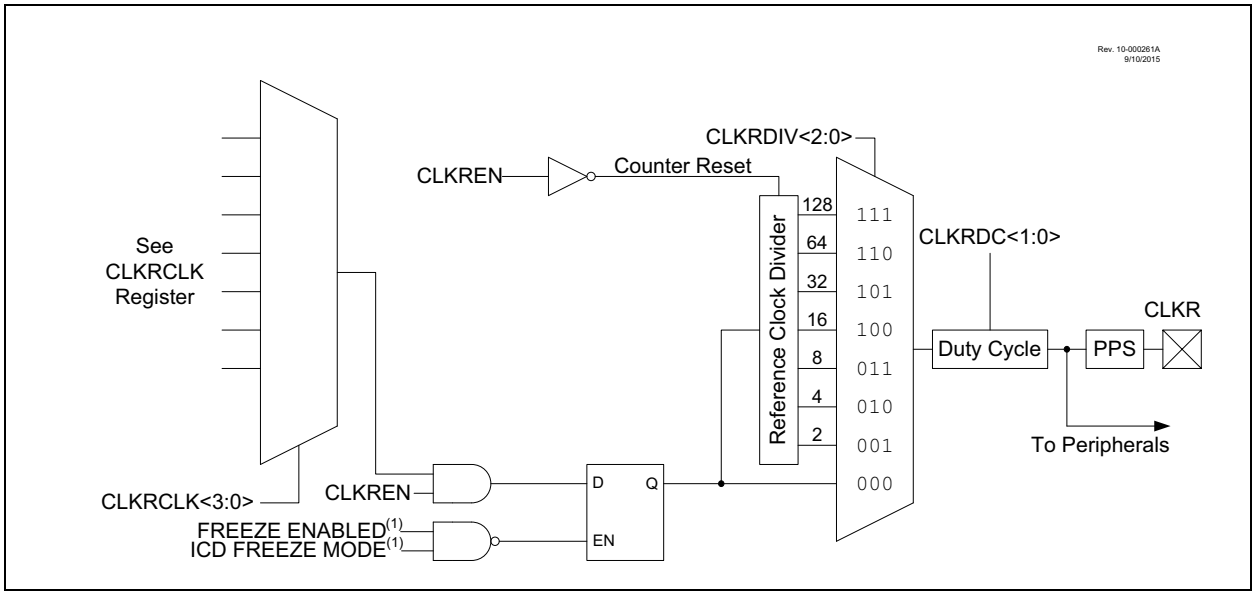
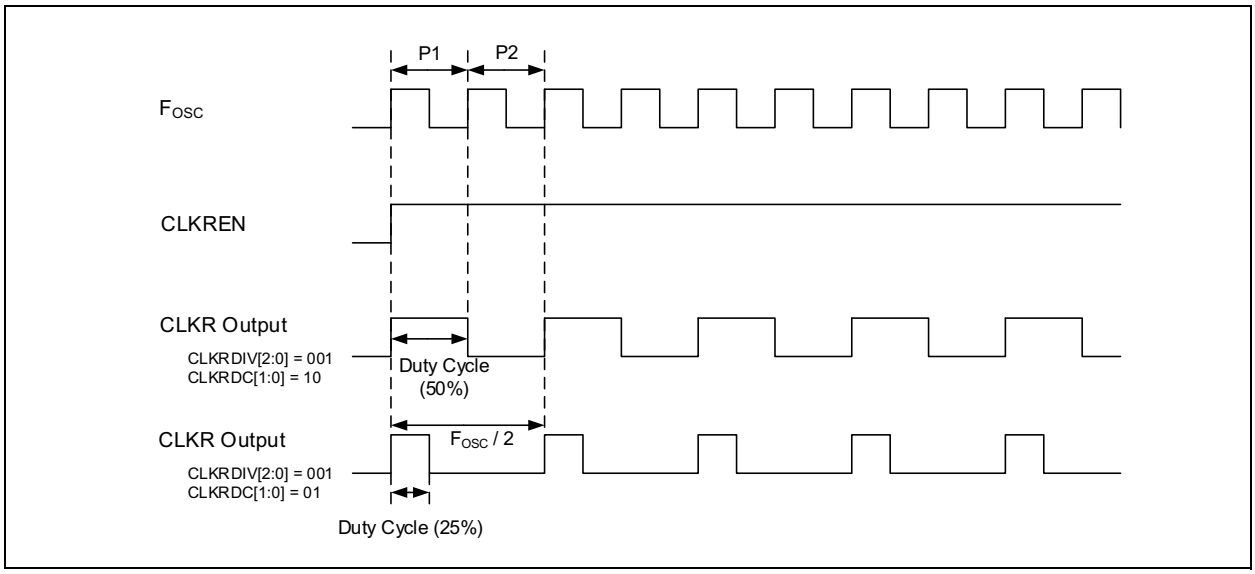
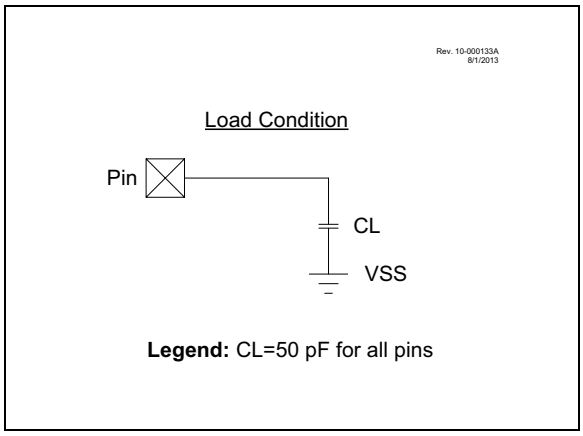



**FIGURE 34-2: CLOCK REFERENCE TIMING**



## 37.4 AC Characteristics

**FIGURE 37-4: LOAD CONDITIONS**




**Legend:** CL=50 pF for all pins