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#### Details

-XF

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	32MHz
Connectivity	I <sup>2</sup> C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	12
Program Memory Size	3.5KB (2K x 14)
Program Memory Type	FLASH
EEPROM Size	224 x 8
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 11x10b; D/A 1x5b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	16-UQFN Exposed Pad
Supplier Device Package	16-UQFN (4x4)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16lf15323-i-jq

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## **PIN DIAGRAMS**



## PIC16(L)F15313/23



## 4.5.2 OVERFLOW/UNDERFLOW RESET

If the STVREN bit in Configuration Words (Register 5-2) is programmed to '1', the device will be Reset if the stack is PUSHed beyond the sixteenth level or POPed beyond the first level, setting the appropriate bits (STKOVF or STKUNF, respectively) in the PCON register.

## 4.6 Indirect Addressing

The INDFn registers are not physical registers. Any instruction that accesses an INDFn register actually accesses the register at the address specified by the File Select Registers (FSR). If the FSRn address specifies one of the two INDFn registers, the read will return '0' and the write will not occur (though Status bits may be affected). The FSRn register value is created by the pair FSRnH and FSRnL.

The FSR registers form a 16-bit address that allows an addressing space with 65536 locations. These locations are divided into three memory regions:

- Traditional/Banked Data Memory
- Linear Data Memory
- Program Flash Memory

## 9.2 Clock Source Types

Clock sources can be classified as external or internal.

External clock sources rely on external circuitry for the clock source to function. Examples are: oscillator modules (ECH, ECM, ECL mode), quartz crystal resonators or ceramic resonators (LP, XT and HS modes).

Internal clock sources are contained within the oscillator module. The internal oscillator block has two internal oscillators and a dedicated Phase Lock Loop (PLL) that are used to generate internal system clock sources. The High-Frequency Internal Oscillator (HFINTOSC) can produce a range from 1 to 32 MHz. The Low-Frequency Internal Oscillator (LFINTOSC) generates a 31 kHz frequency. The external oscillator block can also be used with the PLL. See **Section 9.2.1.4 "4x PLL"** for more details.

The system clock can be selected between external or internal clock sources via the NOSC bits in the OSCCON1 register. See **Section 9.3** "**Clock Switching**" for additional information.

#### 9.2.1 EXTERNAL CLOCK SOURCES

An external clock source can be used as the device system clock by performing one of the following actions:

- Program the RSTOSC<2:0> bits in the Configuration Words to select an external clock source that will be used as the default system clock upon a device Reset
- Write the NOSC<2:0> and NDIV<4:0> bits in the OSCCON1 register to switch the system clock source

See **Section 9.3 "Clock Switching"** for more information.

### 9.2.1.1 EC Mode

The External Clock (EC) mode allows an externally generated logic level signal to be the system clock source. When operating in this mode, an external clock source is connected to the OSC1 input. OSC2/CLKOUT is available for general purpose I/O or CLKOUT. Figure 9-2 shows the pin connections for EC mode.

EC mode has three power modes to select from through Configuration Words:

- ECH High power,  $\leq$  32 MHz
- ECM Medium power,  $\leq$  8 MHz
- \* ECL Low power,  $\leq 0.5~\text{MHz}$

The Oscillator Start-up Timer (OST) is disabled when EC mode is selected. Therefore, there is no delay in operation after a Power-on Reset (POR) or wake-up from Sleep. Because the PIC<sup>®</sup> MCU design is fully static, stopping the external clock input will have the effect of halting the device while leaving all data intact. Upon restarting the external clock, the device will resume operation as if no time had elapsed.





## 9.2.1.2 LP, XT, HS Modes

The LP, XT and HS modes support the use of quartz crystal resonators or ceramic resonators connected to OSC1 and OSC2 (Figure 9-3). The three modes select a low, medium or high gain setting of the internal inverter-amplifier to support various resonator types and speed.

**LP** Oscillator mode selects the lowest gain setting of the internal inverter-amplifier. LP mode current consumption is the least of the three modes. This mode is designed to drive only 32.768 kHz tuning-fork type crystals (watch crystals).

**XT** Oscillator mode selects the intermediate gain setting of the internal inverter-amplifier. XT mode current consumption is the medium of the three modes. This mode is best suited to drive crystals and resonators with a medium drive level specification.

**HS** Oscillator mode selects the highest gain setting of the internal inverter-amplifier. HS mode current consumption is the highest of the three modes. This mode is best suited for resonators that require a high drive setting.

Figure 9-3 and Figure 9-4 show typical circuits for quartz crystal and ceramic resonators, respectively.

# PIC16(L)F15313/23

## REGISTER 10-12: PIR2: PERIPHERAL INTERRUPT REQUEST REGISTER 2

U-0	R/W/HS-0/0	U-0	U-0	U-0	U-0	R/W/HS-0/0	R/W/HS-0/0
_	ZCDIF	_	_	-	—	C2IF <sup>(1)</sup>	C1IF
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	HS = Hardware set

bit 7	Unimplemented: Read as '0'
bit 6	ZCDIF: Zero-Cross Detect (ZCD1) Interrupt Flag bit
	<ul><li>1 = An enabled rising and/or falling ZCD1 event has been detected (must be cleared in software)</li><li>0 = No ZCD1 event has occurred</li></ul>
bit 5-2	Unimplemented: Read as '0'
bit 1	<b>C2IF</b> : Comparator C2 Interrupt Flag bit 1 = Comparator 2 interrupt asserted (must be cleared in software) 0 = Comparator 2 interrupt not asserted
bit 0	<b>C1IF:</b> Comparator C1 Interrupt Flag bit 1 = Comparator 1 interrupt asserted (must be cleared in software) 0 = Comparator 1 interrupt not asserted
Note 1: Pres	sent only on PIC16(L)F15323.

Note:	Interrupt flag bits are set when an interrupt						
	condition occurs, regardless of the state of						
	its corresponding enable bit or the Global						
	Enable bit, GIE, of the INTCON register.						
	User software should ensure the						
	appropriate interrupt flag bits are clear						
	prior to enabling an interrupt.						

#### 13.2 FSR and INDF Access

The FSR and INDF registers allow indirect access to the PFM.

#### 13.2.1 FSR READ

With the intended address loaded into an FSR register a MOVIW instruction or read of INDF will read data from the PFM.

Reading from NVM requires one instruction cycle. The CPU operation is suspended during the read, and resumes immediately after. Read operations return a single byte of memory.

#### 13.2.2 FSR WRITE

Writing/erasing the NVM through the FSR registers (ex. MOVWI instruction) is not supported in the PIC16(L)F15313/23 devices.

#### 13.3 NVMREG Access

The NVMREG interface allows read/write access to all the locations accessible by FSRs, and also read/write access to the User ID locations, and read-only access to the device identification, revision, and Configuration data.

Writing or erasing of NVM via the NVMREG interface is prevented when the device is write-protected.

#### 13.3.1 NVMREG READ OPERATION

To read a NVM location using the NVMREG interface, the user must:

- Clear the NVMREGS bit of the NVMCON1 register if the user intends to access PFM locations, or set NMVREGS if the user intends to access User ID, or Configuration locations.
- 2. Write the desired address into the NVMADRH:NVMADRL register pair ().
- 3. Set the RD bit of the NVMCON1 register to initiate the read.

Once the read control bit is set, the CPU operation is suspended during the read, and resumes immediately after. The data is available in the very next cycle, in the NVMDATH:NVMDATL register pair; therefore, it can be read as two bytes in the following instructions.

NVMDATH:NVMDATL register pair will hold this value until another read or until it is written to by the user.

Upon completion, the RD bit is cleared by hardware.

#### FIGURE 13-1:

#### FLASH PROGRAM MEMORY READ FLOWCHART



## PIC16(L)F15313/23

REGISTE	REGISTER 16-3: PMD2: PMD CONTROL REGISTER 2						
U-0	R/W-0/0	R/W-0/0	U-0	U-0	R/W-0/0	R/W-0/0	R/W-0/0
	DAC1MD	ADCMD	—		CMP2MD	CMP1MD	ZCDMD
bit 7							bit 0
Legend:							
R = Reada	able bit	W = Writable	bit	U = Unimplem	nented bit, read	l as '0'	
u = Bit is ι	unchanged	x = Bit is unkr	nown	-n/n = Value a	t POR and BO	R/Value at all o	ther Resets
'1' = Bit is	set	'0' = Bit is clea	ared	q = Value dep	ends on condit	ion	
bit 7	Unimplemen	ted: Read as '	)'				
bit 6	DAC1MD: Di	sable DAC1 bit					
	1 = DAC mod	dule disabled					
	0 = DAC mo	dule enabled					
bit 5	ADCMD: Dis	able ADC bit					
	1 = ADC mo	dule disabled					
L:1 4 0			· ·				
DIL 4-3	bit 4-3 Unimplemented: Read as '0'						
bit 2	1 = C2 modu	sable Compara	tor C2 bit				
	$1 = C2 \mod 0$	ile enabled					
bit 1	it 1 CMP1MD: Disable Comparator C1 bit						
	1 = C1 module disabled						
	0 = C1 module enabled						
bit 0	ZCDMD: Disa						
1 = ZCD module disabled							
	0 = ZCD modelse	dule enabled					
Note 1:	Present only on F	PIC16(L)F1532	3.				



## FIGURE 21-2: VOLTAGE REFERENCE OUTPUT BUFFER EXAMPLE



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Note 1: The increment registers are double-buffered to allow for value changes to be made without first disabling the NCO module. The full increment value is loaded into the buffer registers on the second rising edge of the NCOx clk signal that occurs immediately after a write to NCOxINCL register. The buffers are not user-accessible and are shown here for reference.

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## 23.2 Comparator Control

Each comparator has two control registers: CMxCON0 and CMxCON1.

The CMxCON0 register (see Register 23-1) contains Control and Status bits for the following:

- Enable
- Output
- Output polarity
- · Hysteresis enable
- · Timer1 output synchronization

The CMxCON1 register (see Register 23-2) contains Control bits for the following:

- · Interrupt on positive/negative edge enables
- The CMxNSEL and CMxPSEL (Register 23-3 and Register 23-4) contain control bits for the following:
  - Positive input channel selection
  - Negative input channel selection

#### 23.2.1 COMPARATOR ENABLE

Setting the CxON bit of the CMxCON0 register enables the comparator for operation. Clearing the CxON bit disables the comparator resulting in minimum current consumption.

### 23.2.2 COMPARATOR OUTPUT

The output of the comparator can be monitored by reading either the CxOUT bit of the CMxCON0 register or the MCxOUT bit of the CMOUT register.

The comparator output can also be routed to an external pin through the RxyPPS register (Register 15-2). The corresponding TRIS bit must be clear to enable the pin as an output.

Note 1: The internal output of the comparator is latched with each instruction cycle. Unless otherwise specified, external outputs are not latched.

## 23.2.3 COMPARATOR OUTPUT POLARITY

Inverting the output of the comparator is functionally equivalent to swapping the comparator inputs. The polarity of the comparator output can be inverted by setting the CxPOL bit of the CMxCON0 register. Clearing the CxPOL bit results in a non-inverted output.

Table 23-2 shows the output state versus input conditions, including polarity control.

#### TABLE 23-2: COMPARATOR OUTPUT STATE VS. INPUT CONDITIONS

Input Condition	CxPOL	CxOUT
CxVN > CxVP	0	0
CxVN < CxVP	0	1
CxVN > CxVP	1	1
CxVN < CxVP	1	0

## REGISTER 23-3: CMxNSEL: COMPARATOR Cx NEGATIVE INPUT SELECT REGISTER

U-0	U-0	U-0	U-0	U-0	R/W-0/0	R/W-0/0	R/W-0/0
—	_	—	_	—		NCH<2:0>	
bit 7							bit 0

## Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-3	Unimplemented: Read as '0'
bit 2-0	NCH<2:0>: Comparator Negative Input Channel Select bits
	111 = CxVN connects to AVss
	110 = CxVN connects to FVR Buffer 2
	101 = CxVN unconnected
	100 = CxVN unconnected

- 011 = CxVN connects to CxIN3- pin
- 010 = CxVN connects to CxIN2- pin
- 001 = CxVN connects to CxIN1- pin
- 000 = CxVN connects to CxIN0- pin

#### REGISTER 23-4: CMxPSEL: COMPARATOR Cx POSITIVE INPUT SELECT REGISTER

U-0	U-0	U-0	U-0	U-0	R/W-0/0	R/W-0/0	R/W-0/0
—	_	—	—	_		PCH<2:0>	
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

#### bit 7-3 Unimplemented: Read as '0'

bit 2-0 PCH<2:0>: Comparator Positive Input Channel Select bits

- 111 = CxVP connects to AVss
- 110 = CxVP connects to FVR Buffer 2
- 101 = CxVP connects to DAC output
- 100 = CxVP unconnected
- 011 = CxVP unconnected
- 010 = CxVP unconnected
- 001 = CxVP connects to CxIN1+ pin
- 000 = CxVP connects to CxIN0+ pin

#### 27.5.5 SOFTWARE START ONE-SHOT MODE

In One-Shot mode the timer resets and the ON bit is cleared when the timer value matches the PRx period value. The ON bit must be set by software to start another timer cycle. Setting MODE<4:0> = 01000 selects One-Shot mode which is illustrated in Figure 27-8. In the example, ON is controlled by BSF and BCF instructions. In the first case, a BSF instruction sets ON and the counter runs to completion and clears ON. In the second case, a BSF instruction starts the cycle, BCF/BSF instructions turn the counter off and on during the cycle, and then it runs to completion.

When One-Shot mode is used in conjunction with the CCP PWM operation the PWM pulse drive starts concurrent with setting the ON bit. Clearing the ON bit while the PWM drive is active will extend the PWM drive. The PWM drive will terminate when the timer value matches the CCPRx pulse width value. The PWM drive will remain off until software sets the ON bit to start another cycle. If software clears the ON bit after the CCPRx match but before the PRx match then the PWM drive will be extended by the length of time the ON bit remains cleared. Another timing cycle can only be initiated by setting the ON bit after it has been cleared by a PRx period count match.

FIGURE 27-8: SOFTWARE START ONE-SHOT MODE TIMING DIAGRAM (MODE = 01000)



#### 28.2.1 CCPX PIN CONFIGURATION

The software must configure the CCPx pin as an output by clearing the associated TRIS bit and defining the appropriate output pin through the RxyPPS registers. See **Section 15.0 "Peripheral Pin Select (PPS) Module"** for more details.

The CCP output can also be used as an input for other peripherals.

Note: Clearing the CCPxCON register will force the CCPx compare output latch to the default low level. This is not the PORT I/O data latch.

#### 28.2.2 TIMER1 MODE RESOURCE

In Compare mode, Timer1 must be running in either Timer mode or Synchronized Counter mode. The compare operation may not work in Asynchronous Counter mode.

See **Section 26.0 "Timer1 Module with Gate Control"** for more information on configuring Timer1.

Note: Clocking Timer1 from the system clock (Fosc) should not be used in Compare mode. In order for Compare mode to recognize the trigger event on the CCPx pin, TImer1 must be clocked from the instruction clock (Fosc/4) or from an external clock source.

### 28.2.3 AUTO-CONVERSION TRIGGER

All CCPx modes set the CCP interrupt flag (CCPxIF). When this flag is set and a match occurs, an Auto-conversion Trigger can take place if the CCP module is selected as the conversion trigger source.

Refer to **Section 20.2.4 "Auto-Conversion Trigger"** for more information.

Note:	Removing the match condition by									
	changing the contents of the CCPRxH									
	and CCPRxL register pair, between the									
	clock edge that generates the									
	Auto-conversion Trigger and the clock									
	edge that generates the Timer1 Reset, will									
	preclude the Reset from occurring									

#### 28.2.4 COMPARE DURING SLEEP

Since Fosc is shut down during Sleep mode, the Compare mode will not function properly during Sleep, unless the timer is running. The device will wake on interrupt (if enabled).

#### 28.3 PWM Overview

Pulse-Width Modulation (PWM) is a scheme that provides power to a load by switching quickly between fully on and fully off states. The PWM signal resembles a square wave where the high portion of the signal is considered the on state and the low portion of the signal is considered the off state. The high portion, also known as the pulse width, can vary in time and is defined in steps. A larger number of steps applied, which lengthens the pulse width, also supplies more power to the load. Lowering the number of steps applied, which shortens the pulse width, supplies less power. The PWM period is defined as the duration of one complete cycle or the total amount of on and off time combined.

PWM resolution defines the maximum number of steps that can be present in a single PWM period. A higher resolution allows for more precise control of the pulse width time and in turn the power that is applied to the load.

The term duty cycle describes the proportion of the on time to the off time and is expressed in percentages, where 0% is fully off and 100% is fully on. A lower duty cycle corresponds to less power applied and a higher duty cycle corresponds to more power applied.

Figure 28-3 shows a typical waveform of the PWM signal.

#### 28.3.1 STANDARD PWM OPERATION

The standard PWM mode generates a Pulse-Width Modulation (PWM) signal on the CCPx pin with up to ten bits of resolution. The period, duty cycle, and resolution are controlled by the following registers:

- · PR2 registers
- T2CON registers
- CCPRxL registers
- CCPxCON registers

Figure 28-4 shows a simplified block diagram of PWM operation.

Note: The corresponding TRIS bit must be cleared to enable the PWM output on the CCPx pin.

#### FIGURE 28-3: CC

CCP PWM OUTPUT SIGNAL



TABLE 31-4:	SUMMARY OF REGISTERS ASSOCIATED WITH CLCx (continued)	
-------------	---	--

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
CLC4GLS1	—		LC4G2D3T	LC4G2D3N	LC4G2D2T	LC4G2D2N	LC4G2D1T	LC4G2D1N	354
CLC4GLS2	—		LC4G3D3T	LC4G3D3N	LC4G3D2T	LC4G3D2N	LC4G3D1T	LC4G3D1N	355
CLC4GLS3	_	_	LC4G4D3T	LC4G4D3N	LC4G4D2T	LC4G4D2N	LC4G4D1T	LC4G4D1N	356
CLCIN0PPS	_	_		CLCIN0PPS<5:0>					191
CLCIN1PPS	—			CLCIN1PPS<5:0>					191
CLCIN2PPS	_	_		CLCIN2PPS<5:0>					191
CLCIN3PPS	_	_		CLCIN3PPS<5:0>					191

Legend: — = unimplemented, read as '0'. Shaded cells are unused by the CLCx modules.

The  $\mathsf{I}^2\mathsf{C}$  interface supports the following modes and features:

- Master mode
- Slave mode
- Byte NACKing (Slave mode)
- · Limited multi-master support
- 7-bit and 10-bit addressing
- Start and Stop interrupts
- Interrupt masking

- Clock stretching
- Bus collision detection
- General call address matching
- Address masking
- · Selectable SDA hold times

Figure 32-2 is a block diagram of the  $I^2C$  interface module in Master mode. Figure 32-3 is a diagram of the  $I^2C$  interface module in Slave mode.

## FIGURE 32-2: MSSP BLOCK DIAGRAM (I<sup>2</sup>C MASTER MODE)



## 33.1 EUSART Asynchronous Mode

The EUSART transmits and receives data using the standard non-return-to-zero (NRZ) format. NRZ is implemented with two levels: a VOH Mark state which represents a '1' data bit, and a VoL Space state which represents a '0' data bit. NRZ refers to the fact that consecutively transmitted data bits of the same value stay at the output level of that bit without returning to a neutral level between each bit transmission. An NRZ transmission port idles in the Mark state. Each character transmission consists of one Start bit followed by eight or nine data bits and is always terminated by one or more Stop bits. The Start bit is always a space and the Stop bits are always marks. The most common data format is eight bits. Each transmitted bit persists for a period of 1/(Baud Rate). An on-chip dedicated 8-bit/16-bit Baud Rate Generator is used to derive standard baud rate frequencies from the system oscillator. See Table 33-3 for examples of baud rate configurations.

The EUSART transmits and receives the LSb first. The EUSART's transmitter and receiver are functionally independent, but share the same data format and baud rate. Parity is not supported by the hardware, but can be implemented in software and stored as the ninth data bit.

#### 33.1.1 EUSART ASYNCHRONOUS TRANSMITTER

The EUSART transmitter block diagram is shown in Figure 33-1. The heart of the transmitter is the serial Transmit Shift Register (TSR), which is not directly accessible by software. The TSR obtains its data from the transmit buffer, which is the TX1REG register.

#### 33.1.1.1 Enabling the Transmitter

The EUSART transmitter is enabled for asynchronous operations by configuring the following three control bits:

- TXEN = 1
- SYNC = 0
- SPEN = 1

All other EUSART control bits are assumed to be in their default state.

Setting the TXEN bit of the TX1STA register enables the transmitter circuitry of the EUSART. Clearing the SYNC bit of the TX1STA register configures the EUSART for asynchronous operation. Setting the SPEN bit of the RC1STA register enables the EUSART and automatically configures the TX/CK I/O pin as an output. If the TX/CK pin is shared with an analog peripheral, the analog I/O function must be disabled by clearing the corresponding ANSEL bit.

**Note:** The TX1IF Transmitter Interrupt flag is set when the TXEN enable bit is set.

#### 33.1.1.2 Transmitting Data

A transmission is initiated by writing a character to the TX1REG register. If this is the first character, or the previous character has been completely flushed from the TSR, the data in the TX1REG is immediately transferred to the TSR register. If the TSR still contains all or part of a previous character, the new character data is held in the TX1REG until the Stop bit of the previous character has been transmitted. The pending character in the TX1REG is then transferred to the TSR in one TcY immediately following the Stop bit sequence commences immediately following the transfer of the data to the TSR from the TX1REG.

#### 33.1.1.3 Transmit Data Polarity

The polarity of the transmit data can be controlled with the SCKP bit of the BAUD1CON register. The default state of this bit is '0' which selects high true transmit idle and data bits. Setting the SCKP bit to '1' will invert the transmit data resulting in low true idle and data bits. The SCKP bit controls transmit data polarity in Asynchronous mode only. In Synchronous mode, the SCKP bit has a different function. See **Section 33.4.1.2 "Clock Polarity"**.

#### 33.1.1.4 Transmit Interrupt Flag

The TX1IF interrupt flag bit of the PIR3 register is set whenever the EUSART transmitter is enabled and no character is being held for transmission in the TX1REG. In other words, the TX1IF bit is only clear when the TSR is busy with a character and a new character has been queued for transmission in the TX1REG. The TX1IF flag bit is not cleared immediately upon writing TX1REG. TX1IF becomes valid in the second instruction cycle following the write execution. Polling TX1IF immediately following the TX1REG write will return invalid results. The TX1IF bit is read-only, it cannot be set or cleared by software.

The TX1IF interrupt can be enabled by setting the TX1IE interrupt enable bit of the PIE3 register. However, the TX1IF flag bit will be set whenever the TX1REG is empty, regardless of the state of TX1IE enable bit.

To use interrupts when transmitting data, set the TX1IE bit only when there is more data to send. Clear the TX1IE interrupt enable bit upon writing the last character of the transmission to the TX1REG.

#### 33.3.5 RECEIVING A BREAK CHARACTER

The Enhanced EUSART module can receive a Break character in two ways.

The first method to detect a Break character uses the FERR bit of the RC1STA register and the received data as indicated by RC1REG. The Baud Rate Generator is assumed to have been initialized to the expected baud rate.

A Break character has been received when:

- · RX1IF bit is set
- · FERR bit is set
- RC1REG = 00h

The second method uses the Auto-Wake-up feature described in **Section 33.3.3 "Auto-Wake-up on Break"**. By enabling this feature, the EUSART will sample the next two transitions on RX/DT, cause an RX1IF interrupt, and receive the next data byte followed by another interrupt.

Note that following a Break character, the user will typically want to enable the Auto-Baud Detect feature. For both methods, the user can set the ABDEN bit of the BAUD1CON register before placing the EUSART in Sleep mode.





## PIC16(L)F15313/23







## TABLE 37-21: EUSART SYNCHRONOUS TRANSMISSION CHARACTERISTICS

Standard	Operating Cor	~				
Param. No.	Symbol	Characteristic	Min.	Max.	Units	Conditions
US120	TCKH2DTV	SYNC XMIT (Master and Slave)	_	80	ns	$3.0V \leq V\text{DD} \leq 5.5V$
		Clock high to data-out valid	$\langle - \rangle$	100	ns	$1.8V \leq V\text{DD} \leq 5.5V$
US121	TCKRF	Clock out rise time and fall time	$\langle - \rangle$	45	ns	$3.0V \leq V\text{DD} \leq 5.5V$
		(Master mode)		50	ns	$1.8V \leq V\text{DD} \leq 5.5V$
US122	TDTRF	Data-out rise time and fall time	$\langle \rangle$	45	ns	$3.0V \leq V\text{DD} \leq 5.5V$
			<u> </u>	50	ns	$1.8V \leq V\text{DD} \leq 5.5V$

## FIGURE 37-16: EUSART SYNCHRONOUS RECEIVE (MASTER/SLAVE) TIMING



## TABLE 37-22: EUSART SYNCHRONOUS RECEIVE REQUIREMENTS

Standard Operating Conditions (unless otherwise stated)						
Param. No. Symbol	Characteristic	Min.	Max.	Units	Conditions	
US125 TDTV2CKL	SYNC RCV (Master and Slave)	10				
	Data-setup before $CK \neq (DT hold time)$	10		ns		
US126 TCKL2DTL	Data-hold after CK $\downarrow$ (DT hold time)	15	_	ns		

## 14-Lead Plastic Dual In-Line (P) – 300 mil Body [PDIP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	Units	INCHES				
Dimensio	on Limits	MIN	NOM	MAX		
Number of Pins	Ν	14				
Pitch	е		.100 BSC			
Top to Seating Plane	Α	-	-	.210		
Molded Package Thickness	A2	.115	.130	.195		
Base to Seating Plane	A1	.015	-	-		
Shoulder to Shoulder Width	Е	.290	.310	.325		
Molded Package Width	E1	.240	.250	.280		
Overall Length	D	.735	.750	.775		
Tip to Seating Plane	L	.115	.130	.150		
Lead Thickness	С	.008	.010	.015		
Upper Lead Width	b1	.045	.060	.070		
Lower Lead Width	b	.014	.018	.022		
Overall Row Spacing §	eB	-	-	.430		

#### Notes:

1. Pin 1 visual index feature may vary, but must be located with the hatched area.

2. § Significant Characteristic.

3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.

4. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-005B

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