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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

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Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	32MHz
Connectivity	I ² C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	12
Program Memory Size	3.5KB (2K x 14)
Program Memory Type	FLASH
EEPROM Size	224 x 8
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 11x10b; D/A 1x5b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	14-TSSOP (0.173", 4.40mm Width)
Supplier Device Package	14-TSSOP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16lf15323-i-st

3.0 ENHANCED MID-RANGE CPU

This family of devices contains an enhanced mid-range 8-bit CPU core. The CPU has 48 instructions. Interrupt capability includes automatic context saving.

The hardware stack is 16-levels deep and has Overflow and Underflow Reset capability. Direct, Indirect, and Relative Addressing modes are available. Two File Select Registers (FSRs) provide the ability to read program and data memory.

FIGURE 3-1: CORE DATA PATH DIAGRAM

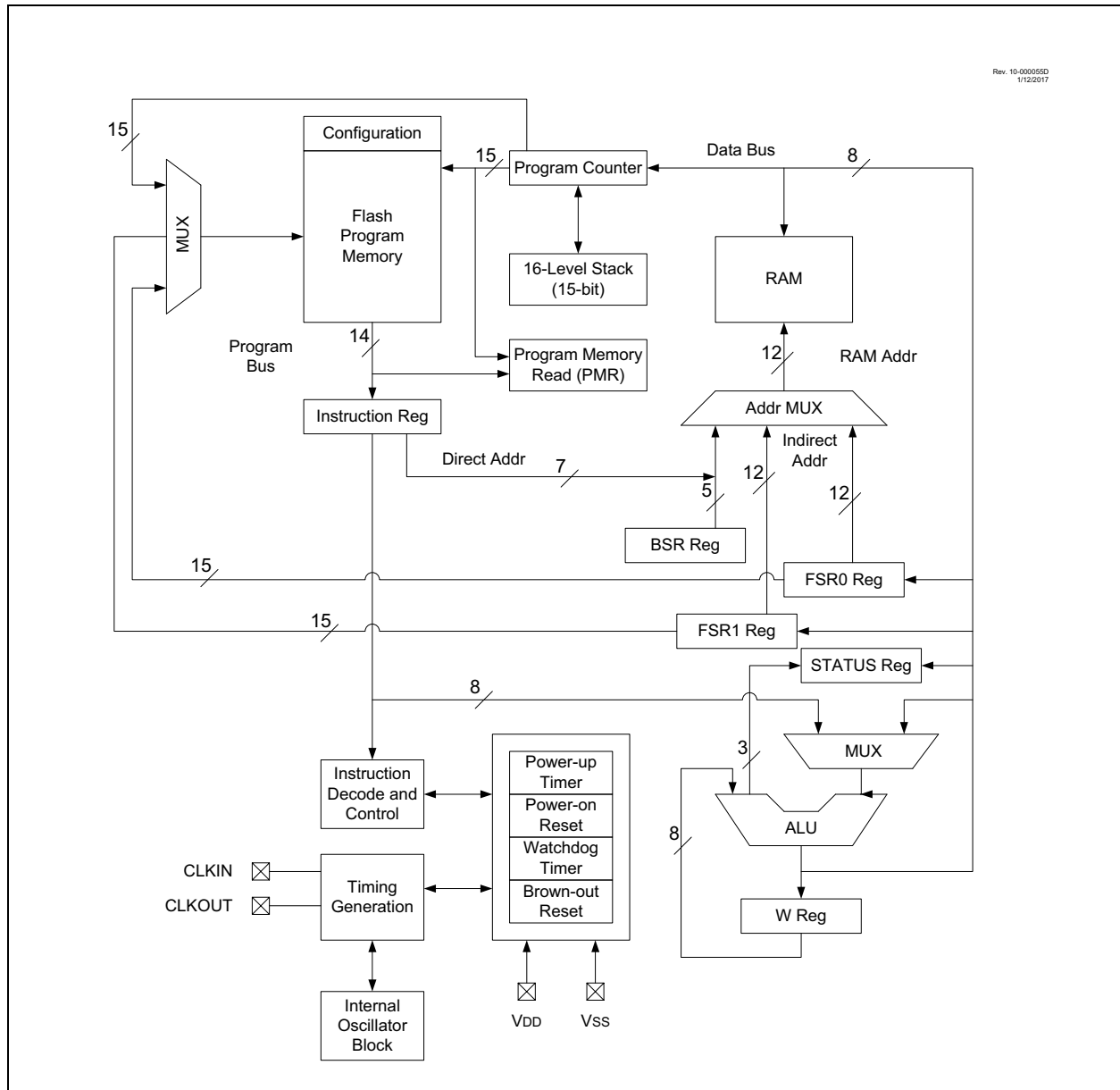


TABLE 4-10: SPECIAL FUNCTION REGISTER SUMMARY BANKS 0-63 (CONTINUED)

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on: MCLR
Bank 8-10											
CPU CORE REGISTERS; see Table 4-3 for specifics											
x0Ch/ x8Ch — x1Fh/ x9Fh	—	Unimplemented									

Legend: x = unknown, u = unchanged, c = depends on condition, - = unimplemented, read as '0', r = reserved. Shaded locations unimplemented, read as '0'.

TABLE 4-10: SPECIAL FUNCTION REGISTER SUMMARY BANKS 0-63 (CONTINUED)

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on: MCLR	
Bank 17												
CPU CORE REGISTERS; see Table 4-3 for specifics												
88Ch	CPUDOZE	IDLEN	DOZEN	ROI	DOE	—	DOZE2	DOZE1	DOZE0	0000 -000	u000 -000	
88Dh	OSCCON1	—	NOSC<2:0>			NDIV<3:0>				-q qq 0000	-q qq 0000	
88Eh	OSCCON2	—	COSC<2:0>			CDIV<3:0>				-q qq qq qq	-q qq qq qq	
88Fh	OSCCON3	CSWHOLD	—	—	ORDY	NOSCR	—	—	—	0--0 0---	0--0 0---	
890h	OSCSTAT	EXTOR	HFOR	MFOR	LFOR	—	ADOR	—	PLL	q000 -q-0	qq qq -q-q	
891h	OSCEN	EXTOEN	HFOEN	MFOEN	LFOEN	—	ADOEN	—	—	0000 -0--	0000 -0--	
892h	OSCTUNE	—	—	HFTUN<5:0>						--10 0000	--10 0000	
893h	OSCFRQ	—	—	—	—	—	HFFRQ<2:0>			---- -qqq	---- -qqq	
894h	—	Unimplemented								—	—	
895h	CLKRCON	CLKREN	—	—	CLKRDC<1:0>		CLKRDIV<2:0>			0--x xxxx	0--u uuuu	
896h	CLKRCLK	—	—	—	—	CLKRCLK<3:0>					---- 0000	---- 0000
897h — 89Fh	—	Unimplemented								—	—	

Legend: x = unknown, u = unchanged, q = depends on condition, - = unimplemented, read as '0', r = reserved. Shaded locations unimplemented, read as '0'.

TABLE 5-1: BOOT BLOCK SIZE BITS

$\overline{\text{BBEN}}$	BBSIZE<2:0>	Actual Boot Block Size User Program Memory Size (words)	Last Boot Block Memory Access
1	xxx	0	—
0	111	512	01FFh
0	110-000	1024	03FFh

Note: The maximum boot block size is half the user program memory size. All selections higher than the maximum are set to half size. For example, all BBSIZE = 000 - 100 produce a boot block size of 4kW on a 8kW device.

REGISTER 9-4: OSCSTAT: OSCILLATOR STATUS REGISTER 1

R-q/q	R-q/q	R-q/q	R-q/q	U-0	R-q/q	U-0	R-q/q
EXTOR	HFOR	MFOR	LFOR	—	ADOR	—	PLLr
bit 7							bit 0

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7	EXTOR: EXTOSC (external) Oscillator Ready bit 1 = The oscillator is ready to be used 0 = The oscillator is not enabled, or is not yet ready to be used.
bit 6	HFOR: HFINTOSC Oscillator Ready bit 1 = The oscillator is ready to be used 0 = The oscillator is not enabled, or is not yet ready to be used.
bit 5	MFOR: MFINTOSC Oscillator Ready bit 1 = The oscillator is ready to be used 0 = The oscillator is not enabled, or is not yet ready to be used.
bit 4	LFOR: LFINTOSC Oscillator Ready bit 1 = The oscillator is ready to be used 0 = The oscillator is not enabled, or is not yet ready to be used.
bit 3	Unimplemented: Read as '0'
bit 2	ADOR: CRC Oscillator Ready bit 1 = The oscillator is ready to be used 0 = The oscillator is not enabled, or is not yet ready to be used.
bit 1	Unimplemented: Read as '0'
bit 0	PLLr: PLL is Ready bit 1 = The PLL is ready to be used 0 = The PLL is not enabled, the required input source is not ready, or the PLL is not locked.

[illegible]

REGISTER 13-5: NVMCON1: NONVOLATILE MEMORY CONTROL 1 REGISTER

U-0	R/W-0/0	R/W-0/0	R/W/HC-0/0	R/W/HC-x/q	R/W-0/0	R/S/HC-0/0	R/S/HC-0/0
—	NVMREGS	LWLO	FREE	WRERR ^(1,2,3)	WREN	WR ^(4,5,6)	RD
bit 7							bit 0

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
S = Bit can only be set	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	HC = Bit is cleared by hardware

bit 7	Unimplemented: Read as '0'
bit 6	NVMREGS: Configuration Select bit 1 = Access DIA, DCI, Configuration, User ID and Device ID Registers 0 = Access PFM
bit 5	LWLO: Load Write Latches Only bit <u>When FREE = 0:</u> 1 = The next WR command updates the write latch for this word within the row; no memory operation is initiated. 0 = The next WR command writes data or erases Otherwise: The bit is ignored
bit 4	FREE: PFM Erase Enable bit <u>When NVMREGS:NVMADR points to a PFM location:</u> 1 = Performs an erase operation with the next WR command; the 32-word pseudo-row containing the indicated address is erased (to all 1s) to prepare for writing. 0 = All erase operations have completed normally
bit 3	WRERR: Program/Erase Error Flag bit ^(1,2,3) This bit is normally set by hardware. 1 = A write operation was interrupted by a Reset, interrupted unlock sequence, or WR was written to one while NVMADR points to a write-protected address. 0 = The program or erase operation completed normally
bit 2	WREN: Program/Erase Enable bit 1 = Allows program/erase cycles 0 = Inhibits programming/erasing of program Flash
bit 1	WR: Write Control bit ^(4,5,6) <u>When NVMREG:NVMADR points to a PFM location:</u> 1 = Initiates the operation indicated by Table 13-4 0 = NVM program/erase operation is complete and inactive.
bit 0	RD: Read Control bit ⁽⁷⁾ 1 = Initiates a read at address = NVMADR1, and loads data to NVMDAT. Read takes one instruction cycle and the bit is cleared when the operation is complete. The bit can only be set (not cleared) in software. 0 = NVM read operation is complete and inactive

- Note**
- 1: Bit is undefined while WR = 1.
 - 2: Bit must be cleared by software; hardware will not clear this bit.
 - 3: Bit may be written to '1' by software in order to implement test sequences.
 - 4: This bit can only be set by following the unlock sequence of **Section 13.3.2 "NVM Unlock Sequence"**.
 - 5: Operations are self-timed, and the WR bit is cleared by hardware when complete.
 - 6: Once a write operation is initiated, setting this bit to zero will have no effect.

15.3 Bidirectional Pins

PPS selections for peripherals with bidirectional signals on a single pin must be made so that the PPS input and PPS output select the same pin. Peripherals that have bidirectional signals include:

- EUSART (synchronous operation)
- MSSP (I²C)

Note: The I²C SCLx and SDAx functions can be remapped through PPS. However, only the RB1, RB2, RC3 and RC4 pins have the I²C and SMBus specific input buffers implemented (I²C mode disables INLVL and sets thresholds that are specific for I²C). If the SCLx or SDAx functions are mapped to some other pin (other than RB1, RB2, RC3 or RC4), the general purpose TTL or ST input buffers (as configured based on INLVL register setting) will be used instead. In most applications, it is therefore recommended only to map the SCLx and SDAx pin functions to the RB1, RB2, RC3 or RC4 pins.

15.4 PPS Lock

The PPS includes a mode in which all input and output selections can be locked to prevent inadvertent changes. PPS selections are locked by setting the PPSLOCKED bit of the PPSLOCK register. Setting and clearing this bit requires a special sequence as an extra precaution against inadvertent changes. Examples of setting and clearing the PPSLOCKED bit are shown in Example 15-1.

EXAMPLE 15-1: PPS LOCK/UNLOCK SEQUENCE

```
; suspend interrupts
    BCF    INTCON,GIE
; BANKSEL PPSLOCK    ; set bank
; required sequence, next 5 instructions
    MOVLW 0x55
    MOVWF PPSLOCK
    MOVLW 0xAA
    MOVWF PPSLOCK
; Set PPSLOCKED bit to disable writes or
; Clear PPSLOCKED bit to enable writes
    BSF    PPSLOCK,PPSLOCKED
; restore interrupts
    BSF    INTCON,GIE
```

15.5 PPS Permanent Lock

The PPS can be permanently locked by setting the PPS1WAY Configuration bit. When this bit is set, the PPSLOCKED bit can only be cleared and set one time after a device Reset. This allows for clearing the PPSLOCKED bit so that the input and output selections can be made during initialization. When the PPSLOCKED bit is set after all selections have been made, it will remain set and cannot be cleared until after the next device Reset event.

15.6 Operation During Sleep

PPS input and output selections are unaffected by Sleep.

15.7 Effects of a Reset

A device Power-on-Reset (POR) clears all PPS input and output selections to their default values (Permanent Lock Removed). All other Resets leave the selections unchanged. Default input selections are shown in Table 15-1 and Table 15-2.

TABLE 15-4: PPS OUTPUT SIGNAL ROUTING OPTIONS (PIC16(L)F15313)

Output Signal Name	RxyPPS Register Value	Remappable to Pins of PORTx
		PIC16(L)F15313
		PORTA
CLKR	0x1B	•
NCO1OUT	0x1A	•
TMR0	0x19	•
SDO1/SDA1	0x16	•
SCK1/SCL1	0x15	•
C1OUT	0x13	•
DT1	0x10	•
TX1/CK1	0x0F	•
PWM6OUT	0x0E	•
PWM5OUT	0x0D	•
PWM4OUT	0x0C	•
PWM3OUT	0x0B	•
CCP2	0x0A	•
CCP1	0x09	•
CWG1D	0x08	•
CWG1C	0x07	•
CWG1B	0x06	•
CWG1A	0x05	•
CLC4OUT	0x04	•
CLC3OUT	0x03	•
CLC2OUT	0x02	•
CLC1OUT	0x01	•

TABLE 15-5: PPS OUTPUT SIGNAL ROUTING OPTIONS (PIC16(L)F15323)

Output Signal Name	RxyPPS Register Value	Remappable to Pins of PORTx	
		PIC16(L)F15323	
		PORTA	PORTC
CLKR	0x1B	•	•
NCO1OUT	0x1A	•	•
TMR0	0x19	•	•
SDO1/SDA1	0x16	•	•
SCK1/SCL1	0x15	•	•
C2OUT	0x14	•	•
C1OUT	0x13	•	•
DT1	0x10	•	•
TX1/CK1	0x0F	•	•
PWM6OUT	0x0E	•	•
PWM5OUT	0x0D	•	•
PWM4OUT	0x0C	•	•
PWM3OUT	0x0B	•	•
CCP2	0x0A	•	•
CCP1	0x09	•	•
CWG1D	0x08	•	•
CWG1C	0x07	•	•
CWG1B	0x06	•	•
CWG1A	0x05	•	•
CLC4OUT	0x04	•	•
CLC3OUT	0x03	•	•
CLC2OUT	0x02	•	•
CLC1OUT	0x01	•	•

18.3 Register Definitions: FVR Control

REGISTER 18-1: FVRCON: FIXED VOLTAGE REFERENCE CONTROL REGISTER

R/W-0/0	R-q/q	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
FVREN	FVRRDY ⁽¹⁾	TSEN ⁽³⁾	TSRNG ⁽³⁾	CDAFVR<1:0>	ADFVR<1:0>		
bit 7							bit 0

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	q = Value depends on condition

bit 7	FVREN: Fixed Voltage Reference Enable bit 1 = Fixed Voltage Reference is enabled 0 = Fixed Voltage Reference is disabled
bit 6	FVRRDY: Fixed Voltage Reference Ready Flag bit ⁽¹⁾ 1 = Fixed Voltage Reference output is ready for use 0 = Fixed Voltage Reference output is not ready or not enabled
bit 5	TSEN: Temperature Indicator Enable bit ⁽³⁾ 1 = Temperature Indicator is enabled 0 = Temperature Indicator is disabled
bit 4	TSRNG: Temperature Indicator Range Selection bit ⁽³⁾ 1 = Temperature in High Range V _{OUT} = 3VT 0 = Temperature in Low Range V _{OUT} = 2VT
bit 3-2	CDAFVR<1:0>: Comparator FVR Buffer Gain Selection bits 11 = Comparator FVR Buffer Gain is 4x, (4.096V) ⁽²⁾ 10 = Comparator FVR Buffer Gain is 2x, (2.048V) ⁽²⁾ 01 = Comparator FVR Buffer Gain is 1x, (1.024V) 00 = Comparator FVR Buffer is off
bit 1-0	ADFVR<1:0>: ADC FVR Buffer Gain Selection bit 11 = ADC FVR Buffer Gain is 4x, (4.096V) ⁽²⁾ 10 = ADC FVR Buffer Gain is 2x, (2.048V) ⁽²⁾ 01 = ADC FVR Buffer Gain is 1x, (1.024V) 00 = ADC FVR Buffer is off

- Note 1:** FVRRDY is always '1'.
Note 2: Fixed Voltage Reference output cannot exceed V_{DD}.
Note 3: See **Section 19.0 "Temperature Indicator Module"** for additional information.

REGISTER 28-4: CCPRxH REGISTER: CCPx REGISTER HIGH BYTE

R/W-x/x	R/W-x/x	R/W-x/x	R/W-x/x	R/W-x/x	R/W-x/x	R/W-x/x	R/W-x/x
CCPRx<15:8>							
bit 7				bit 0			

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Reset
'1' = Bit is set	'0' = Bit is cleared	

bit 7-0

CCPxMODE = Capture mode

CCPRxH<7:0>: Captured value of TMR1H

CCPxMODE = Compare mode

CCPRxH<7:0>: MS Byte compared to TMR1H

CCPxMODE = PWM modes when CCPxFMT = 0:

CCPRxH<7:2>: Not used

CCPRxH<1:0>: Pulse-width Most Significant two bits

CCPxMODE = PWM modes when CCPxFMT = 1:

CCPRxH<7:0>: Pulse-width Most Significant eight bits

32.3.1 CLOCK STRETCHING

When a slave device has not completed processing data, it can delay the transfer of more data through the process of clock stretching. An addressed slave device may hold the SCL clock line low after receiving or sending a bit, indicating that it is not yet ready to continue. The master that is communicating with the slave will attempt to raise the SCL line in order to transfer the next bit, but will detect that the clock line has not yet been released. Because the SCL connection is open-drain, the slave has the ability to hold that line low until it is ready to continue communicating.

Clock stretching allows receivers that cannot keep up with a transmitter to control the flow of incoming data.

32.3.2 ARBITRATION

Each master device must monitor the bus for Start and Stop bits. If the device detects that the bus is busy, it cannot begin a new message until the bus returns to an Idle state.

However, two master devices may try to initiate a transmission on or about the same time. When this occurs, the process of arbitration begins. Each transmitter checks the level of the SDA data line and compares it to the level that it expects to find. The first transmitter to observe that the two levels do not match, loses arbitration, and must stop transmitting on the SDA line.

For example, if one transmitter holds the SDA line to a logical one (lets it float) and a second transmitter holds it to a logical zero (pulls it low), the result is that the SDA line will be low. The first transmitter then observes that the level of the line is different than expected and concludes that another transmitter is communicating.

The first transmitter to notice this difference is the one that loses arbitration and must stop driving the SDA line. If this transmitter is also a master device, it also must stop driving the SCL line. It then can monitor the lines for a Stop condition before trying to reissue its transmission. In the meantime, the other device that has not noticed any difference between the expected and actual levels on the SDA line continues with its original transmission.

Slave Transmit mode can also be arbitrated, when a master addresses multiple slaves, but this is less common.

32.4 I²C MODE OPERATION

All MSSP I²C communication is byte oriented and shifted out MSb first. Six SFR registers and two interrupt flags interface the module with the PIC[®] microcontroller and user software. Two pins, SDA and SCL, are exercised by the module to communicate with other external I²C devices.

32.4.1 BYTE FORMAT

All communication in I²C is done in 9-bit segments. A byte is sent from a master to a slave or vice-versa, followed by an Acknowledge bit sent back. After the eighth falling edge of the SCL line, the device outputting data on the SDA changes that pin to an input and reads in an acknowledge value on the next clock pulse.

The clock signal, SCL, is provided by the master. Data is valid to change while the SCL signal is low, and sampled on the rising edge of the clock. Changes on the SDA line while the SCL line is high define special conditions on the bus, explained below.

32.4.2 DEFINITION OF I²C TERMINOLOGY

There is language and terminology in the description of I²C communication that have definitions specific to I²C. That word usage is defined below and may be used in the rest of this document without explanation. This table was adapted from the Philips I²C specification.

32.4.3 SDA AND SCL PINS

Selection of any I²C mode with the SSPEN bit set, forces the SCL and SDA pins to be open-drain. These pins should be set by the user to inputs by setting the appropriate TRIS bits.

Note 1: Any device pin can be selected for SDA and SCL functions with the PPS peripheral. These functions are bidirectional. The SDA input is selected with the SSPDATPPS registers. The SCL input is selected with the SSPCLKPPS registers. Outputs are selected with the RxyPPS registers. It is the user's responsibility to make the selections so that both the input and the output for each function is on the same pin.

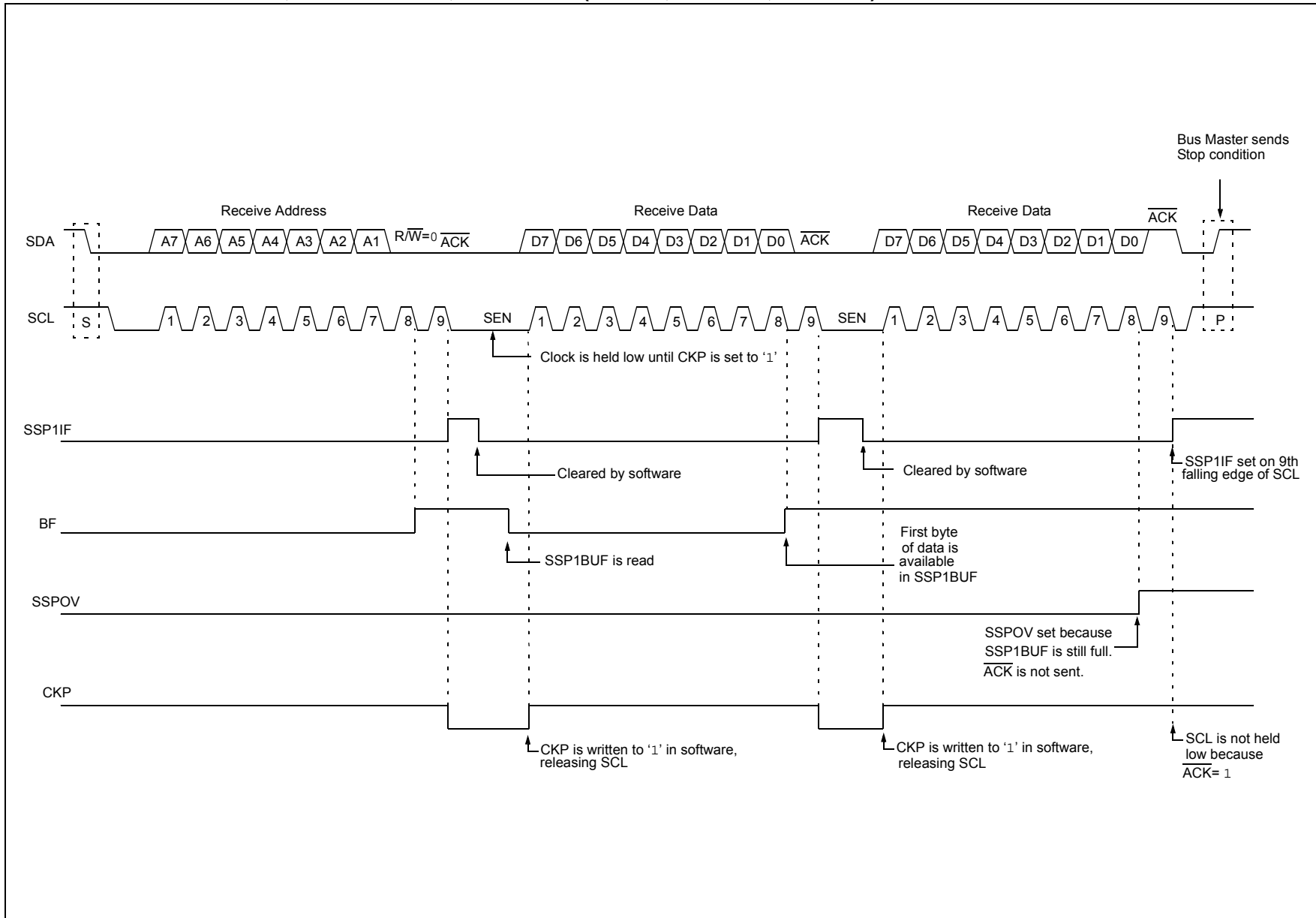
FIGURE 32-15: I²C SLAVE, 7-BIT ADDRESS, RECEPTION (SEN = 1, AHEN = 0, DHEN = 0)

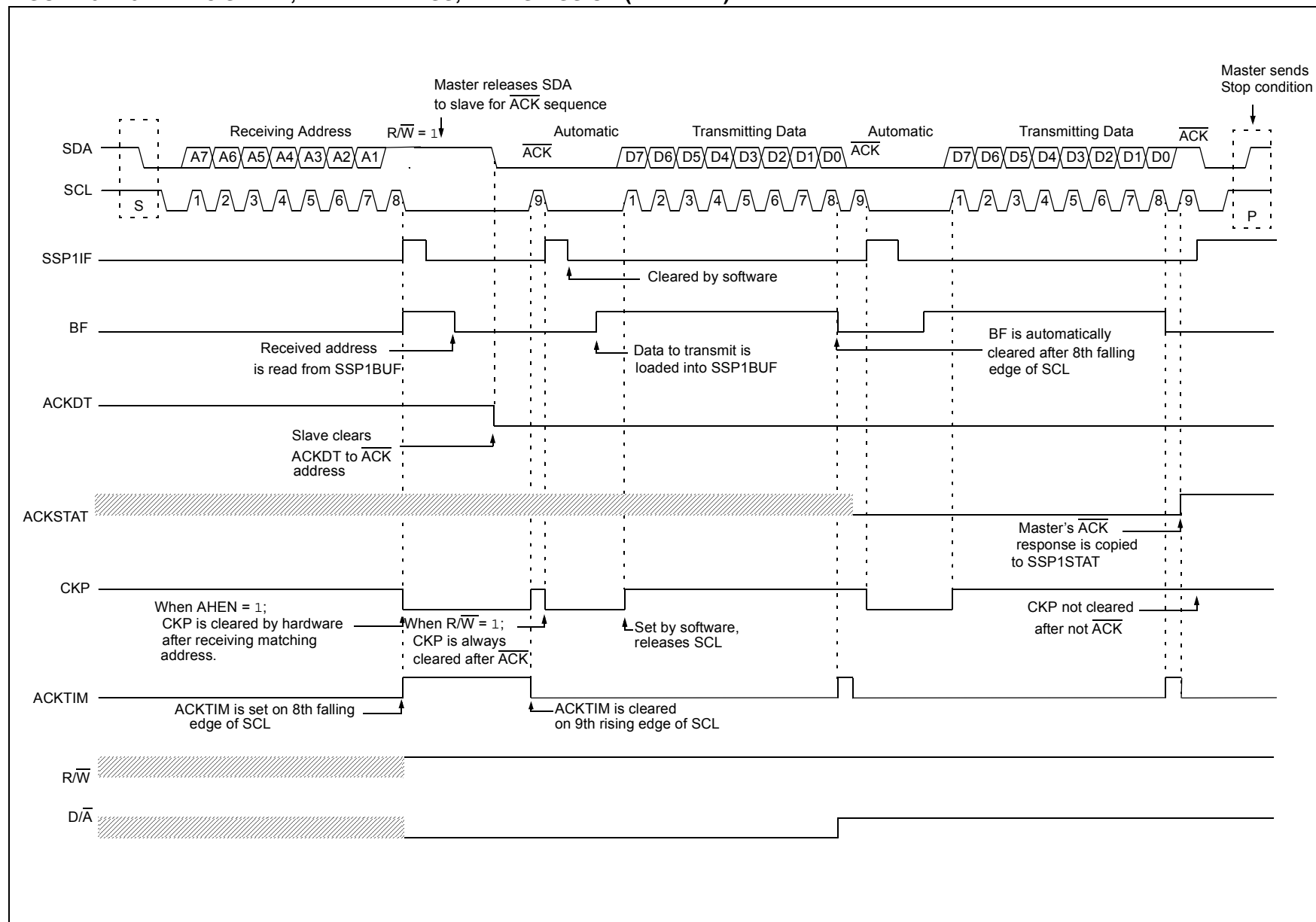
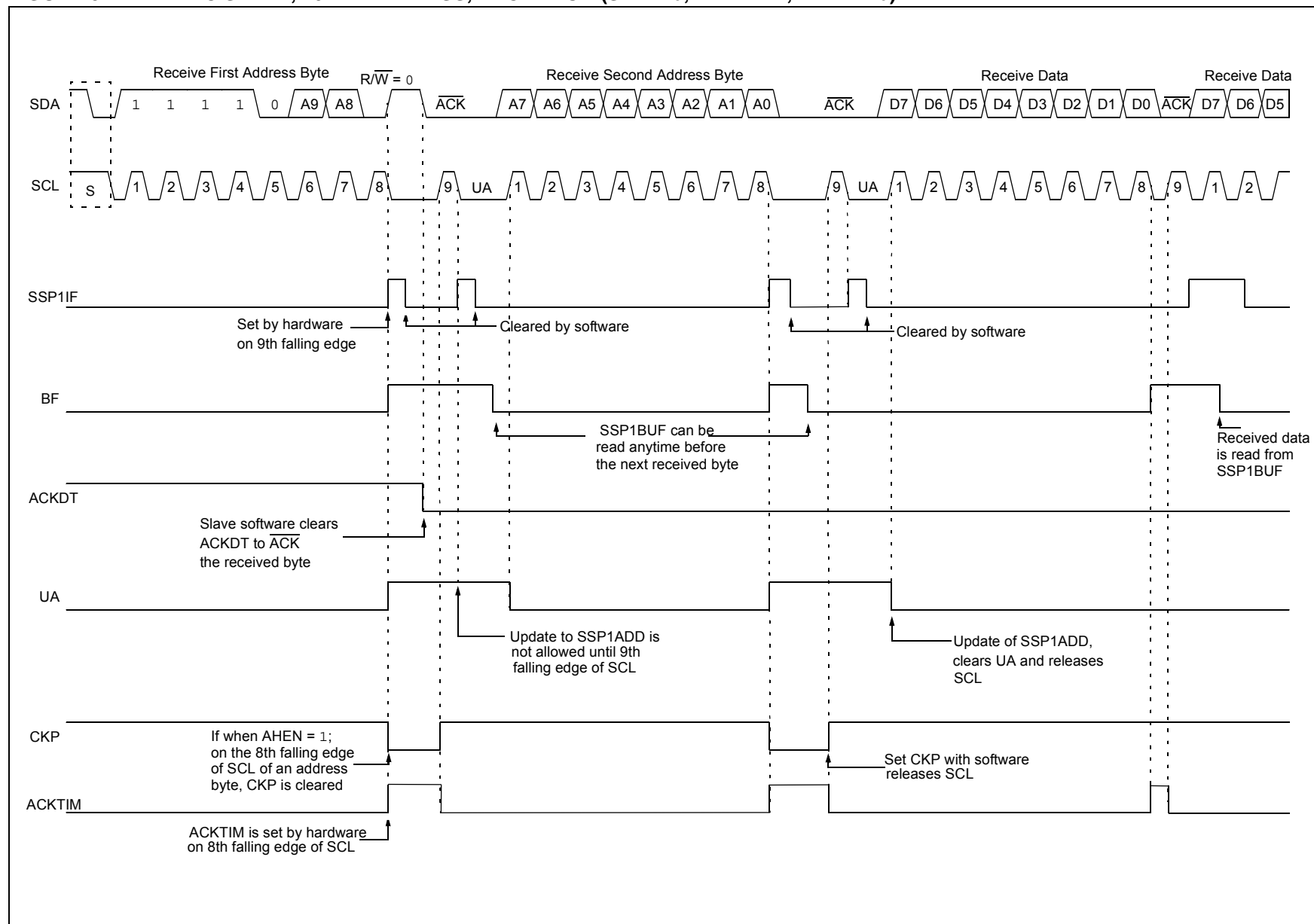
FIGURE 32-19: I²C SLAVE, 7-BIT ADDRESS, TRANSMISSION (AHEN = 1)

FIGURE 32-21: I²C SLAVE, 10-BIT ADDRESS, RECEPTION (SEN = 0, AHEN = 1, DHEN = 0)

32.8 Register Definitions: MSSP1 Control

REGISTER 32-1: SSP1STAT: SSP1 STATUS REGISTER

R/W-0/0	R/W-0/0	R/HS/HC-0	R/HS/HC-0	R/HS/HC-0	R/HS/HC-0	R/HS/HC-0	R/HS/HC-0
SMP	CKE ⁽¹⁾	D/A	P ⁽²⁾	S ⁽²⁾	R/W	UA	BF
bit 7							bit 0

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	HS/HC = Hardware set/clear

bit 7	SMP: SPI Data Input Sample bit <u>SPI Master mode:</u> 1 = Input data sampled at end of data output time 0 = Input data sampled at middle of data output time <u>SPI Slave mode:</u> SMP must be cleared when SPI is used in Slave mode <u>In I²C Master or Slave mode:</u> 1 = Slow rate control disabled for Standard Speed mode (100 kHz and 1 MHz) 0 = Slow rate control enabled for High-Speed mode (400 kHz)
bit 6	CKE: SPI Clock Edge Select bit (SPI mode only) ⁽¹⁾ <u>In SPI Master or Slave mode:</u> 1 = Transmit occurs on transition from active to Idle clock state 0 = Transmit occurs on transition from Idle to active clock state <u>In I²C mode only:</u> 1 = Enable input logic so that thresholds are compliant with SMBus specification 0 = Disable SMBus specific inputs
bit 5	D/A: Data/Address bit (I ² C mode only) 1 = Indicates that the last byte received or transmitted was data 0 = Indicates that the last byte received or transmitted was address
bit 4	P: Stop bit ⁽²⁾ (I ² C mode only. This bit is cleared when the MSSP module is disabled, SSPEN is cleared.) 1 = Indicates that a Stop bit has been detected last (this bit is '0' on Reset) 0 = Stop bit was not detected last
bit 3	S: Start bit ⁽²⁾ (I ² C mode only. This bit is cleared when the MSSP module is disabled, SSPEN is cleared.) 1 = Indicates that a Start bit has been detected last (this bit is '0' on Reset) 0 = Start bit was not detected last
bit 2	R/W: Read/Write bit information (I ² C mode only) This bit holds the R/W bit information following the last address match. This bit is only valid from the address match to the next Start bit, Stop bit, or not ACK bit. <u>In I²C Slave mode:</u> 1 = Read 0 = Write <u>In I²C Master mode:</u> 1 = Transmit is in progress 0 = Transmit is not in progress OR-ing this bit with SEN, RSEN, PEN, RCEN or ACKEN will indicate if the MSSP is in IDLE mode.
bit 1	UA: Update Address bit (10-bit I ² C mode only) 1 = Indicates that the user needs to update the address in the SSP1ADD register 0 = Address does not need to be updated
bit 0	BF: Buffer Full Status bit <u>Receive (SPI and I²C modes):</u> 1 = Receive complete, SSPBUF is full 0 = Receive not complete, SSPBUF is empty <u>Transmit (I²C mode only):</u> 1 = Data transmit in progress (does not include the ACK and Stop bits), SSP1BUF is full 0 = Data transmit complete (does not include the ACK and Stop bits), SSP1BUF is empty

- Note** 1: Polarity of clock state is set by the CKP bit of the SSP1CON register.
 2: This bit is cleared on Reset and when SSPEN is cleared.

36.2 General Format for Instructions

TABLE 36-3: INSTRUCTION SET

Mnemonic, Operands		Description	Cycles	14-Bit Opcode				Status Affected	Notes
				MSb		LSb			
BYTE-ORIENTED FILE REGISTER OPERATIONS									
ADDWF	f, d	Add W and f	1	00	0111	dfff	ffff	C, DC, Z	2
ADDWFC	f, d	Add with Carry W and f	1	11	1101	dfff	ffff	C, DC, Z	2
ANDWF	f, d	AND W with f	1	00	0101	dfff	ffff	Z	2
ASRF	f, d	Arithmetic Right Shift	1	11	0111	dfff	ffff	C, Z	2
LSLF	f, d	Logical Left Shift	1	11	0101	dfff	ffff	C, Z	2
LSRF	f, d	Logical Right Shift	1	11	0110	dfff	ffff	C, Z	2
CLRF	f	Clear f	1	00	0001	1fff	ffff	Z	2
CLRW	—	Clear W	1	00	0001	0000	00xx	Z	
COMF	f, d	Complement f	1	00	1001	dfff	ffff	Z	2
DECF	f, d	Decrement f	1	00	0011	dfff	ffff	Z	2
INCF	f, d	Increment f	1	00	1010	dfff	ffff	Z	2
IORWF	f, d	Inclusive OR W with f	1	00	0100	dfff	ffff	Z	2
MOVF	f, d	Move f	1	00	1000	dfff	ffff	Z	2
MOVWF	f	Move W to f	1	00	0000	1fff	ffff		2
RLF	f, d	Rotate Left f through Carry	1	00	1101	dfff	ffff	C	2
RRF	f, d	Rotate Right f through Carry	1	00	1100	dfff	ffff	C	2
SUBWF	f, d	Subtract W from f	1	00	0010	dfff	ffff	C, DC, Z	2
SUBWFB	f, d	Subtract with Borrow W from f	1	11	1011	dfff	ffff	C, DC, Z	2
SWAPF	f, d	Swap nibbles in f	1	00	1110	dfff	ffff		2
XORWF	f, d	Exclusive OR W with f	1	00	0110	dfff	ffff	Z	2
BYTE ORIENTED SKIP OPERATIONS									
DECFSZ	f, d	Decrement f, Skip if 0	1(2)	00	1011	dfff	ffff		1, 2
INCFSZ	f, d	Increment f, Skip if 0	1(2)	00	1111	dfff	ffff		1, 2
BIT-ORIENTED FILE REGISTER OPERATIONS									
BCF	f, b	Bit Clear f	1	01	00bb	bfff	ffff		2
BSF	f, b	Bit Set f	1	01	01bb	bfff	ffff		2
BIT-ORIENTED SKIP OPERATIONS									
BTFSC	f, b	Bit Test f, Skip if Clear	1 (2)	01	10bb	bfff	ffff		1, 2
BTFSS	f, b	Bit Test f, Skip if Set	1 (2)	01	11bb	bfff	ffff		1, 2
LITERAL OPERATIONS									
ADDLW	k	Add literal and W	1	11	1110	kkkk	kkkk	C, DC, Z	
ANDLW	k	AND literal with W	1	11	1001	kkkk	kkkk	Z	
IORLW	k	Inclusive OR literal with W	1	11	1000	kkkk	kkkk	Z	
MOVLB	k	Move literal to BSR	1	00	000	0k	kkkk		
MOVLPL	k	Move literal to PCLATH	1	11	0001	1kkk	kkkk		
MOVLW	k	Move literal to W	1	11	0000	kkkk	kkkk		
SUBLW	k	Subtract W from literal	1	11	1100	kkkk	kkkk	C, DC, Z	
XORLW	k	Exclusive OR literal with W	1	11	1010	kkkk	kkkk	Z	

- Note 1:** If the Program Counter (PC) is modified, or a conditional test is true, the instruction requires two cycles. The second cycle is executed as a NOP.
- 2:** If this instruction addresses an INDF register and the MSb of the corresponding FSR is set, this instruction will require one additional instruction cycle.

TABLE 37-18: TIMER0 AND TIMER1 EXTERNAL CLOCK REQUIREMENTS

Standard Operating Conditions (unless otherwise stated)									
Operating Temperature $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$									
Param. No.	Sym.	Characteristic		Min.	Typ†	Max.	Units	Conditions	
40*	Tt0H	T0CKI High Pulse Width	No Prescaler	$0.5 T_{CY} + 20$	—	—	ns	N = prescale value	
			With Prescaler	10	—	—	ns		
41*	Tt0L	T0CKI Low Pulse Width	No Prescaler	$0.5 T_{CY} + 20$	—	—	ns		
			With Prescaler	10	—	—	ns		
42*	Tt0P	T0CKI Period		Greater of: 20 or $\frac{T_{CY} + 40}{N}$	—	—	ns		
45*	Tt1H	T1CKI High Time	Synchronous, No Prescaler	$0.5 T_{CY} + 20$	—	—	ns		
			Synchronous, with Prescaler		15	—	—		ns
			Asynchronous		30	—	—		ns
46*	Tt1L	T1CKI Low Time	Synchronous, No Prescaler	$0.5 T_{CY} + 20$	—	—	ns		
			Synchronous, with Prescaler		15	—	—		ns
			Asynchronous		30	—	—		ns
47*	Tt1P	T1CKI Input Period	Synchronous	Greater of: 30 or $\frac{T_{CY} + 40}{N}$	—	—	ns	N = prescale value	
			Asynchronous		60	—	—		ns
49*	TCKEZTMR1	Delay from External Clock Edge to Timer Increment		$2 T_{OSC}$	—	$7 T_{OSC}$	—	Timers in Sync mode	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

FIGURE 37-14: CLC PROPAGATION TIMING

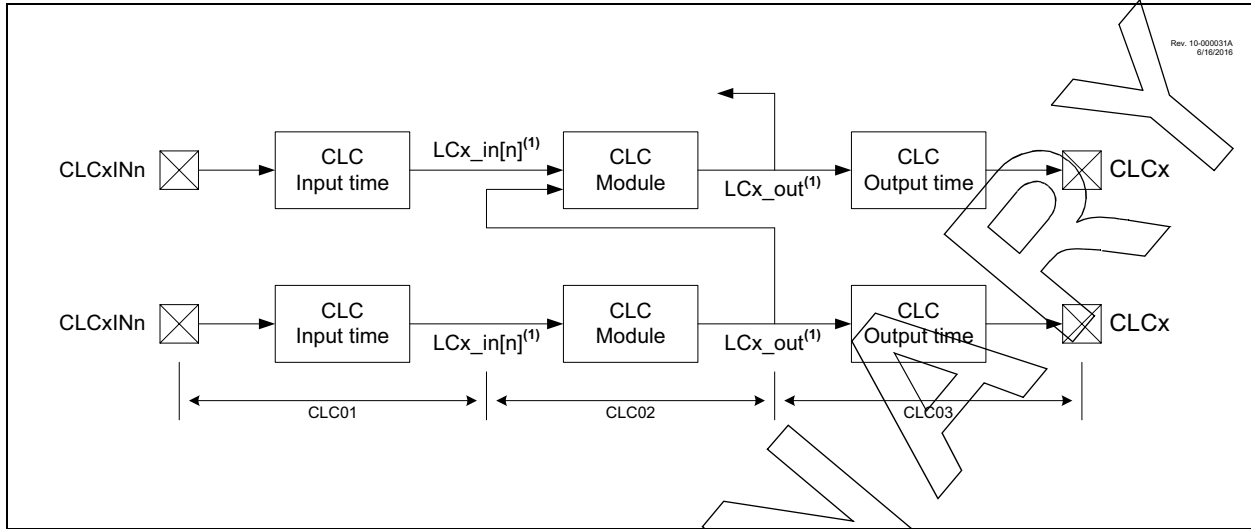


TABLE 37-20: CONFIGURABLE LOGIC CELL (CLC) CHARACTERISTICS

Standard Operating Conditions (unless otherwise stated)							
Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$							
Param. No.	Sym.	Characteristic	Min.	Typ†	Max.	Units	Conditions
CLC01*	TCLCIN	CLC input time	—	7	IO5	ns	(Note 1)
CLC02*	TCLC	CLC module input to output propagation time	—	24 12	— —	ns ns	VDD = 1.8V VDD > 3.6V
CLC03*	TCLCOUT	CLC output time	—	IO7	—	—	(Note 1)
		Rise Time					
		Fall Time	—	IO8	—	—	(Note 1)
CLC04*	FCLCMAX	CLC maximum switching frequency	—	32	Fosc	MHz	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: See Table 37-10 for IO5, IO7 and IO8 rise and fall times.

TABLE 37-25: I²C BUS DATA REQUIREMENTS

Standard Operating Conditions (unless otherwise stated)							
Param. No.	Symbol	Characteristic		Min.	Max.	Units	Conditions
SP100*	THIGH	Clock high time	100 kHz mode	4.0	—	μs	Device must operate at a minimum of 1.5 MHz
			400 kHz mode	0.6	—	μs	Device must operate at a minimum of 10 MHz
			SSP module	1.5Tcy	—		
SP101*	TLOW	Clock low time	100 kHz mode	4.7	—	μs	Device must operate at a minimum of 1.5 MHz
			400 kHz mode	1.3	—	μs	Device must operate at a minimum of 10 MHz
			SSP module	1.5Tcy	—		
SP102*	TR	SDA and SCL rise time	100 kHz mode	—	1000	ns	
			400 kHz mode	20 + 0.1CB	300	ns	CB is specified to be from 10-400 pF
SP103*	TF	SDA and SCL fall time	100 kHz mode	—	250	ns	
			400 kHz mode	20 + 0.1CB	250	ns	CB is specified to be from 10-400 pF
SP106*	THD:DAT	Data input hold time	100 kHz mode	0	—	ns	
			400 kHz mode	0	0.9	μs	
SP107*	TSU:DAT	Data input setup time	100 kHz mode	250	—	ns	(Note 2)
			400 kHz mode	100	—	ns	
SP109*	TAA	Output valid from clock	100 kHz mode	—	3500	ns	(Note 1)
			400 kHz mode	—	—	ns	
SP110*	TBUF	Bus free time	100 kHz mode	4.7	—	μs	Time the bus must be free before a new transmission can start
			400 kHz mode	1.3	—	μs	
SP111	CB	Bus capacitive loading		—	400	pF	

* These parameters are characterized but not tested.

- Note 1:** As a transmitter, the device must provide this internal minimum delay time to bridge the undefined region (min. 300 ns) of the falling edge of SCL to avoid unintended generation of Start or Stop conditions.
- 2:** A Fast mode (400 kHz) I²C bus device can be used in a Standard mode (100 kHz) I²C bus system, but the requirement TSU:DAT ≥ 250 ns must then be met. This will automatically be the case if the device does not stretch the low period of the SCL signal. If such a device does stretch the low period of the SCL signal, it must output the next data bit to the SDA line T_R max. + TSU:DAT = 1000 + 250 = 1250 ns (according to the Standard mode I²C bus specification), before the SCL line is released.