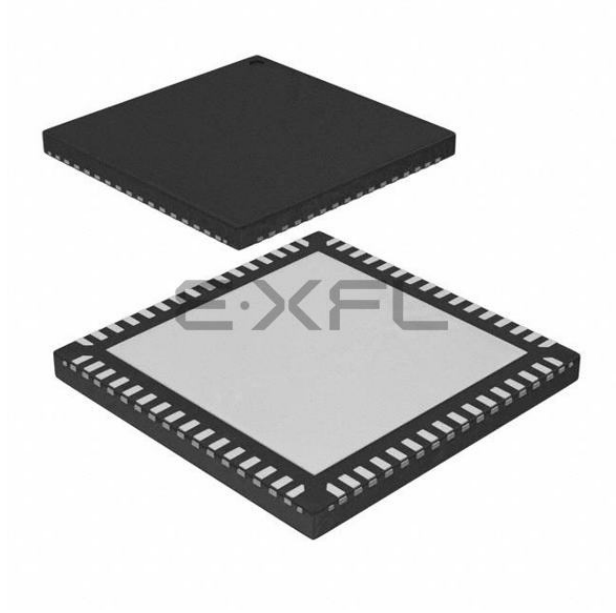

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	AVR
Core Size	8/16-Bit
Speed	32MHz
Connectivity	I²C, IrDA, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	50
Program Memory Size	128KB (64K x 16)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad
Supplier Device Package	64-QFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atxmega128a3u-mhr

MCU are the two-wire interface address match interrupt, asynchronous port interrupts, and the USB resume interrupt.

11.3.3 Power-save Mode

Power-save mode is identical to power down, with one exception. If the real-time counter (RTC) is enabled, it will keep running during sleep, and the device can also wake up from either an RTC overflow or compare match interrupt.

11.3.4 Standby Mode

Standby mode is identical to power down, with the exception that the enabled system clock sources are kept running while the CPU, peripheral, and RTC clocks are stopped. This reduces the wake-up time.

11.3.5 Extended Standby Mode

Extended standby mode is identical to power-save mode, with the exception that the enabled system clock sources are kept running while the CPU and peripheral clocks are stopped. This reduces the wake-up time.

12.4.2 Brownout Detection

The on-chip brownout detection (BOD) circuit monitors the V_{CC} level during operation by comparing it to a fixed, programmable level that is selected by the BODLEVEL fuses. If disabled, BOD is forced on at the lowest level during chip erase and when the PDI is enabled.

12.4.3 External Reset

The external reset circuit is connected to the external $\overline{\text{RESET}}$ pin. The external reset will trigger when the $\overline{\text{RESET}}$ pin is driven below the $\overline{\text{RESET}}$ pin threshold voltage, V_{RST}, for longer than the minimum pulse period, t_{EXT}. The reset will be held as long as the pin is kept low. The $\overline{\text{RESET}}$ pin includes an internal pull-up resistor.

12.4.4 Watchdog Reset

The watchdog timer (WDT) is a system function for monitoring correct program operation. If the WDT is not reset from the software within a programmable timeout period, a watchdog reset will be given. The watchdog reset is active for one to two clock cycles of the 2MHz internal oscillator. For more details see “WDT – Watchdog Timer” on page 29.

12.4.5 Software Reset

The software reset makes it possible to issue a system reset from software by writing to the software reset bit in the reset control register.The reset will be issued within two CPU clock cycles after writing the bit. It is not possible to execute any instruction from when a software reset is requested until it is issued.

12.4.6 Program and Debug Interface Reset

The program and debug interface reset contains a separate reset source that is used to reset the device during external programming and debugging. This reset source is accessible only from external debuggers and programmers.

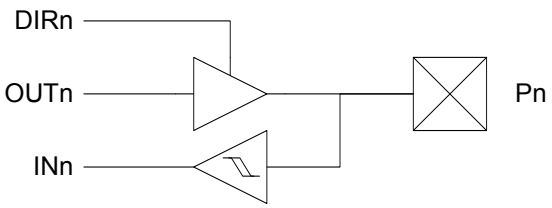
Program address (base address)	Source	Interrupt description
0x018	TWIC_INT_base	Two-Wire Interface on Port C Interrupt base
0x01C	TCC0_INT_base	Timer/Counter 0 on port C Interrupt base
0x028	TCC1_INT_base	Timer/Counter 1 on port C Interrupt base
0x030	SPIC_INT_vect	SPI on port C Interrupt vector
0x032	USARTC0_INT_base	USART 0 on port C Interrupt base
0x038	USARTC1_INT_base	USART 1 on port C Interrupt base
0x03E	AES_INT_vect	AES Interrupt vector
0x040	NVM_INT_base	Non-Volatile Memory Interrupt base
0x044	PORTB_INT_base	Port B Interrupt base
0x048	ACB_INT_base	Analog Comparator on Port B Interrupt base
0x04E	ADCB_INT_base	Analog to Digital Converter on Port B Interrupt base
0x056	PORTE_INT_base	Port E INT base
0x05A	TWIE_INT_base	Two-Wire Interface on Port E Interrupt base
0x05E	TCE0_INT_base	Timer/Counter 0 on port E Interrupt base
0x06A	TCE1_INT_base	Timer/Counter 1 on port E Interrupt base
0x072	SPIE_INT_vect	SPI on port E Interrupt vector
0x074	USARTE0_INT_base	USART 0 on port E Interrupt base
0x07A	USARTE1_INT_base	USART 1 on port E Interrupt base
0x080	PORTD_INT_base	Port D Interrupt base
0x084	PORTA_INT_base	Port A Interrupt base
0x088	ACA_INT_base	Analog Comparator on Port A Interrupt base
0x08E	ADCA_INT_base	Analog to Digital Converter on Port A Interrupt base
0x09A	TCD0_INT_base	Timer/Counter 0 on port D Interrupt base
0x0A6	TCD1_INT_base	Timer/Counter 1 on port D Interrupt base
0x0AE	SPID_INT_vector	SPI D Interrupt vector
0x0B0	USARTD0_INT_base	USART 0 on port D Interrupt base
0x0B6	USARTD1_INT_base	USART 1 on port D Interrupt base
0x0D0	PORTF_INT_base	Port F Interrupt base
0x0D8	TCF0_INT_base	Timer/Counter 0 on port F Interrupt base
0x0EE	USARTF0_INT_base	USART 0 on port F Interrupt base
0x0FA	USB_INT_base	USB on port D Interrupt base

15.3 Output Driver

All port pins (Pn) have programmable output configuration. The port pins also have configurable slew rate limitation to reduce electromagnetic emission.

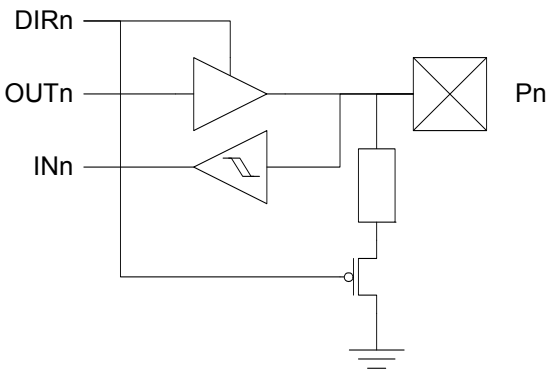
15.3.1 Push-pull

Figure 15-1. I/O configuration - Totem-pole.



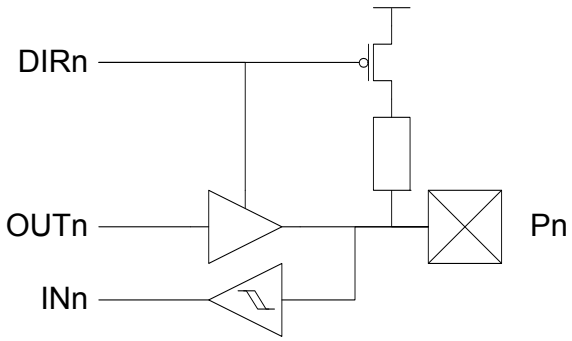
15.3.2 Pull-down

Figure 15-2. I/O configuration - Totem-pole with pull-down (on input).



15.3.3 Pull-up

Figure 15-3. I/O configuration - Totem-pole with pull-up (on input).



A timer/counter can be clocked and timed from the peripheral clock with optional prescaling or from the event system. The event system can also be used for direction control and capture trigger or to synchronize operations.

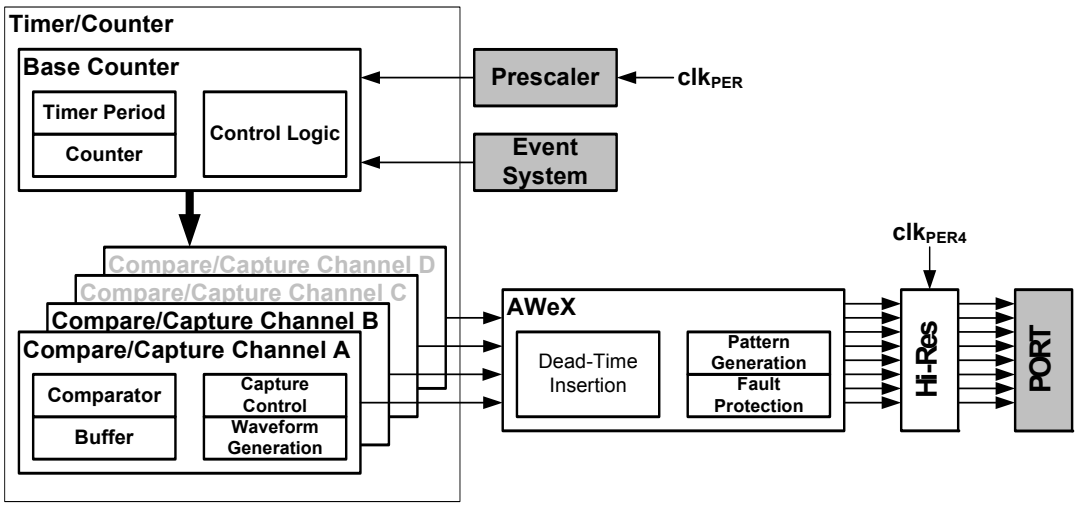
There are two differences between timer/counter type 0 and type 1. Timer/counter 0 has four CC channels, and timer/counter 1 has two CC channels. All information related to CC channels 3 and 4 is valid only for timer/counter 0. Only Timer/Counter 0 has the split mode feature that split it into two 8-bit Timer/Counters with four compare channels each.

Some timer/counters have extensions to enable more specialized waveform and frequency generation. The advanced waveform extension (AWeX) is intended for motor control and other power control applications. It enables low- and high-side output with dead-time insertion, as well as fault protection for disabling and shutting down external drivers. It can also generate a synchronized bit pattern across the port pins.

The advanced waveform extension can be enabled to provide extra and more advanced features for the Timer/Counter. This are only available for Timer/Counter 0. See “AWeX – Advanced Waveform Extension” on page 39 for more details.

The high-resolution (hi-res) extension can be used to increase the waveform output resolution by four or eight times by using an internal clock source running up to four times faster than the peripheral clock. See “Hi-Res – High Resolution Extension” on page 40 for more details.

Figure 16-1. Overview of a Timer/Counter and closely related peripherals.



PORTC, PORTD and PORTE each has one Timer/Counter 0 and one Timer/Counter1. PORTF has one Timer/Counter 0. Notation of these are TCC0 (Time/Counter C0), TCC1, TCD0, TCD1, TCE0, TCE1 and TCF0, respectively.

25. IRCOM – IR Communication Module

25.1 Features

- Pulse modulation/demodulation for infrared communication
- IrDA compatible for baud rates up to 115.2Kbps
- Selectable pulse modulation scheme
  - 3/16 of the baud rate period
  - Fixed pulse period, 8-bit programmable
  - Pulse modulation disabled
- Built-in filtering
- Can be connected to and used by any USART

25.2 Overview

Atmel AVR XMEGA devices contain an infrared communication module (IRCOM) that is IrDA compatible for baud rates up to 115.2Kbps. It can be connected to any USART to enable infrared pulse encoding/decoding for that USART.

31. Programming and Debugging

31.1 Features

- Programming
  - External programming through PDI or JTAG interfaces
    - Minimal protocol overhead for fast operation
    - Built-in error detection and handling for reliable operation
  - Boot loader support for programming through any communication interface
- Debugging
  - Nonintrusive, real-time, on-chip debug system
  - No software or hardware resources required from device except pin connection
  - Program flow control
    - Go, Stop, Reset, Step Into, Step Over, Step Out, Run-to-Cursor
  - Unlimited number of user program breakpoints
  - Unlimited number of user data breakpoints, break on:
    - Data location read, write, or both read and write
    - Data location content equal or not equal to a value
    - Data location content is greater or smaller than a value
    - Data location content is within or outside a range
  - No limitation on device clock frequency
- Program and Debug Interface (PDI)
  - Two-pin interface for external programming and debugging
  - Uses the Reset pin and a dedicated pin
  - No I/O pins required during programming or debugging
- JTAG interface
  - Four-pin, IEEE Std. 1149.1 compliant interface for programming and debugging
  - Boundary scan capabilities according to IEEE Std. 1149.1 (JTAG)

31.2 Overview

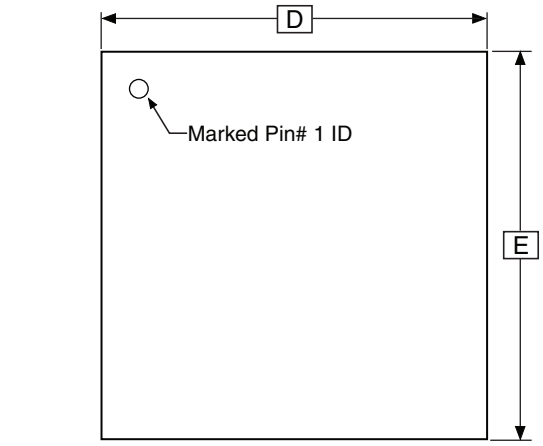
The Program and Debug Interface (PDI) is an Atmel proprietary interface for external programming and on-chip debugging of a device.

The PDI supports fast programming of nonvolatile memory (NVM) spaces; flash, EEPOM, fuses, lock bits, and the user signature row.

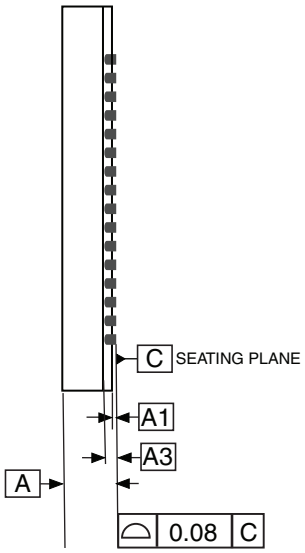
Debug is supported through an on-chip debug system that offers nonintrusive, real-time debug. It does not require any software or hardware resources except for the device pin connection. Using the Atmel tool chain, it offers complete program flow control and support for an unlimited number of program and complex data breakpoints. Application debug can be done from a C or other high-level language source code level, as well as from an assembler and disassembler level.

Programming and debugging can be done through two physical interfaces. The primary one is the PDI physical layer, which is available on all devices. This is a two-pin interface that uses the Reset pin for the clock input (PDI_CLK) and one other dedicated pin for data input and output (PDI_DATA). A JTAG interface is also available on most devices, and this can be used for programming and debugging through the four-pin JTAG interface. The JTAG interface is IEEE Std. 1149.1 compliant, and supports boundary scan. Any external programmer or on-chip debugger/emulator can be directly connected to either of these interfaces. Unless otherwise stated, all references to the PDI assume access through the PDI physical layer.

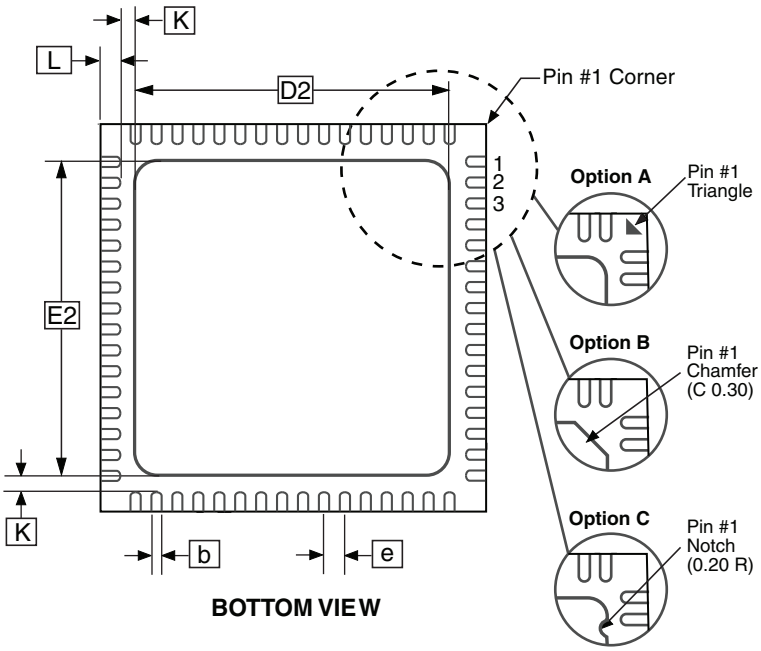
35.2 64M2



TOP VIEW



SIDE VIEW



BOTTOM VIEW

COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	0.80	0.90	1.00	
A1	–	0.02	0.05	
A3		0.20 REF		
b	0.18	0.25	0.30	
D	8.90	9.00	9.10	
D2	7.50	7.65	7.80	
E	8.90	9.00	9.10	
E2	7.50	7.65	7.80	
e		0.50 BSC		
L	0.35	0.40	0.45	
K	0.20	0.27	0.40	

Notes: 1. JEDEC Standard MO-220, (SAW Singulation) Fig. 1, VMMD.
2. Dimension and tolerance conform to ASMEY14.5M-1994.

2014-05-30

	TITLE	DRAWING NO.	REV.
Atmel 2325 Orchard Parkway San Jose, CA 95131	**64M2**, 64-pad, 9 x 9 x 1.0mm Bod y, Lead Pitch 0.50mm , 7.65mm Exposed Pad,Quad Flat No Lead Package (QFN)	64M2	F

Symbol	Parameter	Condition		Min.	Typ.	Max.	Units
R_Q	Negative impedance (1)	XOSCPWR=0, FRQRANGE=0	0.4MHz resonator, CL=100pF	2.4k			Ω
			1MHz crystal, CL=20pF	8.7k			
			2MHz crystal, CL=20pF	2.1k			
		XOSCPWR=0, FRQRANGE=1, CL=20pF	2MHz crystal	4.2k			
			8MHz crystal	250			
			9MHz crystal	195			
		XOSCPWR=0, FRQRANGE=2, CL=20pF	8MHz crystal	360			
			9MHz crystal	285			
			12MHz crystal	155			
		XOSCPWR=0, FRQRANGE=3, CL=20pF	9MHz crystal	365			
			12MHz crystal	200			
			16MHz crystal	105			
		XOSCPWR=1, FRQRANGE=0, CL=20pF	9MHz crystal	435			
			12MHz crystal	235			
			16MHz crystal	125			
		XOSCPWR=1, FRQRANGE=1, CL=20pF	9MHz crystal	495			
			12MHz crystal	270			
			16MHz crystal	145			
		XOSCPWR=1, FRQRANGE=2, CL=20pF	12MHz crystal	305			
			16MHz crystal	160			
		XOSCPWR=1, FRQRANGE=3, CL=20pF	12MHz crystal	380			
			16MHz crystal	205			
	ESR	SF = Safety factor				$\min(R_Q)/SF$	kΩ
C_{XTAL1}	Parasitic capacitance XTAL1 pin				5.2		pF
C_{XTAL2}	Parasitic capacitance XTAL2 pin				6.8		pF
C_{LOAD}	Parasitic capacitance load				2.95		pF

Note: 1. Numbers for negative impedance are not tested in production but guaranteed from design and characterization.

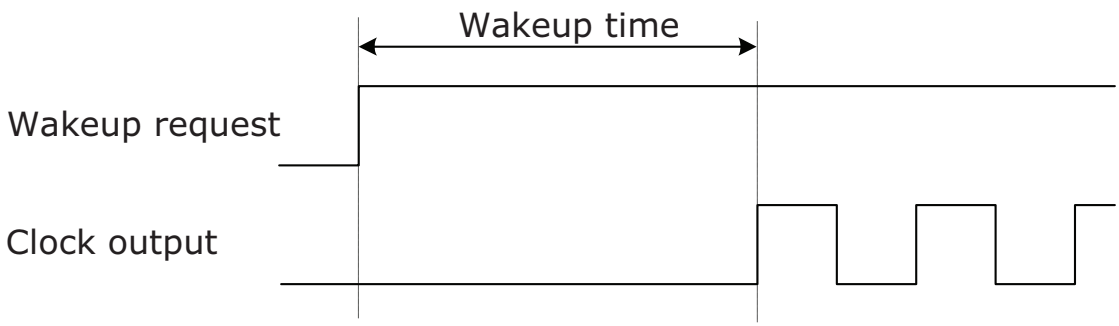
36.2.4 Wake-up time from sleep modes

Table 36-38. Device wake-up time from sleep modes with various system clock sources.

Symbol	Parameter	Condition	Min.	Typ. (1)	Max.	Units
t_{wakeup}	Wake-up time from Idle, Standby, and Extended Standby mode	External 2MHz clock		2		µs
		32.768kHz internal oscillator		120		
		2MHz internal oscillator		2		
		32MHz internal oscillator		0.2		
	Wake-up time from Power-save and Power-down mode	External 2MHz clock		4.5		µs
		32.768kHz internal oscillator		320		
		2MHz internal oscillator		9		
		32MHz internal oscillator		5		

Note: 1. The wake-up time is the time from the wake-up request is given until the peripheral clock is available on pin, see Figure 36-2. All peripherals and modules start execution from the first clock cycle, expect the CPU that is halted for four clock cycles before program execution starts.

Figure 36-9. Wake-up time definition.



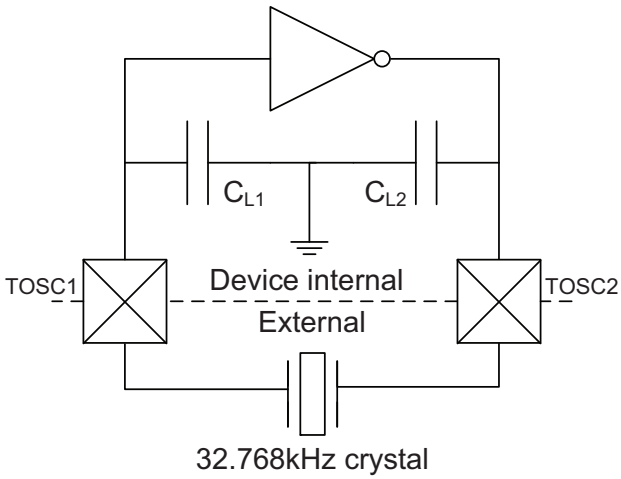
36.2.14.8 External 32.768kHz crystal oscillator and TOSC characteristics

Table 36-62. External 32.768kHz crystal oscillator and TOSC characteristics.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
ESR/R1	Recommended crystal equivalent series resistance (ESR)	Crystal load capacitance 6.5pF			60	kΩ
		Crystal load capacitance 9.0pF			35	
C_{TOSC1}	Parasitic capacitance TOSC1 pin			4.2		pF
C_{TOSC2}	Parasitic capacitance TOSC2 pin			4.3		pF
	Recommended safety factor	capacitance load matched to crystal specification	3			

Note: 1. See Figure 36-4 for definition.

Figure 36-11. TOSC input capacitance.



The parasitic capacitance between the TOSC pins is C_{L1} + C_{L2} in series as seen from the crystal when oscillating without external capacitors.

36.3.3 Current consumption

Table 36-68. Current consumption for active mode and sleep modes.

Symbol	Parameter	Condition		Min.	Typ.	Max.	Units
I_{CC}	Active Power consumption (1)	32kHz, Ext. Clk	V_{CC} = 1.8V		60		µA
			V_{CC} = 3.0V		140		
		1MHz, Ext. Clk	V_{CC} = 1.8V		260		
			V_{CC} = 3.0V		600		
		2MHz, Ext. Clk	V_{CC} = 1.8V		510	600	
			V_{CC} = 3.0V		1.1	1.5	mA
		32MHz, Ext. Clk			10.6	15	
	Idle Power consumption (1)	32kHz, Ext. Clk	V_{CC} = 1.8V		4.3		µA
			V_{CC} = 3.0V		4.8		
		1MHz, Ext. Clk	V_{CC} = 1.8V		78		
			V_{CC} = 3.0V		150		
		2MHz, Ext. Clk	V_{CC} = 1.8V		150	350	
			V_{CC} = 3.0V		290	600	
		32MHz, Ext. Clk			4.7	7.0	mA
	Power-down power consumption	T = 25°C	V_{CC} = 3.0V		0.1	1.0	µA
		T = 85°C			1.8	5.0	
		T = 105°C			6.5	17	
		WDT and Sampled BOD enabled, T = 25°C	V_{CC} = 3.0V		1.3	3.0	
		WDT and Sampled BOD enabled, T = 85°C			3.1	7.0	
		WDT and Sampled BOD enabled, T = 105°C			7.3	20	
	Power-save power consumption (2)	RTC from ULP clock, WDT and sampled BOD enabled, T = 25°C	V_{CC} = 1.8V		1.2		µA
			V_{CC} = 3.0V		1.3		
		RTC from 1.024kHz low power 32.768kHz TOSC, T = 25°C	V_{CC} = 1.8V		0.6	2	
			V_{CC} = 3.0V		0.7	2	
		RTC from low power 32.768kHz TOSC, T = 25°C	V_{CC} = 1.8V		0.8	3	
			V_{CC} = 3.0V		1.0	3	
	Reset power consumption	Current through $\overline{\text{RESET}}$ pin substracted	V_{CC} = 3.0V		250		µA

Notes: 1. All Power Reduction Registers set.
2. Maximum limits are based on characterization, and not tested in production.

37.2.1.3 Power-down mode supply current

Figure 37-98. Power-down mode supply current vs. V_{CC}.

All functions disabled.

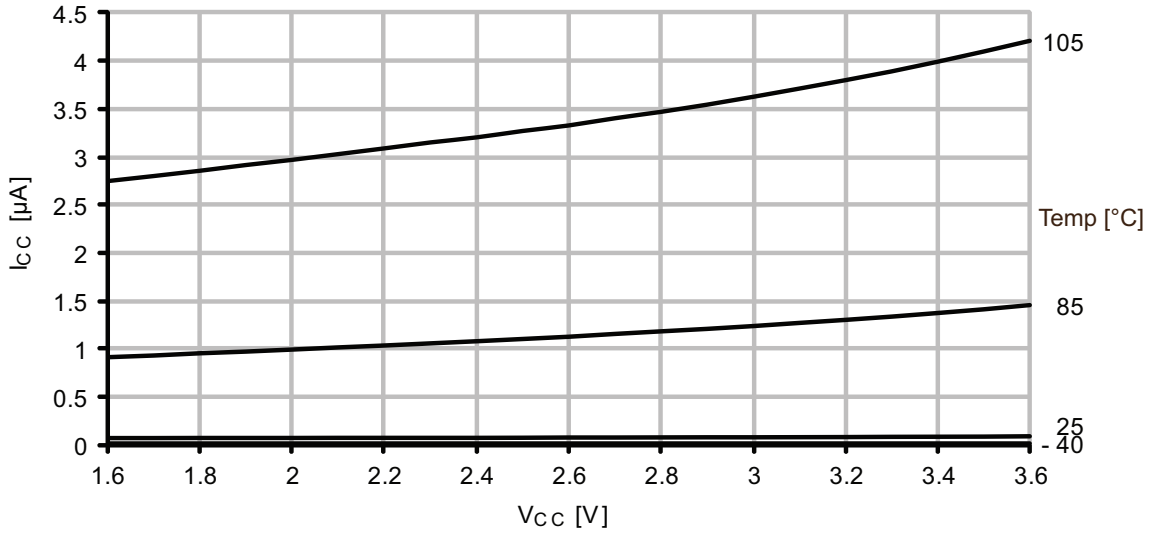
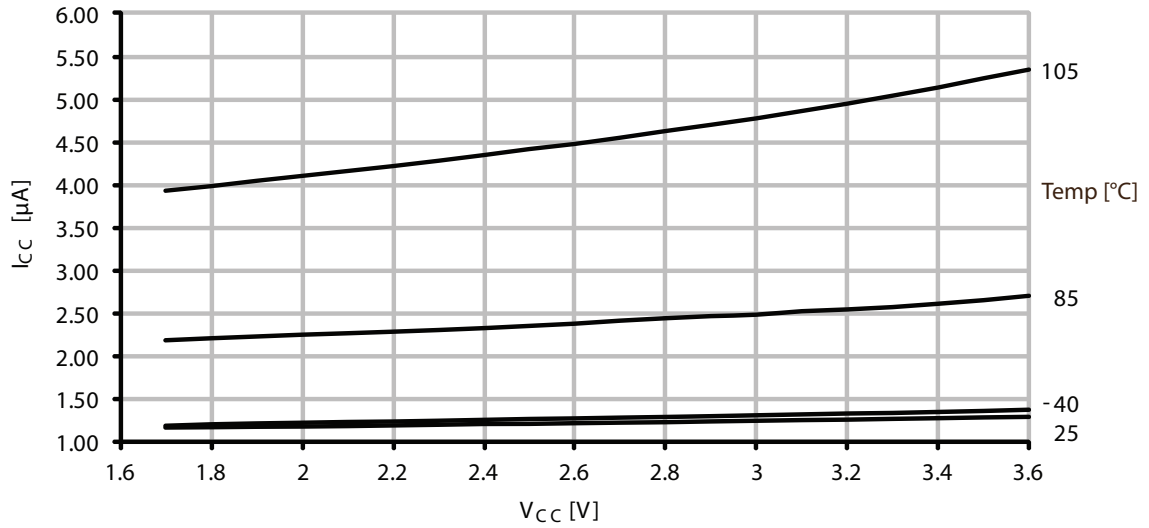


Figure 37-99. Power-down mode supply current vs. V_{CC}.

Watchdog and sampled BOD enabled.



37.2.8 External Reset Characteristics

Figure 37-144. Minimum Reset pin pulse width vs. V_{CC}.

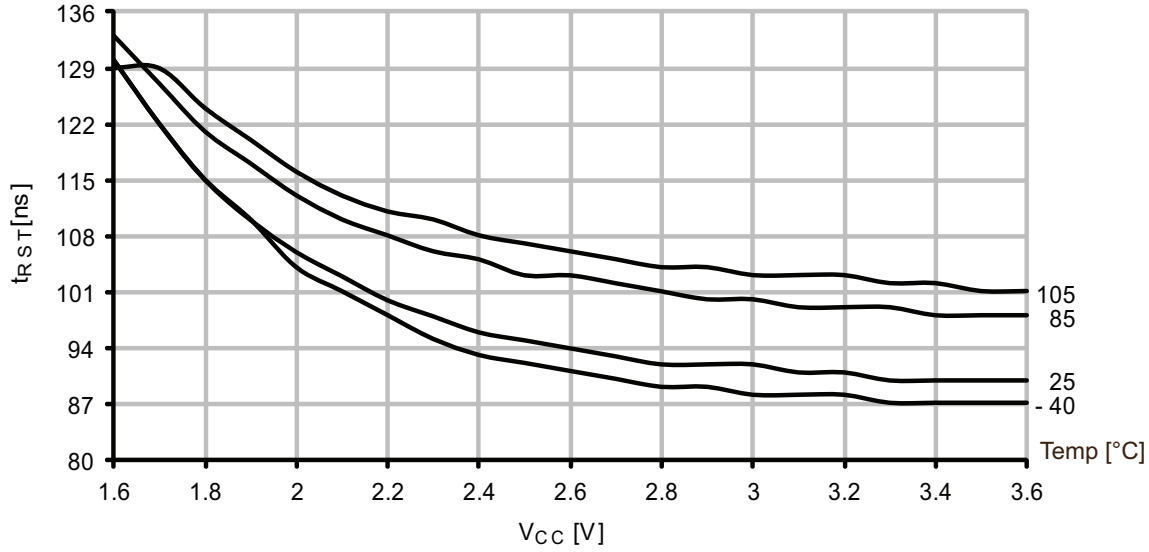


Figure 37-145. Reset pin pull-up resistor current vs. reset pin voltage.

V_{CC} = 1.8V.

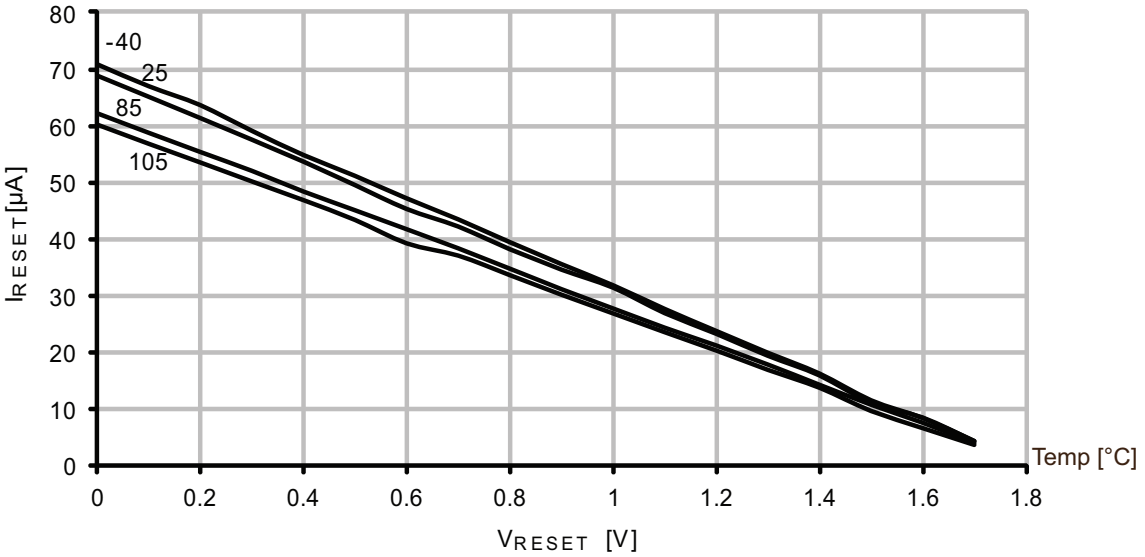


Figure 37-155. 2MHz internal oscillator frequency vs. temperature.

DFLL enabled, from the 32.768kHz internal oscillator.

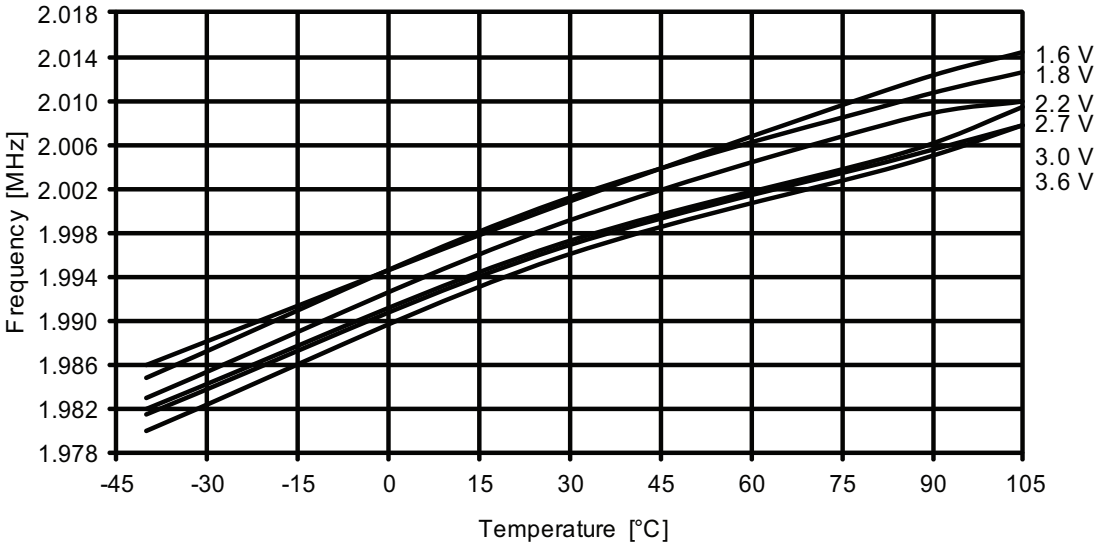


Figure 37-156. 2MHz internal oscillator CALA calibration step size.

V_{CC} = 3V.

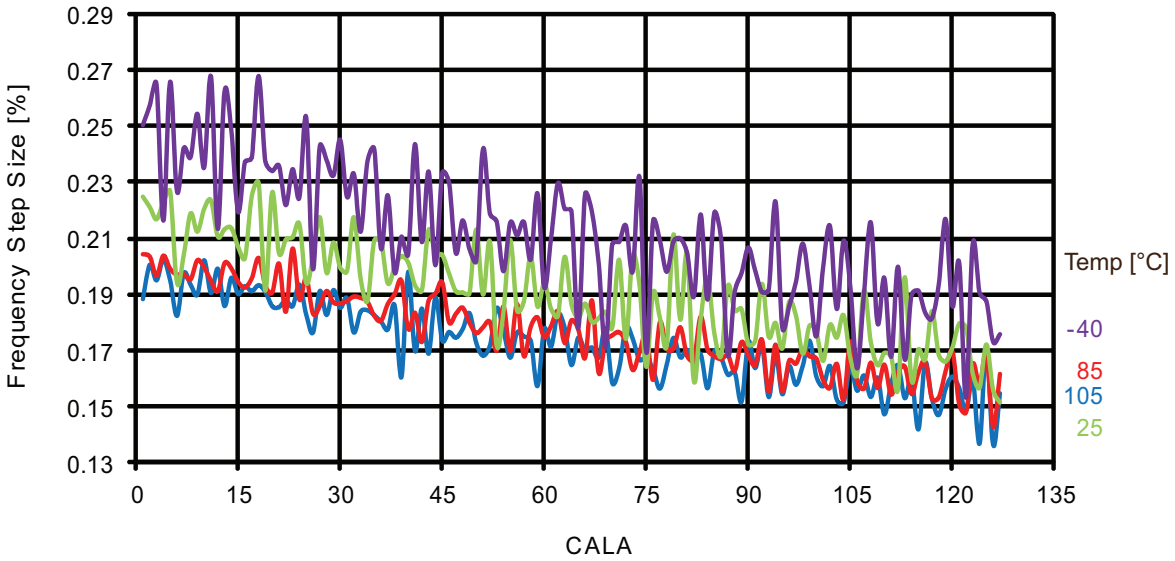


Figure 37-171. Active mode supply current vs. V_{CC}.

f_{SYS} = 2MHz internal oscillator.

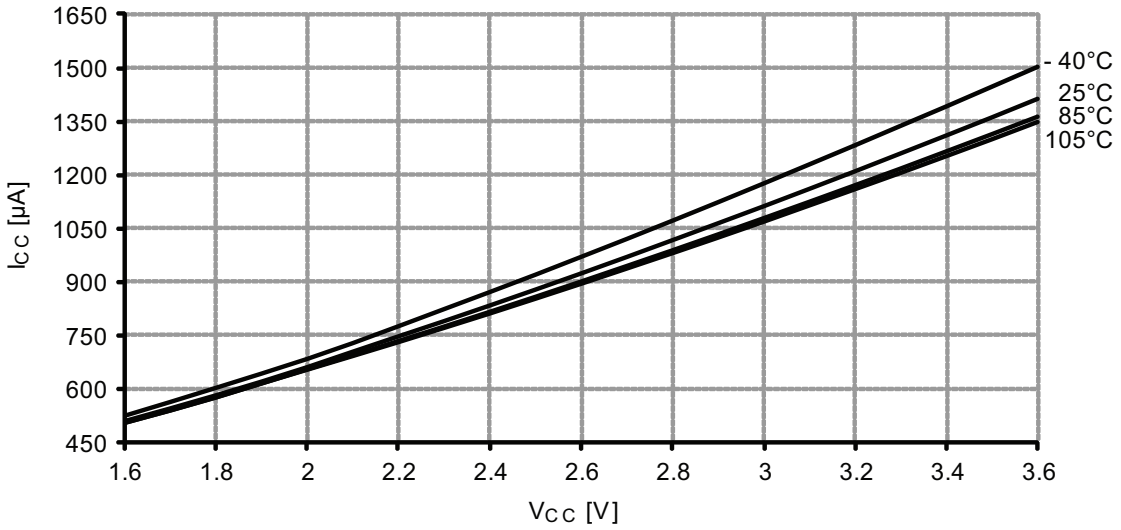


Figure 37-172. Active mode supply current vs. V_{CC}.

f_{SYS} = 32MHz internal oscillator prescaled to 8MHz.

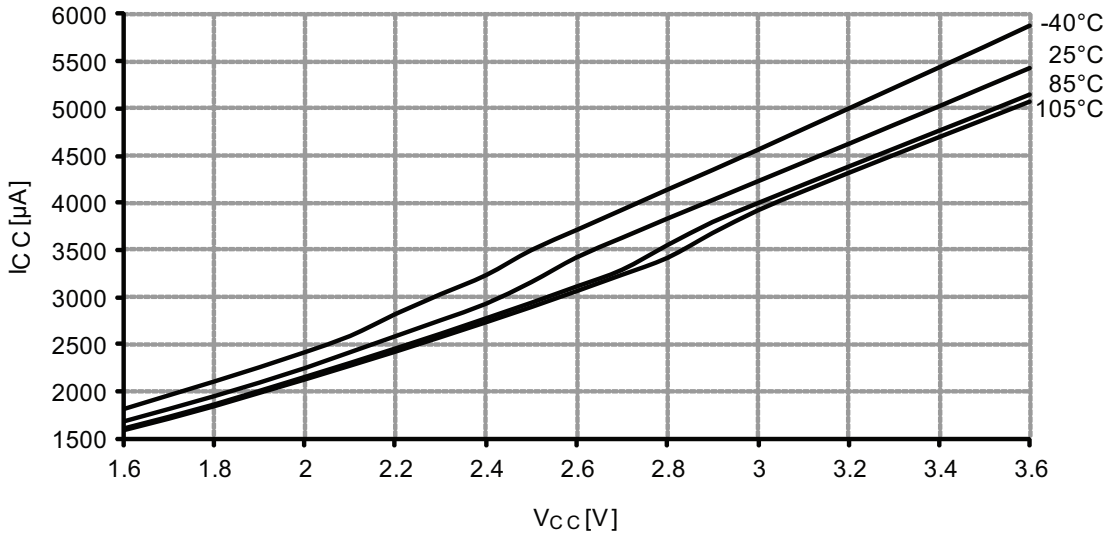


Figure 37-252. Active mode supply current vs. V_{CC}.

f_{SYS} = 32.768kHz internal oscillator.

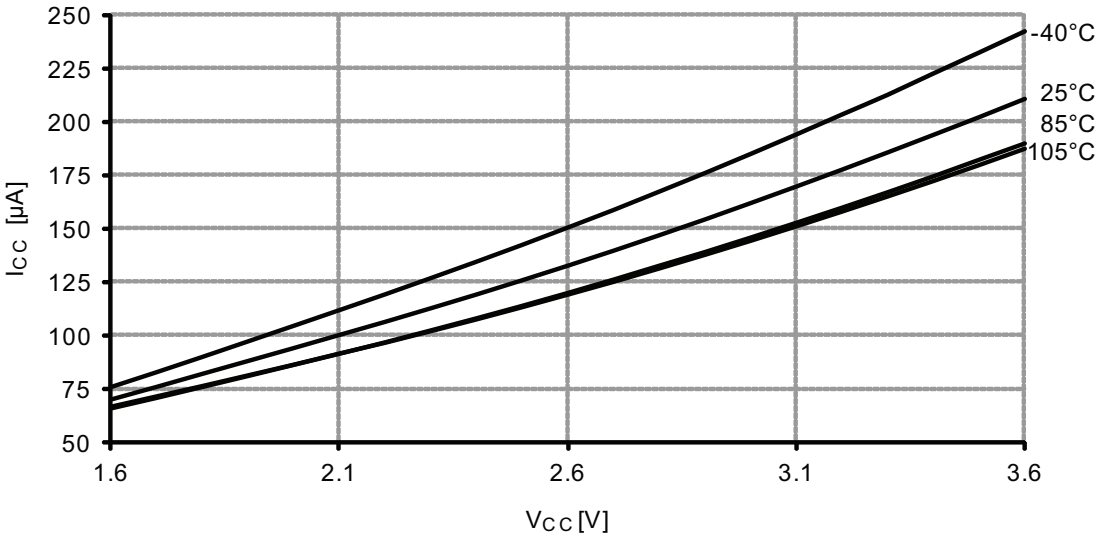
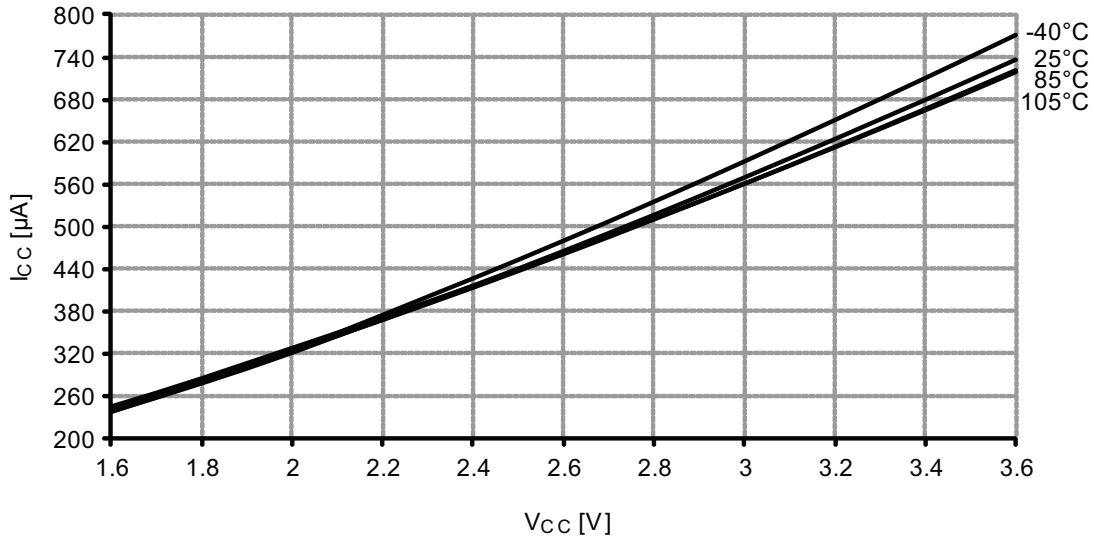


Figure 37-253. Active mode supply current vs. V_{CC}.

f_{SYS} = 1MHz external clock.



37.4.2.3 Thresholds and Hysteresis

Figure 37-280. I/O pin input threshold voltage vs. V_{CC}.
T = 25°C.

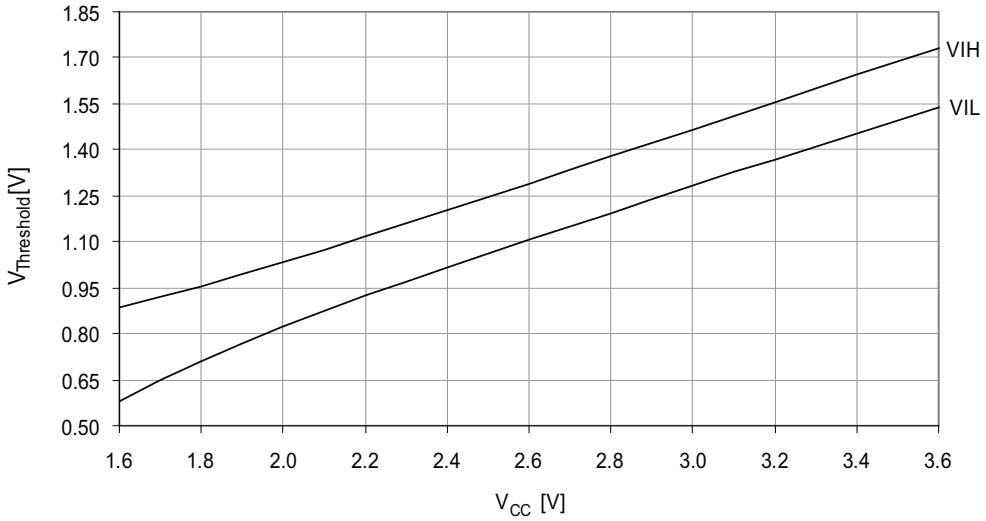
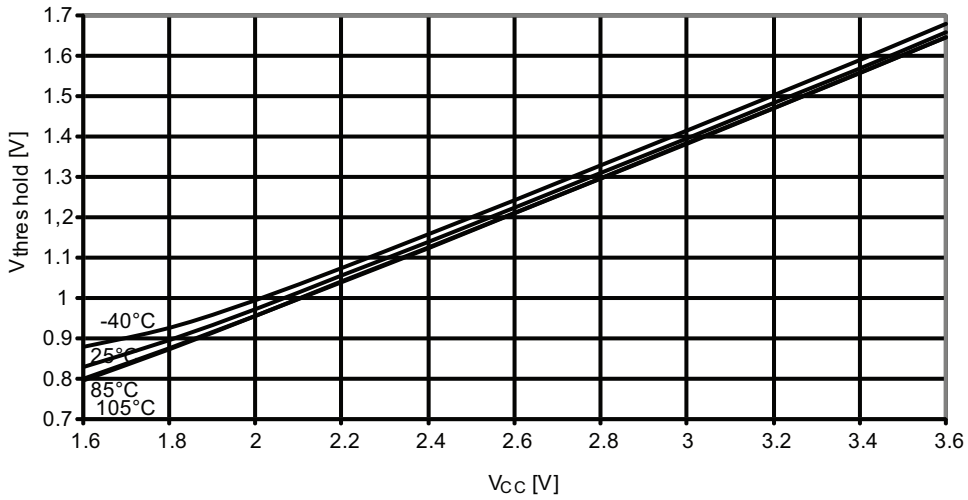


Figure 37-281. I/O pin input threshold voltage vs. V_{CC}.
V_{IH} I/O pin read as "1".



37.4.5 Analog Comparator Characteristics

Figure 37-300. Analog comparator hysteresis vs. V_{CC}

High-speed, small hysteresis.

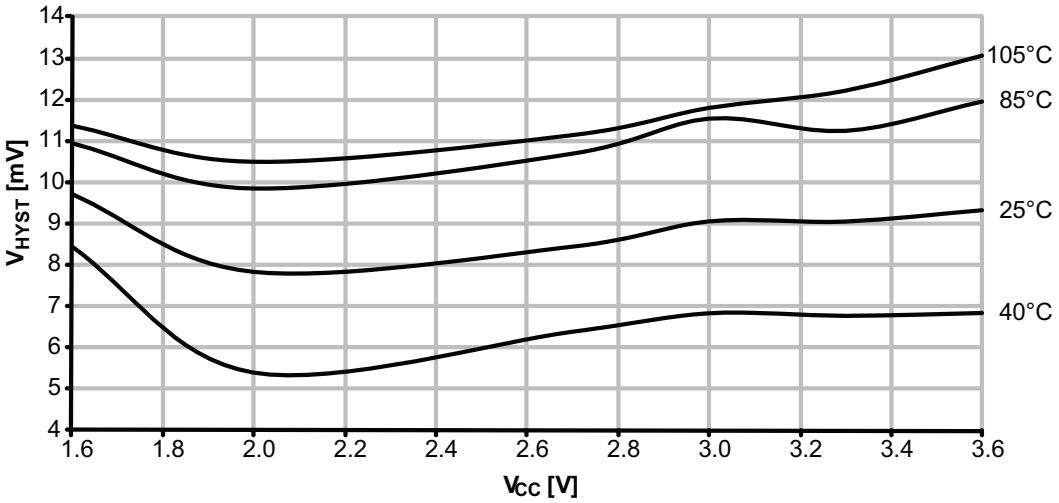
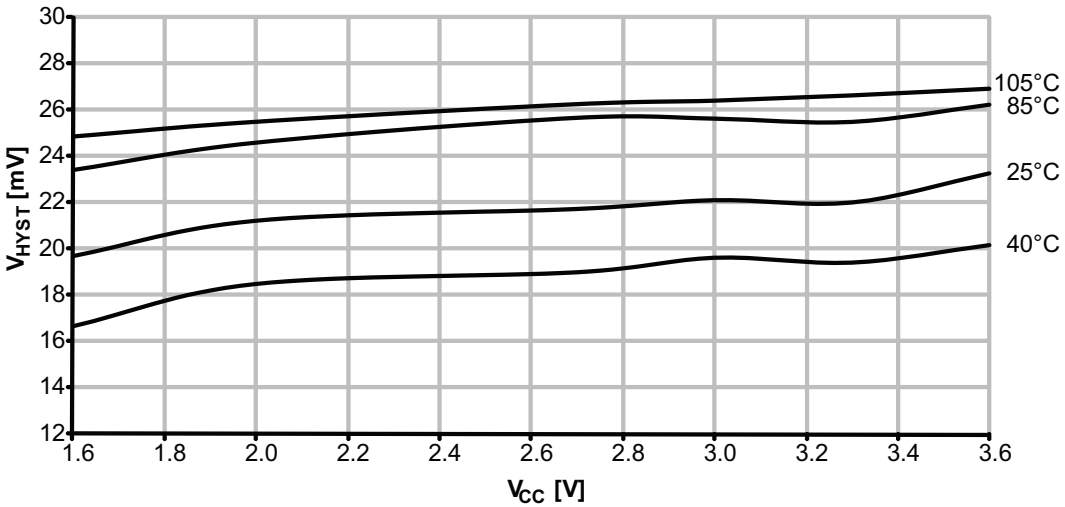


Figure 37-301. Analog comparator hysteresis vs. V_{CC}

Low power, small hysteresis.



37.4.7 BOD Characteristics

Figure 37-308. BOD thresholds vs. temperature.

BOD level = 1.6V.

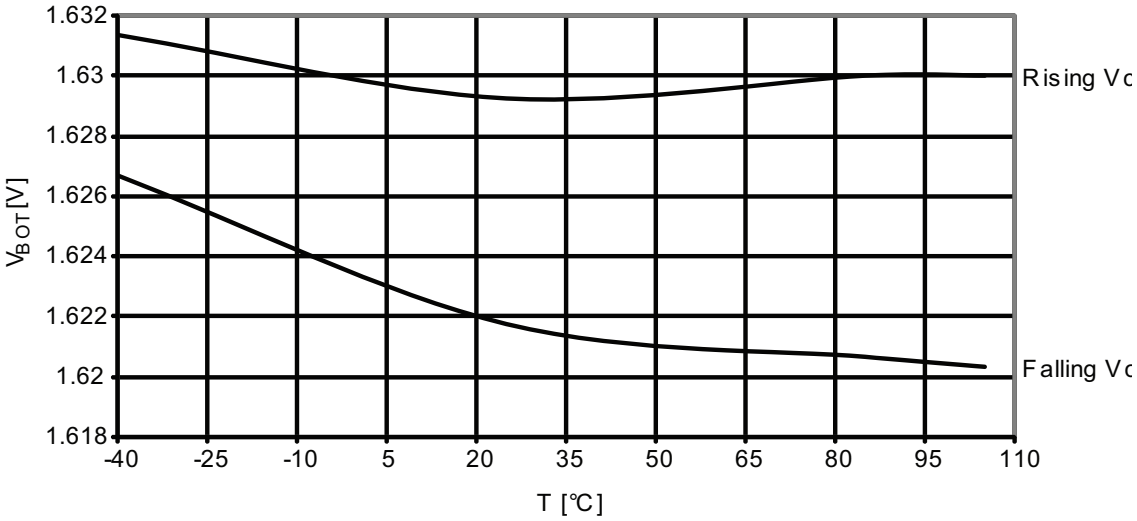


Figure 37-309. BOD thresholds vs. temperature.

BOD level = 3.0V.