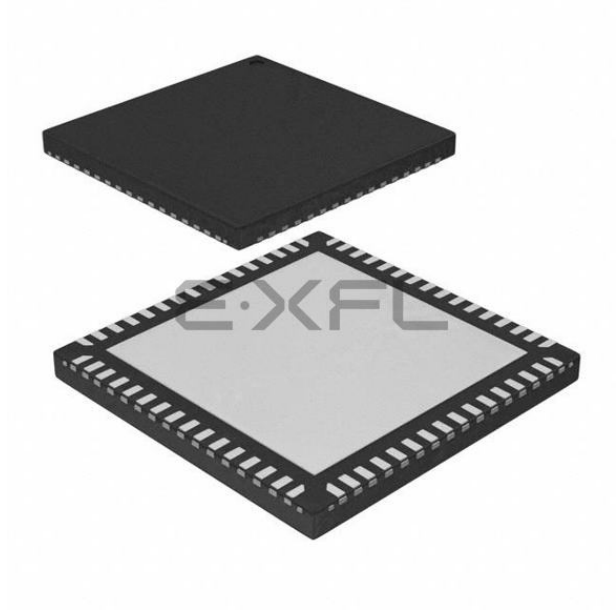

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	AVR
Core Size	8/16-Bit
Speed	32MHz
Connectivity	I²C, IrDA, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	50
Program Memory Size	128KB (64K x 16)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad
Supplier Device Package	64-QFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atxmega128a3u-mnr

Table 7-3. Data memory map (Hexadecimal address).

Byte Address	ATxmega192A3U	Byte Address	ATxmega128A3U	Byte Address	ATxmega64A3U
0	I/O Registers (4K)	0	I/O Registers (4K)	0	I/O Registers (4K)
FFF		FFF		FFF	
1000	EEPROM (2K)	1000	EEPROM (2K)	1000	EEPROM (2K)
17FF		17FF		17FF	
	RESERVED		RESERVED		RESERVED
2000	Internal SRAM (16K)	2000	Internal SRAM (8K)	2000	Internal SRAM (4K)
5FFF		3FFF		2FFF	

Byte Address	ATxmega256A3U
0	I/O Registers (4K)
FFF	
1000	EEPROM (4K)
13FF	
	RESERVED
2000	Internal SRAM (16K)
27FF	

7.6 EEPROM

XMEGA AU devices have EEPROM for nonvolatile data storage. It is either addressable in a separate data space (default) or memory mapped and accessed in normal data space. The EEPROM supports both byte and page access. Memory mapped EEPROM allows highly efficient EEPROM reading and EEPROM buffer loading. When doing this, EEPROM is accessible using load and store instructions. Memory mapped EEPROM will always start at hexadecimal address 0x1000.

7.7 I/O Memory

The status and configuration registers for peripherals and modules, including the CPU, are addressable through I/O memory locations. All I/O locations can be accessed by the load (LD/LDS/LDD) and store (ST/STS/STD) instructions, which are used to transfer data between the 32 registers in the register file and the I/O memory. The IN and OUT instructions can address I/O memory locations in the range of 0x00 to 0x3F directly. In the address range 0x00 - 0x1F, single-cycle instructions for manipulation and checking of individual bits are available.

The I/O memory address for all peripherals and modules in XMEGA A3U is shown in the “Peripheral Module Address Map” on page 64.

7.7.1 General Purpose I/O Registers

The lowest 16 I/O memory addresses are reserved as general purpose I/O registers. These registers can be used for storing global variables and flags, as they are directly bit-accessible using the SBI, CBI, SBIS, and SBIC instructions.

16. TC0/1 – 16-bit Timer/Counter Type 0 and 1

16.1 Features

- Seven 16-bit timer/counters
  - Four timer/counters of type 0
  - Three timer/counters of type 1
  - Split-mode enabling two 8-bit timer/counter from each timer/counter type 0
- 32-bit Timer/Counter support by cascading two timer/counters
- Up to four compare or capture (CC) channels
  - Four CC channels for timer/counters of type 0
  - Two CC channels for timer/counters of type 1
- Double buffered timer period setting
- Double buffered capture or compare channels
- Waveform generation:
  - Frequency generation
  - Single-slope pulse width modulation
  - Dual-slope pulse width modulation
- Input capture:
  - Input capture with noise cancelling
  - Frequency capture
  - Pulse width capture
  - 32-bit input capture
- Timer overflow and error interrupts/events
- One compare match or input capture interrupt/event per CC channel
- Can be used with event system for:
  - Quadrature decoding
  - Count and direction control
  - Capture
- Can be used with DMA and to trigger DMA transactions
- High-resolution extension
  - Increases frequency and waveform resolution by 4x (2-bit) or 8x (3-bit)
- Advanced waveform extension:
  - Low- and high-side output with programmable dead-time insertion (DTI)
- Event controlled fault protection for safe disabling of drivers

16.2 Overview

Atmel AVR XMEGA devices have a set of seven flexible 16-bit Timer/Counters (TC). Their capabilities include accurate program execution timing, frequency and waveform generation, and input capture with time and frequency measurement of digital signals. Two timer/counters can be cascaded to create a 32-bit timer/counter with optional 32-bit capture.

A timer/counter consists of a base counter and a set of compare or capture (CC) channels. The base counter can be used to count clock cycles or events. It has direction control and period setting that can be used for timing. The CC channels can be used together with the base counter to do compare match control, frequency generation, and pulse width waveform modulation, as well as various input capture operations. A timer/counter can be configured for either capture or compare functions, but cannot perform both at the same time.

20. RTC – 16-bit Real-Time Counter

20.1 Features

- 16-bit resolution
- Selectable clock source
  - 32.768kHz external crystal
  - External clock
  - 32.768kHz internal oscillator
  - 32kHz internal ULP oscillator
- Programmable 10-bit clock prescaling
- One compare register
- One period register
- Clear counter on period overflow
- Optional interrupt/event on overflow and compare match

20.2 Overview

The 16-bit real-time counter (RTC) is a counter that typically runs continuously, including in low-power sleep modes, to keep track of time. It can wake up the device from sleep modes and/or interrupt the device at regular intervals.

The reference clock is typically the 1.024kHz output from a high-accuracy crystal of 32.768kHz, and this is the configuration most optimized for low power consumption. The faster 32.768kHz output can be selected if the RTC needs a resolution higher than 1ms. The RTC can also be clocked from an external clock signal, the 32.768kHz internal oscillator or the 32kHz internal ULP oscillator.

The RTC includes a 10-bit programmable prescaler that can scale down the reference clock before it reaches the counter. A wide range of resolutions and time-out periods can be configured. With a 32.768kHz clock source, the maximum resolution is 30.5µs, and time-out periods can range up to 2000 seconds. With a resolution of 1s, the maximum timeout period is more than18 hours (65536 seconds). The RTC can give a compare interrupt and/or event when the counter equals the compare register value, and an overflow interrupt and/or event when it equals the period register value.

Figure 20-1. Real-time counter overview.

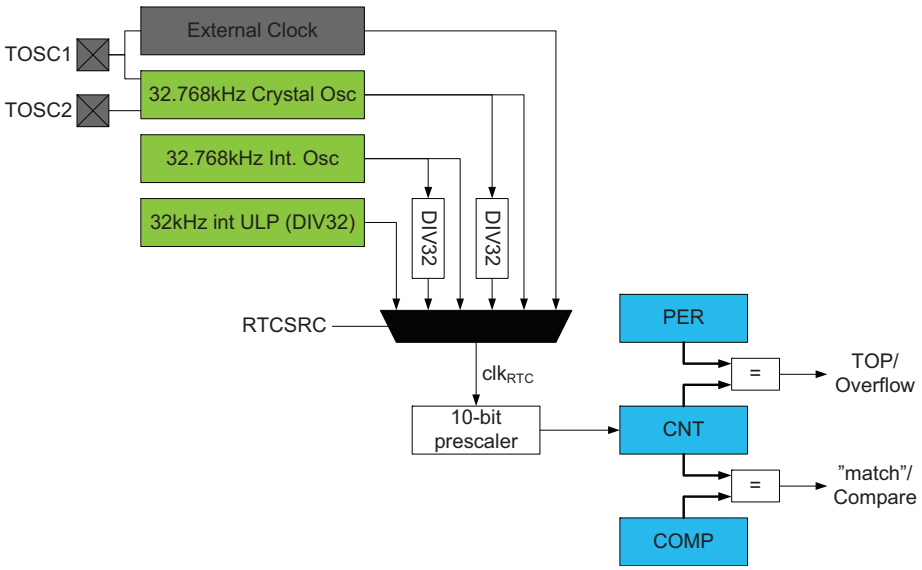


Table 36-53. Programming time.

Symbol	Parameter	Condition	Min.	Typ. (1)	Max.	Units
	Chip Erase	128KB Flash, EEPROM (2) and SRAM Erase		75		ms
	Application Erase	Section erase		6		ms
	Flash	Page Erase		4		ms
		Page Write		4		
		Atomic Page Erase and Write		8		
	EEPROM	Page Erase		4		ms
		Page Write		4		
		Atomic Page Erase and Write		8		

Notes: 1. Programming is timed from the 2MHz internal oscillator.
2. EEPROM is not erased if the EESAVE fuse is programmed.

36.2.14 Clock and Oscillator Characteristics

36.2.14.1 Calibrated 32.768kHz Internal Oscillator characteristics

Table 36-54. 32.768kHz internal oscillator characteristics.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
	Frequency			32.768		kHz
	Factory calibration accuracy	T = 85°C, V_{CC} = 3.0V	-0.5		0.5	%
	User calibration accuracy		-0.5		0.5	%

36.2.14.2 Calibrated 2MHz RC Internal Oscillator characteristics

Table 36-55. 2MHz internal oscillator characteristics.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
	Frequency range	DFLL can tune to this frequency over voltage and temperature	1.8		2.2	MHz
	Factory calibrated frequency			2.0		MHz
	Factory calibration accuracy	T = 85°C, V_{CC}= 3.0V	-1.5		1.5	%
	User calibration accuracy		-0.2		0.2	%
	DFLL calibration stepsize			0.22		%

36.2.15 SPI Characteristics

Figure 36-12. SPI timing requirements in master mode.

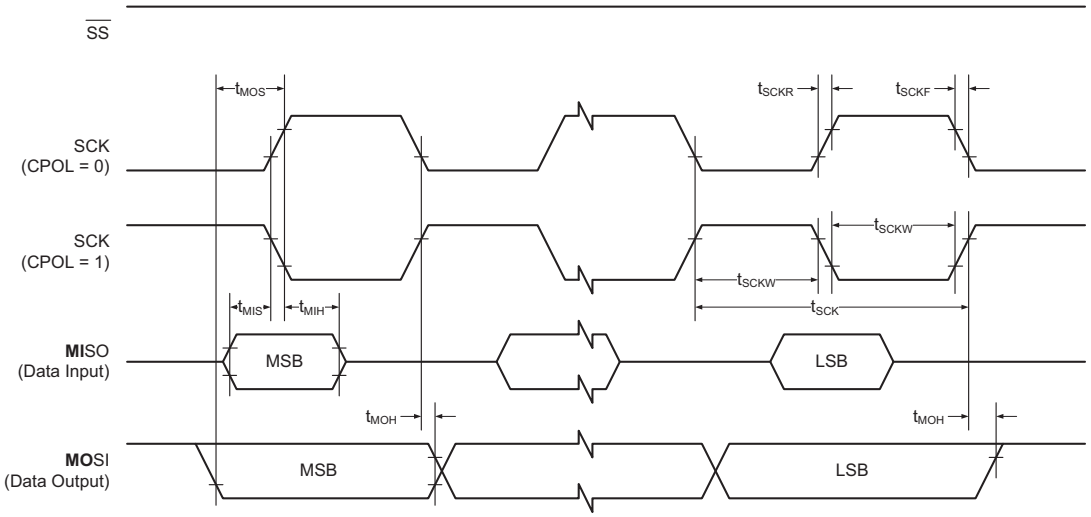
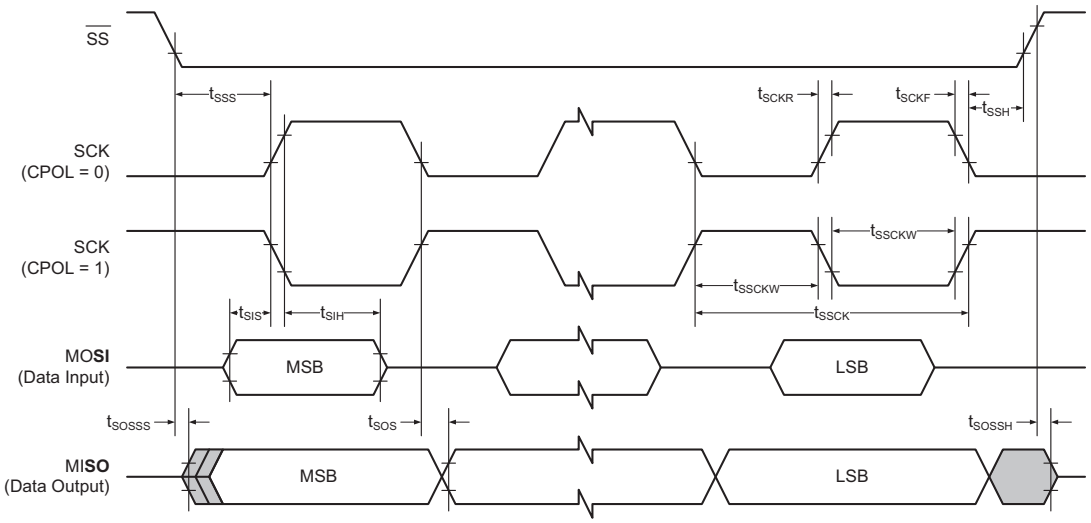


Figure 36-13. SPI timing requirements in slave mode.



36.4.3 Current consumption

Table 36-100. Current consumption for active mode and sleep modes.

Symbol	Parameter	Condition		Min.	Typ.	Max.	Units
I_{CC}	Active Power consumption (1)	32kHz, Ext. Clk	V_{CC} = 1.8V		60		µA
			V_{CC} = 3.0V		140		
		1MHz, Ext. Clk	V_{CC} = 1.8V		280		
			V_{CC} = 3.0V		600		
		2MHz, Ext. Clk	V_{CC} = 1.8V		510	500	
			V_{CC} = 3.0V		1.1	1.5	mA
		32MHz, Ext. Clk			10.6	15	
	Idle Power consumption (1)	32kHz, Ext. Clk	V_{CC} = 1.8V		4.3		µA
			V_{CC} = 3.0V		4.8		
		1MHz, Ext. Clk	V_{CC} = 1.8V		78		
			V_{CC} = 3.0V		150		
		2MHz, Ext. Clk	V_{CC} = 1.8V		150	350	
			V_{CC} = 3.0V		290	600	
		32MHz, Ext. Clk			4.7	7.0	mA
	Power-down power consumption	T = 25°C	V_{CC} = 3.0V		0.1	1.0	µA
		T = 85°C			1.8	5.0	
		T = 105°C			6.5	17	
		WDT and Sampled BOD enabled, T = 25°C	V_{CC} = 3.0V		1.3	3.0	
		WDT and Sampled BOD enabled, T = 85°C			3.1	7.0	
		WDT and Sampled BOD enabled, T = 105°C			7.3	20	
	Power-save power consumption (2)	RTC from ULP clock, WDT and sampled BOD enabled, T = 25°C	V_{CC} = 1.8V		1.2		µA
			V_{CC} = 3.0V		1.3		
		RTC from 1.024kHz low power 32.768kHz TOSC, T = 25°C	V_{CC} = 1.8V		0.6	2	
			V_{CC} = 3.0V		0.7	2	
		RTC from low power 32.768kHz TOSC, T = 25°C	V_{CC} = 1.8V		0.8	3	
			V_{CC} = 3.0V		1.0	3	
	Reset power consumption	Current through $\overline{\text{RESET}}$ pin substracted	V_{CC} = 3.0V		250		µA

Notes: 1. All Power Reduction Registers set.
2. Maximum limits are based on characterization, and not tested in production.

Symbol	Parameter	Condition		Min.	Typ.	Max.	Units
t_{delay}	Propagation delay	V_{CC} = 3.0V, T= 85°C	mode = HS		30	90	ns
		mode = HS			30		
		V_{CC} = 3.0V, T= 85°C	mode = LP		130	500	
		mode = LP			130		
	64-Level Voltage Scaler	Integral non-linearity (INL)			0.3	0.5	lsb

36.4.9 Bandgap and Internal 1.0V Reference Characteristics

Table 36-112. Bandgap and Internal 1.0V reference characteristics.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
	Startup time	As reference for ADC or DAC	1 Clk_{PER} + 2.5µs			µs
		As input voltage to ADC and AC		1.5		
	Bandgap voltage			1.1		V
INT1V	Internal 1.00V reference	T= 85°C, after calibration	0.99	1	1.01	V
	Variation over voltage and temperature	Relative to T= 85°C, V_{CC} = 3.0V		±1.0		%

36.4.10 Brownout Detection Characteristics

Table 36-113. Brownout detection characteristics.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{BOT}	BOD level 0 falling V_{CC}		1.60	1.62	1.72	V
	BOD level 1 falling V_{CC}			1.8		
	BOD level 2 falling V_{CC}			2.0		
	BOD level 3 falling V_{CC}			2.2		
	BOD level 4 falling V_{CC}			2.4		
	BOD level 5 falling V_{CC}			2.6		
	BOD level 6 falling V_{CC}			2.8		
	BOD level 7 falling V_{CC}			3.0		
t_{BOD}	Detection time	Continuous mode		0.4		µs
		Sampled mode		1000		
V_{HYST}	Hysteresis			1.6		%

Figure 37-21. I/O pin pull-up resistor current vs. input voltage.

V_{CC} = 3.0V.

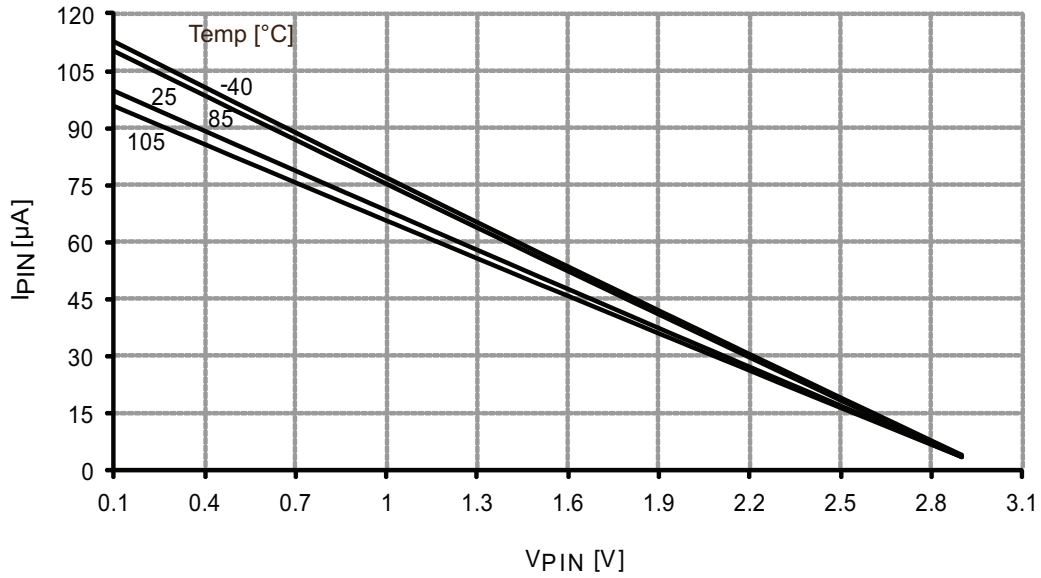


Figure 37-22. I/O pin pull-up resistor current vs. input voltage.

V_{CC} = 3.3V.

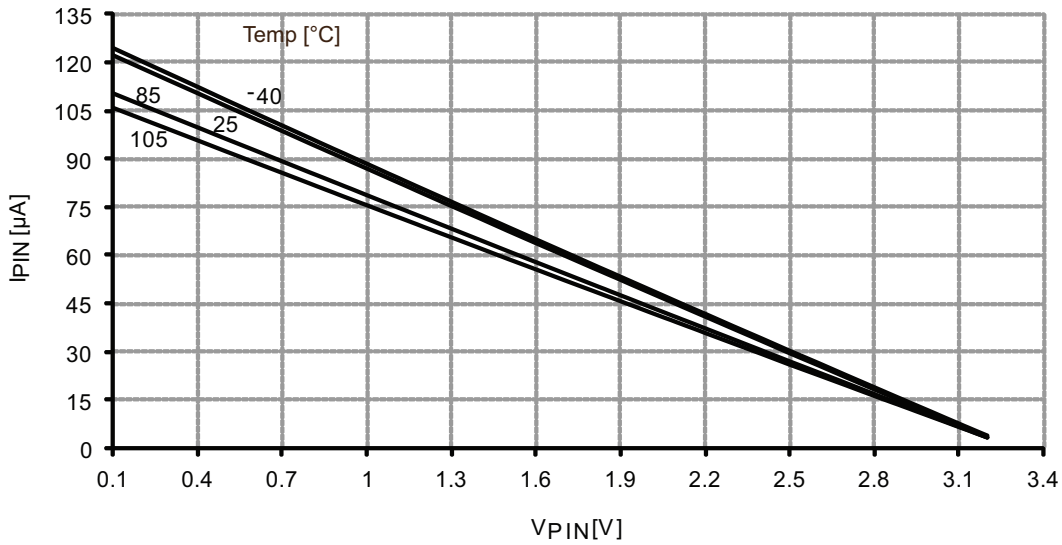


Figure 37-72. 2MHz internal oscillator frequency vs. temperature.

DFLL enabled, from the 32.768kHz internal oscillator.

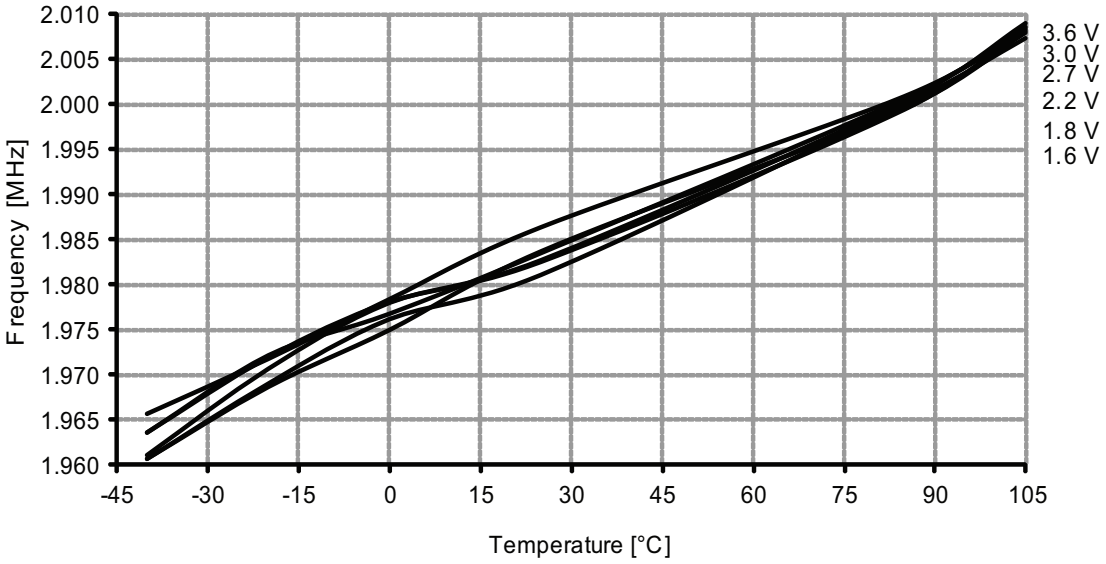
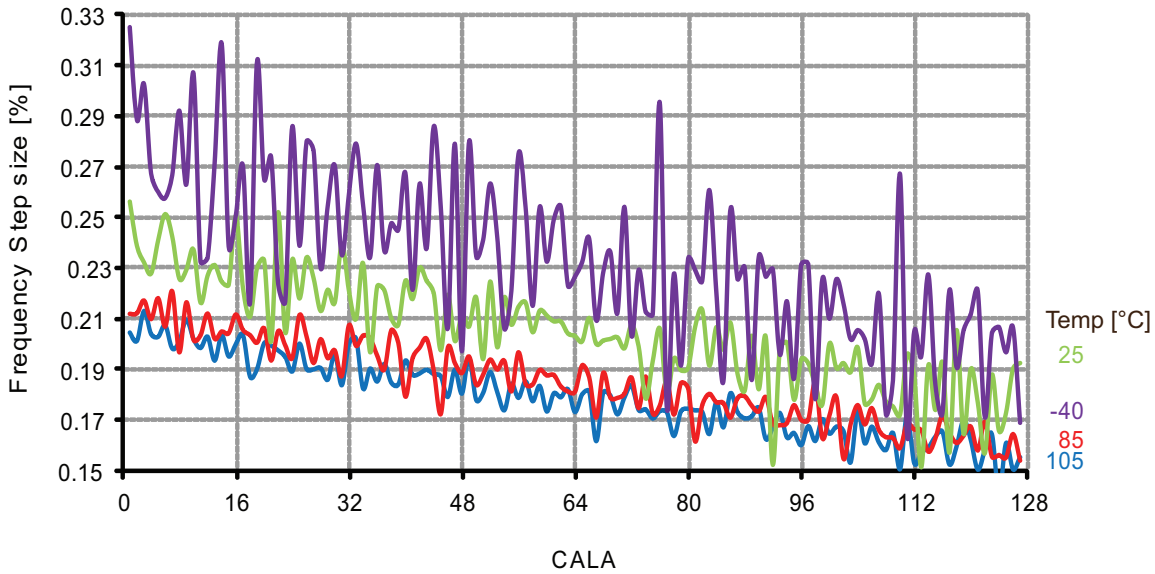


Figure 37-73. 2MHz internal oscillator CALA calibration step size.

V_{CC} = 3V.



37.2.3 ADC Characteristics

Figure 37-118. INL error vs. external V_{REF}.

T = 25°C, V_{CC} = 3.6V, external reference.

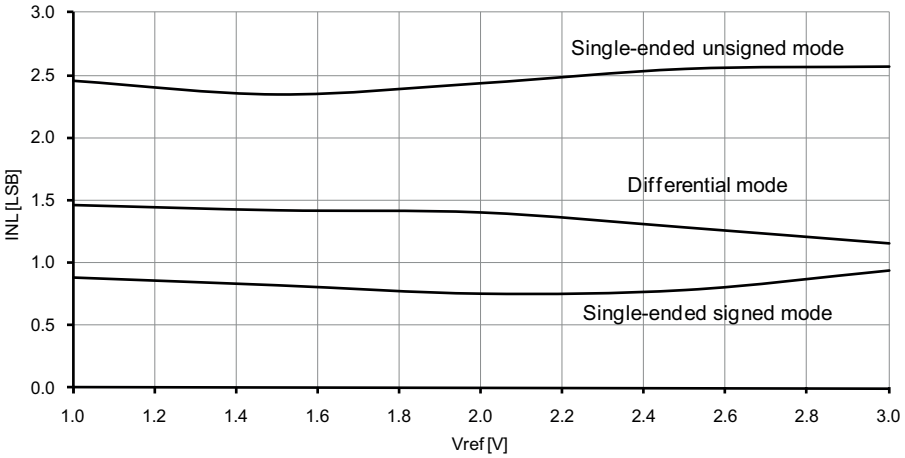
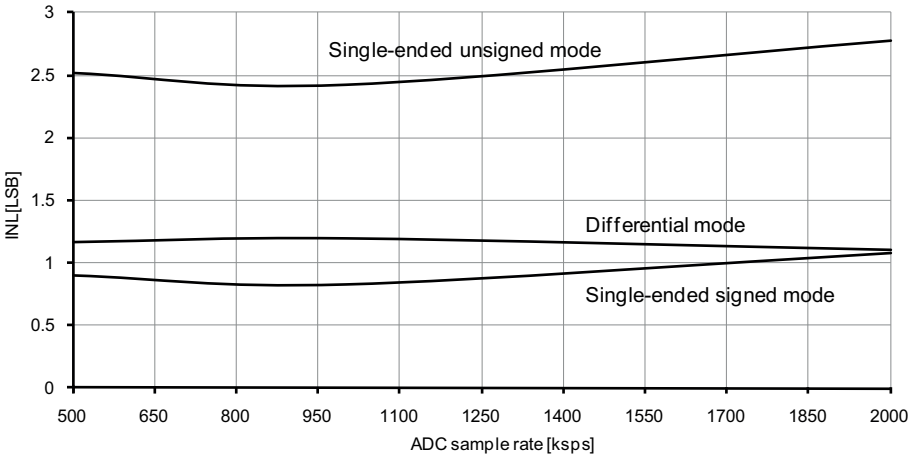


Figure 37-119. INL error vs. sample rate.

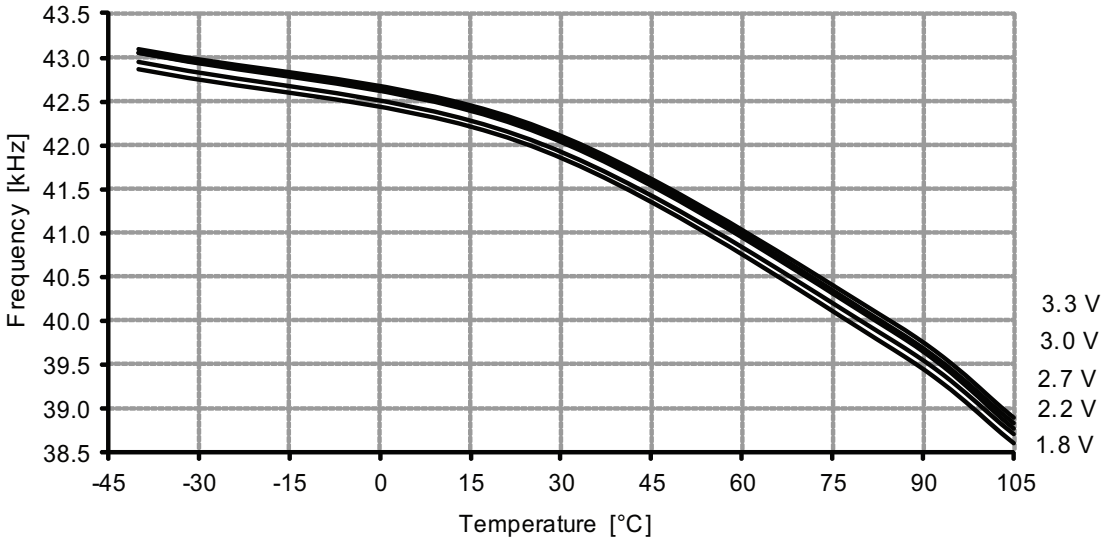
T = 25°C, V_{CC} = 3.6V, V_{REF} = 3.0V external.



37.2.10 Oscillator Characteristics

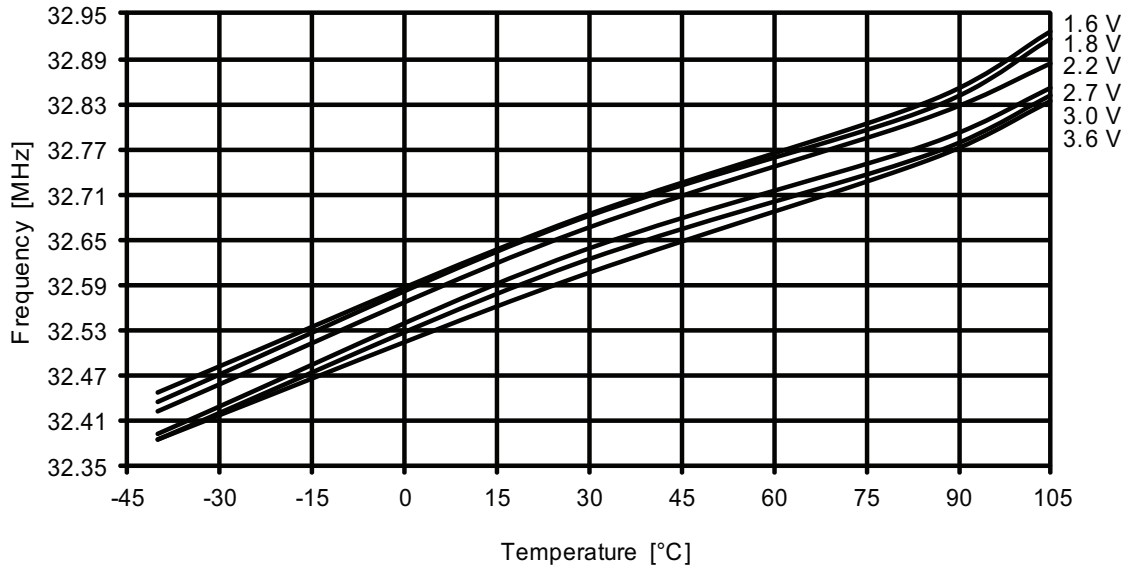
37.2.10.1 Ultra Low-Power internal oscillator

Figure 37-151. Ultra Low-Power internal oscillator frequency vs. temperature.



37.2.10.2 32.768kHz Internal Oscillator

Figure 37-152. 32.768kHz internal oscillator frequency vs. temperature.



37.2.10.4 32MHz Internal Oscillator

Figure 37-157. 32MHz internal oscillator frequency vs. temperature.

DFLL disabled.

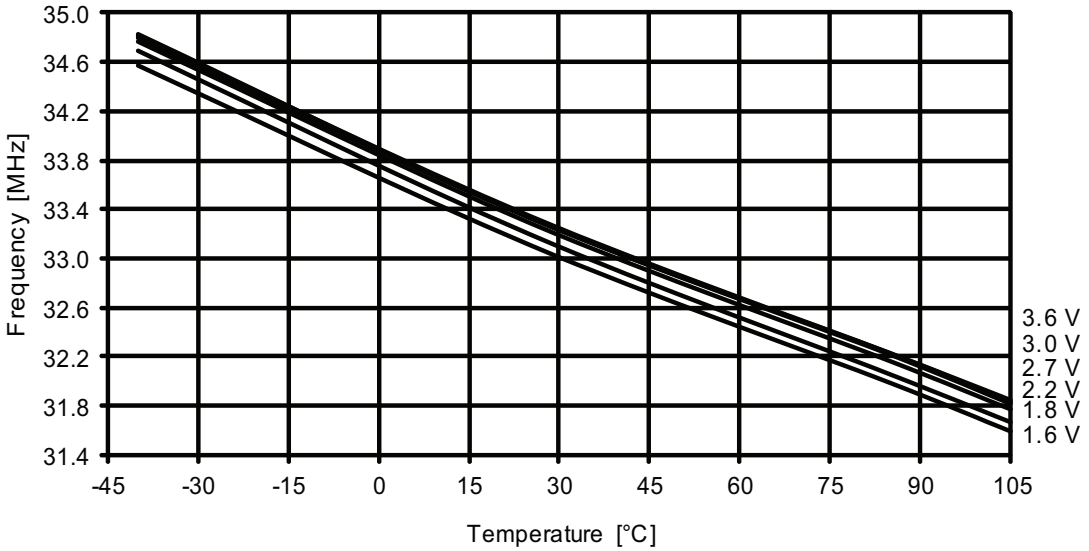


Figure 37-158. 32MHz internal oscillator frequency vs. temperature.

DFLL enabled, from the 32.768kHz internal oscillator.

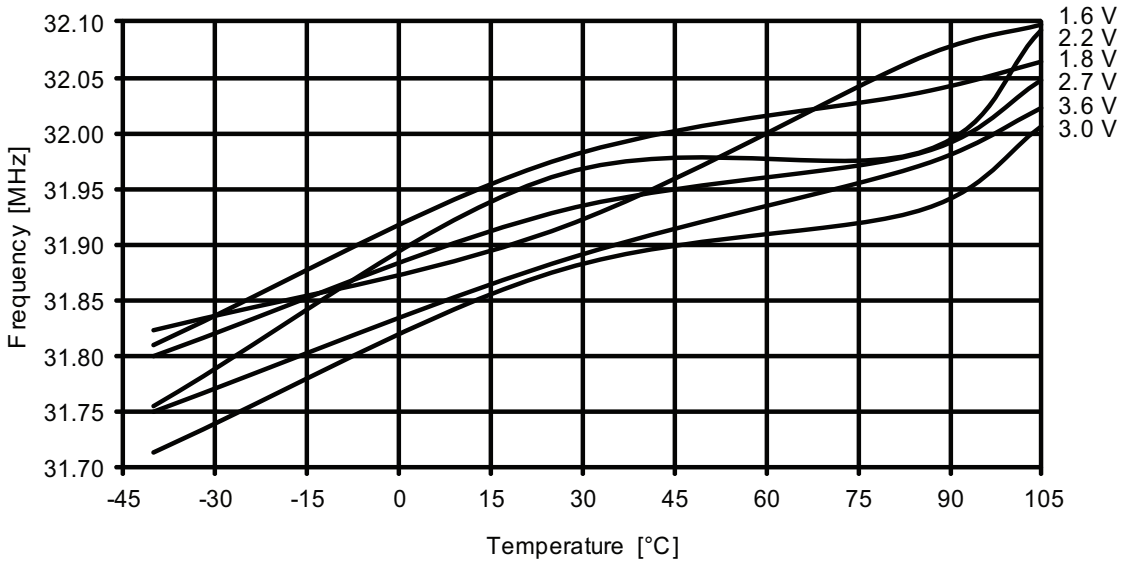


Figure 37-171. Active mode supply current vs. V_{CC}.

f_{SYS} = 2MHz internal oscillator.

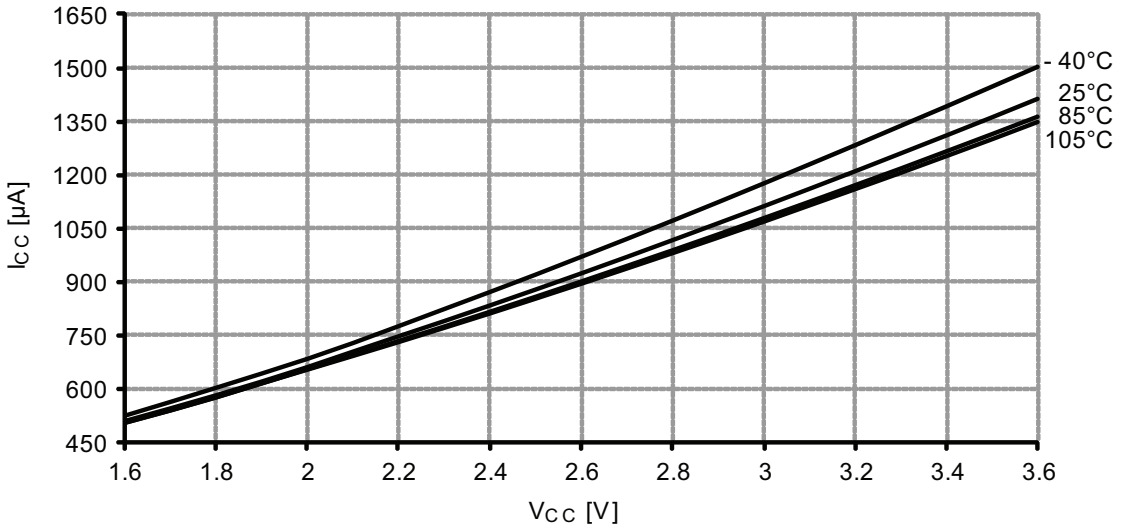


Figure 37-172. Active mode supply current vs. V_{CC}.

f_{SYS} = 32MHz internal oscillator prescaled to 8MHz.

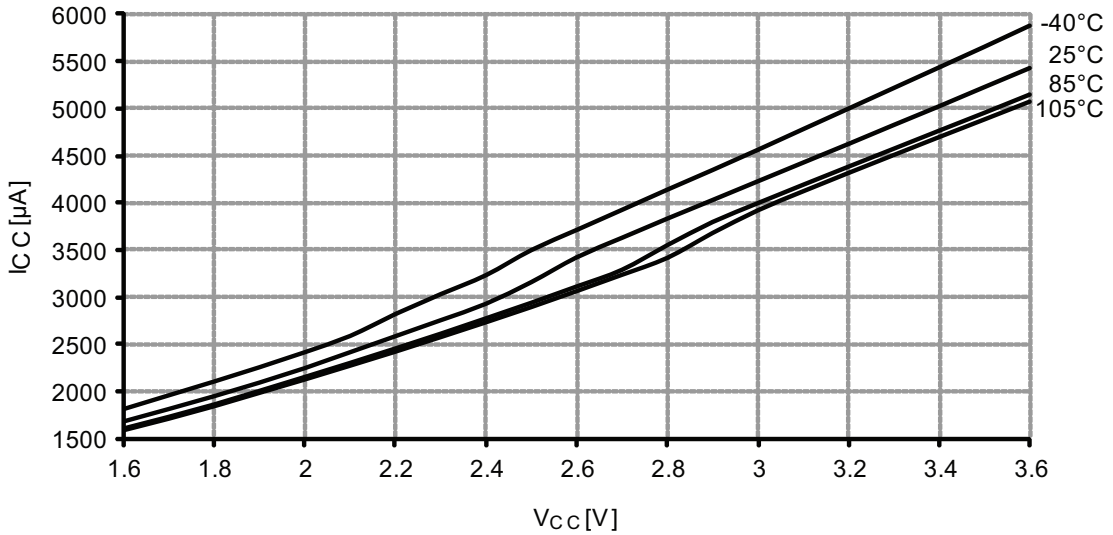


Figure 37-193. I/O pin output voltage vs. sink current.

V_{CC} = 1.8V.

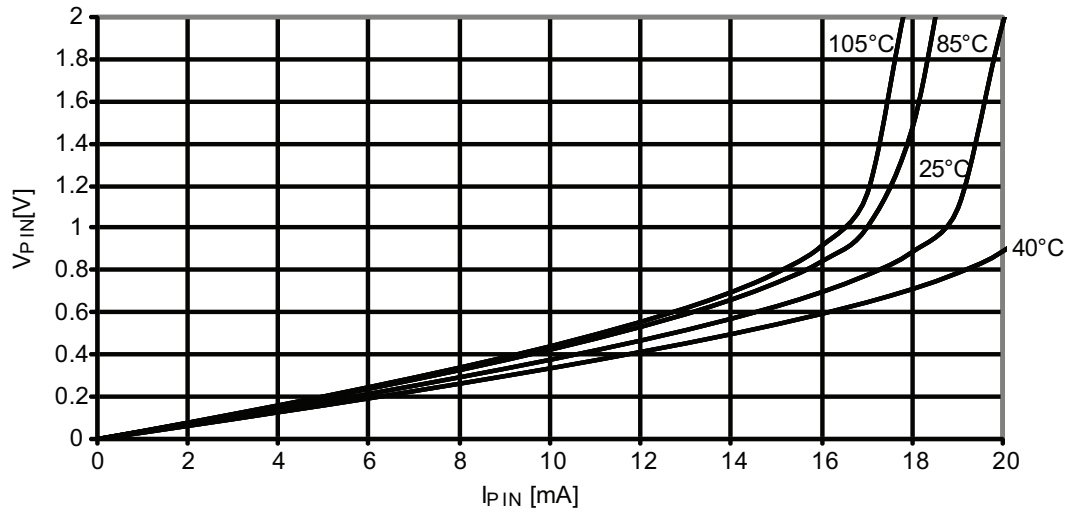


Figure 37-194. I/O pin output voltage vs. sink current.

V_{CC} = 3.0V.

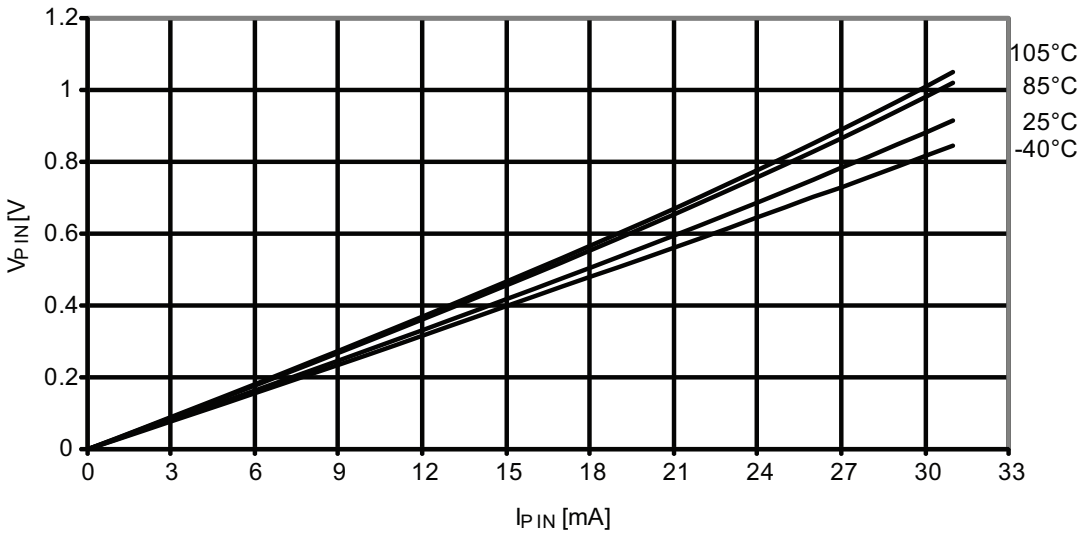
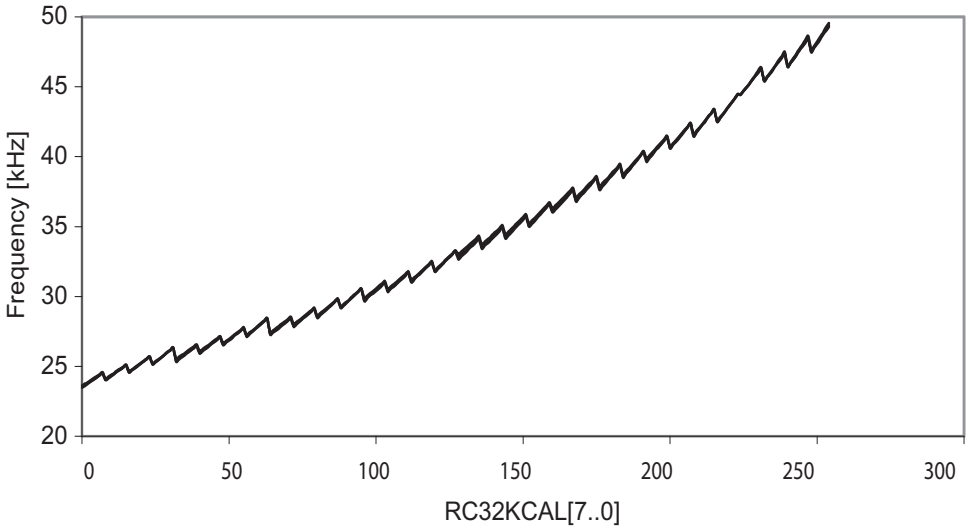


Figure 37-236. 32.768kHz internal oscillator frequency vs. calibration value.

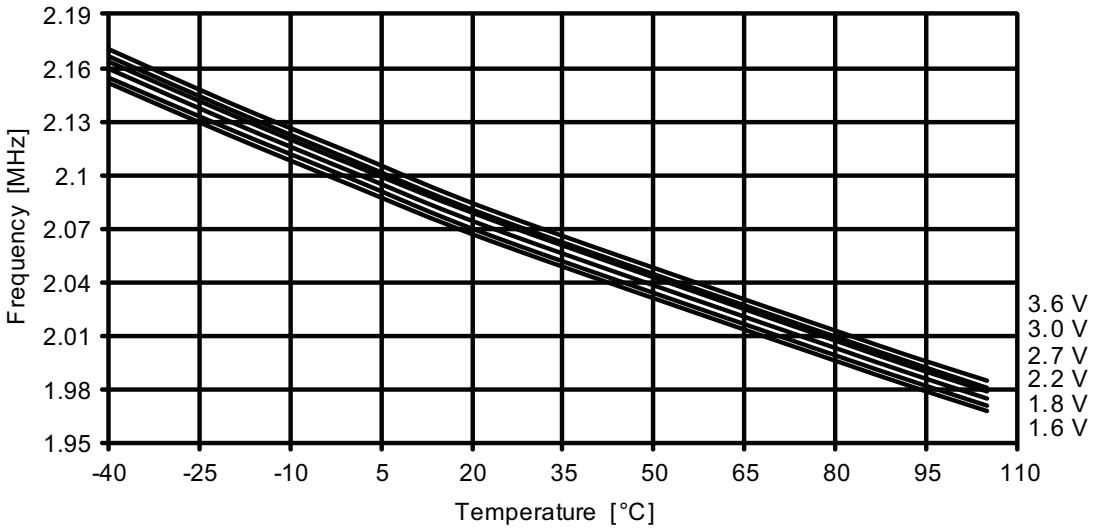
V_{CC} = 3.0V, T = 25°C.



37.3.10.3 2MHz Internal Oscillator

Figure 37-237. 2MHz internal oscillator frequency vs. temperature.

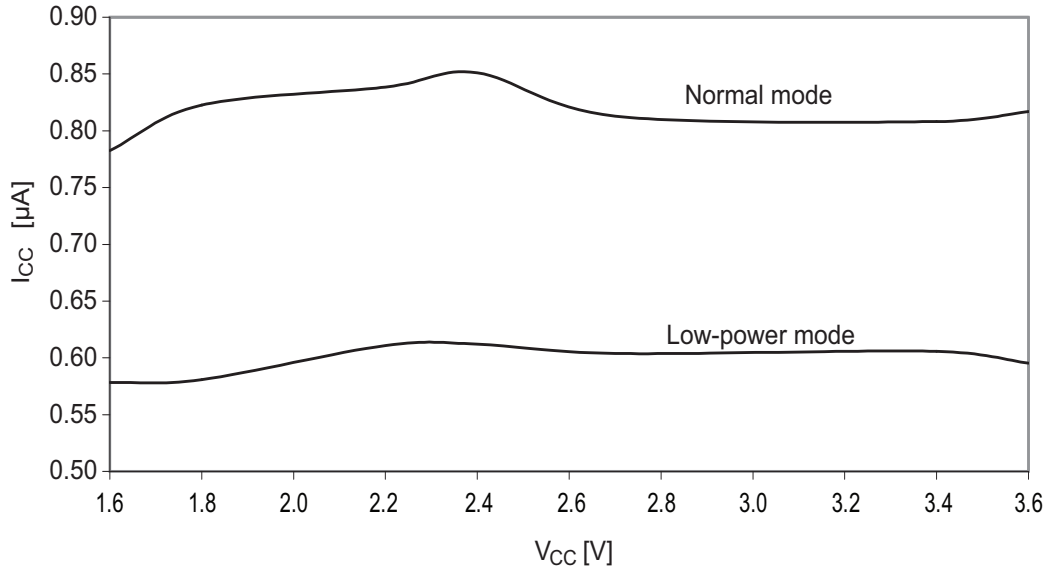
DFLL disabled.



37.4.1.4 Power-save mode supply current

Figure 37-266. Power-save mode supply current vs. V_{CC}.

Real Time Counter enabled and running from 1.024kHz output of 32.768kHz TOSC.



37.4.1.5 Standby mode supply current

Figure 37-267. Standby supply current vs. V_{CC}.

Standby, f_{SYS} = 1MHz.

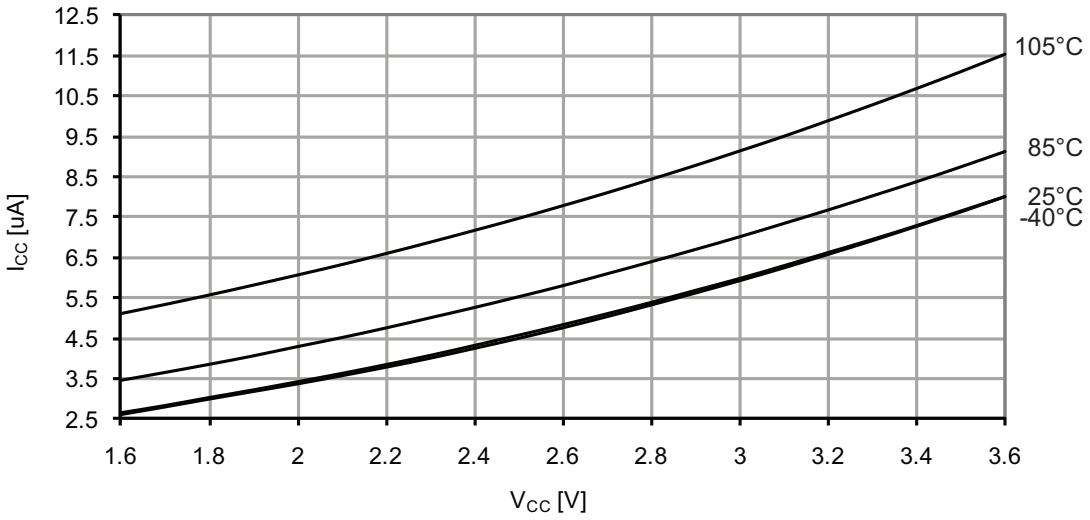


Figure 37-270. I/O pin pull-up resistor current vs. input voltage.

V_{CC} = 3.0V.

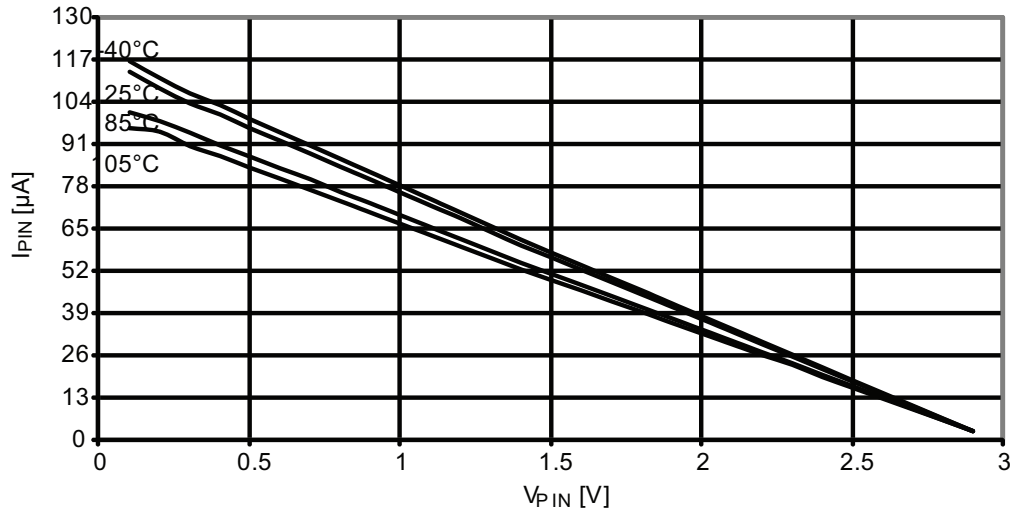
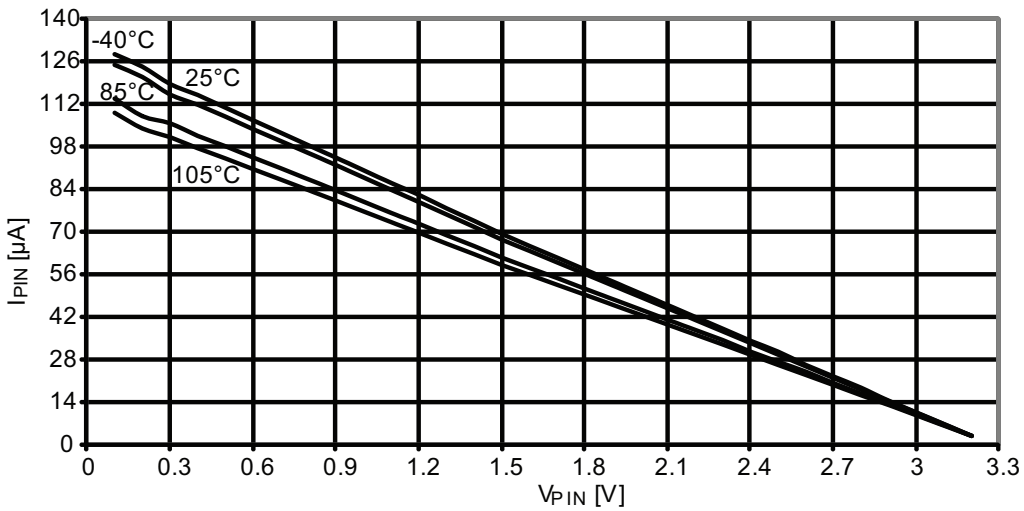


Figure 37-271. I/O pin pull-up resistor current vs. input voltage.

V_{CC} = 3.3V.



37.4.2.2 Output Voltage vs. Sink/Source Current

Figure 37-272. I/O pin output voltage vs. source current.
V_{CC} = 1.8V.

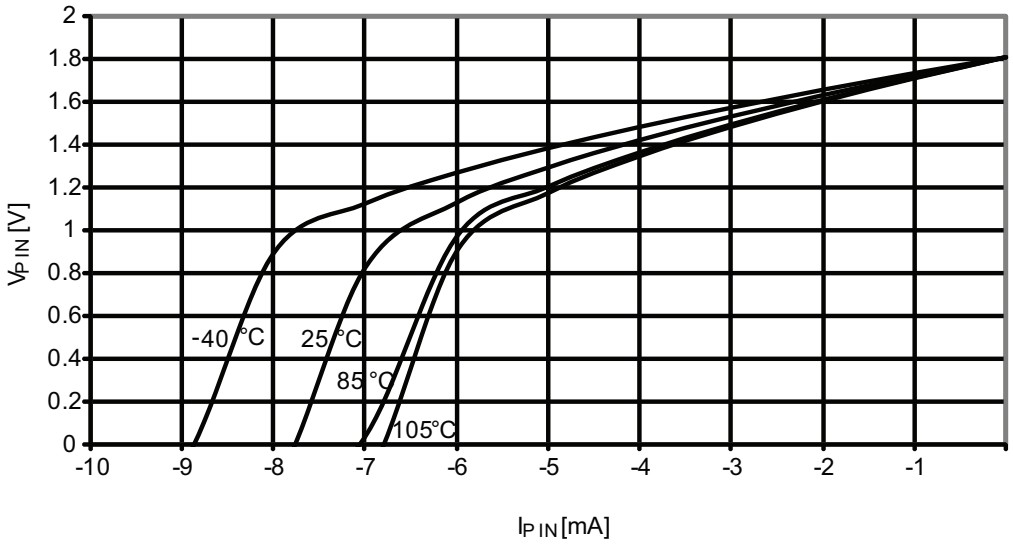


Figure 37-273. I/O pin output voltage vs. source current.
V_{CC} = 3.0V.

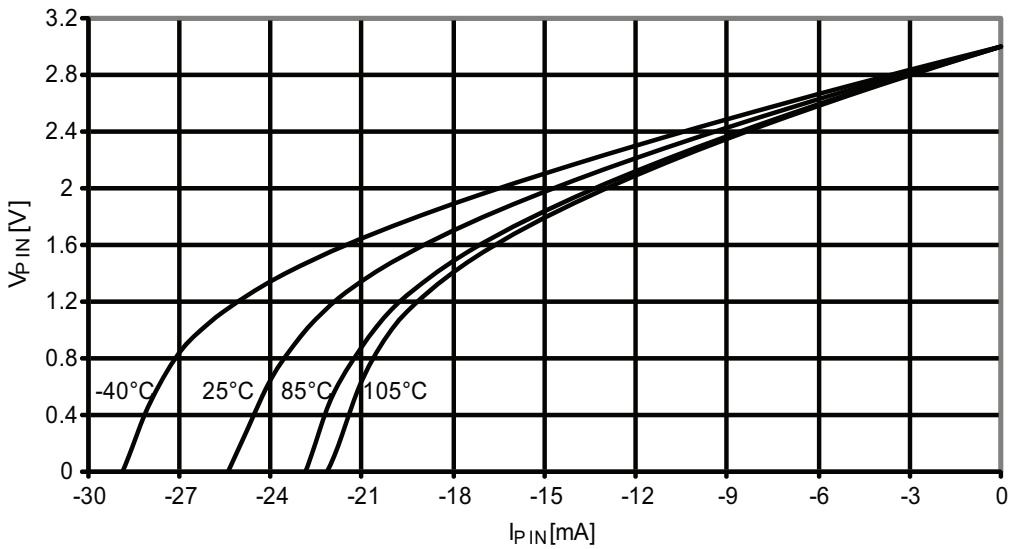
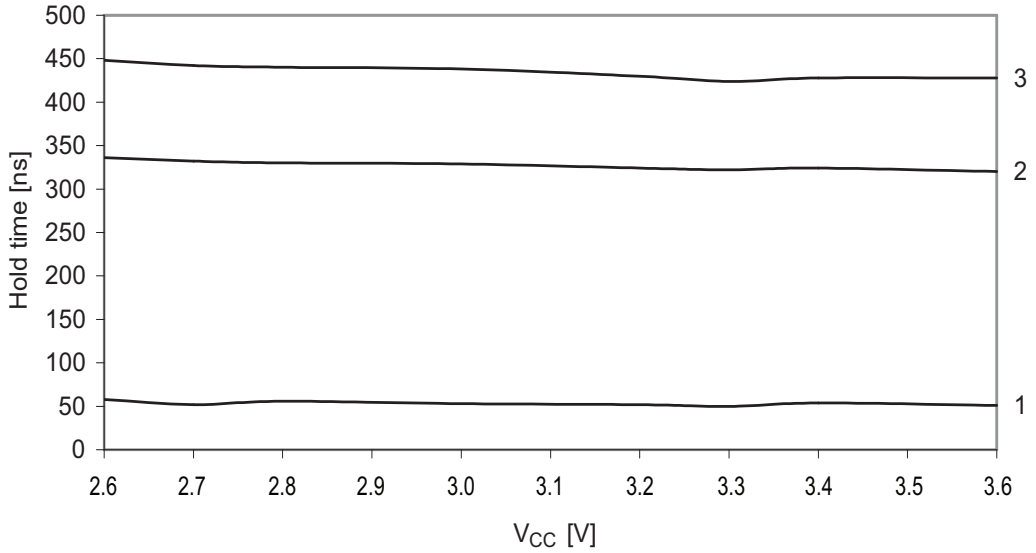
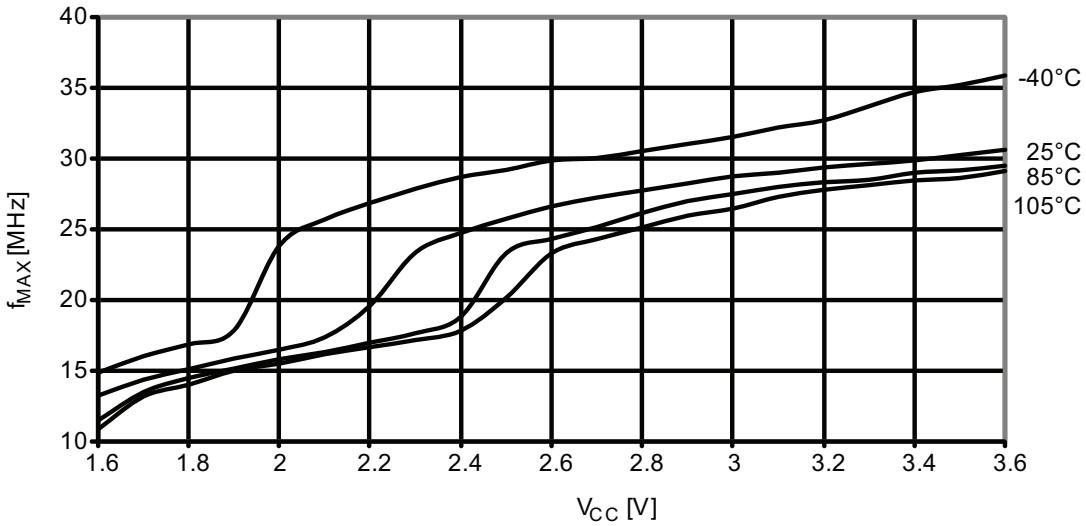


Figure 37-331. SDA hold time vs. supply voltage.



37.4.12 PDI characteristics

Figure 37-332. Maximum PDI frequency vs. V_{CC}.



39. Datasheet Revision History

Please note that the referring page numbers in this section are referred to this document. The referring revision in this section are referring to the document revision.

39.1 8386E – 09/2014

1.	Updated "Ordering Information" on page 3: – Added Ordering information for ATxmega64A3U/128a3U/192A3U/256A3U @ 105°C
	– Updated "Electrical Characteristics" on page 73 and onwards concerning "Power Consumption" and "Endurance and data retention" for ATxmega64A3U/128a3U/192A3U/256A3U @ 105°C
2.	– Updated "Typical Characteristics" on page 161 and onwards for ATxmega64A3U/128a3U/192A3U/256A3U @ 105°C
3.	– Corrected values for Active Current Consumption for 192A3U in Table 36-68 on page 119 and for 256A3U in Table 36-100 on page 141.
4	– Updated plots for Active supply current for 192A3U in Figure 37-167 on page 245 and Figure 37-168 on page 245
5	– Updated plots for Active supply current for 256A3U in Figure 37-251 on page 287 and Figure 37-252 on page 288
6.	– Corrected values for Bootloader start and end address for 128A3U in Table 7-1 on page 14.
7.	– Changed Vcc to AVcc in Section 28. "ADC – 12-bit Analog to Digital Converter" on page 52and in Section 30.1 "Features" on page 56.
8.	– Changed unit notation for parameter $t_{SU;DAT}$ to ns in Table 36-32 on page 93, Table 36-64 on page 115, Table 36-96 on page 137 and Table 36-128 on page 159.
9.	– Added information in Section 38. "Errata" on page 329 on missing calibration of DAC channel 1.

39.2 8386D – 03/2014

1.	Updated "Port A - alternate functions." on page 61: – Removed ACDP POS from the Table 32-1 on page 61
2.	Updated "Port B - alternate functions." on page 61: – ACDB POS changed to ADCB POS/GAINPOS in the Table 32-2 on page 61

39.3 8386C – 02/2013

1.	Updated the datasheet using the Atmel new datasheet template.
2.	Added column for TWI with external driver interface for Port C and E in "Alternate Pin Functions" on page 61.
3.	Removed TWID from Port D and updated pin numbers in"Alternate Pin Functions" on page 61.
4.	Added TOSC and removed AWEXE to/from Port E in "Alternate Pin Functions" on page 61.
5.	Added notes to table for Port D and E in "Alternate Pin Functions" on page 61.